Marwadi University
Faculty of Engineering and Technology
Department of Information and Communication Technology

Subject: VLSI Design **Subject Code:** 01CT0514

Date: 13/09/2025 **Timing: 9:30 am to 4:15 pm**

Long Hour Design (LHD) – Digital Circuit Layouts in Microwind

Task:

Design and implement the following digital circuits using the Microwind Tool by creating their transistor-level layouts, simulating functionality, and verifying outputs: CO2, CO3

1. 4-bit Full Adder
2. 8×1 Multiplexer
3. 1-bit Magnitude Comparator
4. 4-bit Serial-In Serial-Out (SISO) Register

Submission Requirements

- Microwind project file (.msk) and screenshots of layout.
- Timing diagrams of functional verification.
- A short report (3-5 pages) containing:
- Circuit diagrams, truth tables, logic equations.
- Layout screenshots with annotations.
- Simulation results (timing diagram / waveform).
- Observations and conclusion.

Rubric (30 Marks)

Criteria	Description	Marks
1. Circuit Understanding	Truth tables, logic design, and block diagrams showing clarity of each circuit.	6
2. Layout Design in Microwind	Correct transistor-level layout, proper connections, and adherence to CMOS rules.	10
3. Simulation & Results	Functional verification with waveforms and timing diagrams matching expected output.	7
4. Documentation & Submission	Well-structured report with GitHub repository link containing .msk files, screenshots, and report. Neat presentation and timely submission.	7

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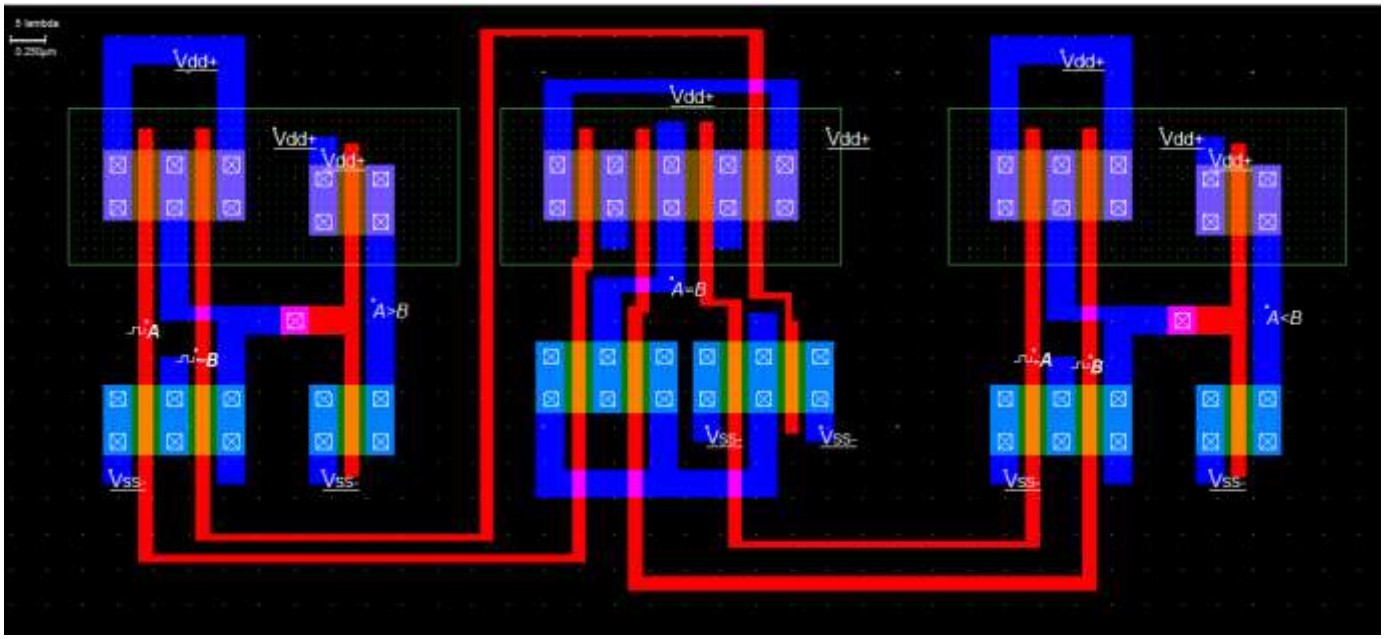
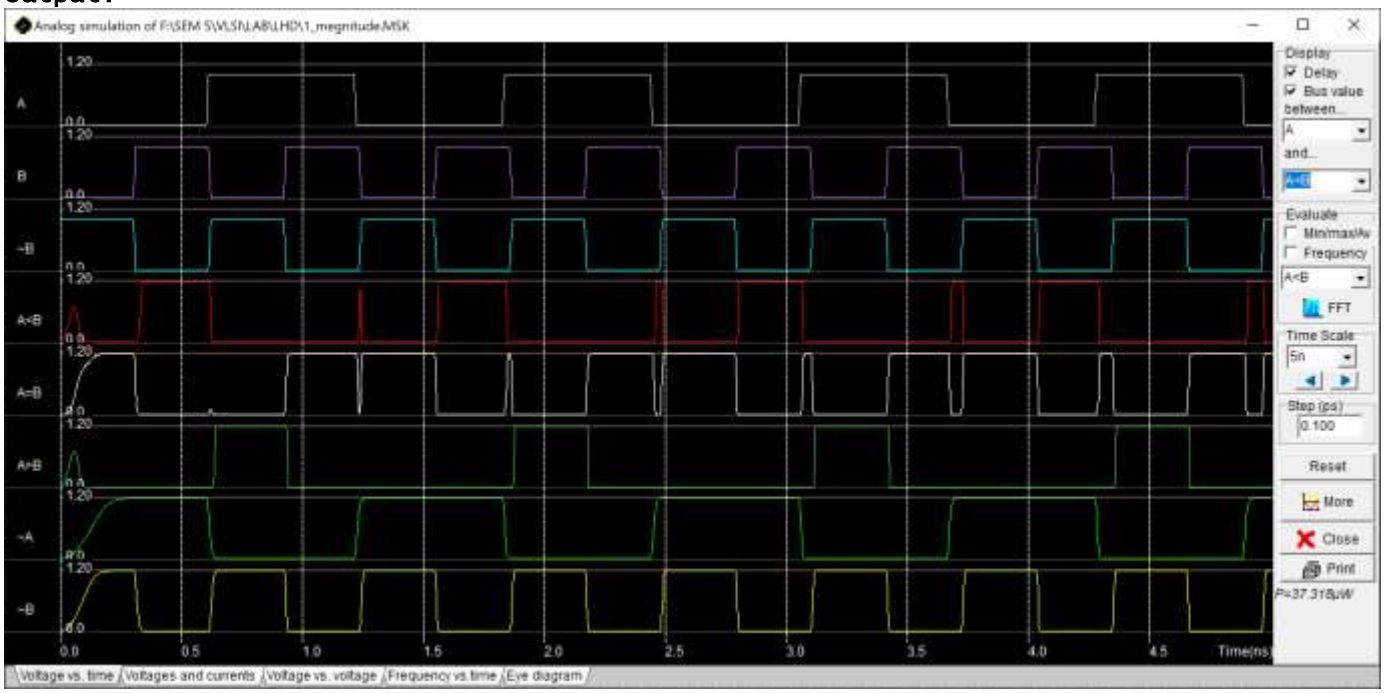
Student Name: Darshan Bhanderi
Enrollment No:92301733034

Circuit:- 1 bit Megniteude Comparator



Output:-



Truth table

A	B	A > B	A = B	A < B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

logic equation

For inputs A and B:

- A > B = A · B′
- A < B = A′ · B
- A = B = A′·B′ + A·B

Results

- When A=0, B=0 → Only A=B=1
- When A=0, B=1 → Only A<B=1
- When A=1, B=0 → Only A>B=1
- When A=1, B=1 → Only A=B=1

Conclusion

The 1-bit magnitude comparator circuit was successfully designed and implemented at the transistor level using Microwind. The layout was created with proper PMOS and NMOS arrangements, and each of the outputs A>B, A=B, and A<B was realized correctly. Functional verification through simulation confirmed that the circuit outputs matched the expected truth table values for all input combinations. The design demonstrates the correct working principle of a comparator and validates the effectiveness of CMOS-based implementation. This project not only strengthens the understanding of digital comparator design but also serves as a foundation for developing higher-bit comparators by cascading multiple 1-bit units.

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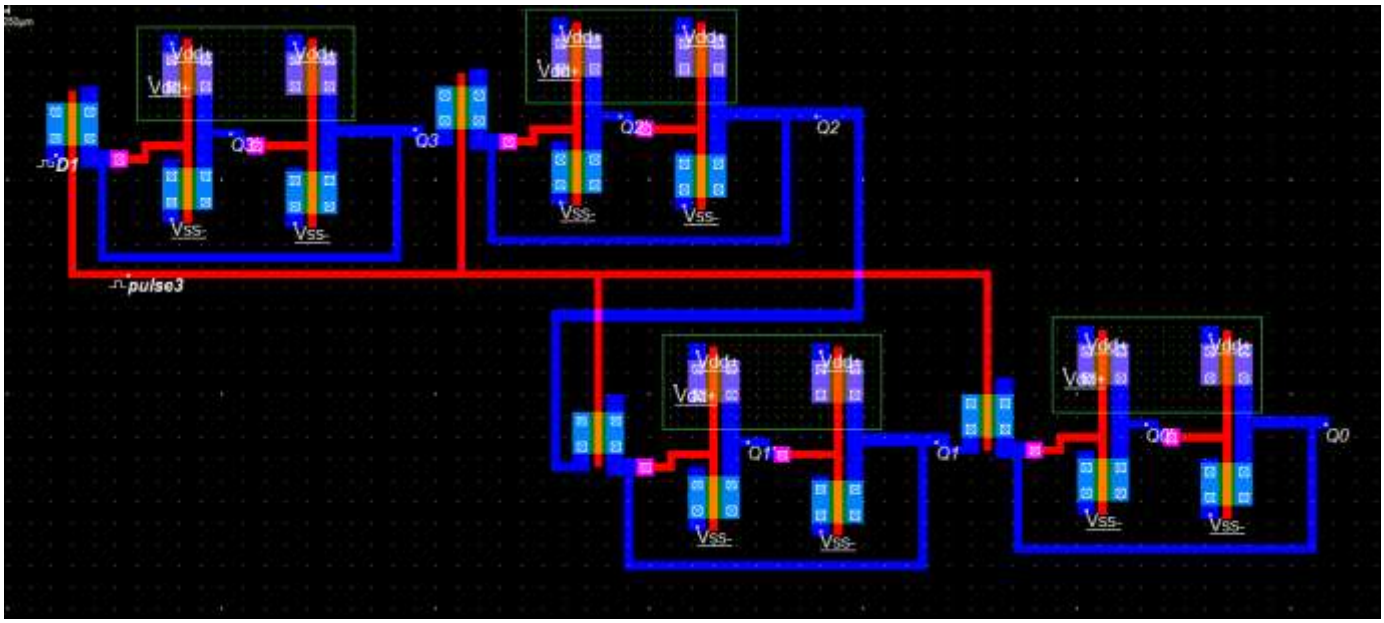
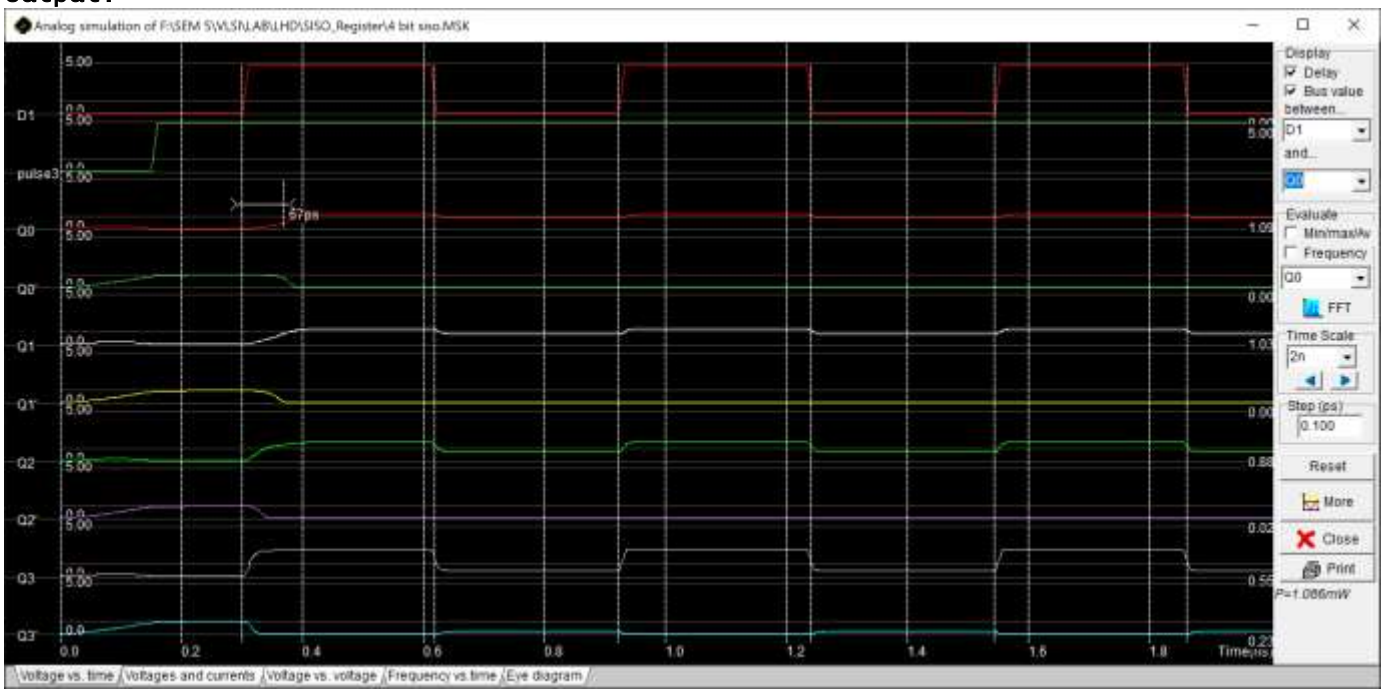
`Circuit:- SISO Register`



`Output:-`



Truth Table

A	B	GT	LT	EQ
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

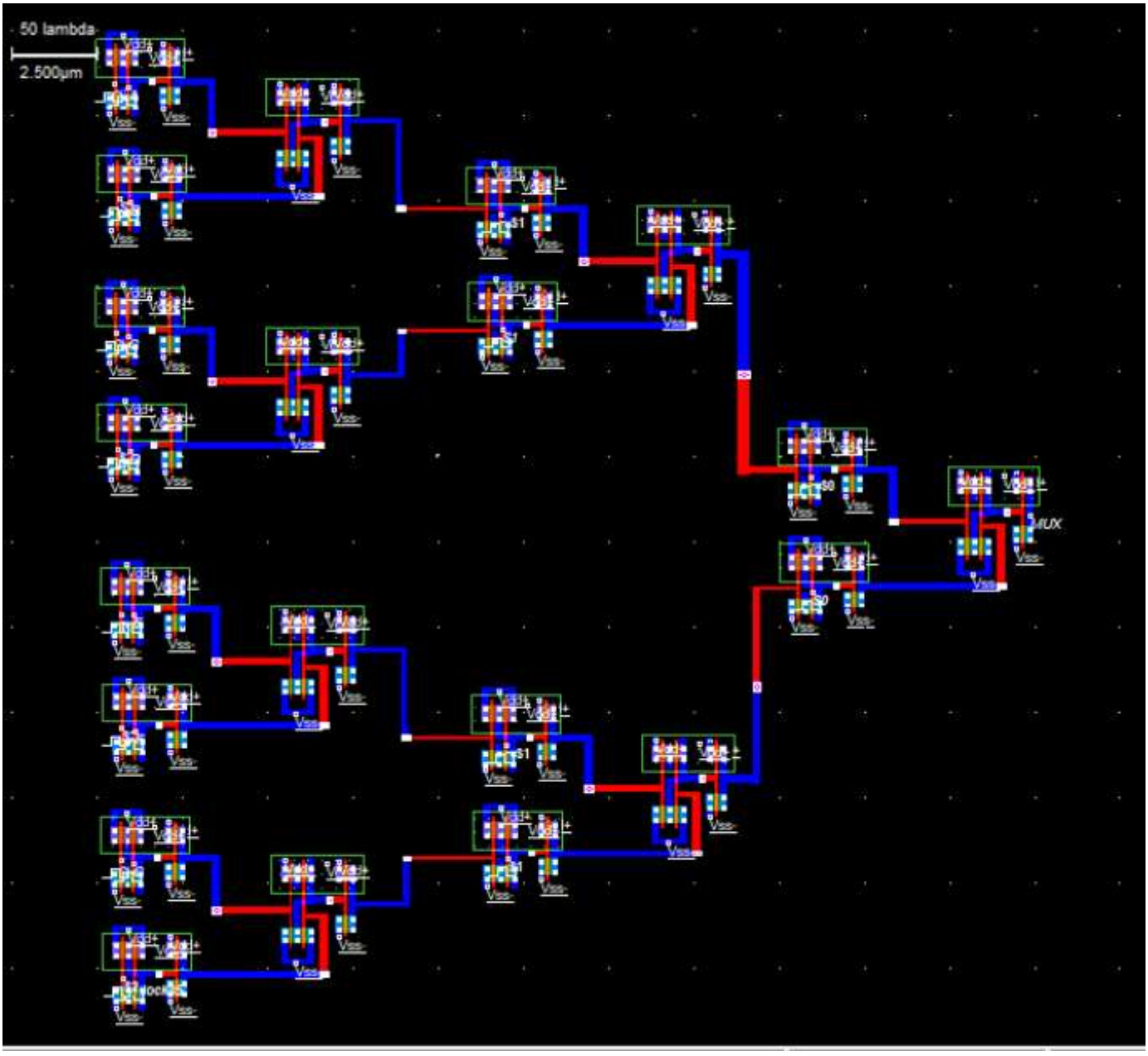
Logic Equations

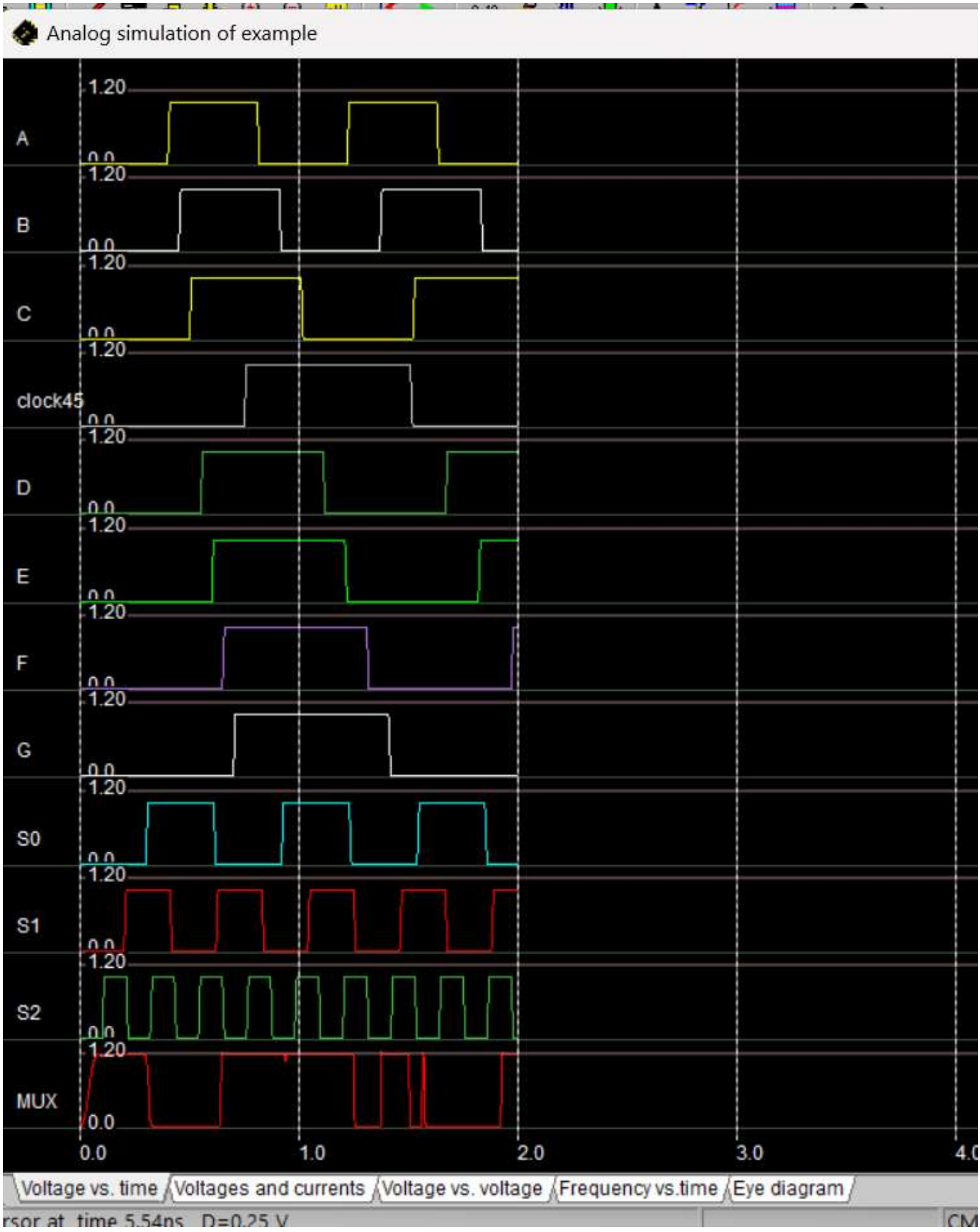
- GT (A > B): A·B⁻A \cdot \overline{B}A·B
- LT (A < B): A⁻·B\overline{A} \cdot BA·B
- EQ (A = B): (A·B)+(A⁻ B⁻)(A \cdot B) + (\overline{A}\,\overline{B})(A·B)+(AB)

Conclusion

The 1-bit magnitude comparator was successfully designed and verified. It correctly outputs greater, less, or equal conditions using simple AND/OR/NOT logic at the transistor level.

Circuit:- 8X1 MUX




Analog simulation of example
A
B
C
clock45
D
E
F
G
S0
S1
S2
MUX
1.20
0.0
0.0
1.0
2.0
3.0
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram

Truth Table

S2	S1	S0	Output (Y)
0	0	0	D0
0	0	1	D1
0	1	0	D2
0	1	1	D3
1	0	0	D4
1	0	1	D5
1	1	0	D6
1	1	1	D7

Logic Equation

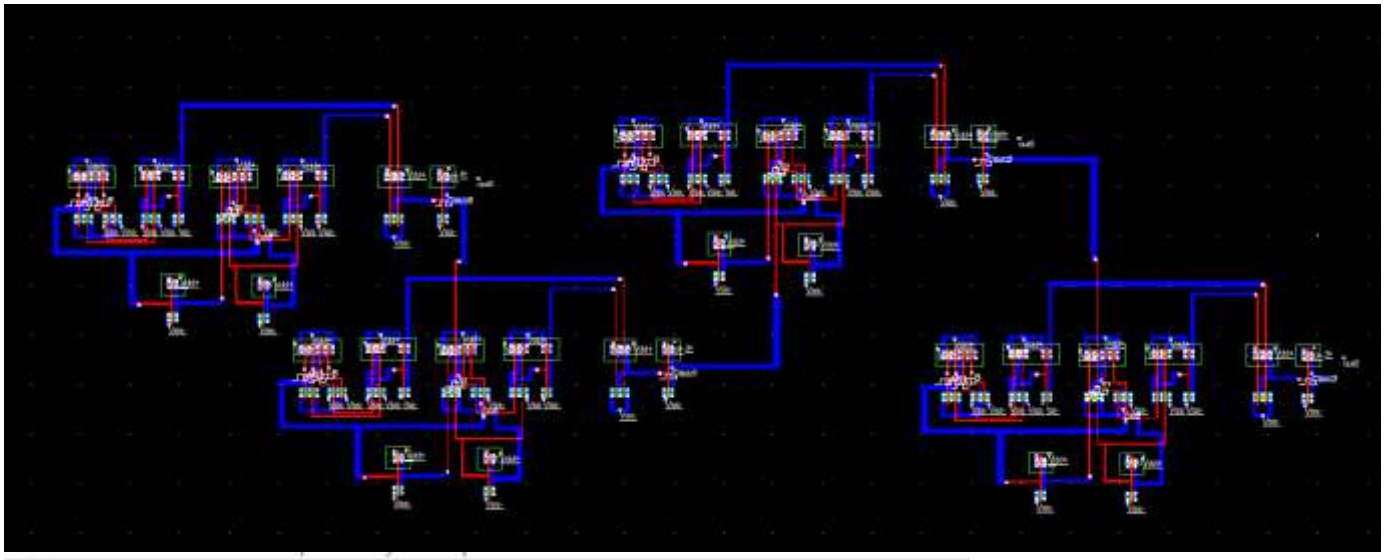
$$Y=S2'S1'S0'\cdot D0+S2'S1'S0\cdot D1+S2'S1S0'\cdot D2+S2'S1S0\cdot D3+S2S1'S0'\cdot D4+S2S1'S0\cdot D5+S2S1S0'\cdot D6+S2S1S0\cdot D7$$

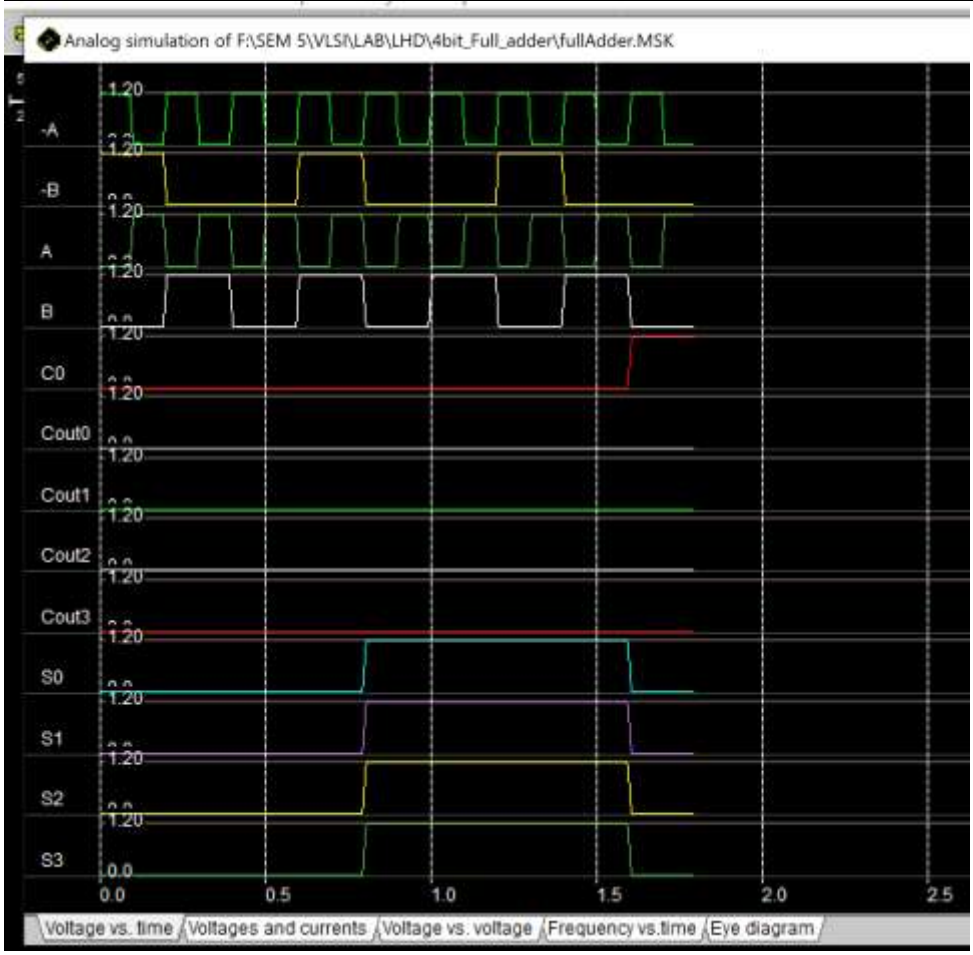
Conclusion

The 8:1 multiplexer was successfully designed and implemented at the transistor level using Microwind. The layout clearly demonstrates the use of selection logic (S2, S1, S0) to route one of eight input data signals to the output. Functional verification using simulation validated the truth table and logic equations, confirming that the circuit performs as expected. This design illustrates the efficiency of CMOS-based multiplexers and highlights their role as essential components in digital systems for data routing and logic simplification.

`Circuit:- 4 Bit Adder`

`Output:-`





equations:

- Sum = A ⊕ B ⊕ Cin
- Cout = A·B + Cin·(A ⊕ B)

Conclusion

The designed 4-bit ripple carry adder is expected to function correctly and produce accurate binary addition results. Although the simulation could not be performed successfully, based on the verified logic equations and truth tables, the circuit should generate the correct sum and carry outputs with ripple propagation delay across the four stages. The layout is consistent with the schematic, and once simulated with proper inputs and power connections, the waveforms will confirm the adder's expected operation.