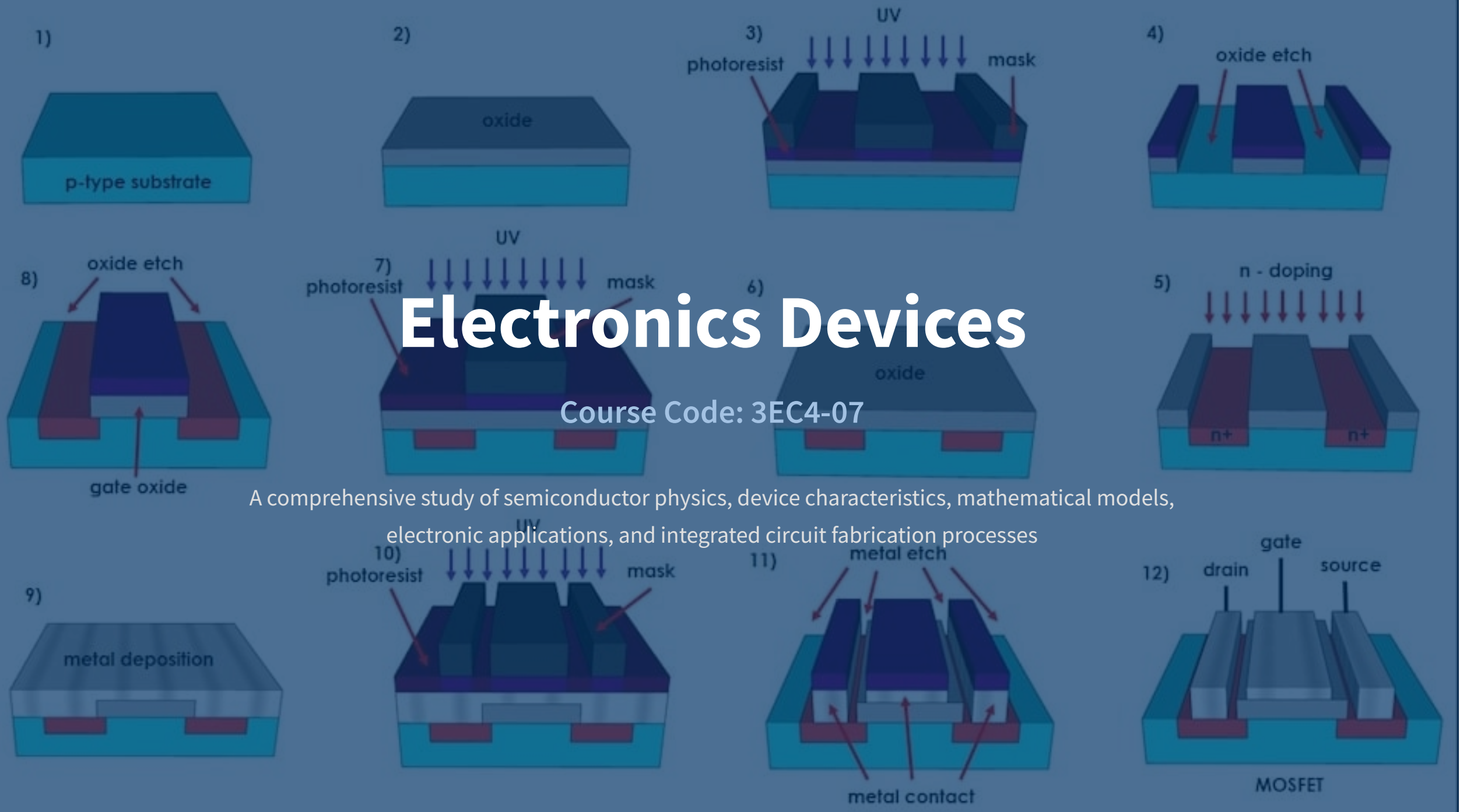
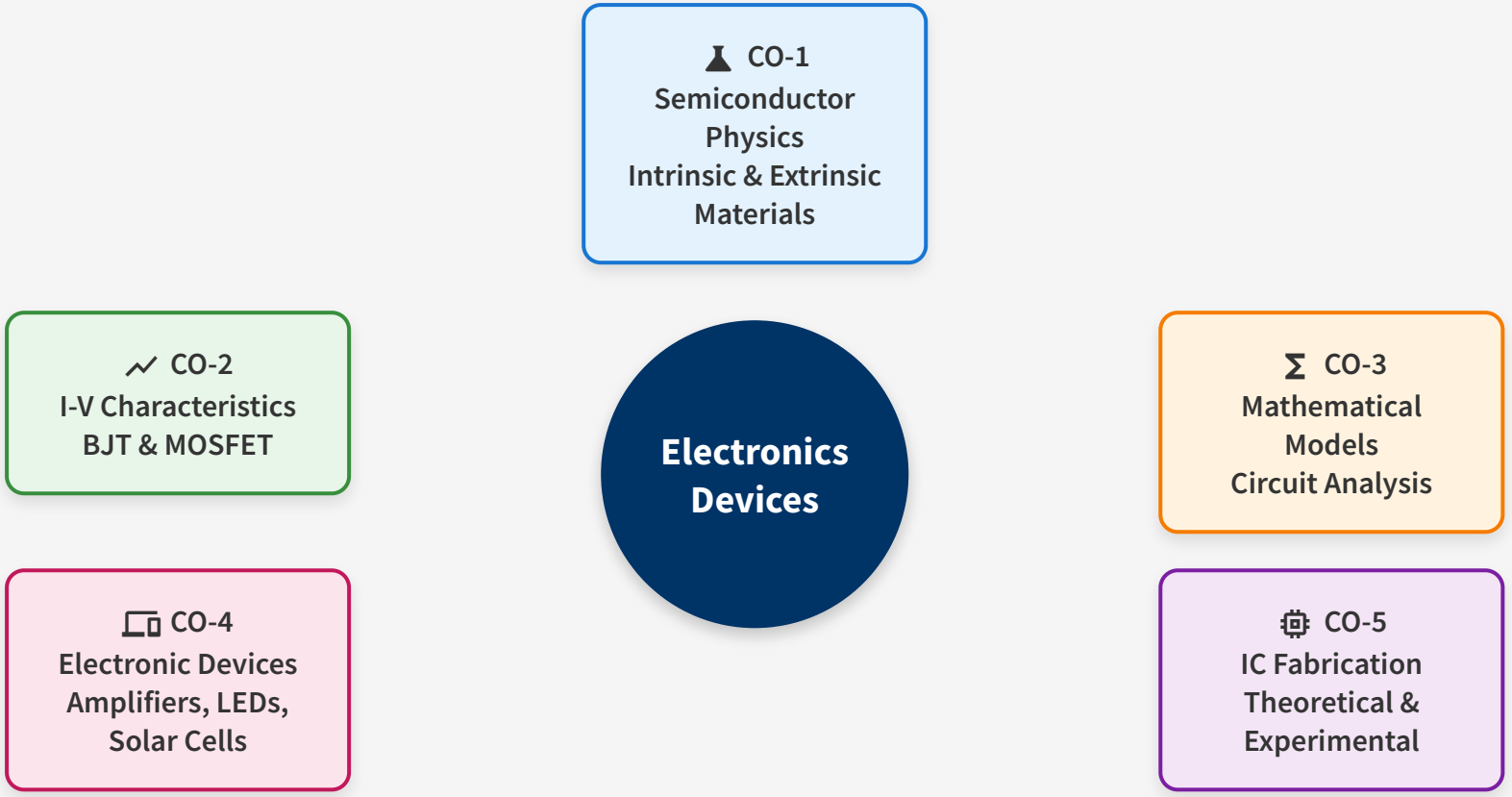


Electronics Devices

Course Code: 3EC4-07

A comprehensive study of semiconductor physics, device characteristics, mathematical models, electronic applications, and integrated circuit fabrication processes

Course Overview: Electronics Devices (3EC4-07)



CO-1.1: Introduction to Semiconductor Physics

Basic Concepts

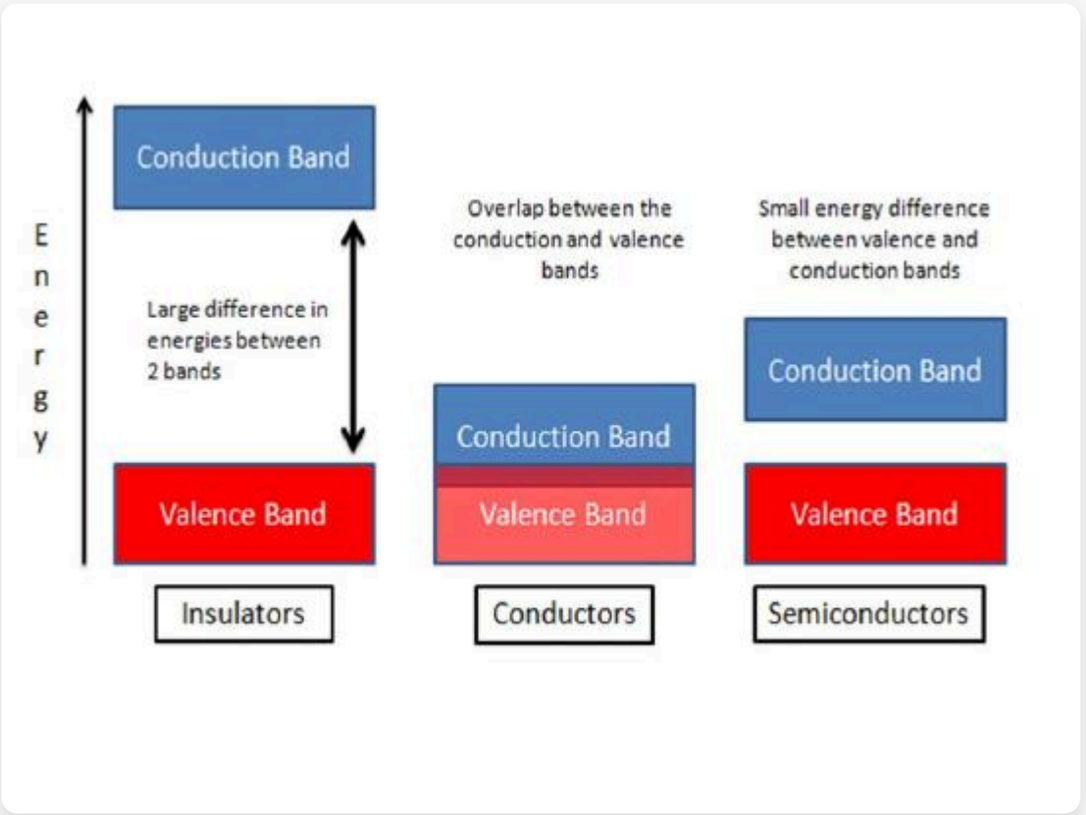
- Materials with electrical properties between **conductors** and **insulators**
- Electrical conductivity can be controlled by **doping** and external factors
- Most common semiconductors: **Silicon (Si)** and **Germanium (Ge)**

Band Theory

- **Valence band**: Electrons bound to atoms
- **Conduction band**: Free electrons that conduct electricity
- **Energy gap (Eg)**: Energy difference between valence and conduction bands
- In semiconductors, Eg is moderate (0.7-3.0 eV)

Semiconductor Classification

- **Intrinsic**: Pure semiconductor material
- **Extrinsic**: Doped semiconductor material
- Extrinsic types: **n-type** (electron majority carriers) and **p-type** (hole majority carriers)



CO-1.2: Intrinsic Semiconductors

Crystal Structure

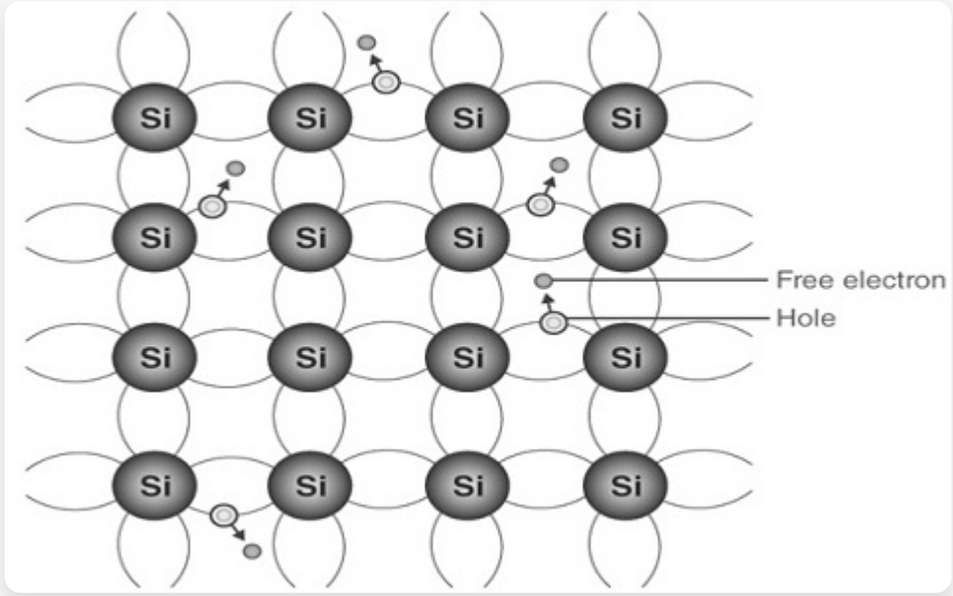
- **Pure semiconductor material** without impurities
- Silicon: **Diamond cubic lattice** with 4 covalent bonds per atom
- Germanium: Similar structure with larger lattice constant

Electron-Hole Pairs

- Thermal excitation creates **electron-hole pairs**
- Electrons promoted from valence to conduction band
- Holes act as **positive charge carriers**
- Generation-recombination equilibrium at thermal equilibrium

Carrier Concentration

- Intrinsic carrier concentration: $n_i = p_i$
- Temperature dependent: $n_i \propto T^{3/2} e^{-E_g/2kT}$
- At 300K: Si ($n^i \approx 1.5 \times 10^{10} cm^{-3}$), Ge ($n^i \approx 2.4 \times 10^{13} cm^{-3}$)



Conductivity

- Intrinsic conductivity: $\sigma = q(n_i\mu_n + p_i\mu_p)$
- Temperature dependent: $\sigma \propto e^{-E_g/2kT}$
- Electron mobility > Hole mobility
- Conductivity increases exponentially with temperature

$$\sigma_i = q \cdot n_i(\mu_n + \mu_p)$$

CO-1.3: Extrinsic Semiconductors

Doping Process

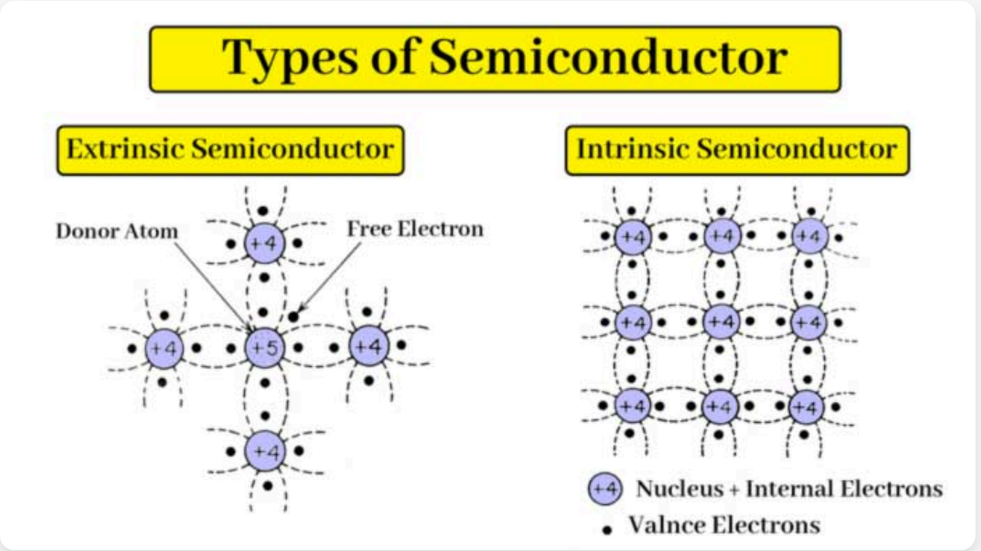
- **Intentional introduction** of impurity atoms
- Typical doping ratio: **1 impurity atom per 10^8 semiconductor atoms**
- Purpose: **Modify electrical properties** and increase conductivity
- Methods: Diffusion, ion implantation

n-Type Semiconductors

- Doped with **pentavalent impurities** (Group V elements)
- Common dopants: **Phosphorus (P)**, Arsenic (As), Antimony (Sb)
- **Donor atoms** provide extra electrons
- Electrons are **majority carriers**, holes are minority carriers

p-Type Semiconductors

- Doped with **trivalent impurities** (Group III elements)
- Common dopants: **Boron (B)**, Aluminum (Al), Gallium (Ga)
- **Acceptor atoms** create holes
- Holes are **majority carriers**, electrons are minority carriers



Comparison of Extrinsic Types

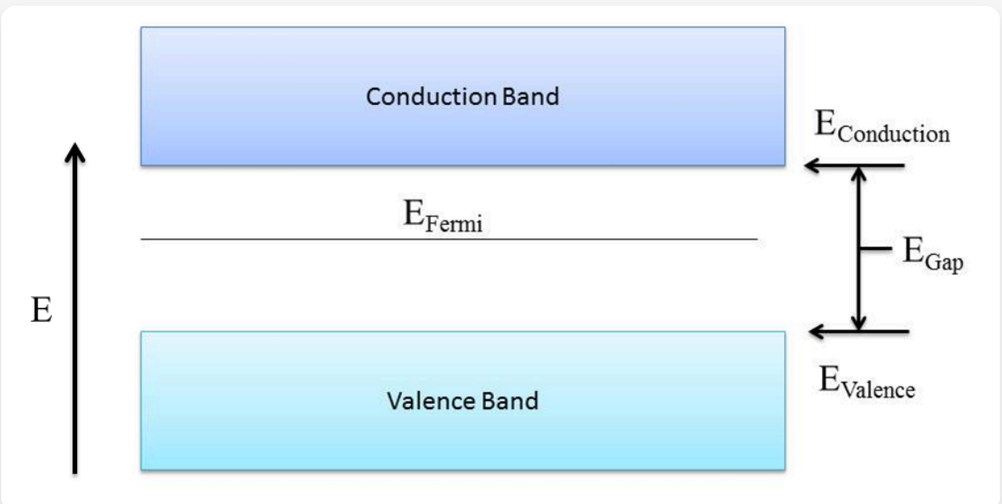
Property	n-Type	p-Type
Dopant Type	Pentavalent (Group V)	Trivalent (Group III)
Majority Carriers	Electrons	Holes
Minority Carriers	Holes	Electrons
Conductivity	$\sigma = q \cdot n \cdot \mu_n$	$\sigma = q \cdot p \cdot \mu_p$

$$n_d \approx N_D \text{ (donor concentration)}$$
$$p_a \approx N_A \text{ (acceptor concentration)}$$

CO-1.4: Energy Band Diagrams and Carrier Transport

Energy Band Diagrams

- **Intrinsic:** Fermi level near middle of band gap
- **n-type:** Fermi level shifts upward toward conduction band
- **p-type:** Fermi level shifts downward toward valence band
- Dopant energy levels: **Donor levels** near conduction band, **Acceptor levels** near valence band



Drift Mechanism

- Carrier motion under **electric field**
- Drift velocity: $v_d = \mu E$
- Drift current density: $J_{drift} = qn\mu_n E + qp\mu_p E$

Diffusion Mechanism

- Carrier motion due to **concentration gradient**
- Fick's Law: $J_{diff} = -qD_n\nabla n - qD_p\nabla p$
- Einstein relation: $D = \mu \cdot kT/q$
- Total current: $J = J_{drift} + J_{diff}$

Comparison of Transport Mechanisms

Property	Drift	Diffusion
Driving Force	Electric Field	Concentration Gradient
Direction	Same as field for electrons	From high to low concentration
Key Parameter	Mobility (μ)	Diffusion Coefficient (D)

Total Current Density:

$$J_n = qn\mu_n E + qD_n\nabla n$$

$$J_p = qp\mu_p E - qD_p\nabla p$$

CO-2.1: BJT Characteristics

Structure & Types

- Three-layer semiconductor device with**three terminals**
- **NPN:**P-type base between N-type emitter and collector
- **PNP:**N-type base between P-type emitter and collector
- Current flow:**Emitter → Base → Collector**

Operating Regions

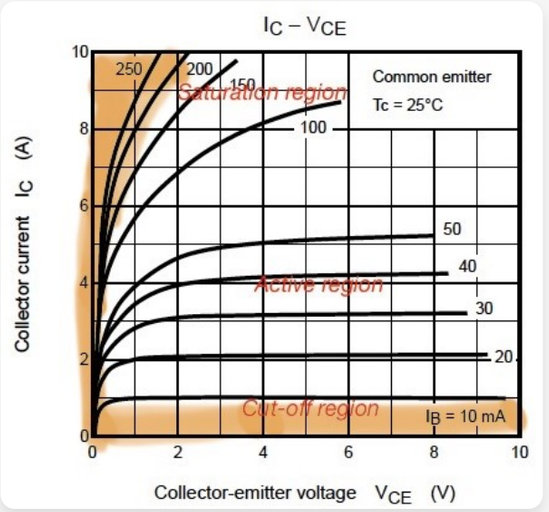
- **Cutoff:**Both junctions reverse-biased (no current)
- **Active:**EBJ forward-biased, CBJ reverse-biased (amplification)
- **Saturation:**Both junctions forward-biased (switch ON)
- Current relationship:$I_E = I_C + I_B$

Active Region Equations:

$$I_C = \beta \cdot I_B$$

$$I_E = (\beta+1) \cdot I_B$$

$$\alpha = \beta/(\beta+1)$$



I-V Characteristics

- **Input characteristics:**I_B vs. V_{BE} (diode-like)
- **Output characteristics:**I_C vs. V_{CE} (family of curves)
- Exponential relationship in active region:$I_C = I_S \cdot e^{V_{BE}/V_T}$

NPN vs PNP Comparison

Property	NPN	PNP
Majority Carriers	Electrons	Holes
Current Direction	Collector → Emitter	Emitter → Collector
Switching Speed	Faster	Slower

CO-2.2: BJT Current-Voltage Equations

Σ Active Region Equations

Collector Current:

$$I_C = I_S \cdot e^{V_{BE}/V_T}$$

Base Current:

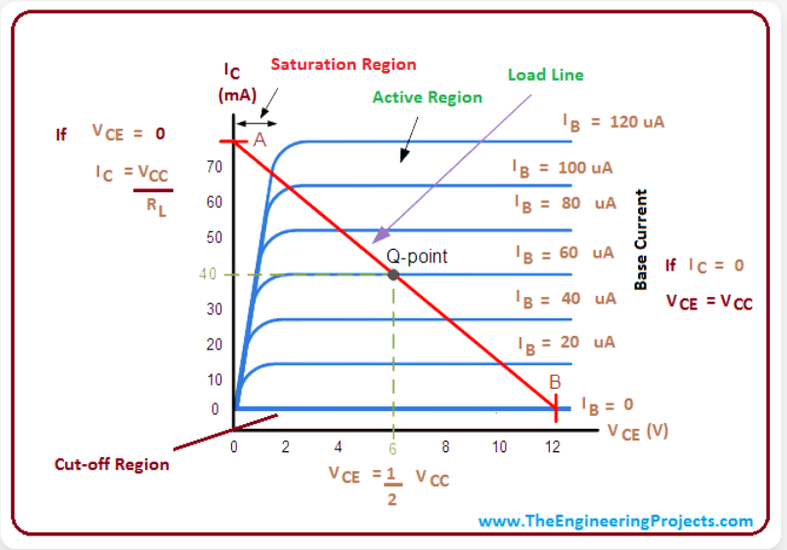
$$I_B = I_C/\beta = (I_S/\beta) \cdot e^{V_{BE}/V_T}$$

Emitter Current:

$$I_E = I_C + I_B = I_C(1 + 1/\beta)$$

Early Effect

- Base width modulation due to V_{CE} changes
- Increases collector current in active region
- Modified equation: $I_C = I_S \cdot e^{V_{BE}/V_T \cdot (1 + V_{CE}/V_A)}$
- V_A = Early voltage (typically 50-100V)



Temperature Effects

- V_{BE} decreases with temperature (~2mV/°C)
- I_S increases exponentially with temperature
- β increases with temperature
- Temperature coefficient: $dI_C/dT \approx I_C(kT/qV_{BE} + 1/T)$

Temperature-Dependent Saturation Current:

$$I_S(T) = I_S(T_0) \cdot (T/T_0)^3 \cdot e^{-E_g/k \cdot (1/T - 1/T_0)}$$

CO-2.3: MOSFET Characteristics

Structure & Types

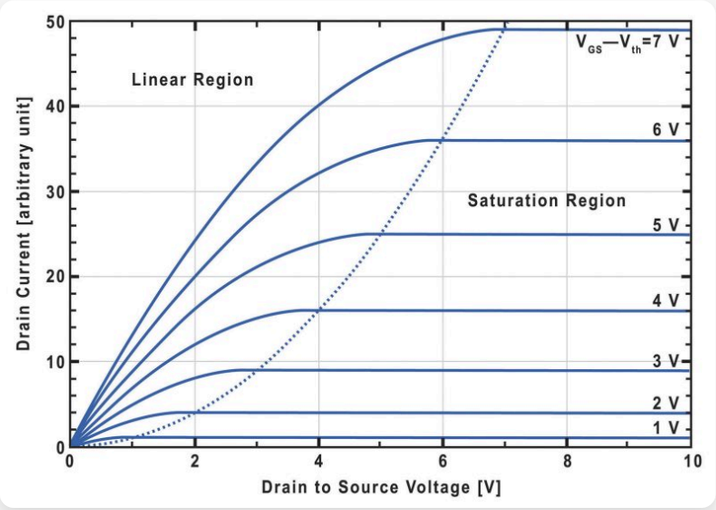
- Three-terminal device: **Gate, Source, Drain**
- **Enhancement mode:** No channel at $V^{GS}=0$
- **Depletion mode:** Channel exists at $V^{GS}=0$
- Channel types: **n-channel** (NMOS) and **p-channel** (PMOS)

Operating Regions

- **Cutoff:** $V^{GS} < V^{th}$ (no channel)
- **Triode/Linear:** $V^{GS} > V^{th}$, $V^{DS} < V^{GS} - V^{th}$
- **Saturation:** $V^{GS} > V^{th}$, $V^{DS} \geq V^{GS} - V^{th}$
- Channel pinches off at $V^{DS} = V^{GS} - V^{th}$

Threshold Voltage:

$$V_{th} = V_{FB} + 2\Phi_F + (\sqrt{(2q\varepsilon_{si}N_A 2\Phi_F)})/C_{ox}$$



I-V Characteristics

- **Transfer characteristics:** I^D vs. V^{GS}
- **Output characteristics:** I^D vs. V^{DS} (family of curves)
- Square-law relationship in saturation: $I_D \propto (V_{GS} - V_{th})^2$

NMOS vs PMOS Comparison

Property	NMOS	PMOS
Channel Type	Electrons	Holes
Current Direction	Drain → Source	Source → Drain
Mobility	Higher	Lower

CO-2.4: MOSFET Current-Voltage Equations and Comparison

Σ MOSFET I-V Equations

Cutoff Region:

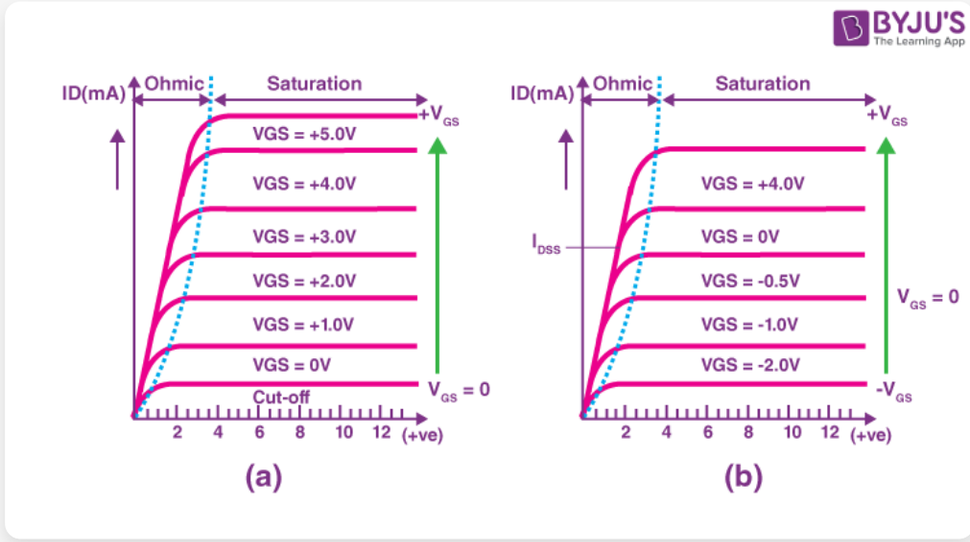
$I_D = 0$ (for $V_{GS} < V_{th}$)

Triode Region:

$I_D = K[(V_{GS} - V_{th})V_{DS} - V_{DS}^2/2]$

Saturation Region:

$I_D = (K/2)(V_{GS} - V_{th})^2$



Body Effect

- Threshold voltage changes with **source-bulk voltage**
- Modified threshold: $V_{th} = V_{th0} + \gamma(\sqrt{(2\Phi_F + V_{SB})} - \sqrt{(2\Phi_F)})$
- γ = body effect coefficient
- Significant when source is not at bulk potential

BJT vs MOSFET Comparison

Parameter	BJT	MOSFET
Control Mechanism	Current-controlled	Voltage-controlled
Input Impedance	Low	Very high
Switching Speed	Faster	Slower
Power Consumption	Higher	Lower
Integration Density	Lower	Higher

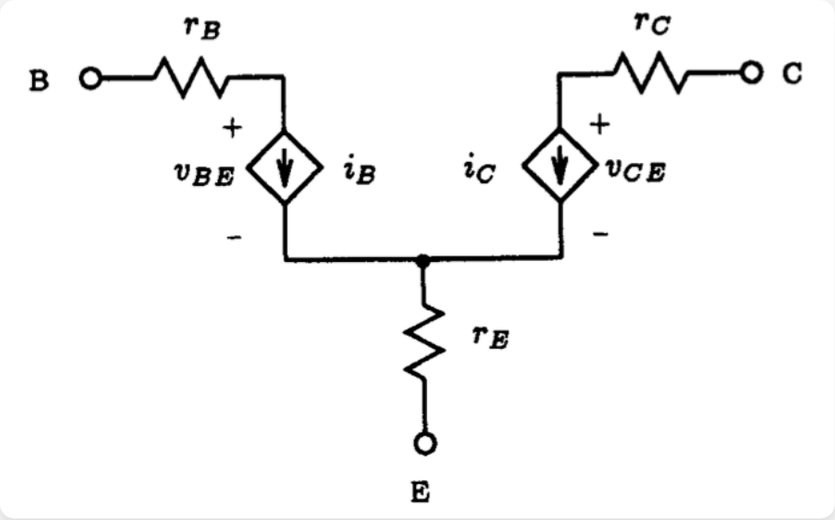
CO-3.1: BJT SPICE Models

SPICE Introduction

- **Simulation Program with Integrated Circuit Emphasis**
- Industry standard for **circuit simulation**
- Uses **mathematical models** to predict circuit behavior
- Enables analysis of complex circuits before physical implementation

BJT Model Parameters

Parameter	Description	Typical Value
IS	Saturation current	10^{-15} A
BF	Forward beta (β_F)	100-200
VAF	Forward Early voltage	50-100 V
NF	Forward emission coefficient	1.0



Equivalent Circuit Model

- Large-signal model includes **nonlinear elements**
- Current sources represent **exponential I-V relationships**
- Resistors model **ohmic regions** of the device
- Capacitors model **junction capacitances**

```
.MODEL Q2N2222 NPN (IS=1.41E-14 BF=200 VAF=74.3
IKF=0.28 ISE=2.41E-13 NE=1.857 BR=3 VAR=24)
```

Collector Current (Active Region):

$$I_C = I_S \cdot e^{V_{BE}/N_F V_T \cdot (1 + V_{CE}/V_{AF})}$$

CO-3.2: MOSFET SPICE Models

MOSFET Model Parameters

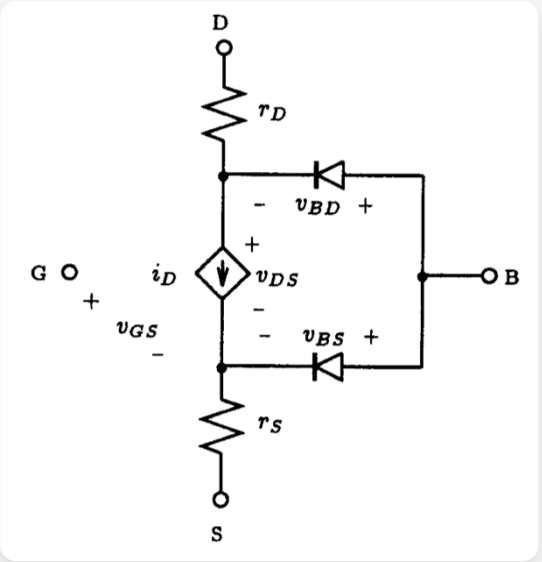
Parameter	Description	Typical Value
VTO	Zero-bias threshold voltage	0.5-1.0 V
KP	Transconductance parameter	20-100 μA/V^2
LAMBDA	Channel-length modulation	0.01-0.1 V^{-1}
GAMMA	Body effect coefficient	0.3-0.6 V^{1}/^{2}

Model Levels

Level 1
Schichman-Hodges
Square-law model

Level 2
Grove-Frohman
Includes short-channel effects

Level 3
Semi-empirical
Improved accuracy



Equivalent Circuit Model

- Current source models**channel conduction**
- Diodes model**junction behavior**
- Resistors model**series resistances**
- Capacitors model**junction capacitances**

```
.MODEL NMOSFET NMOS (LEVEL=1 VTO=0.7 KP=110E-6
LAMBDA=0.04 GAMMA=0.4)
```

Σ Level 1 Equations

- **Cutoff:** $I_D = 0$
- **Triode:** $I_D = KP \cdot (W/L) \cdot [(V_{GS}-V_{TH})V_{DS}-V_{DS}^2/2]$
- **Saturation:** $I_D = (KP/2) \cdot (W/L) \cdot (V_{GS}-V_{TH})^2$

CO-3.3: Small-Signal Models

Hybrid-pi Model for BJT

- Linearized model around **DC operating point**
- Key parameters: **g_m, r_π, r_o**
- Current-controlled voltage source
- Valid for **small AC signals** superimposed on DC bias

BJT Hybrid-pi Parameters

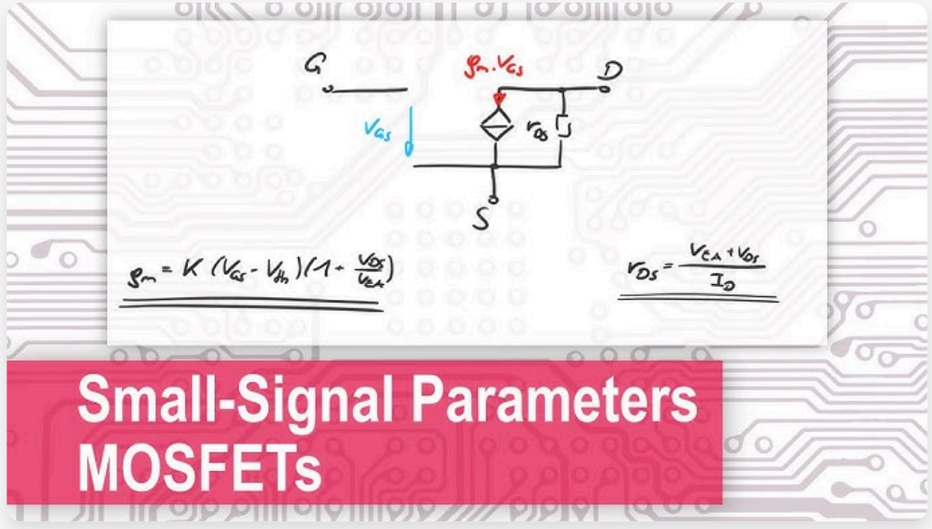
Transconductance: $g_m = I_C/V_T$

Input resistance: $r_\pi = \beta/g_m$

Output resistance: $r_o = V_A/I_C$

Small-Signal MOSFET Model

- Similar to BJT but **voltage-controlled**
- Key parameters: **g_m, r_{ds}, C_{gs}, C_{gd}**
- Infinite input resistance at low frequencies



MOSFET Small-Signal Parameters

Transconductance: $g_m = 2K(V_{GS}-V_{TH})$

Output resistance: $r_{ds} = 1/(\lambda I_D)$

Intrinsic gain: $A_v = g_m r_{ds}$

Parameter Extraction Techniques

- **g_m**: From slope of I^D vs. V^{GS} curve
- **r_o/r_{ds}**: From slope of I^C/I^D vs. V^{CE}/V^{DS}
- **Capacitances**: From S-parameter measurements
- **Temperature coefficients**: From measurements at different temperatures

CO-3.4: Application in Circuit Analysis

Biasing Techniques

- **Fixed bias:** Simple but unstable with temperature
- **Self-bias:** Improved stability through feedback
- **Voltage divider bias:** Most stable, widely used
- **Current mirror bias:** Used in integrated circuits

BJT Voltage Divider Bias

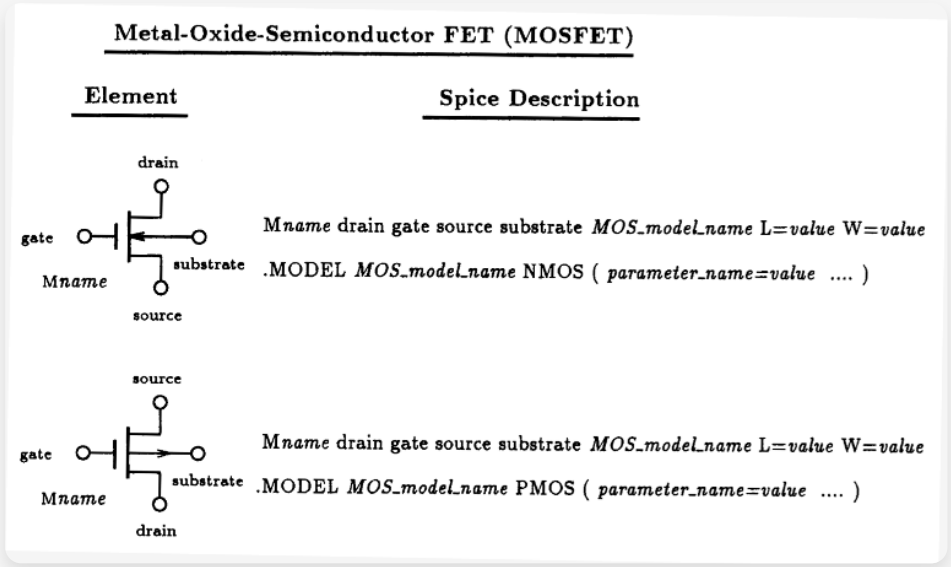
$V_B = V_{CC} \cdot R_2/(R_1+R_2)$

$I_C \approx (V_B - V_{BE})/R_E$

Stability factor: $S = (\beta+1)(1+R_B/R_E)$

Frequency Response Analysis

- **Low-frequency response:** Coupling and bypass capacitors
- **High-frequency response:** Device internal capacitances
- **Miller effect:** Amplifies input capacitance



MOSFET Current Mirror

$I_{out} = (W/L)_2/(W/L)_1 \cdot I_{ref}$

Key for biasing in analog ICs

Accuracy depends on device matching

Practical Examples

- **Amplifier design:** Gain, input/output impedance
- **Oscillator circuits:** Frequency stability analysis
- **Switching circuits:** Rise/fall time prediction
- **Temperature compensation:** Using model parameters

Gain Bandwidth Product:

$f_T = g_m/(2\pi C_\pi) \approx \beta \cdot f_\beta$

CO-4.1: Amplifier Configurations

BJT Configurations

Common-Emitter (CE)

- High voltage gain
- High current gain
- Moderate input impedance
- 180° phase shift

Common-Base (CB)

- High voltage gain
- Current gain ≈ 1
- Low input impedance
- No phase shift

Common-Collector (CC)

- Voltage gain ≈ 1
- High current gain
- High input impedance
- No phase shift

MOSFET Configurations

Common-Source (CS)

- High voltage gain
- High input impedance
- 180° phase shift
- Analogous to CE

Common-Gate (CG)

- High voltage gain
- Low input impedance
- No phase shift
- Analogous to CB

Common-Drain (CD)

- Voltage gain ≈ 1
- High input impedance
- No phase shift
- Analogous to CC

Key Characteristics Comparison

Configuration	Voltage Gain	Input Impedance	Phase Shift
CE / CS	High	Medium / High	180°
CB / CG	High	Low	0°
CC / CD	≈ 1	High	0°

CO-4.2: Light Emitting Diodes (LEDs)

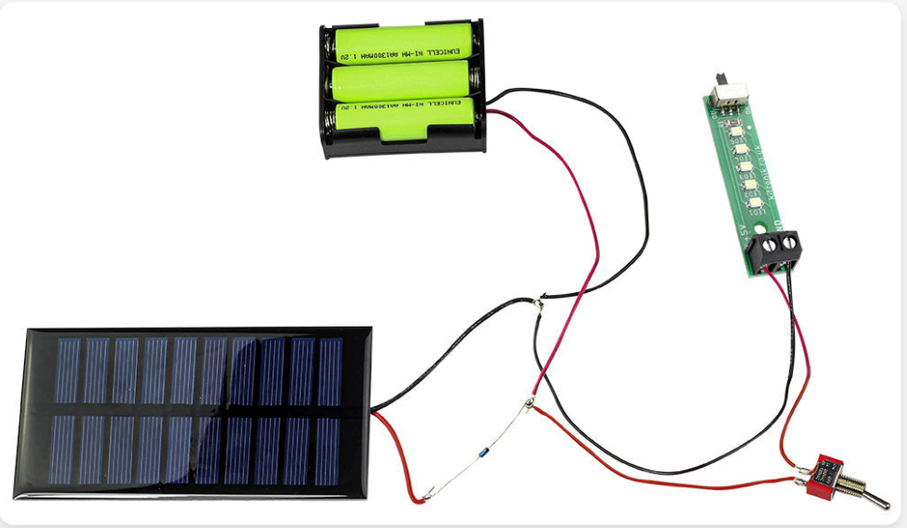
Operating Principles

- **Electroluminescence:** Light emission from electrical energy
- **Radiative recombination:** Electron-hole pairs release photons
- Photon energy: **$E = h\nu = E_g$**
- Color determined by **bandgap energy**

Materials & Structure

- **Direct bandgap materials:** GaAs, GaN, InP
- **Indirect bandgap materials:** Si, Ge (inefficient for LEDs)
- Structure: **p-n junction** with transparent encapsulant
- Doping: **p-type** and **n-type** regions for carrier injection

Wavelength-Color Relationship:
$\lambda = hc/E_g = 1.24/E_g$ (eV) [μm]



I-V Characteristics

- Similar to regular diode with **higher forward voltage**
- Forward voltage: **1.8-3.5V** (depends on color)
- Light output: **proportional to forward current**
- Efficiency: **20-50%** (much higher than incandescent)

Applications

- Display panels
- Lighting systems
- Traffic signals
- Optical sensors

CO-4.3: Solar Cells

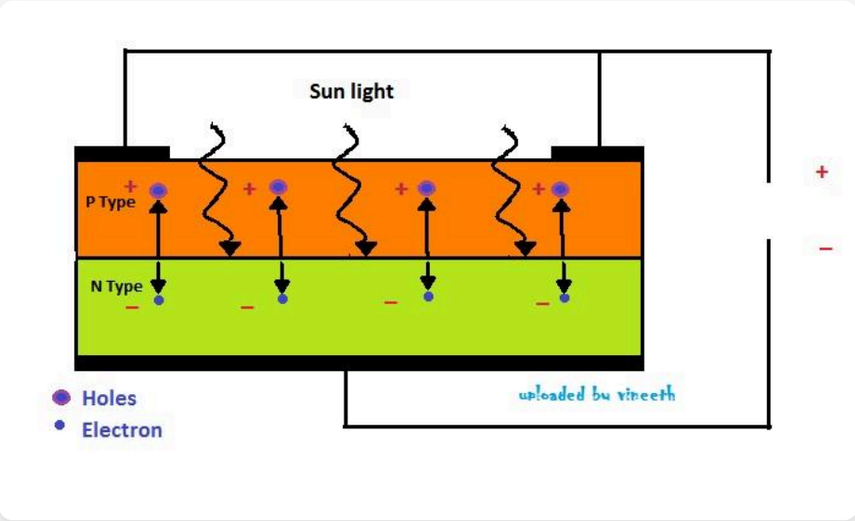
Photovoltaic Effect

- **Light absorption** creates electron-hole pairs
- **Built-in electric field** separates charge carriers
- Photons with **$h\nu \geq E_g$** generate current
- Excess energy lost as **heat**

p-n Junction Structure

- **Front contact:** Transparent conductive layer
- **Anti-reflection coating:** Maximizes light absorption
- **p-n junction:** Creates electric field
- **Back contact:** Metal electrode

Maximum Theoretical Efficiency (Shockley-Queisser):
$\eta_{max} \approx 33\%$ for Si ($E_g = 1.1$ eV)



I-V Characteristics

- **Short-circuit current (I_{SC}):** Maximum current at V=0
- **Open-circuit voltage (V_{OC}):** Maximum voltage at I=0
- **Maximum power point (MPP):** Optimal V and I
- Fill factor: **$FF = P_{max}/(V_{OC}I_{SC})$**

Efficiency Factors

- Bandgap energy
- Material purity
- Cell thickness
- Surface recombination

CO-4.4: Device Comparison and Integration

BJT vs MOSFET Performance

Parameter	BJT	MOSFET
Switching Speed	Higher	Lower
Power Consumption	Higher	Lower
Input Impedance	Lower	Higher
Integration Density	Lower	Higher
Thermal Stability	Lower	Higher

Device Selection Criteria

- Switching speed
- Power efficiency
- Integration density
- Application requirements

Integrated Circuit Applications

Digital Logic

- CMOS technology dominates
- Low power consumption
- High integration density

Analog Circuits

- BJTs for high-speed applications
- MOSFETs for precision
- BiCMOS combines both

Power Electronics

- MOSFETs for switching
- IGBTs for high power
- Wide bandgap materials

CO-5.1: IC Fabrication Overview

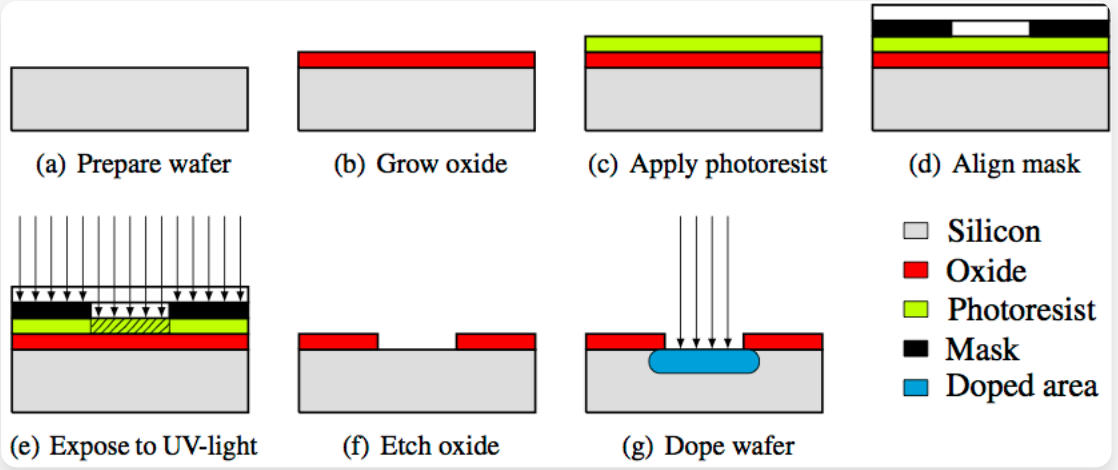
IC Fabrication Introduction

- Process of creating **integrated circuits** on semiconductor wafers
- Combines **physics**, **chemistry**, and **engineering**
- Enables **miniaturization** and **mass production**
- Critical for modern **electronics industry**

Cleanroom Requirements

Class 1-100 Cleanrooms

- **Particle control:** < 100 particles/ft^3
- **Temperature control:** ±0.1°C
- **Humidity control:** 40-50% RH
- **Specialized filtration:** HEPA/ULPA



Process Flow

- Wafer preparation
- Lithography
- Etching
- Deposition
- Oxidation
- Doping

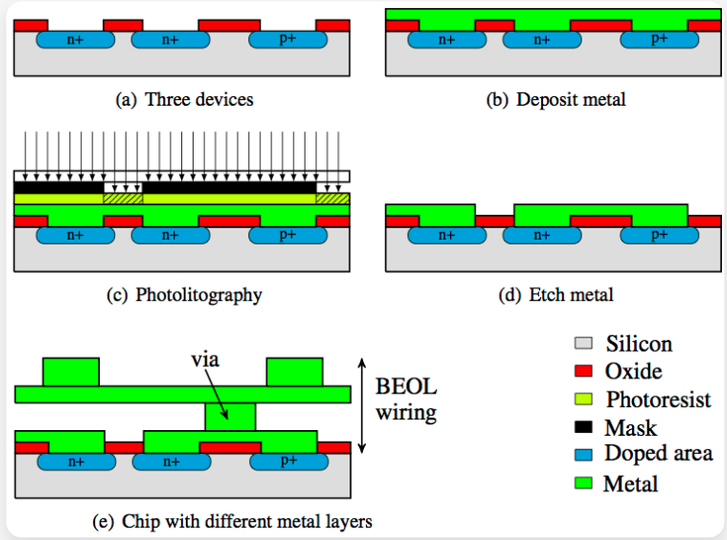
CO-5.2: Wafer Preparation and Oxidation

Crystal Growth

- **Czochralski (CZ) method:** Most common for Si
- **Float-zone (FZ) method:** Higher purity Si
- **Liquid encapsulation:** For compound semiconductors
- Growth parameters: **temperature gradient**, **pull rate**, **rotation**

Wafer Slicing & Polishing

- **Slicing:** Diamond saws create thin wafers
- **Lapping:** Removes saw damage, flattens surface
- **Etching:** Chemical removal of surface damage
- **Polishing:** Creates mirror-like surface
- Standard wafer sizes: **200mm**, **300mm**



Thermal Oxidation

Oxidation Methods

- **Dry oxidation:** $Si + O_2 \rightarrow SiO_2$ (slow, high quality)
- **Wet oxidation:** $Si + H_2O \rightarrow SiO_2$ (faster, lower quality)

Temperature: 800-1200°C

Oxide thickness: 10nm-10µm

Growth rate: ~100nm/hr

Stress control critical

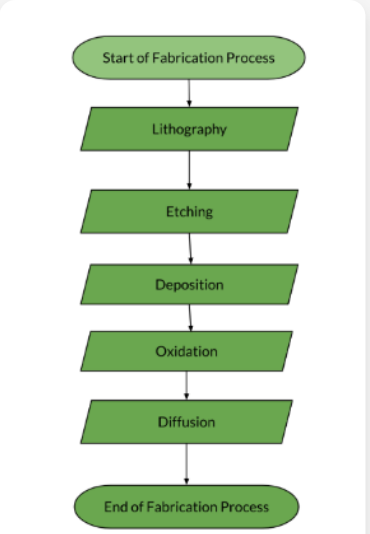
CO-5.3: Lithography and Etching

Photolithography Process

- **Wafer cleaning:**Removes contaminants
- **Photoresist coating:**Spin coating creates uniform layer
- **Soft bake:**Removes solvent from resist
- **Exposure:**UV light transfers pattern
- **Development:**Removes exposed/unexposed areas
- **Hard bake:**Improves resist adhesion

Mask Design

- **CAD tools:**Layout design software
- **Resolution limits:**Feature size constraints
- **Critical dimension (CD):**Smallest feature size
- **Optical proximity correction:**Compensates for diffraction



Etching Techniques

Wet Etching

Dry Etching

Etching Comparison

- **Wet:** Isotropic, fast, simple equipment
- **Dry:** Anisotropic, precise, complex equipment

Pattern Transfer

- **Additive process:**Material deposition in pattern
- **Subtractive process:**Material removal in pattern
- **Lift-off technique:**Pattern deposition then resist removal
- **Alignment:**Critical for multi-layer patterns

CO-5.4: Doping and Metallization

Doping Processes

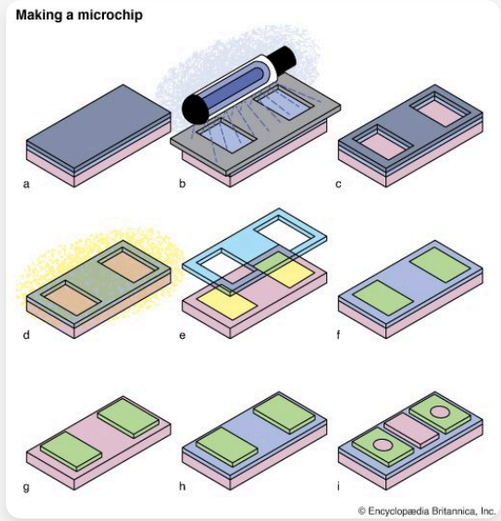
Diffusion | Ion Implantation

Diffusion

- **High temperature** process (900-1100°C)
- **Source:** Solid or gas dopants
- **Profile:** Gaussian distribution
- **Limitation:** Lateral diffusion

Ion Implantation

- **Room temperature** process
- **Source:** Ion beam
- **Profile:** Precise control
- **Advantage:** Maskable doping



Metallization

- **Materials:**Aluminum, copper, tungsten
- **Deposition:**Physical vapor deposition (PVD)
- **Patterning:**Photolithography + etching
- **Damascene process:**Copper interconnects

Packaging

- **Die attachment:**Epoxy or solder
- **Wire bonding:**Gold or aluminum wires
- **Encapsulation:**Plastic or ceramic
- **Lead frames:**Connection to PCB

Summary: Key Concepts & Interconnections

CO-1: Semiconductor Physics

- **Intrinsic:** Pure semiconductors
- **Extrinsic:** Doped semiconductors
- **n-type:** Electron majority carriers
- **p-type:** Hole majority carriers

CO-2: I-V Characteristics

- **BJT:** Current-controlled device
- **MOSFET:** Voltage-controlled device
- **Operating regions:** Cutoff, Active/Saturation
- **Mathematical models:** Exponential/Square-law

CO-3: Mathematical Models

- **SPICE models:** Circuit simulation
- **Small-signal models:** Hybrid-pi
- **Parameter extraction:** Model accuracy
- **Circuit analysis:** Design tools

CO-4: Electronic Devices

- **Amplifiers:** Signal processing
- **LEDs:** Light emission
- **Solar cells:** Energy conversion
- **Device selection:** Application-specific

CO-5: IC Fabrication

- **Wafer preparation:** Crystal growth
- **Lithography:** Pattern transfer
- **Etching:** Material removal
- **Doping:** Impurity introduction

Key Applications

- **Digital circuits:** Logic gates, processors
- **Analog circuits:** Amplifiers, filters
- **Power electronics:** Converters, drivers
- **Optoelectronics:** Displays, sensors

Interconnections

Physics → Characteristics | Characteristics → Models | Models → Applications | Applications → Fabrication

References

Textbooks

- **Sedra & Smith**- Microelectronic Circuits
- **Jaeger & Blalock**- Microelectronic Circuit Design
- **Streetman & Banerjee**- Solid State Electronic Devices
- **Sze & Ng**- Physics of Semiconductor Devices

Research Papers

- **SPICE Models**- IEEE Trans. on Electron Devices
- **Nakamura et al.**- GaN LED Technology (Nature)
- **Shockley & Queisser**- Solar Cell Efficiency
- **Schichman & Hodges**- MOSFET Modeling

Online Resources

- **GeeksforGeeks**- Semiconductor Tutorials
- **Electronics-Tutorials.ws**- Device Characteristics
- **All About Circuits**- Circuit Analysis
- **LibreTexts**- Semiconductor Physics

Academic Resources

- **MIT OpenCourseWare**- Microelectronics
- **Berkeley EECS**- Device Modeling
- **Stanford EE**- IC Fabrication
- **Purdue ECE**- Semiconductor Devices

For additional resources and detailed information, refer to course materials and university library databases.

Questions & Answers

Thank You For Your Attention

Feel free to ask questions about any of the topics covered

- **Semiconductor Physics**
- **Device Characteristics**
- **Mathematical Models**
- **Electronic Applications**
- **IC Fabrication**
- **Practical Examples**

Contact: electronics@example.edu