KESHAV MEMORIAL INSTITUTE OF TECHNOLOGY Narayanaguda, Hyderbad-500029

FACULTY PROFILE

1. NAME :KOMIRA YAKAIAH

2. JNTUH REGISTRATIONID :8299-150408-125903

3. DATE OFBIRTH :15-02-1983

4. DESIGNATION :ASSISTANT PROFESSOR

5. YEARS OF EXPERIENCE :13

6. UGDEGREE :B.TECH(ECE)

7. PGDEGREE :M.TECH(VLSI SD)

8. Ph.D(AREA OF THE PH.D WORK) :---

9. SUBJECTS TAUGHT

> DIGITAL SIGNAL PROCESSING

> CONTROL SYSTEM

> SIGNALS AND SYSTEM

VLSI DESIGN

> SIGNALS AND STOCHASTIC PROCESS

> Etc....

10. PAPER PUBLICATIONS IN INTERNATIONAL JOURNALS:

- i. Design of low voltage low power high gain full swing operational amplifier
- ii. A reconfigurable vlsi architecture for mixed radix fft
- iii. Analysis of multiple reduced hypercube interconnection network properties of both diameter and network cost

11. PAPER PUBLICATIONS IN INTERNATIONAL CONFERENCES:

Title with Page Nos.	Details of	ISSN/ISBN No.
	Conferen	
	ce	
	Publicati	
	on	
	Title with Page Nos.	Conferen ce Publicati

12. PAPER PUBLICATIONS IN NATIONAL CONFERENCES:

S. No.	Title with Page Nos.	Details of Conference Publication	ISSN/ISBN No.
1	DESIGN OF BLANKING		
	INTERFACE MODULE (BIM) &		
	DUTY CYCLE MEASUREMENT		
	(DCM) MODULE FOR EXTERNAL		
	SYSTEM INTERFACE UNIT FOR		
	RECEIVER APPLICATION		
2	Implementation of an Adaptive Filter for Pattern Processing in an 'N' Element Patch Antenna Array using space frequency adaptive processor		

- 13. RESEARCH PROJECTS UNDERTAKEN WITH NAME OF THE SPONSORING AGENCY:
- 14. RESEARCH GUIDANCE: College
- 15. CONTRIBUTIONS AT THE DEPARTMENTAL LEVEL:
- 16. CONTRIBUTIONS ATTHE COLLEGE LEVEL:
- 17. REFRESHER COURSES/ WORKSHOPS/CONFERENCES ATTENDED:

	Attended:			
	Name of the Course / Summer School	Place	Duration	Sponsoring Agency
1	Attended a two week Workshop on CMOS, MIXED SIGNAL AND RFIC DESIGN conducted by IIT-Kharagpur	Hyderabad	15 days	IIT Karagpur
2	Advanced front end VLSI systems prototyping using FPGA's	Hyderabad	6 days	KMIT
3				
4				
5				
6				

18. WORKSHOPS/ CONFERENCES/SEMINARS/FDP's ORGANIZED:

WORKSHOPS/ CONFERENCES/SEMINARS/FDP	Place	Duration	Sponsoring Agency
Organized FDP on Advance vlsi system	Hyderabad	6 days	KMIT

19. MEMBERSHIPOFPROFESSIONALBODIES: Member of ISTE

20. ANY OTHER CONTRIBUTION: