

# KESHAV MEMORIAL INSTITUTE OF TECHNOLOGY

## Narayanaguda,Hyderbad-500029

### FACULTY PROFILE

photo



1. NAME : J.Kamal Vijetha
2. JNTUH REGISTRATION ID : 78150406-161537
3. DATE OF BIRTH : 31/12/1982
4. DESIGNATION : Assistant professor
5. YEARSOFEXPERIENCE : 12 years
6. UG DEGREE : 2004
7. PG DEGREE : 2008
8. Ph.D(AREA OF THE PH.D WORK) :
9. SUBJECTSTAUGHT :
  - Basic Electrical Engineering
  - Analog Electronics
  - VLSI
  - Embedded system
  - Digital electronics
  - Image Processing

### 10. PAPER PUBLICATIONS INTERNATIONAL JOURNALS:

- I. **Design and Simulation of Low Power 10T Full Adder using Cadence 16nM Technology** J.Kamal Vijetha<sup>1</sup> , G. Hari Krishna<sup>2</sup> <sup>1</sup>, <sup>2</sup>Electronics and Communication Engineering, Keshav Memorial Institute of Technology 'International Journal for Research in Applied Science & Engineering Technology (IJRASET) ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.177 Volume 7 Issue VII, July 2019
- II. **Design Of Folded Cascode Operational Amplifier Using 1.8micron CMOS Technology** K.Rajesh Kumar, <sup>2</sup> V.Praveena, <sup>3</sup> J.Kamal Vijetha, January 2018, Volume 5, Issue 1 JETIR (ISSN-2349-5162) Electronics and Communication Engineering KMIT, Hyderabad, India
- III. **Secure Electronic Voting Machine with Finger Print Based Biometric System** Nalluri Veda Kumar<sup>1</sup> , G.V.R.L.Maccalay<sup>2</sup> , J.Kamal Vijetha<sup>3</sup> <sup>1,2</sup>, ISSN: 2321-9653 International Journal for Research in Applied Science & Engineering Technology (IJRASET) ©IJRASET 2015: All Rights are Reserved 618
- IV. **Controlling Relays Using Pass Key & Added Servers Using Iot** Jeji Katuri <sup>#1</sup> , J.Kamal Vijetha<sup>#2</sup> , Jagan Rampalli<sup>#3</sup> <sup>#1</sup>.Asst.Professor,Electrical & Electronics Engineering, CMR Technical Campus, Hyd. <sup>#2</sup>.Asst.Professor, Electronics & Communications Engineering, KMIT, Hyd <sup>#3</sup>.Asst.Professor, Electrical & Electronics Engineering, GNIT, Hyd. In 4 th international conference 2019 ICIEEE.GNIT,HYDERABAD

**11. PAPER PUBLICATIONS IN INTERNATIONAL CONFERENCES:**

S. No.	Title with Page Nos.	Details of Conference Publication	ISSN/ISBN No.
1	Example....	NCRTIT-13, Elsevier, March'13	ISBN 978-93-5107-051-1

**12. PAPER PUBLICATIONS IN NATIONAL CONFERENCES:**

S. No.	Title with Page Nos.	Details of Conference Publication	ISSN/ISBN No.

**13. RESEARCH PROJECTS UNDERTAKEN WITH NAME OF THE SPONSORING AGENCY:****14. RESEARCH GUIDANCE:****15. CONTRIBUTIONS AT THE DEPARTMENTAL LEVEL:**

- Placement cell committee in 2020
- Comprehensive Viva In charge 2017
- Involved in NBA Criterion 9.2 & 9.3
- Overall mentoring In charge 2018
- As Class In charge
- As Mentor for students

**16. CONTRIBUTIONS AT THE COLLEGE LEVEL:**

- Was part of Trishul programme.2016
- Part of website committee from 2019
- Was part of SIH 2019- guided 2 teams upto internal hackthon

# 17. REFRESHERCOURSES/WORKSHOPS/CONFERENCESATTENDED:

	<b>Attended:</b>			
	<b>Name of the Course / Summer School</b>	<b>Place</b>	<b>Duration</b>	<b>Sponsoring Agency</b>
1	Introduction to Data Science in Python	Online,Course era	2 months	KMIT
2	Programming for everybody	online Course era	2 months	KMIT
3	Introduction to artifical intelligence	online Course era	2 months	KMIT
4	Online quiz in Digital Systems	HITS hyderabad	1 day	KMIT
5	Three Days Online FDP on IOT	Lendi, Kakinada	27 th to 29 th May 2020	KMIT
6	NPTEL online Certification in BEE	online	Jul-dec2019	KMIT
7	NPTEL online Certification in ElectronicDevice Fabrication	online	Jul-dec2019	KMIT
8	Under Gone a orkshop on" Research Trends and Embedded systems",	JNTUH	November 2016	KMIT
9	Under Gone a workshop on" Research Trends and Embedded systems",	KMIT	March 2017	KMIT
10	Participated in <b>25th International conference</b> on" VLSI system Design" conducted by,	IEEE & VEDAII.T.	Jan 2012.	
11	Participated in <b>Two Day workshop</b> on on" VLSI system Design" conducted by,	JNTU, Kakinada.	Sep 2008.	
12	Participated in <b>Two Day workshop</b> on "CMOS VLSI and ASIC Design" conducted by,	JNTU, Hyderabad	August 2007.	
13	Participated in <b>Two Day workshop</b> on "CMOS VLSI and ASIC Design" conducted	by, JNTU, Hyderabad	August 2007.	
14	Undergone <b>short term Course</b> on "Low power VLSI"	in SNIST ,Hyderabad	Dec 2007	

15	Undergone <b>IBM Academic Initiative</b> on “Open Source & IBM Software Workshop”	<b>IBM</b>	Dec 2006.	
16	Trained for <i>Refresher Course</i> conducted by .	UGC-ASC, JNTU, Hyderabad during December 2004 .	December 2004 .	

**18. WORKSHOPS/ CONFERENCES/SEMINARS/FDP'sORGANIZED:**

WORKSHOPS/ CONFERENCES/SEMINARS/FDP	Place	Duration	Sponsoring Agency

**19. MEMBERSHIPOFPROFESSIONALBODIES:** Member of The Society of Digital Information and Wireless Communications

**20. ANY OTHERCONTRIBUTION:**