College Station
Texas(TX), 77840

# Likhith Kumar Reddy Usthili

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## Education

**Texas A&M University (GPA: 4.0/4.0)** **College Station, Texas, USA** **Aug 2022 – Aug 2024(Expected)**

- **Master of Science (MS) in Computer Engineering(VLSI)**
- **Coursework :** Adv Digital System Design, Computer Architecture, Parallel Computing, Microprocessor System Design.

**Amrita Vishwa Vidhyapeetam (3.7/4)** **Kerala, India** **July 2014 – June 2018**

- Bachelor of Technology in Electronics and Communication Engineering, First Class Graduate (Distinction).
- **Coursework :** Digital electronics and System Design, VLSI Design, Microcontrollers and processors.

## Work Experience And Research Interns

**Senior Engineer | Multimedia** **Samsung Semiconductor India R&D** **Nov 2019 - Aug 2022**

- Chip design and verification in Multimedia(ISP) IP DV team under System LSI at Samsung Semiconductor India R&D (SSIR).
- RTL Design of IP modules and wrappers. Review of CDC reports mitigating violations for a subsystem.
- Full ownership of post-processing blocks of ISP. Lead the test bench architecture and test plan creation for the flagship camera feature.
- Implemented the register abstract model to access the DUT registers and memories using UVM RAL.
- Built constrained random Test benches using UVM and system-level test case development, regressions and failure analysis. Worked on AXI and AHB interface BFM.
- Experience in design, simulation, debugging, assertions, waveform analysis, coverage development, closure and automation using scripting languages like Perl, python.

**Research Assistant | Cache Labs** **Amrita Vishwa Vidyapeetam ,India** **August 2018 – August 2019**

- Building a roofline model and estimating the performance of a given kernel of application on CPU, GPU and FPGA.
- Mapping the work distribution of a kernel and a computing platform or combination of platforms to maximize the kernel computing efficiency.
- Building a single board computer on a zed board and running multiple applications using Xilinx SDK.

**Research Scholar | Dr.Das Labs** **Pennsylvania State University,USA** **Jan 2018 - June 2018**

- Studied spatiotemporal dynamics of T-cells lymphocytes for generating secure cryptographic keys and extended for physically unclonable functions (PUF).
- Implemented MATLAB image processing algorithm for generating 2D cryptographic keys from pixelated T-cell images.
- **Techniques:** Image processing, image segmentation, filters and subject detection, cryptography, Raman Spectroscopy, electron ablation, exfoliation.
- **Publications:**"Biological One-Way Function for Secure Key Generation" in Applied theory and simulations. **Link**.
- **Publications:** "Biological - Physically Unclonable Function (Bio-PUF)" in Nature Communication Physics. **Link**.

## Skills

- **Programming:** Verilog, System Verilog, UVM (Intermediate), Assembly language.
- **Tools:** Xilinx, Vivado HLS, Cadance Xcelium, IMC, Simvision, Questasim, Spyglass CDC, Lint.
- **Scripting Languages:** Perl , TCL, Python(Intermediate). **Protocol:** UART, AHB, APB, AXI.

## Academic Experience

- **Edge-Detection, UART** Complete RTL Design and verification using UVM and C-based reference model with Scorboarding, assertion checks and coverage closure.
- **Cache Simulator** Designed to simulate cache substitutions using replacement policies (FIFO and LRU) and write back. Simulates the hit/miss behavior on traces and outputs the stats.
- **Hybrid Branch Predictor** Worked on developing a hybrid branch predictor using TAGE and Loop Predictor. The chooser was implemented using a 3-bit tournament prediction algorithm.
- **Physical design of an 8-bit adder (Layout Design )** Implemented schematic and layout of Inverter, NAND, XOR and 8-Bit Adder(using fundamental adders) and verified using NC-Verilog.
- **Intelligent parking model with security System:** A Miniature Model of Security system with PIC16F877A microcontroller.