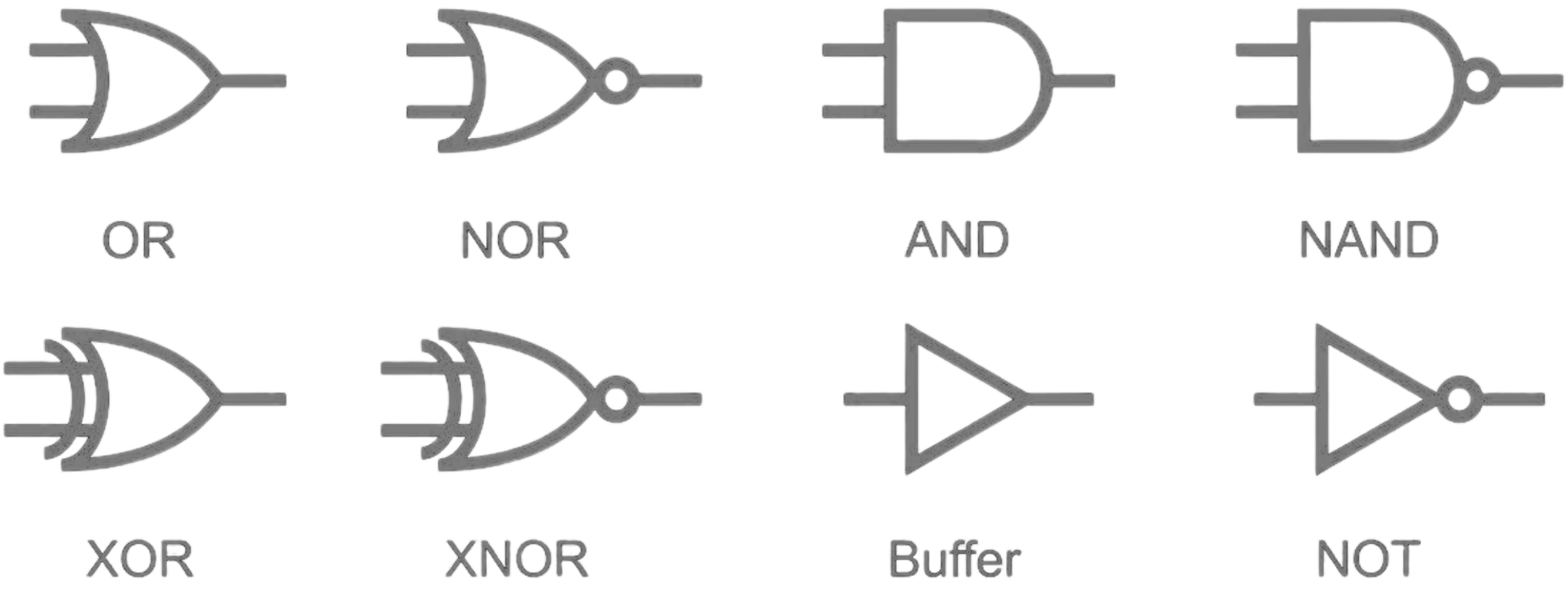
DIGITAL DESIGN



JAIRAJ MIRASHI
DESIGN VERIFICATION ENGINEER

RONALD J TOCCI & MORRIS MANO

Syllabus :

↳ (Ronald - J Tocci)
↳ (Morris Mano)

Basics

- Logic Gates (with and without propogation Delay)
- Boolean Algebra
- Simplification (K-MAP)
- Number System

Combinational Circuits

- Full adder / Half adder
- Ripple carry adder
- Carry look Ahead Adder
- Half and full subtractor
- MUX, DEMUX → (with and without delay)
- ENCODER, DECODER
- Comparator, Convertors
- Parity checkers
- Imp. Equivalent circuit of each logic Gate

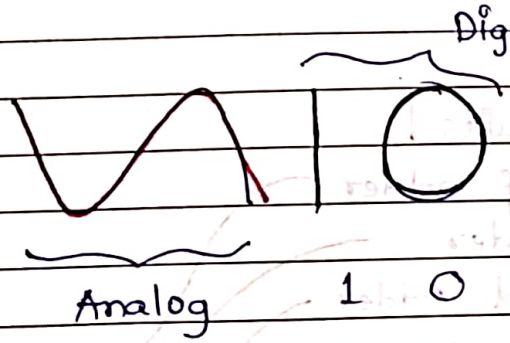
Sequencial Circuits

- Imp. Flip - flops (SR, JK, T & D), transition Diagram
- Latches
- Counters (Asynchronus & Synchronus) comparisons
- UP / Down counters.
- shift registers and its applications
- Imp. concept of setup and hold time

PAGE NO. :
DATE : / /

Advantages of Digital Electronics (DE)

- Data compression is possible in digital electronics
- Storage of information / data is possible in DE
- DE system is less immune to noise. Performance of digital communication is better with respect to analog communication (In reference with noise).



Sony vaio

Ex: Digital speedometer
Digital watches
Scanner
camera → Pixel.
Microphone
Data storage (Pen drives)

Digital Electronics → circuit Designing (using logic Gates)
↓
Information in form of 1's and 0's

High	Low
1	0
+5 V	0 V ⏚ (ground)
Mark	space

PAGE NO. :
DATE : / /

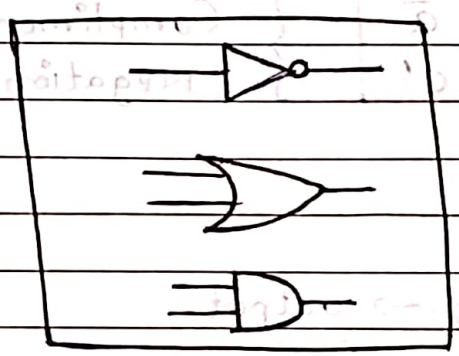
- Logic Gate : Basic fundamental unit of DE

↳ which consist of n number of input but it can have only one output

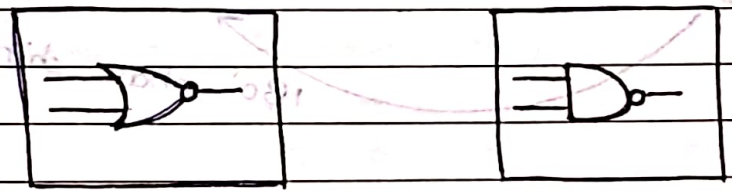
- classification of logic gates

① Basic Gates → NOT, OR, AND, Buffer
② Special Gates → XOR, XNOR.
③ universal Gates → NAND, NOR

Basic Logic Gate : using this we can design any digital electronic circuit.



Universal Logic Gate : using this we can design any digital electronic circuit.

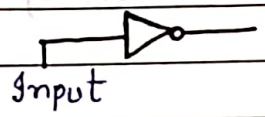


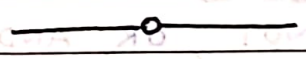
PAGE NO. :
DATE : / /

BASIC LOGIC GATES.

① NOT - GATE / Invertor / Phase Shifter

Symbol



input a  Y output

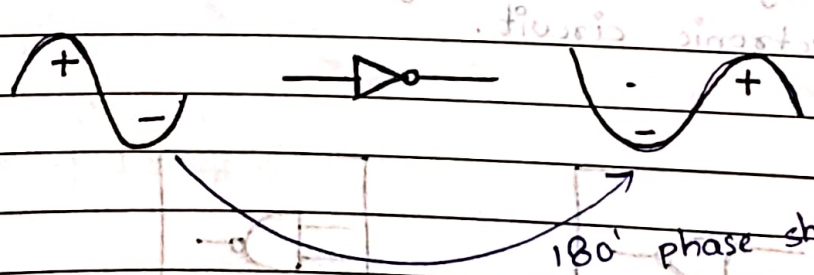
Input C Y output

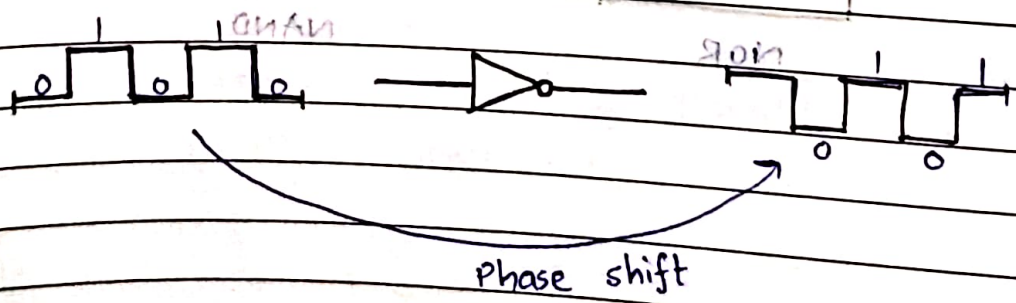
Mathematically,

$$\boxed{\begin{aligned} Y &= \bar{a} \\ Y &= C' \end{aligned}} \Bigg\} \begin{array}{l} \text{Complimentory operator} \\ \text{Negation / Not operator} \end{array}$$

Truth table

Single Input →	a	Y → output
	0	1
	1	0

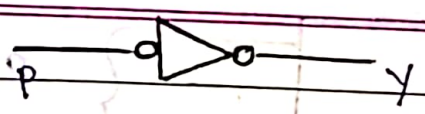




PAGE NO. :
DATE : / /

5

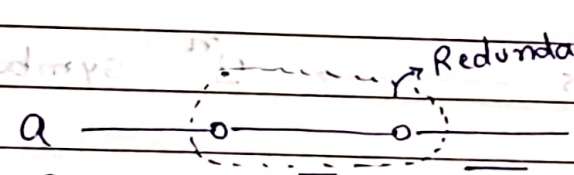
- Buffer



$\boxed{Y = P}$

(Two invertors)

Axiom :



$\equiv$ a —— Y.

a	$\bar{a}$	$\bar{\bar{a}}$
1	0	1
0	1	0

output is same as input

Conclusion :

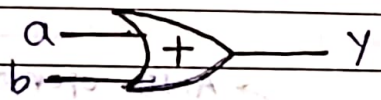
$$\bar{\bar{a}} = a$$
$$\overline{\overline{xy}} = xy$$
$$\overline{\overline{\overline{abc}}} = \overline{abc}$$

$\boxed{\bar{\bar{f}} = f}$.

(2) OR - Gate

Symbol

OR operator



Mathematically

$\boxed{Y = a+b}$ → $a \vee b$

a OR b.

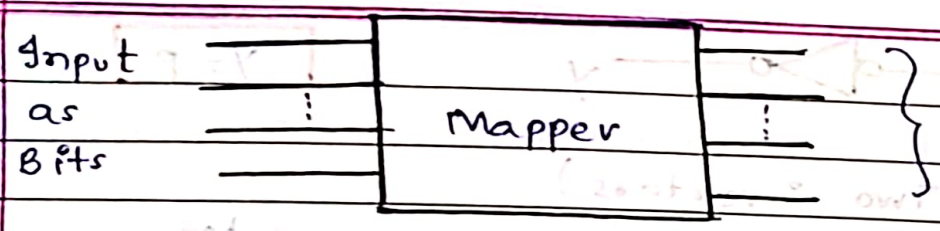
Truth table : (2 input OR)

a	b	Y
0	0	0
0	1	1
1	0	1
1	1	1

→ unique output.

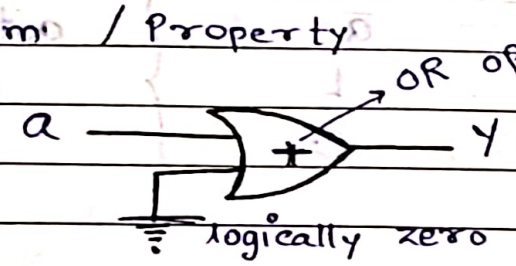
{ output is logically zero when all inputs are logically zero }

PAGE NO. :
DATE : / /



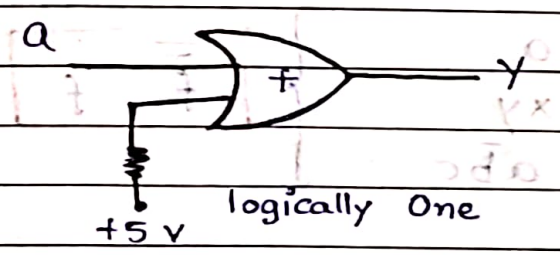
n-Bits $\longrightarrow$ 2^n symbols

Axiom / Property



Additive Identity

$a + 0 = a$

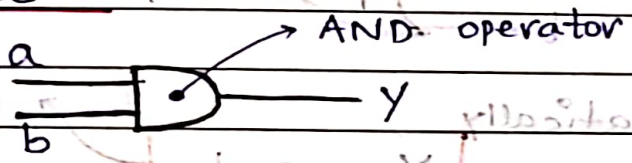


$a + 1 = 1$

Any function + 1 = 1.

AND - Gate :

symbol



Mathematically

$Y = a.b$ $\rightarrow$ $a \wedge b$

(a AND b)

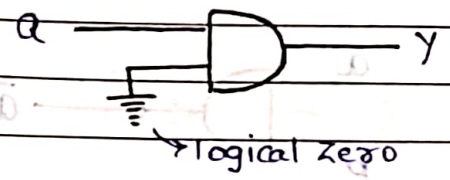
Truth - Table

a	b	Y
0	0	0
0	1	0
1	0	0
1	1	1

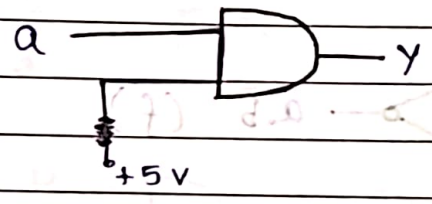
$\longrightarrow$ unique output. (for all input 1)

PAGE NO. :
DATE : / /

Axiom :



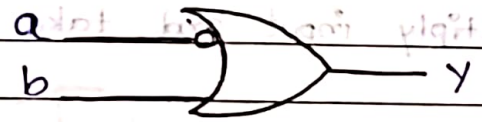
$a \cdot 0 = 0$



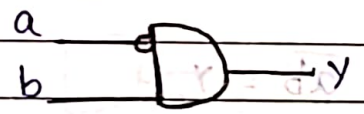
$a \cdot 1 = a$ → Multiplicative Identity.

Note : (Any function $\cdot\, 0 = 0$)

Inhibitor : (meaning to stop)



$y = \bar{a} + b$

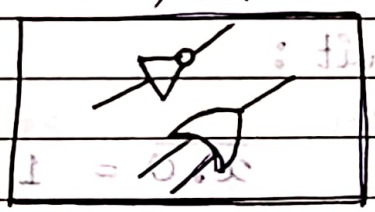


$y = \bar{a} \cdot b$.

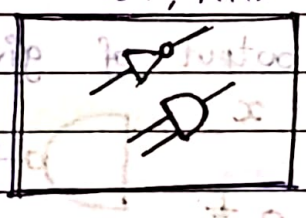
} Inhibitor circuit

- Inhibitor is constructed using basic logic gate.
- It is also an example of universal logic gate

NOT, OR



NOT, AND

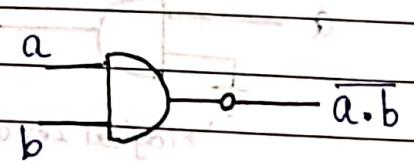


sufficient enough to design any circuit

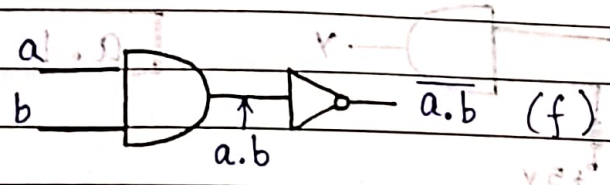
PAGE NO. :
DATE : / /

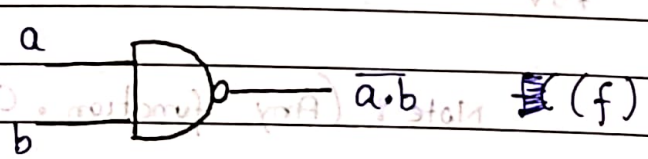
Universal Logic Gates

① NAND → AND Gate
Not Gate at the output of AND gate



Symbol





Mathematically : $\boxed{Y = \overline{a.b}}$

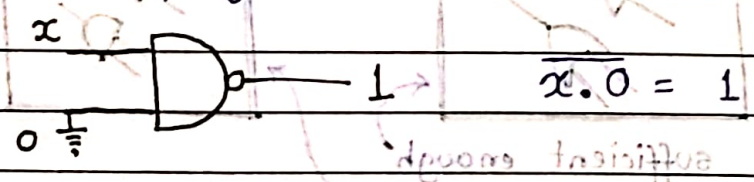
Note : Multiply input and take compliment

Truth table :

a	b	ab	$\overline{ab} = Y$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

unique input → unique output

Ex Find the output of given circuit :

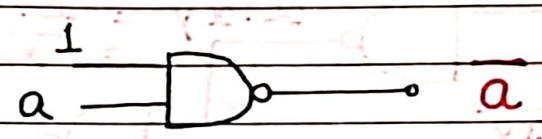


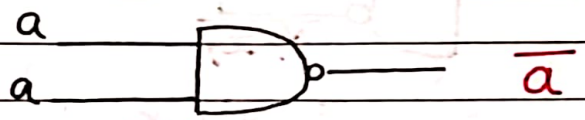
If 1 input of NAND Gate is 0, then output is 1 and it is independent of other input.

PAGE NO. :
DATE : / /

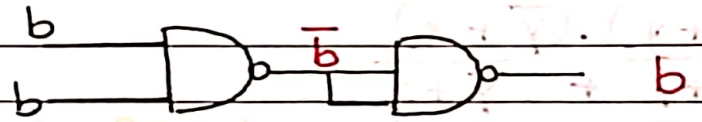
a

Find the simplified output for given circuit

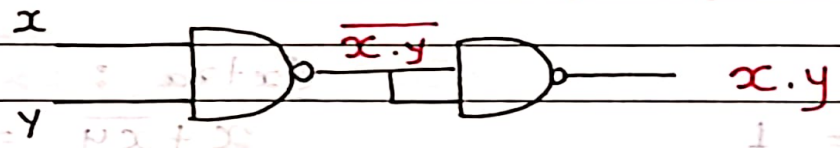




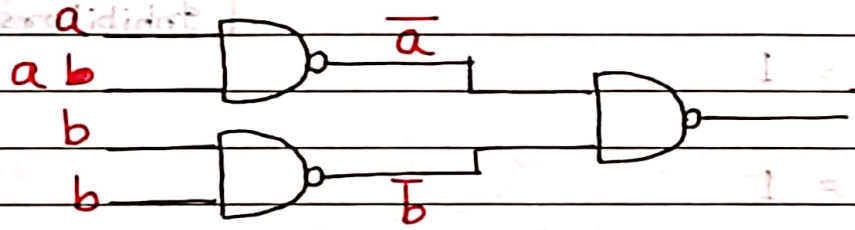
[NOT GATE]
(Requires 1 NAND)



[buffer]



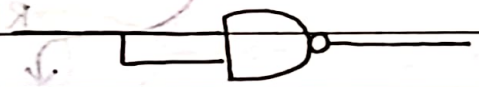
[AND GATE]
[Requires 2 NAND]



$\overline{\overline{a}.\overline{b}} = a+b$

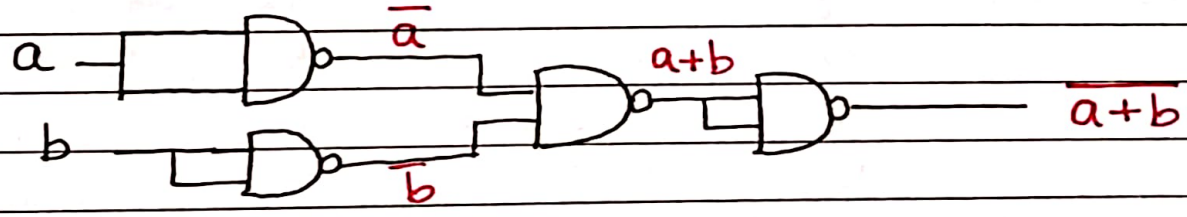
[OR GATE]
(Requires 3 NAND)

Short circuit NAND.



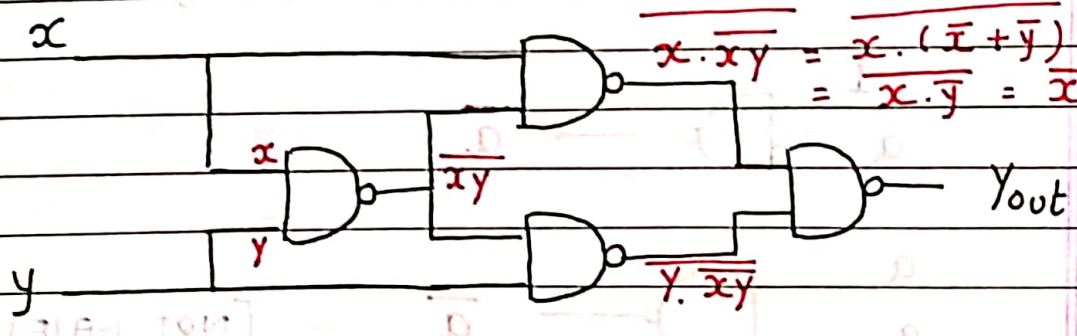
[Same input]

Design NOR Gate using NAND



PAGE NO. :
DATE : / /

Ex Find output



$$Y_{out} = \overline{(\overline{x}+y).(\overline{y}+x)}$$
$$= \overline{\overline{x}+y} + \overline{\overline{y}+x}$$
$$\boxed{Y_{out} = x.\overline{y} + y\overline{x}}$$

X-OR (4 Nand required)

Axiom :

$x + \overline{x} = 1$

$ab + \overline{ab} = 1$

$f + \overline{f} = 1$

Extra :

$x + \overline{xy} = \overline{x} + y$

[Inhibitor's output]

Distributive Law :

$x + y.z = (x+y).(x+z)$

RHS

Axiom :

$x.\overline{x} = 0$

$ab.\overline{ab} = 0$

$f.\overline{f} = 0$

$xx + xy + xz + yz$

$x[1+y+z] + yz$

$x + yz$ (LHS)

PAGE NO. :
DATE : / /

11

Ex Apply distributive law to the given function

$$W + xy\overline{W} \rightarrow \text{redundant}$$

Ans.)

$$(W + x)(W + y)(W + \overline{W})$$
$$= W + xy \checkmark$$

Proof for $a.b + \overline{a.b} = 1$

$$(a.b + \overline{a}) + \overline{b}$$
$$= \overline{a} + b + \overline{b}$$
$$= \overline{a} + 1$$
$$= 1 \checkmark$$

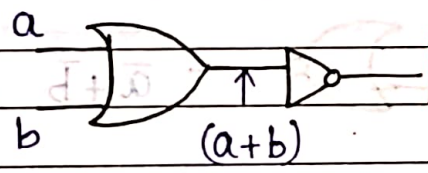
Absorption Law

$$\boxed{A + \overline{A}B = A + B}$$

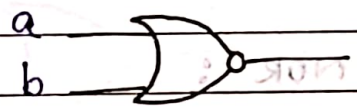
② NAND (OR) Gate $\boxed{\text{NOR}}$

Not Gate in output of OR gate — OR gate

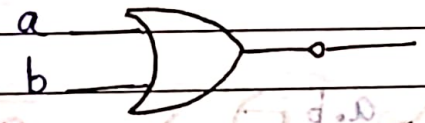
Symbol :



$$\boxed{Y_{out} = \overline{a+b}}$$



$\overline{a+b}$



$\overline{a+b}$

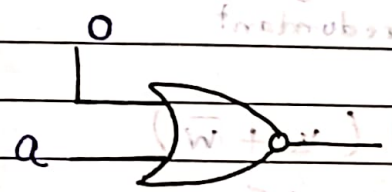
Note
Add and take compliment

Truth Table :

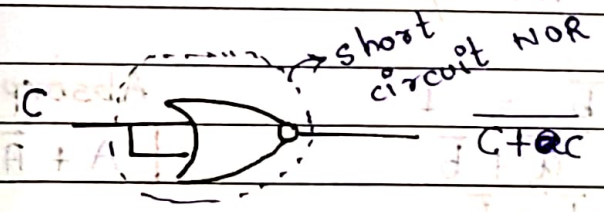
	a	b	a+b	$\overline{a+b}$
unique input	0	0	0	1 → unique output
	0	1	1	0
	1	0	1	0
	1	1	1	0

PAGE NO. :
DATE : / /

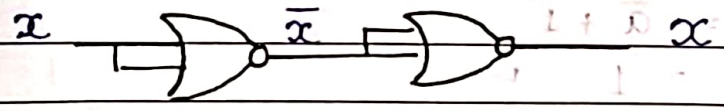
) Find the simplified output for given circuit



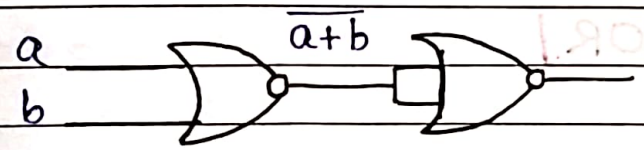
$\overline{0+a} = \overline{a}$



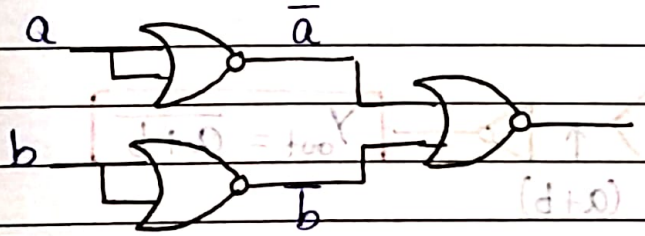
$\overline{C+C} = \overline{C}$ [NOT Gate]
(Required 1 NOR)



[Buffer]

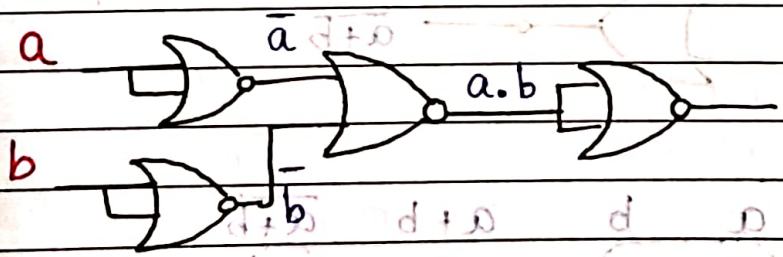


$a+b$ [OR Gate]
[Required 2 NOR]



$\overline{\overline{a}+\overline{b}} = a.b$ [And Gate]
(Required 3 NOR)

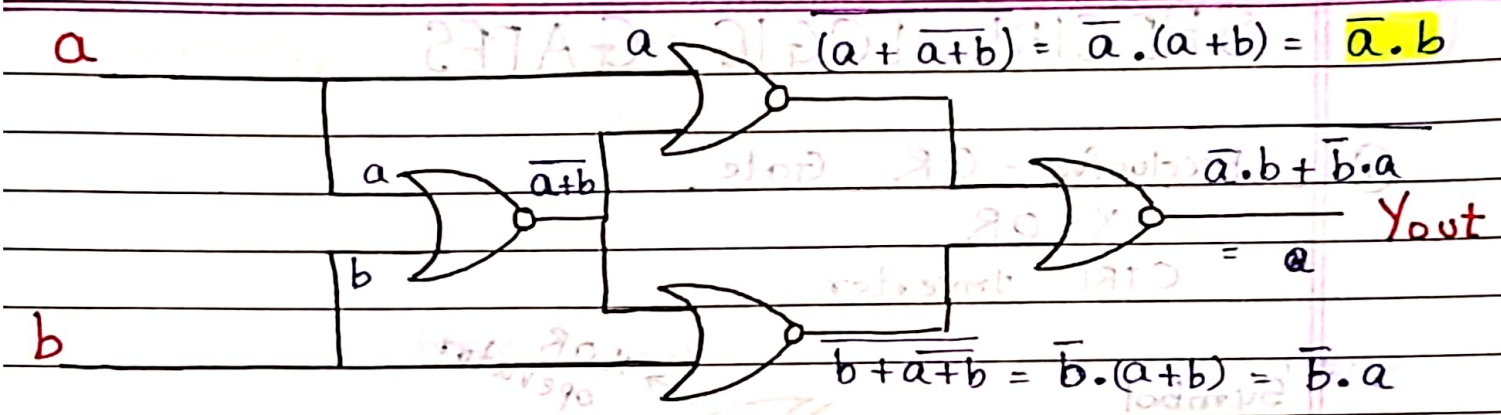
Design NAND using NOR :



$\overline{a.b}$

4 NOR gates required to make 1 NAND Gate.

PAGE NO. :
DATE : / /

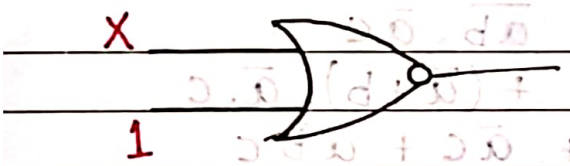


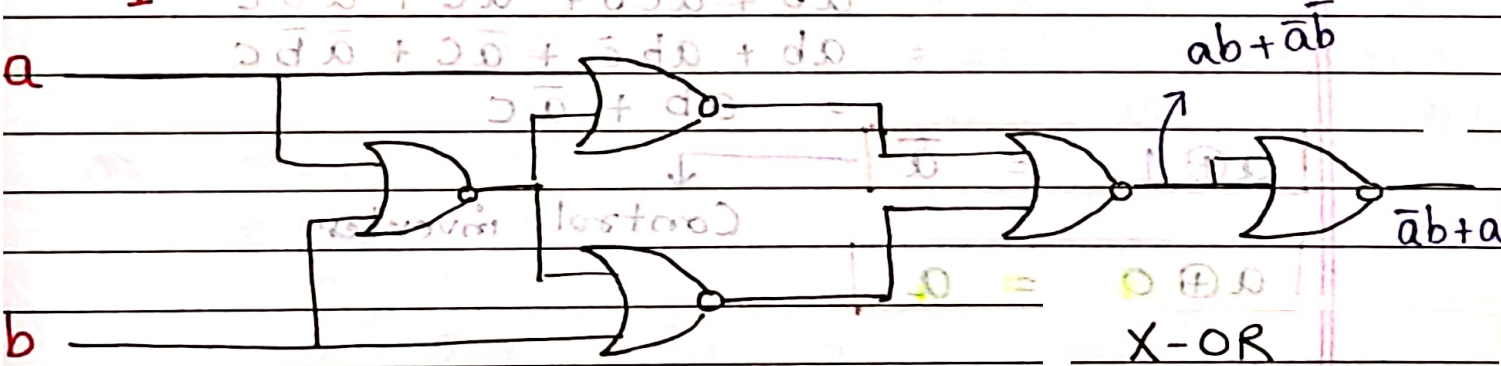
$$\overline{\overline{a}.b+\overline{b}.a} = \overline{\overline{a}.b}\ \&\ \overline{\overline{b}.a}$$
$$= (a+\overline{b})(b+\overline{a})$$
$$\boxed{Y_{out} = ab+\overline{a}\,\overline{b}}$$

X-NOR.
(4 Nor Required)

Note :

$$\boxed{\begin{aligned} \overline{\overline{a}b+a\overline{b}} &= ab+\overline{a}\,\overline{b} \\ \overline{\overline{a}\,\overline{b}+ab} &= \overline{a}b+\overline{b}a \end{aligned}}$$





X-OR
using NOR Gate
5 Nor require.

PAGE NO. :
DATE : / /

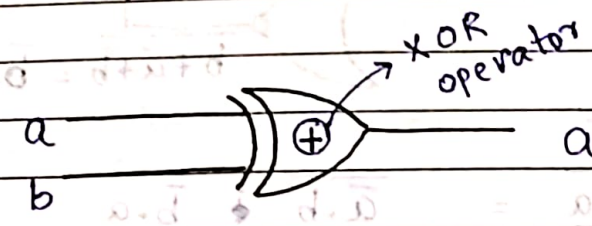
SPECIAL LOGIC GATES

① Exclusive - OR Gate

X - OR

CTRL - Inverter

Symbol



$a \oplus b = a\bar{b} + \bar{a}b$

Truth table

	a	b	$\bar{a}$	$\bar{b}$	$a\bar{b}$	$\bar{a}b$	$Y = a\bar{b} + \bar{a}b$
	0	0	1	1	0	0	0
$a \neq b$	0	1	1	0	0	1	1
	1	0	0	1	1	0	1
	1	1	0	0	0	0	0

Ex

$$ab \oplus \bar{a}c = ab.\overline{\bar{a}c} + \overline{ab}.\bar{a}c$$
$$= ab.(a+\bar{c}) + (\bar{a}+\bar{b}).\bar{a}.c$$
$$= ab + a\bar{c}b + \bar{a}c + \bar{a}\bar{b}c$$
$$= ab + ab\bar{c} + \bar{a}c + \bar{a}\bar{b}c$$
$$= ab + \bar{a}c$$

$\boxed{a \oplus 1 = \bar{a}}$ → Control inverter

$\boxed{a \oplus 0 = a}$

PAGE NO.:
DATE: / /

Ex Simplify $a \oplus b \oplus \bar{a}$ (using comutative law).

$= a \oplus \bar{a} \oplus b$ $(a \oplus \bar{a} = 1)$

$= 1 \oplus b$ (using AXIOM)

$= \bar{b}$ ✓

Note $\boxed{1 \oplus f = \bar{f}}$

Ex Simplify : $\bar{a} b \oplus \overline{ab}$

$xy + x\bar{y} = x$

$= \overline{\bar{a}b}\ \overline{ab} + \bar{a}b\ ab$

$= (a+\bar{b})(\bar{a}+\bar{b})$

using $(x+y)(x+\bar{y}) = x$

$= 0 + a\bar{b} + \bar{a}\bar{b} + \bar{b}$

$= \bar{b}(a + \bar{a} + 1)$

$= \bar{b}$ ✓

Ex Simplify :

① $\overline{a\bar{b}} \oplus \bar{a}b$

$= a\bar{b}\ \bar{a}b + \overline{a\bar{b}}\ \overline{\bar{a}b}$

$= 0 + (\bar{a}+b)\cdot(a+\bar{b})$

$= 0 + \bar{a}\bar{b} + ab + 0$

$= ab + \bar{a}\bar{b}$

② $x\bar{y} \oplus x \oplus \bar{x}\bar{y}$

$= x(\bar{y}+1) \oplus \bar{x}\bar{y}$

$= xy \oplus \bar{x}\bar{y}$

$= xy \cdot \overline{\bar{x}\cdot\bar{y}} + \overline{xy}\ \bar{x}\bar{y}$

$= xy(x+y) + (\bar{x}+\bar{y})\bar{x}\bar{y}$

$= xy + xy + \bar{x}\bar{y} + \bar{x}\bar{y}$

$= xy + \bar{x}\bar{b}$

③ $a \oplus b \oplus c$. ✗

$(a\bar{b} + \bar{a}b) \oplus c$.

$= (a\bar{b} \oplus c) + (\bar{a}b \oplus c)$

$a\bar{b}\bar{c} + (\bar{a}+b)c + \bar{a}b\bar{c} + (a+\bar{b}$

$a\bar{b}\bar{c} + \bar{a}c + bc + \bar{a}b\bar{c} + ac + \bar{b}$

$a\bar{b}\bar{c} + \bar{a}b\bar{c} + c$

PAGE NO. :
DATE : / /

imp

③ $a \oplus b \oplus c$

$a \oplus (\bar{b}c + b\bar{c})$. $\quad x = \bar{b}c + b\bar{c}$

$a \oplus x \quad \bar{x} = bc + \bar{b}\bar{c}$

$\bar{a}x + a\bar{x}$

$\bar{a}(\bar{b}c + b\bar{c}) + a(bc + \bar{b}\bar{c})$

$= \underset{001}{\bar{a}\bar{b}c} + \underset{010}{\bar{a}b\bar{c}} + \underset{111}{abc} + \underset{100}{a\bar{b}\bar{c}}$ ✓ SOP

1 2 7 4

Ex

$\Sigma_m(1, 2, 4, 7)$. ✓

Truth Table for 3 input XOR gate:

②

a	b	c	$a \oplus b$	$a \oplus b \oplus c$
0	0	0	0	0
0	0	1	0	1
0	1	0	1	1
0	1	1	1	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	0	1

odd no of 1 in input.

msb lsb

1 0 2 4

1×10^3, 0×10^2, 2×10^1, 4×10^0

msb = place value highest.

PAGE NO. :
DATE : / /

SOP → we focus on output as High logic.

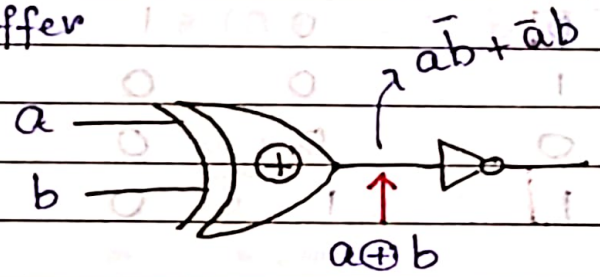
- output of XOR is 1 when input consist of odd number of 1's
- XOR gate is also reffered as odd parity detector.

$$\underset{1}{1} \oplus \underset{2}{1} \oplus 0 + \underset{3}{1} + 0 + \underset{4}{1} + \underset{5}{1} + 0 + \underset{6}{1} = 0.$$

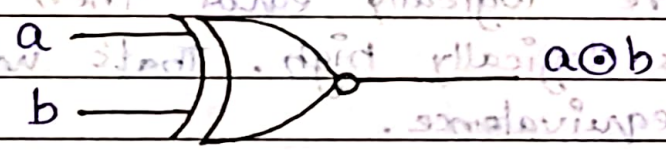
even 1's = 0

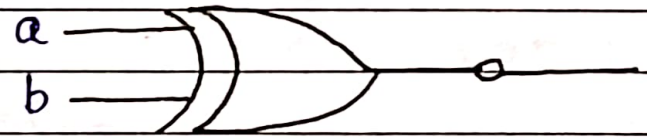
Exclusive - NOR
XNOR
Gate of equivalence.
Equality detector
Coincidence detector
CTRL Buffer

Symbol.



$\overline{a \oplus b} = ab + \bar{a}\bar{b}$
$= a \odot b$
↓
XNOR operator





PAGE NO. :
DATE : / /

NOTE :

A NAND

$$a \oplus b = \bar{a}b + a\bar{b}$$

A NOR

$$a \odot b = ab + \bar{a}\bar{b}$$

$$\overline{a \oplus b} = \overline{\bar{a}b + a\bar{b}} = \bar{a}\bar{b} + ab$$

$$\overline{a \odot b} = \overline{\bar{a}\bar{b} + ab} = \bar{a}b + a\bar{b} = a \oplus b.$$

IMP :

XOR $\boxed{\text{2 input}}$ XNOR

Truth table :

	a	b	ab	$\bar{a}\bar{b}$	$a \odot b$
a=b	0	0	0	1	1
	0	1	0	0	0
	1	0	0	0	0
a=b	1	1	1	0	1

NOTE :

When inputs are logically equal then output of XNOR Gate is logically high. That's why we call it as gate of equivalence.

$$\boxed{a \odot \bar{a} = a.\bar{a} + \bar{a}.\bar{a} = 0}$$

$$\boxed{a \odot 1 = a.1 + \bar{a}.\bar{1} = a}$$

$$\bar{a} \odot \overline{ab} = \overline{\bar{a}.\overline{ab}} + \bar{a}.\overline{ab}$$
$$= a.ab + \bar{a}(\bar{a}+\bar{b})$$
$$= ab + \bar{a} + \bar{a}b$$
$$= ab + \bar{a}$$
$$= b + \bar{a}$$

Eg $\bar{a} \odot a\bar{b} = \overline{\bar{a}.a\bar{b}} + \bar{a}.a\bar{b}$
$$= a.(\bar{a}+b) + 0$$
$$= 0 + ab + 0$$
$$= ab \checkmark$$

$$ab \odot \bar{a}b = \overline{ab.\bar{a}b} + ab.\bar{a}b$$
$$= (\bar{a}+\bar{b}).(a+\bar{b}) + 0 = \bar{a}\bar{b} + a\bar{b} + \bar{b}$$
$$= \bar{b} \checkmark$$

$$a \odot b \odot \bar{b} = a \odot 0$$
$$= \overline{a.0} + a.0 = \bar{a}.1 + 0 = \bar{a}$$

$$a \odot b \odot c = (a \odot b) \odot c$$
$$= (ab + \bar{a}\bar{b}) \odot c$$
$$= \overline{(ab+\bar{a}\bar{b}).\bar{c}} + (ab+\bar{a}\bar{b}).c$$
$$= (\overline{ab})(\overline{\bar{a}\bar{b}}).\bar{c} + cab + c\bar{a}\bar{b}$$
$$= \bar{a}\bar{b}c + \bar{a}b\bar{c} + a\bar{b}\bar{c} + abc. = \Sigma_m(1,2,4,7)$$

ERROR

PAGE NO.: _____
DATE: / /

③

3 INPUT XNOR.

	a	b	c	$a \odot b$	$a \odot b \odot c$	
	0	0	0	1	0	
$\bar{a}\bar{b}c$	0	0	1	1	1	✓
$\bar{a}b\bar{c}$	0	1	0	0	1	✓
	0	1	1	0	0	
$a\bar{b}\bar{c}$	1	0	0	0	1	✓
	1	0	1	0	0	
	1	1	0	1	0	
abc	1	1	1	1	1	✓

NOTE :

Output of XNOR is $\boxed{\text{high / 1}}$ when input combination consist of $\boxed{\text{even number of zero}}$

That is why we call XNOR Gate as even parity detector

$$a \oplus b \neq a \odot b$$

(mathematically) $a \oplus b \oplus c = a \odot b \odot c$

(practically) $a \oplus b \oplus c \neq a \odot b \odot c$.

Ex. $0 \oplus 1 \oplus 0 \oplus 0 \oplus 1 \oplus 0 \oplus 1 = 1$

↑ XOR (odd 1) is true.

NOTE [Output of XOR is only effected by number of 1's ∴ odd parity]

$0 \odot 1 \odot 0 \odot 0 \odot 1 \odot 1 \odot 1 \odot 0 = 1$

↑ XNOR (even 0) is true

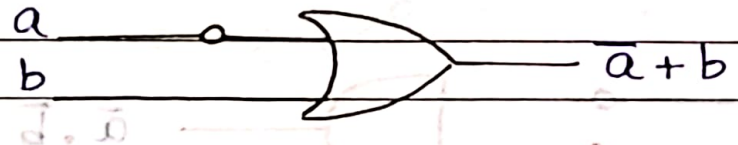
NOTE: [Output of XNOR sequence is only effected by number of 0's]

PAGE NO. :
DATE : / /

INHIBITOR

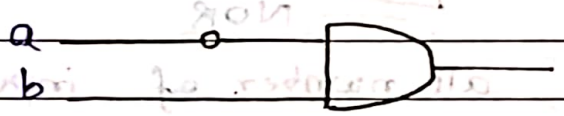
Practical application of inhibitor circuit is enabling and disabling of circuit.

NOT + OR



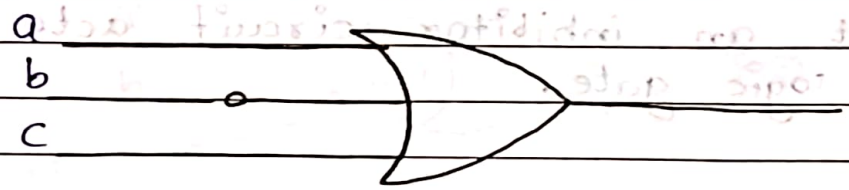
$\bar{a}+b$

NOT + AND

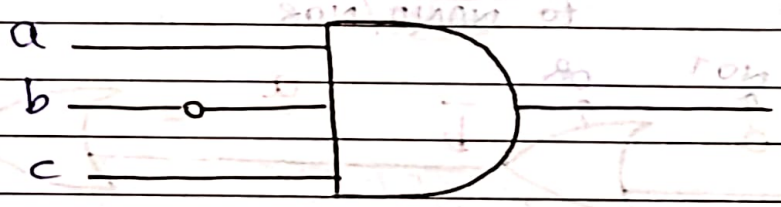


$\bar{a}.b$

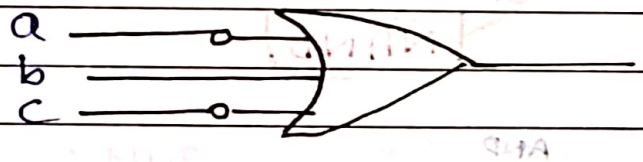
Higher order Inhibitor :



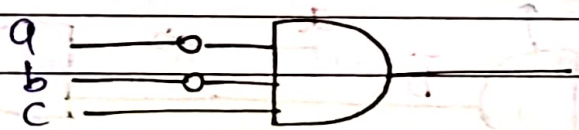
$a+\bar{b}+c$



$a\bar{b}c$

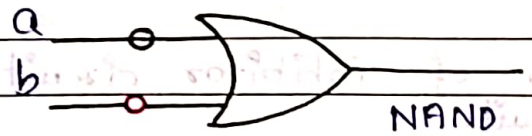


$\bar{a}+b+\bar{c}$

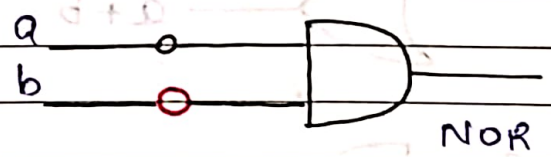


$\bar{a}\bar{b}c$

PAGE NO. :
DATE : / /



$\bar{a} + \bar{b} = \overline{a \cdot b}$



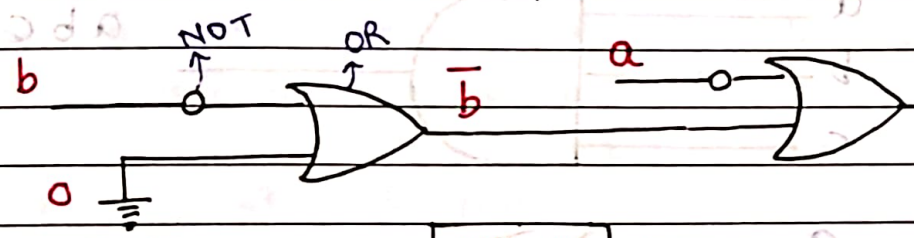
$\bar{a} \cdot \bar{b} = \overline{a + b}$

Applicable to all number of input.

Q Prove that an inhibitor circuit acts as universal logic gate.

Inhibitor → (transform to NAND/NOR) → universal.

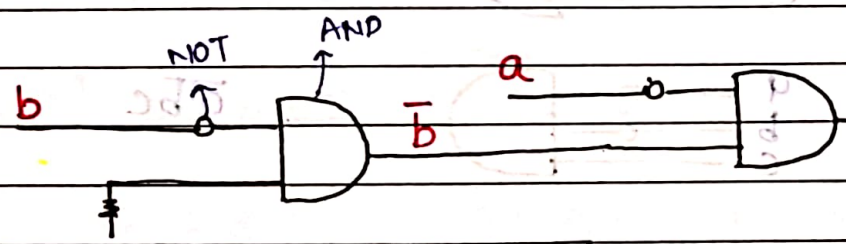
NOT
OR
Functionally Complete



$\bar{a} + \bar{b} = \overline{a \cdot b}$

NAND

NOT
AND
Functionally Complete.



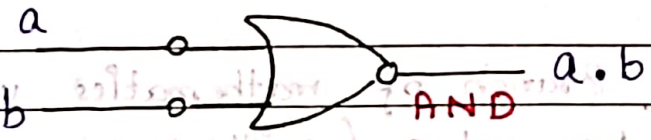
$\bar{a} \cdot \bar{b} = \overline{a + b}$

NOR

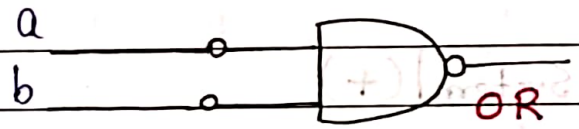
PAGE NO. :
DATE : / /

23

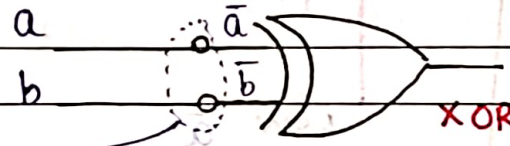
Ex: Find the simplified output :



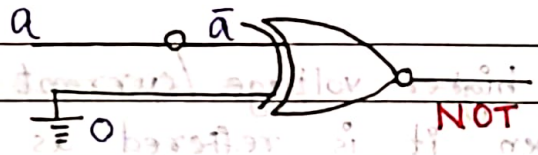
$a.b$



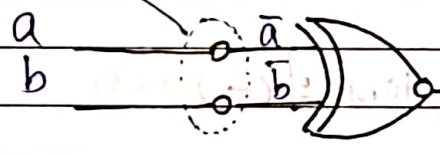
$a+b$



$\bar{a}\oplus\bar{b} = a\bar{b}+\bar{a}b = a\oplus b$

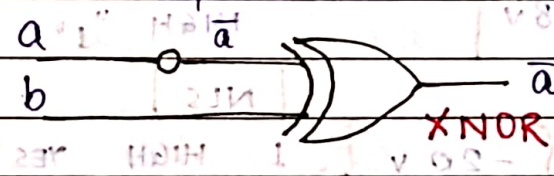


$\bar{a}$



$\overline{\bar{a}\oplus\bar{b}} = \overline{a\oplus b} = ab+\bar{a}\bar{b}$

XOR and XNOR are 'number of input' dependent circuits, Rest of the OR, AND, NOT can be generalized to any ~~in~~ number of inputs



$\bar{a}\oplus b = \bar{a}\bar{b}+ab = a\odot b$

$c\oplus b = c\oplus b$

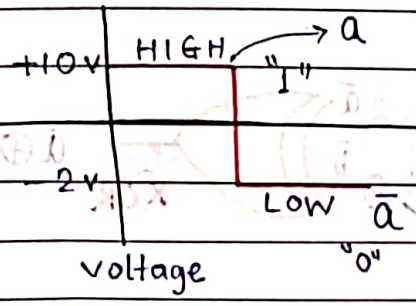
PAGE NO. :
DATE : / /

BASICS OF BOOLEAN ALGEBRA

By George Boole

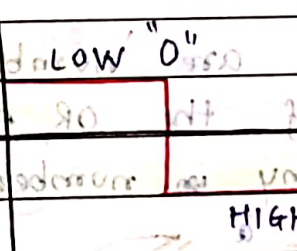
Definition : Branch of mathematics which deals with only two values (with two amplitude level), high and low.

Positive logic System (+)



- If relatively higher voltage / current is assigned as high logic then it is reffered as positive logic system.

Negative Logic System : (−)



	PLS		NLS	
Ex No LOW 0	−20 V	1	HIGH	YES
YES HIGH 1	−15 V	0	LOW	NO

PAGE NO. :
DATE : / /

Example.

+ve logic OR

a	b	z
0	0	0
0	1	1
1	0	1
1	1	1

-ve logic OR

a	b	z
1	1	0
1	0	0
0	1	0
0	0	1

equivalent to +ve AND

$\boxed{a+b}$ (PLS) $\boxed{a \cdot b}$ (NLS)

-ve logic OR truth table is same as +ve logic AND.

$+ \rightleftarrows \cdot$

Commutative Law

OR $a + b = b + a$

AND $a \cdot b = b \cdot a$

NOR $\overline{a+b} = \overline{b+a}$

NAND $\overline{a \cdot b} = \overline{b \cdot a}$

XOR $a \oplus b = b \oplus a$

XNOR $a \odot b = b \odot a$

Commutative Law is followed by all logic gates.

PAGE NO. :
DATE : / /

ASSOCIATE LAW

$$(a+b)+c = a+(b+c) \quad \text{OR}$$

$$(a\cdot b)\cdot c = a\cdot(b\cdot c) \quad \text{AND}$$

INVALID

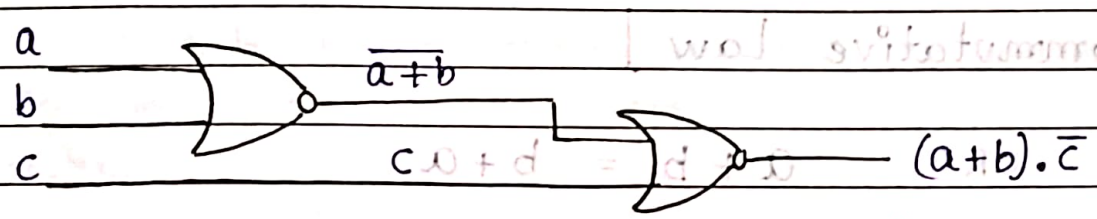
$$\overline{\overline{a+b}+c} \neq \overline{a+\overline{b+c}}$$

$$\overline{\overline{a\cdot b}\cdot c} \neq \overline{a\cdot\overline{b\cdot c}}$$

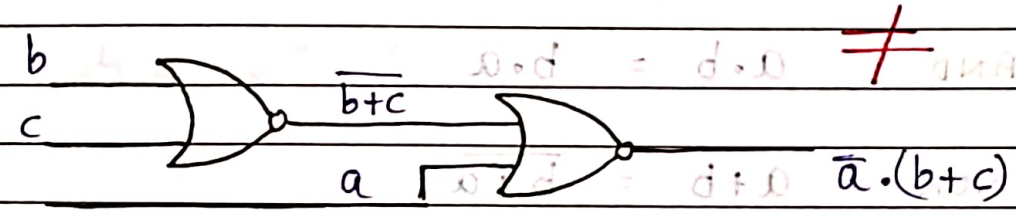
$$(a\oplus b)\oplus c = a\oplus(b\oplus c)$$

$$(a\odot b)\odot c = a\odot(b\odot c)$$

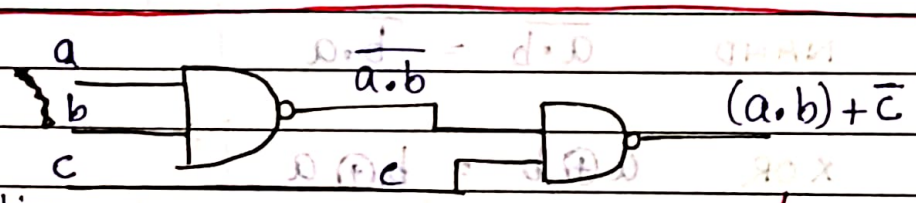
Associative law is invalid for NAND and NOR.



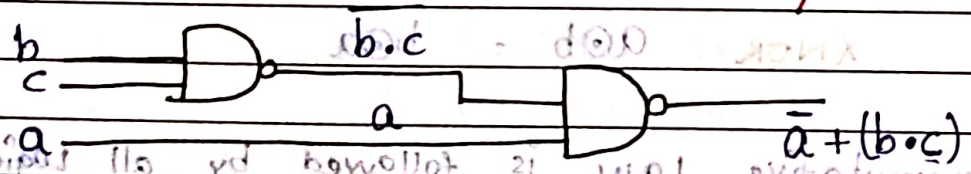
$\neq$



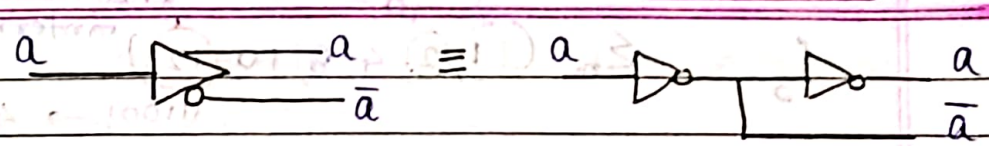
NAND-NAND implementation is also reffered as AND OR Implementation (Provided that inversion is available)



$\neq$



PAGE NO. :
DATE : / /



[used in PLA, programmable logic Array]

REPRESENTATION of BOOLEAN FUNCTION

① SSOP / Min term representation

Standard Sum of Product

OR Canonical Sum of Product

- In general we call it a "SOP"

variable representat"

$a = 1$

$\bar{a} = 0$

SOP

Mathematical representation: $\underset{\text{sum}}{\sum_m}\underbrace{(1, 2, 4, 7)}_{\text{minterms}} \equiv \sum(1,2,4,7)$

② SPOS / Max term representation.

Standard Product of sum

OR Canonical Product of sum

in General we call it as POS

variable representat"

$a = 0$

$\bar{a} = 1$

POS

Mathematical Representation : $\underset{\text{PRODUCT}}{\prod} \underbrace{M(1, 2, 4, 6)}_{\text{max terms}}$

$\equiv M(1,2,46)$

Analysis of SOP :

minimum (m) maximum (m)

$f_1 = \Sigma_m(0, 1, 3)$

$(11)_2 \rightarrow$ 2 bits. $\therefore$ 2 variable function.

MSB LSB.

$f_1(x, y) = \Sigma_m(\underset{00}{0}, \underset{01}{1}, \underset{11}{3})$.

$\bar{x}.\bar{y} + \bar{x}.y + x.y$

SOP (a & b) missing

$01 \equiv \bar{c}d$

$10 \equiv c\bar{d}$

$f_3 = \Sigma_m (1, 2, 4, 8, 10, 12)$ — maximum minterm.

$(1100)_2 \rightarrow$ 4 bits.

$\therefore$ 4 variable function.

$$f_3(a,b,c,d) = \bar{a}\bar{b}\bar{c}\bar{d} + \bar{a}\bar{b}c\bar{d} + \bar{a}b\bar{c}\bar{d} + \underbrace{a\bar{b}\bar{c}\bar{d} + a\bar{b}c\bar{d} + ab\bar{c}\bar{d}}_{\text{SSOP}}$$

Solve for "f"

①

a	b	f	
0	0	1	$\bar{a}\bar{b}$
0	1	1	$\bar{a}b$
1	0	1	$a\bar{b}$
1	1	0	

$f = \bar{a}\bar{b} + \bar{a}b + a\bar{b}$

$\bar{a} + a\bar{b}$

$\bar{a} + \bar{b} = \overline{a.b}$ NAND.

②

a	b	f	
0	0	0	
0	1	1	$\bar{a}b$
1	0	1	$a\bar{b}$
1	1	1	ab

$f = \bar{a}b + a\bar{b} + ab.$

$= a + b$ = OR

③

a	b	f	
0	0	1	$\bar{a}\bar{b}$
0	1	0	
1	0	0	
1	1	1	ab

$f = \bar{a}\bar{b} + ab = a \odot b$

= X-NOR

Note :

④

⑤

⑥

PAGE NO. :
DATE : / /

29

For solving SOP function w.r.t truth table we focus at the output for high logic.

x	y	f	
0	0	1	$\bar{x}\bar{y}$
0	1	1	$\bar{x}y$
1	0	0	
1	1	0	

$f = \bar{x}\bar{y} + \bar{x}y$
$= \bar{x}$ = inverter.

x	y	f	
0	0	1	$\bar{x}\bar{y}$
0	1	1	$\bar{x}y$
1	0	1	$x\bar{y}$
1	1	1	xy

$f = \bar{x}\bar{y} + \bar{x}y + x\bar{y} + xy$
$= 1$ Always
(Independent of input)

a	b	f	
0	0	0	
0	1	0	
1	0	0	
1	1	1	ab

$f = a \cdot b$ = AND.

Analysis of POS

$f_1 = \Pi_M(0, 1, 2)$ → maximum term max term

00 01 $10_2 \Rightarrow$ 2 bits.

2 variable function

$f_1(x, y) = (\bar{x}+y) \cdot (x+\bar{y}) \cdot (\bar{x}+y)$

000 001 011 110

$f_2 = \Pi_M(0, 1, 3, 6)$

$f_3 = \Pi_M(1, 2, 4, 8, 10, 14)$

$f_2(x,y) = (x+y+z) \cdot (x+y+\bar{z}) \cdot (\bar{x}+\bar{y}+\bar{z}) \cdot (\bar{x}+\bar{y} \cdot z)$

PAGE NO.: _____
DATE: _____

$$f = \Pi_M(\overset{0001}{1}, \overset{0010}{2}, \overset{0100}{4}, \overset{1000}{8}, \overset{1010}{10}, 14)$$

maximum
max term

$1110_2 \Rightarrow 4$ bits.

$\therefore$ 4 variable function.

$$f(a,b,c,d) = (a+b+c+\bar{d})\cdot(a+b+\bar{c}+d)$$
$$\cdot(a+\bar{b}+c+d)\cdot(\bar{a}+b+c+d)$$
$$\underbrace{\cdot(\bar{a}+b+\bar{c}+d)\cdot(\bar{a}+\bar{b}+\bar{c}+d)}_{\text{Product of Sum}}$$

Note: for solving POS function w.r.t K-map / truth table we focus at the output for zero logic.

Ex.

a	b	f
0	0	1
0	1	1
1	0	1
1	1	0 ✓

$f = \cancel{(a+b)\cdot(a+\bar{b})\cdot(\bar{a}+b)}$

$= \cancel{a\cdot(\bar{a}+b)}$

$=$

$f = \bar{a}+\bar{b} = \overline{a\cdot b}$

Ex

a	b	f
0	0	0 ✓
0	1	1
1	0	1
1	1	1

$f = a+b.$

Ex

a	b	f
0	0	0 ✓
0	1	0 ✓
1	0	0 ✓
1	1	0 ✓

$f = (x+y)(x+\bar{y})(\bar{x}+y)(\bar{x}+\bar{y})$

$= x\cdot\bar{x}$

$= 0$, Always.

1 carry

$$\begin{array}{r} 110 \\ +\ 011 \\ \hline 001 \end{array}$$

3 bit Binary addition

PAGE NO. :
DATE : / /

Ex.

x	y	f
0	0	0 ✓
0	1	0 ✓
1	0	0 ✓
1	1	1

$$f = (x+y)(x+\bar{y})(\bar{x}+y)$$
$$= x.(\bar{x}+y)$$
$$= x.y.$$

Ex.

x	y	f
0	0	1
0	1	1
1	0	0 ✓
1	1	0 ✓

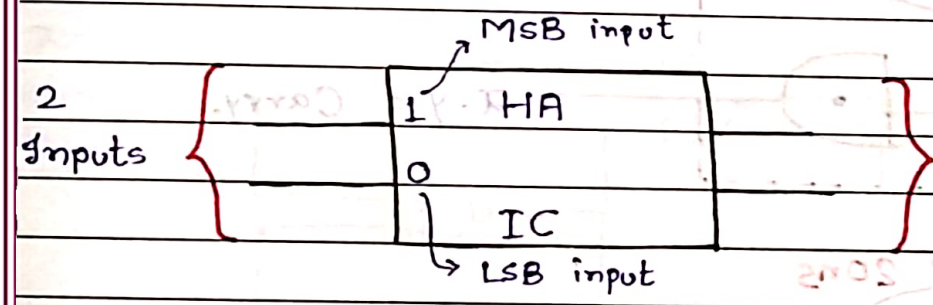
$$f = (\bar{x}+b)(\bar{x}+\bar{b})$$
$$= \bar{x}$$

Ex

x	y	f
0	0	1
0	1	0 ✓
1	0	0 ✓
1	1	1

$$f = (\bar{x}+y)(x+\bar{y}).$$
$$= \bar{x}\bar{y} + xy.$$

Half Adder



0 carry	0 carry	1 carry	1 carry	1 carry
0	0	1	9	72
+ 0	+ 1	+ 1	+ 2	48
0	10	0	1	20
1 bit binary addition			1 bit decimal addition	2 bit decimal addition

PAGE NO. :
DATE : / /

Note : Half adder perform 1 bit binary addition.

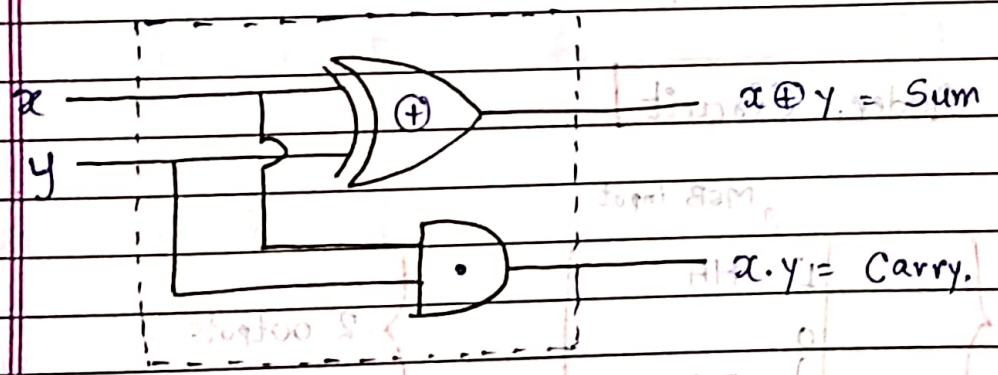
Augend — { 5 + 7 = 12 } — sum / carry.

Addend

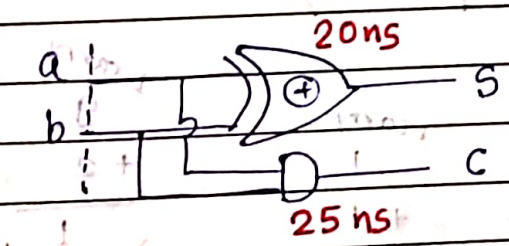
Truth table of HA circuit.

x	y	Sum (S)	carry (C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$\boxed{\begin{aligned} \text{Sum} &= x \oplus y. \\ \text{Carry} &= x \cdot y. \end{aligned}}$$



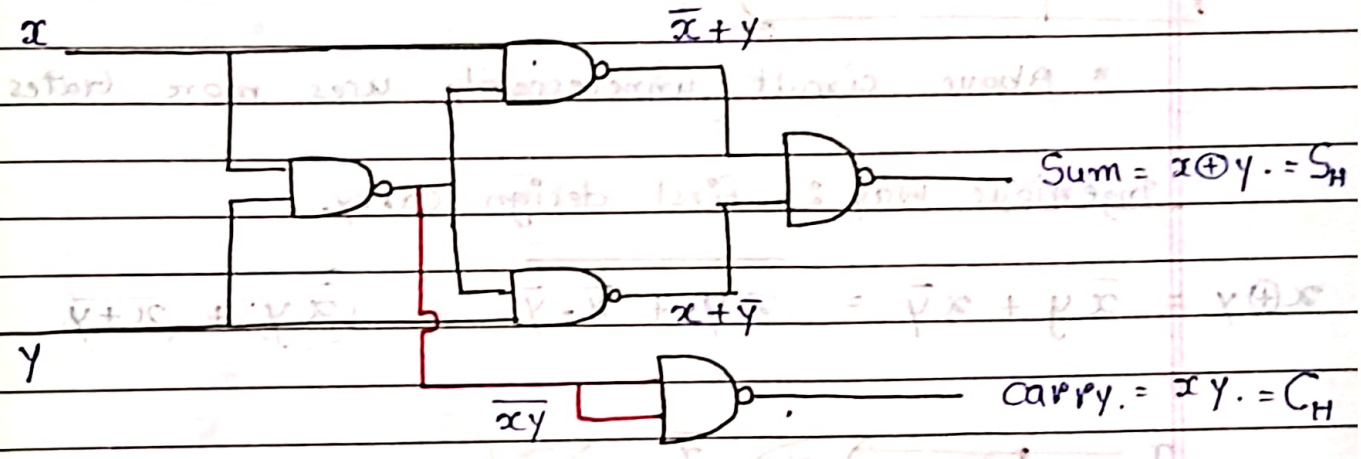
Ex



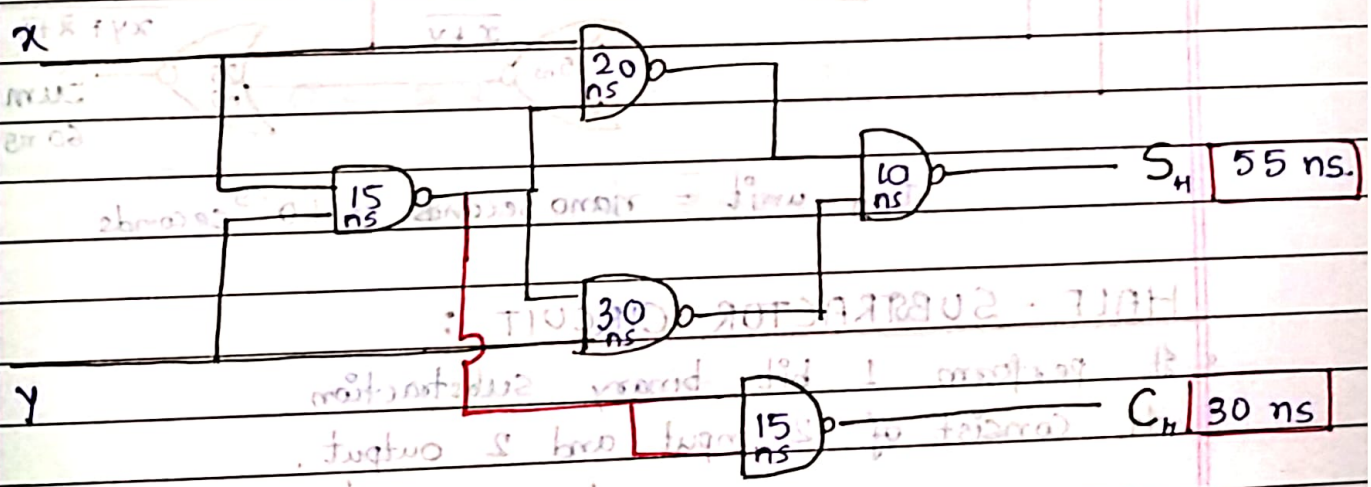
a, b is applied at t = 0
reference time

- Propogation delay of S and C are independent of each other and only depends on X-OR and AND
- for the given circuit, output of sum and carry is purely dependent on only propogation delay of logic gates.

- Half adder designing using NAND (5 Nand required)

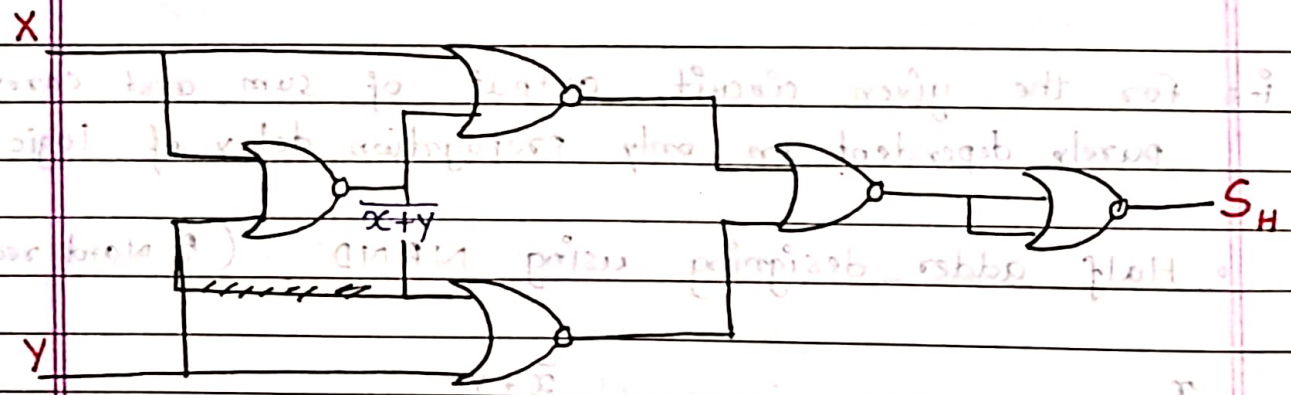


Example Based on propogation Delay:



PAGE NO. :
DATE : / /

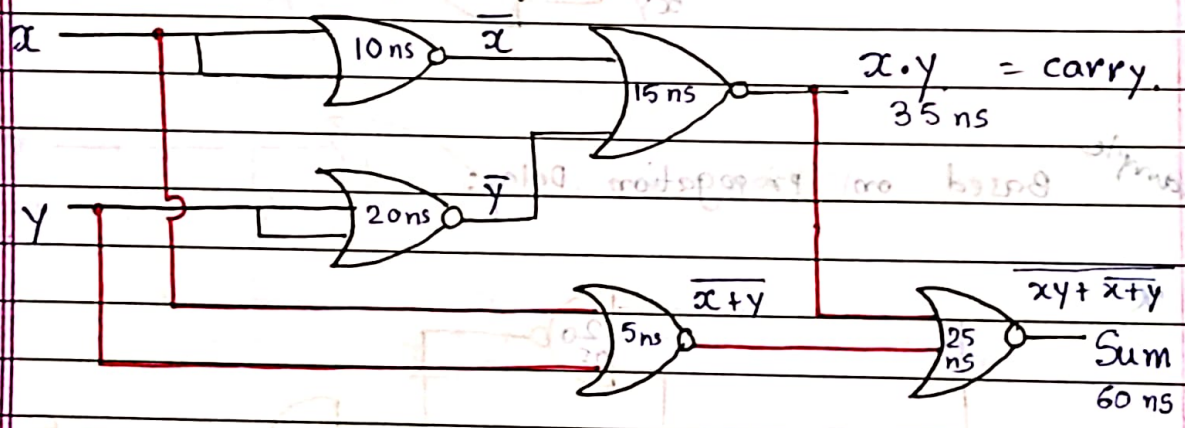
HALF ADDER USING NOR.



* Above circuit unnecessarily uses more Gates.

Ingenious way : first design carry.

$$x \oplus y = \bar{x}y + x\bar{y} = xy + \bar{x}\cdot\bar{y} = \overline{\overline{xy} + \overline{x+y}}$$



t_{pD} unit = nano seconds = 10^{-9} seconds

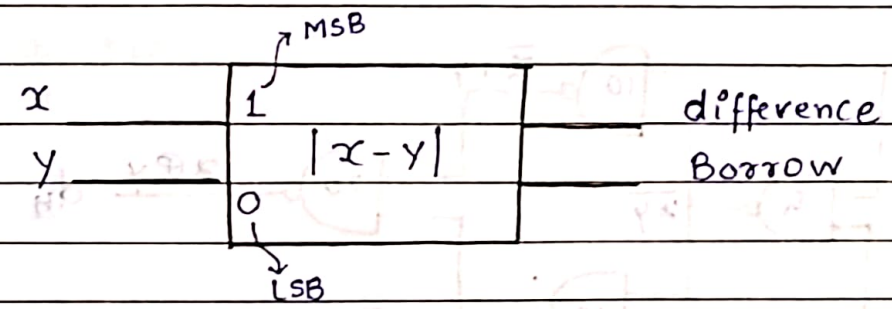
HALF - SUBSTRACTOR CIRCUIT :

- It perform 1 bit binary substraction.
- It consist of 2 input and 2 output.

Mathematically $\overset{\text{minuend}}{x} - \overset{\text{subtrahend}}{y} = \text{result}$

result → difference, Borrow

subtrahend > minuend then borrow



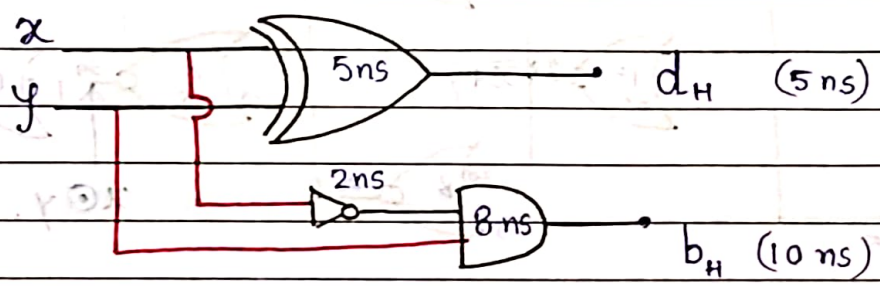
$$\begin{array}{r} 1000 \\ -\ 782 \\ \hline 218 \end{array}$$

Ex

$$\begin{array}{r} 1010000 \\ -\ 0111101 \\ \hline 0100011 \end{array}$$

Truth table

x	y	difference	Borrow
0	0	0	0
0	1	1 $\bar{x}y$	1 $\bar{x}y$
1	0	1 $x\bar{y}$	0
1	1	0	0

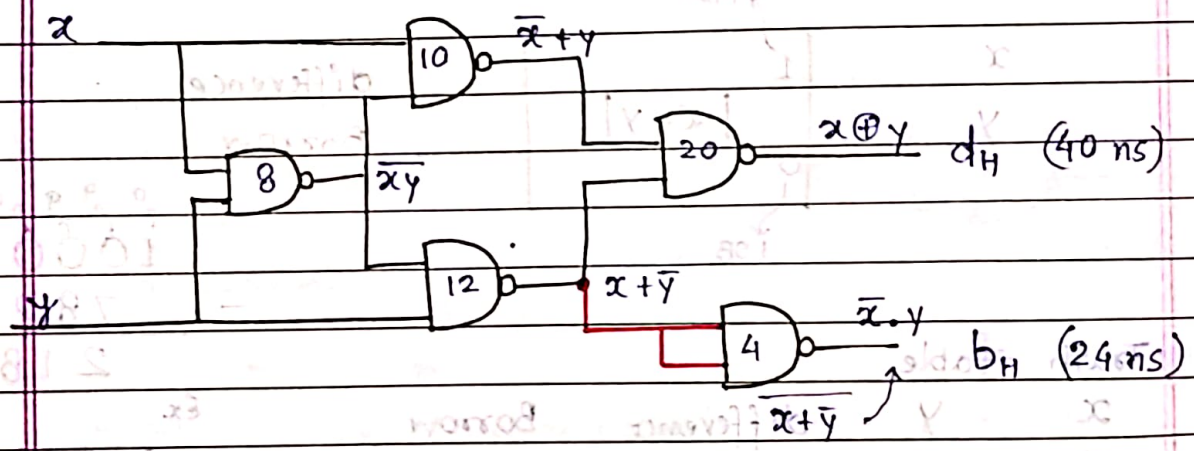


$$d = \bar{x}y + x\bar{y} = x \oplus y.$$

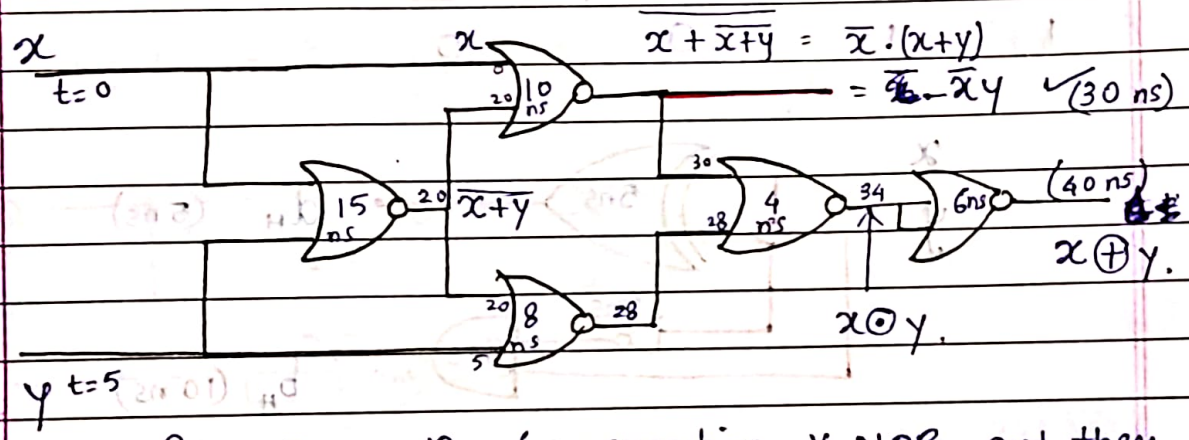
$$b = \bar{x}.y \quad \Big| \quad \overline{msb}.lsb$$

PAGE NO. :
DATE : / /

Half Substractor using NAND



Home work : Design half subtractor using NOR (5 NOR)



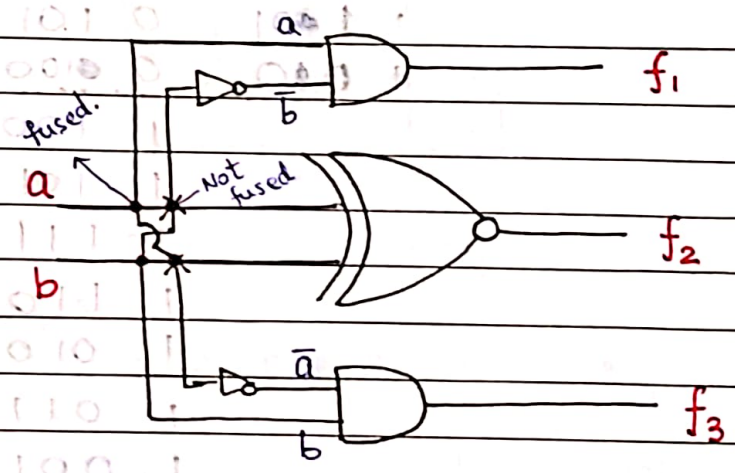
See page - 13 for creating X-NOR and then compliment it to get X-OR as 2-input X-OR and X-NOR are compliment to each other.

(Q.) If t = 0 x is applied
t = 5 y is applied.

Q.) 1 bit magnitude comparator circuit

Truth table

a	b	$f_1 (a>b)$	$f_2 (a=b)$	$f_3 (a<b)$
0	0	0	1 $\bar{a}\bar{b}$	0
0	1	0	0	1 $\bar{a}b$
1	0	1 $a\bar{b}$	0	0
1	1	0	1 ab	0
			$\hookrightarrow a \odot b$	



- XNOR Gate is also reffered as Gate of equivalence

K-MAPs.

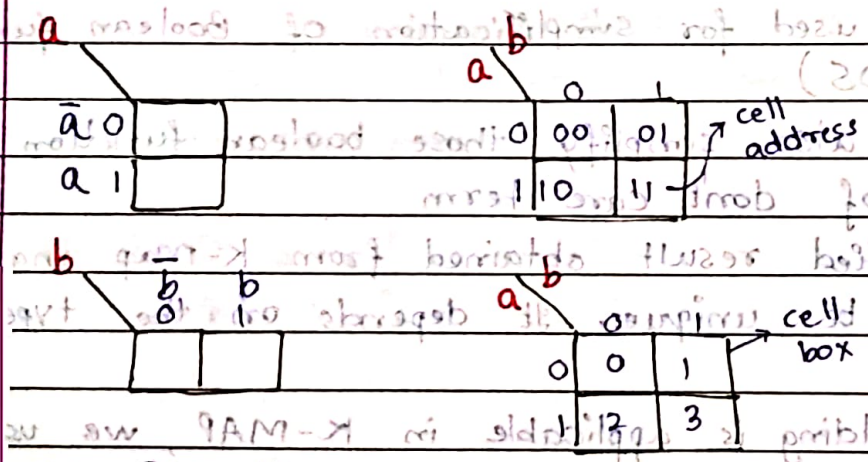
- Technique used for simplification of Boolean function (SOP / POS)
- we can also simplify those boolean function which consists of don't care term
- The simplified result obtained from K-Map may or may not be unique. It depends on the type of approach.
- Since, folding is applicable in K-MAP, we use Grey code / reflected code, as we cannot use binary code for K-MAP simplification because folding is not allowed.

PAGE NO. :
DATE : / /

GREY CODE

1 bit	2 bit	3 bit	4 bit
0	00	000	0000
1	01	001	0001
	11	011	0011
	10	010	0010
		110	0110
		111	0111
		101	0101
		100	0100
			1100
			1101
			1111
			1110
			1010
			1011
			1001
			1000

K-map table :



1 variable K-map
1 variable function

2 variable K-map
2 variable function

PAGE NO. :
DATE : / /

x \ yz	00	01	11	10
0	000 0	001 1	011 3	010 2
1	100 4	101 5	111 7	110 6

ab \ c	0	1
00	0	1
01	2	3
11	6	7
10	4	5

3-variable K-map.

n-variable $\longrightarrow$ 2^n cells.

ab \ cd	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

4-variable K-map

w \ xyz	000	001	011	010	110	111	101	100
0	0	1	3	2	6	7	5	4
1	8	9	11	10	14	15	13	12

① $f_1 = \Sigma m(1, 2, 4, 7)$

② $f_2 = \Pi m(0, 1, 4, 6)$

③ $f_3 = \Sigma m(1, 2, 8, 10, 11)$

④ $f_4 = \Sigma m(0, 1, 4) + \Sigma d(5, 7)$.

Draw the corresponding K-MAP table for the given functions

PAGE NO. :
DATE : / /

f_1 :

a \ bc	00	01	11	10
0	0 (0)	1 (1)	0 (3)	1 (2)
1	1 (4)	0 (5)	1 (7)	0 (6)

→ SOP

f_2 :

a \ bc	00	01	11	10
0	0 (0)	0 (1)	1 (3)	1 (2)
1	0 (4)	1 (5)	1 (7)	0 (6)

→ POS

f_3 :

ab \ cd	00	01	11	10
00		1		1
01				
11	1			
10	1			1

→ SOP.

f_4 :

a \ bc	00	01	11	10
0	1	1		
1	1	X	X	

→ SOP

Digital :

0 & 1 ; two amplitude levels

3rd amplitude is 'X' dont care

Physically : false input / output

→ Noise in Digital circuit.

PAGE NO.:
DATE: / /

41

Procedure to solve K-map

(i) By looking at the given boolean function, draw the respective K-MAP

(ii) Fill the K-MAP cells using either 1's ~~and~~ or 0's based on the function SOP / POS

(iii) If dont care term is mentioned then also consider it and fill it in the K-MAP.

(iv) After filling form a group as per priority given below.

2^n
⋮
16 Hex
8 octa
4 Quad
2 pair
1 single

(v) If don't care term is helpful ~~the~~ in forming higher order group then do consider it.

(vi) Do not form a group which consist of only don't care term.

(vii) Avoid redundancy while forming group.

*(viii) while forming group, take the minimum help from don't care term

*(ix) K-Map can be used for conversion of SOP to POS and vice versa.

(x) If K-map is completely filled with 1 along with 'X' then answer simplifies to 1

PAGE NO. :
DATE : / /

Ex Simplify the K-MAP.

a \ b	0	1
0	1	1
1		

$\bar{a}$

x \ y	0	1
0	1	
1	1	

$\bar{y}$

a \ b	0	1
0	1	
1		

$\bar{a}\bar{b}$

a \ b	0	1
0		1
1		1

b

a \ b	0	1
0	1	
1		1

$\bar{a}\bar{b} + ab$

x \ y	0	1
0		1
1	1	

$\bar{a}b + a\bar{b}$

PAGE NO. :
DATE : / /

a \ b	0	1
0	1	1
1	1	

$\bar{b} + \bar{a}$

a \ b	0	1
0	1	
1	1	X

$\bar{b}$

x \ y	0	1
0		1
1	1	1

$x + y$

a \ b	0	1
0	X	
1	1	X

a ✓

$\bar{b}$ ✓

a \ b	0	1
0		X
1		1

b

a \ b	0	1
0	1	1
1	1	X

1

a \ b	0	1
0		X
1	1	

$a\bar{b}$

a \ b	0	1
0	X	X
1	X	X

1 if SOP ?

0 if POS.

∴ NOISY SYSTEM

x \ y	0	1
0	1	1
1	1	1

1

a \ b	0	1
0	X	X
1		

0 if SOP ?

1 if POS

Noisy system.

a \ b	0	1
0	1	1
1		X

$\bar{a}$

PAGE NO.: _____
DATE: / /

1 $\bar{b}\bar{c}$

a \ bc	00	01	11	10
0	1			
1	1			

4 $\bar{a}\bar{b} + ab$

a \ bc	00	01	11	10
0	1	1		
1			1	1

2 $\bar{b}\bar{c} + bc$

a \ bc	00	01	11	10
0	1		1	
1	1		1	

5 $\bar{x}$

x \ yz	00	01	11	10
0	1	1	1	1
1				

3 z

x \ yz	00	01	11	10
0		1	1	
1		1	1	

6 $\bar{a}\bar{b} + ac$

a \ bc	00	01	11	10
0	1	1		
1		1	1	

7 $a + b\bar{c}$

a \ bc	00	01	11	10
0				1
1	1	1	1	1

10 $\bar{a}\bar{c}$

a \ bc	00	01	11	10
0	1			1
1				

8 $\bar{x} + \bar{y} + z$

x \ yz	00	01	11	10
0	1	1	1	
1	1	1	1	

9 $\bar{a} + c$

a \ bc	00	01	11	10
0	1	1	1	1
1		1	1	

11 $\bar{z}$

x \ yz	00	01	11	10
0	1			1
1	1			1

12 $\bar{c}$

a \ bc	00	01	11	10
0	1	X		1
1	1	X		1

PAGE NO. :
DATE : / /

45

(3) $\bar{a} + \bar{b}c$

a \ bc	00	01	11	10
0	1	1	X	1
1		1		

(4) $\bar{c}$

a \ bc	00	01	11	10
0	X			1
1	1			X

15 $\bar{b} + \bar{c}$

a \ bc	00	01	11	10
0	1	1		X
1	1	1		1

16 a

a \ bc	00	01	11	10
0		X	X	
1	1	X	X	1

17. $\bar{x}\bar{z} + xz + \bar{x}y$

x \ yz	00	01	11	10
0	1		1	1
1		1	1	

redundant

$\cancel{\bar{a}\bar{b} + a\bar{b} + \bar{a}b}$

x \ yz	00	01	11	10
0	1		1	1
1		1	1	

18

a \ bc	00	01	11	10
0		1		1
1	1		1	

$a\bar{b}\bar{c} + \bar{a}\bar{b}c + abc + \bar{a}b\bar{c}$

$= a(\bar{b}\bar{c} + bc) + \bar{a}(b\bar{c} + \bar{b}c)$

$= a\,\overline{b \oplus c} + \bar{a}\,(b \oplus c)$

$= a \oplus b \oplus c$

$$\left.\begin{array}{r} 7 \\ +\ 8 \\ +\ 9 \end{array}\right\} \text{1 bit addition} \qquad \left.\begin{array}{r} 28 \\ +\ 39 \end{array}\right\} \text{2 bit addition}$$

$$\left.\begin{array}{r} 011 \\ +\ 101 \end{array}\right\} \text{3 bit addition}$$

Full Adder

$$\left.\begin{array}{r} 1 \\ +\ 0 \\ +\ 1 \end{array}\right\} \text{1 bit addition}$$

PAGE NO.:
DATE: / /

FULL ADDER

- consists of 3-inputs and two outputs.
- perform 1 bit binary addition of 3 input bits.

Truth Table

	x	y	z	Sum (S)	Carry (C)
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1

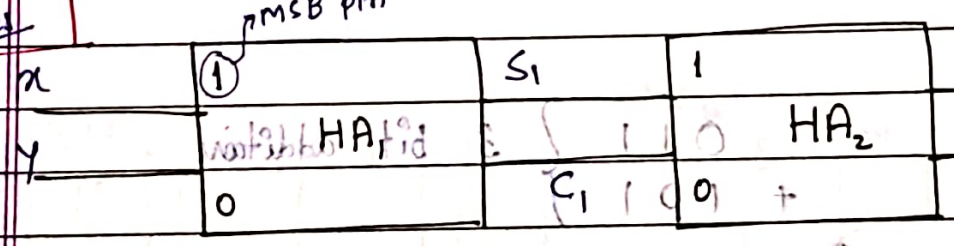
x \ yz	00	01	11	10
0		1		1
1	1		1	

x \ yz	00	01	11	10
0			1	
1		1	1	1

$Sum = \Sigma_m(1,2,4,7)$ $\qquad$ $Carry = \Sigma_m(3,5,6,7)$

$sum = x \oplus y \oplus z$ $\qquad$ $carry = yz + xz + xy$

Ques



$S_1 = x \oplus y$ $\qquad$ $S_2 = S_1 \oplus C_1 = x \oplus y \oplus C_1 = x \oplus y$

$C_1 = x \cdot y$ $\qquad$ $C_2 = S_1 \cdot C_1 = [x \oplus y] \cdot C_1$

$= (x \oplus y) \cdot (x \cdot y)$

$= 0$

PAGE NO. :
DATE : / /

If two half adder are connected in cascade, shown in figure, then find the simplified expression for S_2 and C_2 in terms of input x and y.

$$S_2 = (x\bar{y} + \bar{x}y) \oplus xy$$
$$= \overline{(x\bar{y} + \bar{x}y)}.xy + (x\bar{y} + \bar{x}y)(\overline{xy})$$
$$= A + (x\bar{y} + \bar{x}y)(\bar{x} + \bar{y})$$
$$= A + \bar{x}y + x\bar{y}$$
$$= x \oplus y.$$

$$A = (\bar{x}\bar{y} + xy)\, xy.$$
$$S_2 = (\bar{x}\bar{y} + xy)xy + \bar{x}y + x\bar{y}$$
$$S_2 = xy + \bar{x}y + x\bar{y}$$
$$= x + \bar{x}y$$

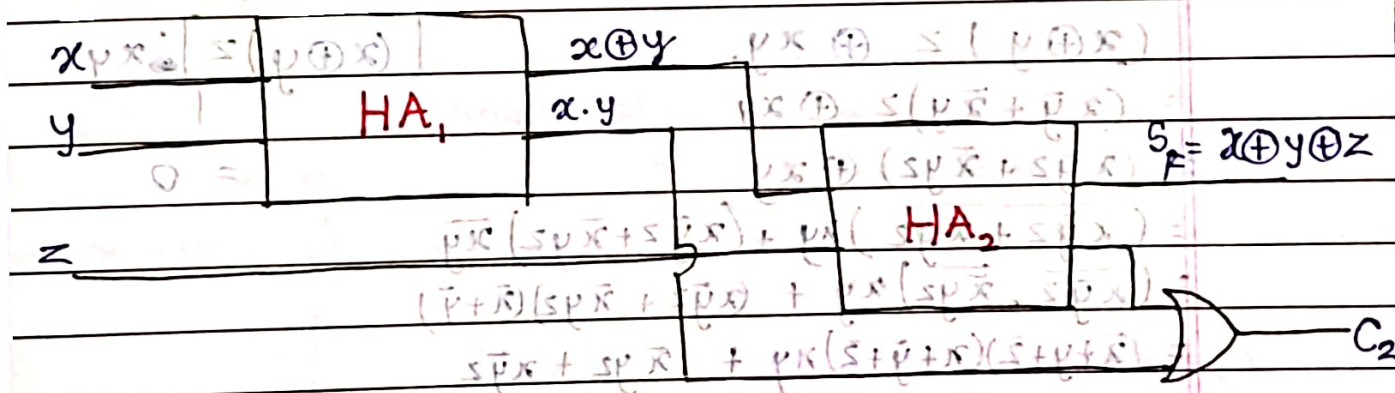
$$\boxed{\begin{aligned} S_2 &= x + y \\ C_2 &= 0 \end{aligned}}$$

Ex Design FA using HA.

FA sum $= x \oplus y \oplus z$ HA sum $= x \oplus y$

carry $= xy + yz + zx$ carry $= x.y$.

2 boolean functions are same to be equal if they have same minterm and maxterms. i.e they must have same K-map.

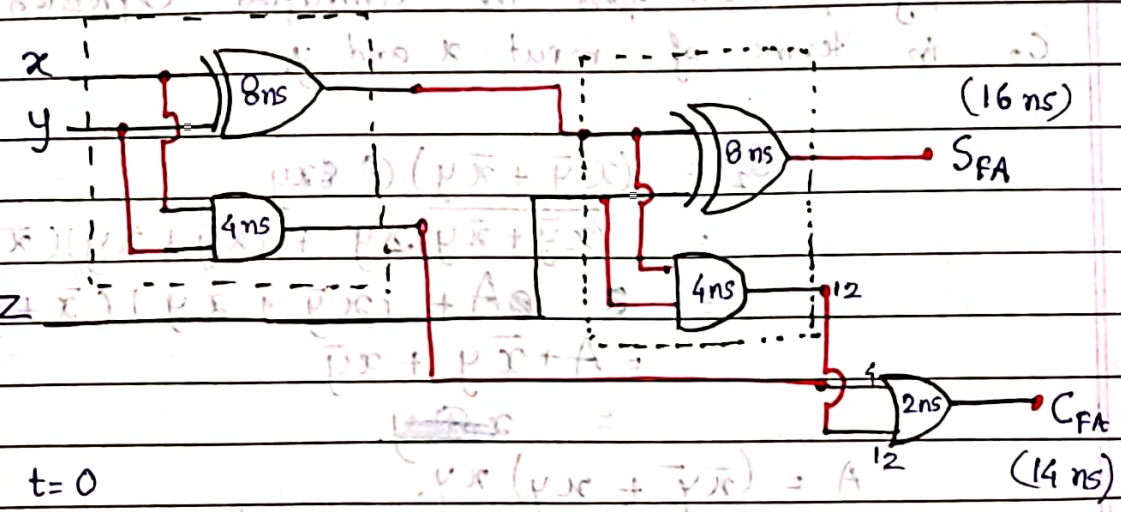


$$C_F = (x \oplus y).z + xy$$
$$\equiv xy + yz + xz$$
$$\equiv \Sigma m(3, 5, 6, 7)$$

$\boxed{\text{FFA} \equiv 2\text{HA} + \text{OR Gate}}$

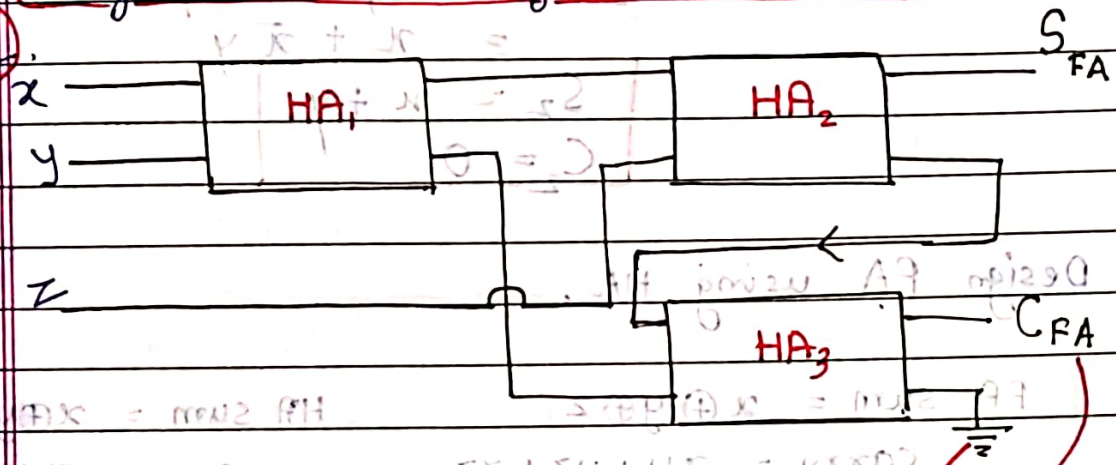
Generalized result of carry

Full Adder Circuit :



Design Full adder using 3 Full Adder :

Ex



$(x \oplus y)z \oplus xy$

$= (x\bar{y} + \bar{x}y)z \oplus xy$

$= (x\bar{y}z + \bar{x}yz) \oplus xy$

$= (\overline{x\bar{y}z + \bar{x}yz})\,xy + (x\bar{y}z + \bar{x}yz)\,\overline{xy}$

$= (\overline{x\bar{y}z} \cdot \overline{\bar{x}yz})\,xy + (x\bar{y}z + \bar{x}yz)(\bar{x} + \bar{y})$

$= (\bar{x} + y + \bar{z})(x + \bar{y} + \bar{z})\,xy + \bar{x}yz + x\bar{y}z$

$= xy + xy\bar{z} + xy\bar{z} + xy\bar{z} + \bar{x}yz + x\bar{y}z$

$= xy + xy\bar{z} + \bar{x}yz + x\bar{y}z$

$= xy + \bar{x}yz + x\bar{y}z$

$= xy + z.(x \oplus y)$ → carry of FA

$\boxed{(x \oplus y)z} \cdot xy$

$= 0$

(2002) - modified

Ex $f(A,B) = A' + B$

the simplified function expression $f(f(x+y, z), z)$ is

(a) $x' + z$

(b) xyz

(c) $xy' + z$

✓(d) None of these.

$f(x+y, z) = \overline{x+y} + z = \bar{x}\bar{y} + z$

$f((\bar{x}\bar{y} + z), z) = \overline{\bar{x}\bar{y} + z} + z = (x+y).\bar{z} + z$

$= x\bar{z} + y\bar{z} + z$

$= x + y + z$

$xy\bar{z}$
100
110

$f(A,B) = A' + B$

$f(f(x+y, y), z)$

(a) $x' + z$

(b) xyz

(c) $xy' + z$

(d) None of these

$f(x+y, y) = \bar{x}.\bar{y} + y$

$= y + \bar{x}$

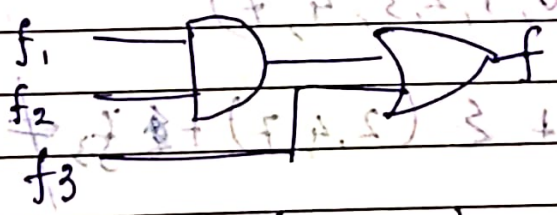
$f \Rightarrow \overline{y + \bar{x}} + z$

$f \Rightarrow \bar{y}.x + z$ ✓

Consider the circuit shown below:

The function f_1, f_2 and f in Canonical SOP notation is given.

$\Sigma(8) + \Sigma(?) = \Sigma(8,9)$



$f_1 \cdot f_2 + f_3 = f$.

$f(w,x,y,z) = \Sigma(8,9)$

$f_1(w,x,y,z) = \Sigma(8,9,10)$

$f_2(w,x,y,z) = \Sigma(7,8,12,13,14,15)$

$f_3 = \Sigma(9)$ ✓

PAGE NO.: _____
DATE: / /

* Multiplication of 2 K-Map generates common 1 in output K-map.
* Addition of 2 K map will generate 1 in all location in union of those K-maps.

Modified Ex

$$\overline{(f_1 \cdot f_2)} \cdot \overline{f_3} = f.$$

$$(\overline{f_1} + \overline{f_2}) \cdot \overline{f_3}$$

$$= \overline{f_1} + \overline{f_2} + f_3$$

$$= f_1 \cdot f_2 + f_3$$

$f = \Sigma(1,4,5)$

$f_1 = \Sigma(0,1,3,5)$

$f_2 = \Sigma(6,5)$

$f_3 = ?$

$$\Sigma(5) + \Sigma(?) = \Sigma(1,4,5)$$

$\Sigma(1,4)$

or

$\Sigma(1,4,5)$

Imp Ex Modified.

$$(f_1 \oplus f_2) \cdot \overline{f_3} = f.$$

$$(f_1 f_2 + \overline{f_1}\,\overline{f_2}) + f_3$$

$$f_1 f_2 + \overline{f_1}\,\overline{f_2} + f_3 = f.$$

$\overline{f_1} = \Sigma(2,4,6,7)$ $\quad \overline{f_1} \cdot \overline{f_2} = \Sigma(2,4,7)$

$\overline{f_2} = \Sigma(0,1,2,3,4,7)$

$$\Sigma(5) + \Sigma(2,4,7) + f_3 \neq \Sigma(1,4,5)$$

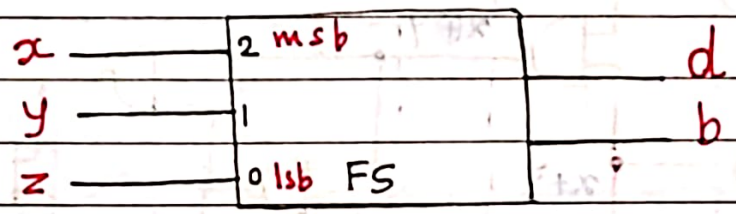
PAGE NO. :
DATE : / /

5

FULL SUBTRACTOR CIRCUIT

- It consist of 3 input and two output

$x - y - z$

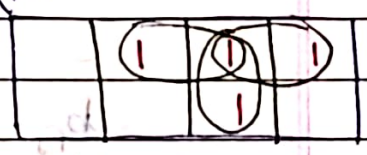


x	y	z	d	b
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$d = \Sigma_m (1, 2, 4, 7) = x \oplus y \oplus z$

$b = \Sigma_m (1, 2, 3, 7) \Rightarrow$

$= \bar{x}y + yz + \bar{x}z$

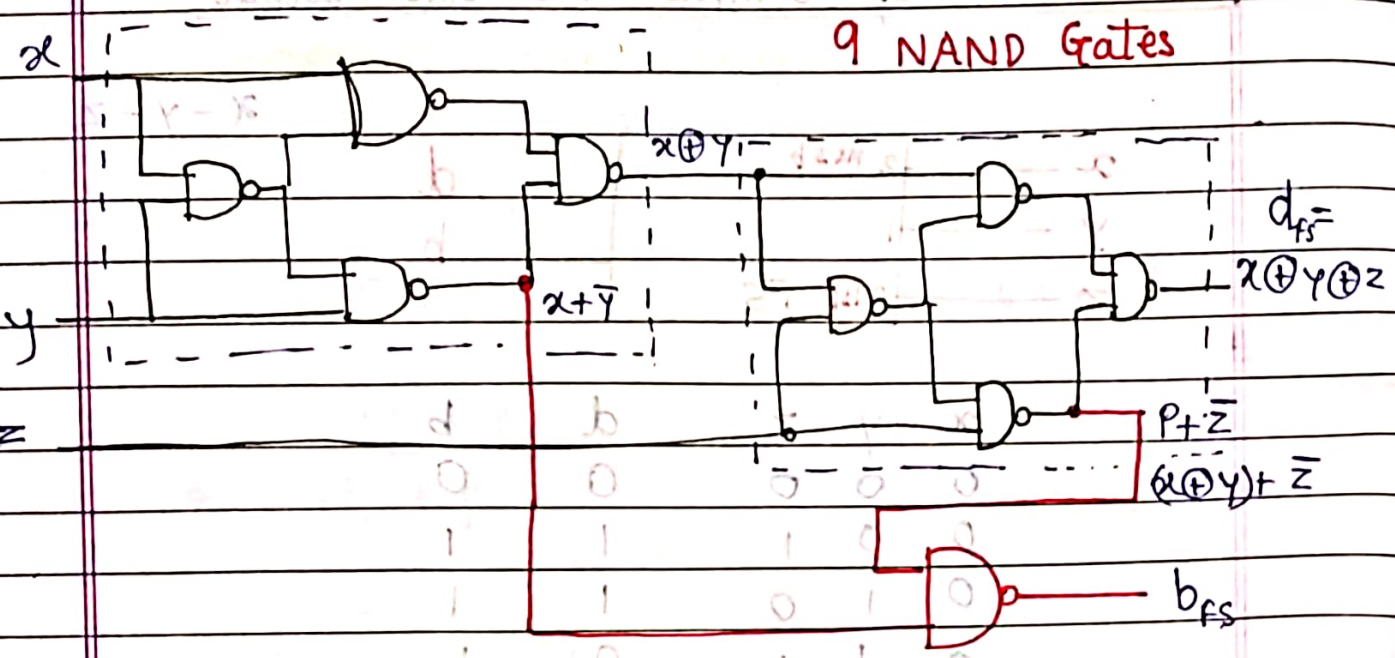


H.W. Design Full Subtractor using Half subtractor.

- Implement full adder and full subtractor using NAND gate.

PAGE NO. :
DATE : / /

IMPLEMENTATION OF FULL SUBTRACTOR (using NAND)



$b_{f.s.}$ $\overline{((x \oplus y) + \bar{z}) \cdot (x + \bar{y})}$

$= (\overline{x \oplus y}) \cdot z + \bar{x} \cdot y$ — ①.

borow of F.S $= \bar{x}y + yz + z\bar{x}$.

draw K-MAP :

x \ yz				
		1	1	1
			1	

$b_{fs} = \bar{x}\bar{y}z + \bar{x}y\bar{z} + xyz + xyz$

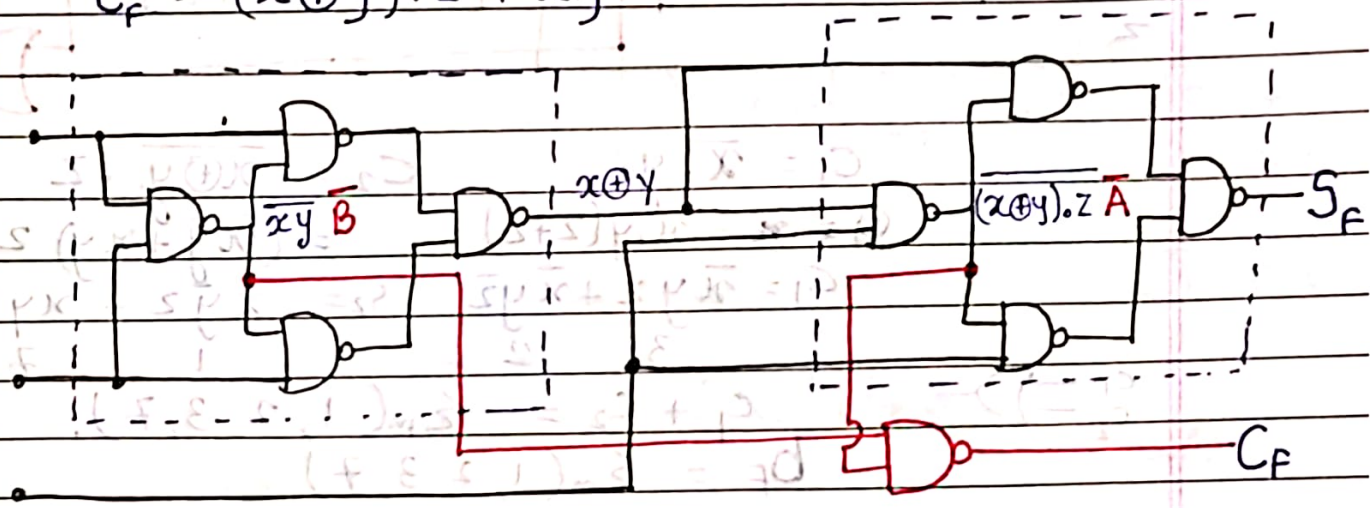
$= \overline{(x \oplus y)} \cdot z + \bar{x}y$. — ②

As ① and ② are same, circuit is correct.

FULL ADDER using NAND GATE only :-

$S_F = x \oplus y \oplus z$

$C_F = (x \oplus y).z + xy$



NAND : $\overline{A.B} = \overline{A} + \overline{B}$

or

$A + B = \overline{\overline{A} . \overline{B}}$

$C_F = (x \oplus y).z + xy.$

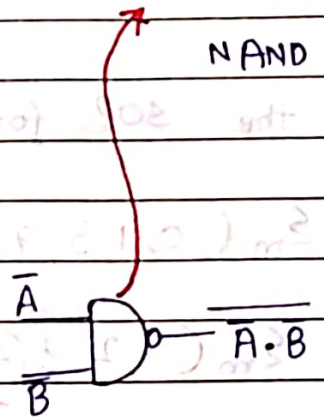
$\quad\quad\quad A \quad\quad\quad B$

$\Rightarrow \overline{\overline{A} + \overline{B}}$

$\Rightarrow \overline{\overline{A} . \overline{B}}$

$\Rightarrow \overline{\underbrace{\overline{(x \oplus y).z}}_{A} . \underbrace{\overline{xy}}_{B}}$

$\Rightarrow \overline{\overline{A} . \overline{B}}$



FULL SUBTRACTOR USING 2 ~~HA~~ HS :

$d_F = x \oplus y \oplus z$

$b_F = \overline{x}.y + yz + \overline{x}z$

$\quad = \overline{x}.y + (\overline{x} + y).z$

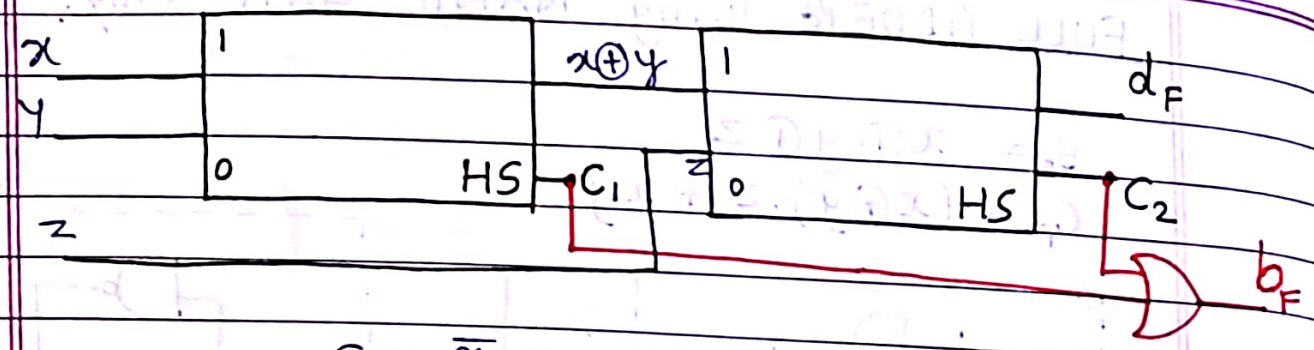
or

$b_F = \overline{x}.y(z + \overline{z}) + \overline{x}z(y + \overline{y}) + yz(x + \overline{x})$

$b_F = \overline{x}.y.z + \overline{x}y\overline{z} + \overline{x}\overline{y}z + xyz.$

$\Sigma_m(1, 3, 2, 7)$

PAGE NO.:
DATE: / /

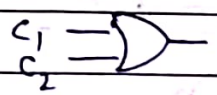


$C_1 = \bar{x} \cdot y$ $\qquad$ $C_2 = \overline{x \oplus y} \cdot z$

$= \bar{x} \cdot y (z + \bar{z})$ $\qquad$ $= (\bar{x}\bar{y} + xy) z$

$C_1 = \bar{x} y z + \bar{x} y \bar{z}$ $\qquad$ $C_2 = \bar{x} \bar{y} z + x y z$

3 $\quad$ 2 $\qquad$ 1 $\quad$ 7

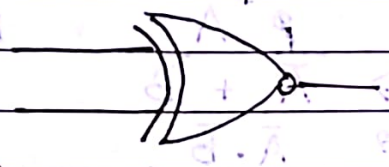


$C_1 + C_2 = \Sigma_m(1, 2, 3, 7)$

$\therefore b_F = \Sigma_m(1, 2, 3, 7)$

Ques Find the SOP form at the output.

$f_1 = \Sigma_m(0, 1, 3, 7)$



$f_2 = \Sigma_m(1, 2, 3, 4)$ This was 6

$f_1' = \Sigma_m(1, 2, 4, 5, 6)$

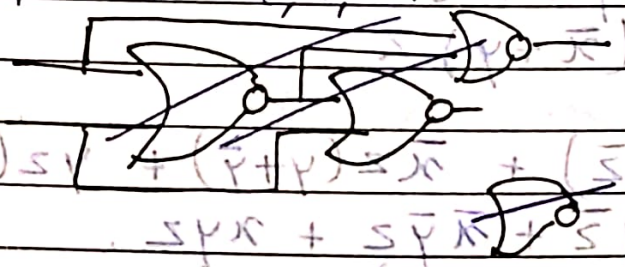
$f_2' = \Sigma_m(0, 5, 6, 7)$

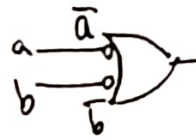
$f_1 \bar{f}_2 + \bar{f}_1 f_2$

$\Sigma_m(0, 7) + \Sigma_m(2, 4)$

$= \Sigma(0, 2, 4, 7)$

Ex Find the output for the given circuit where input is a, b, c.

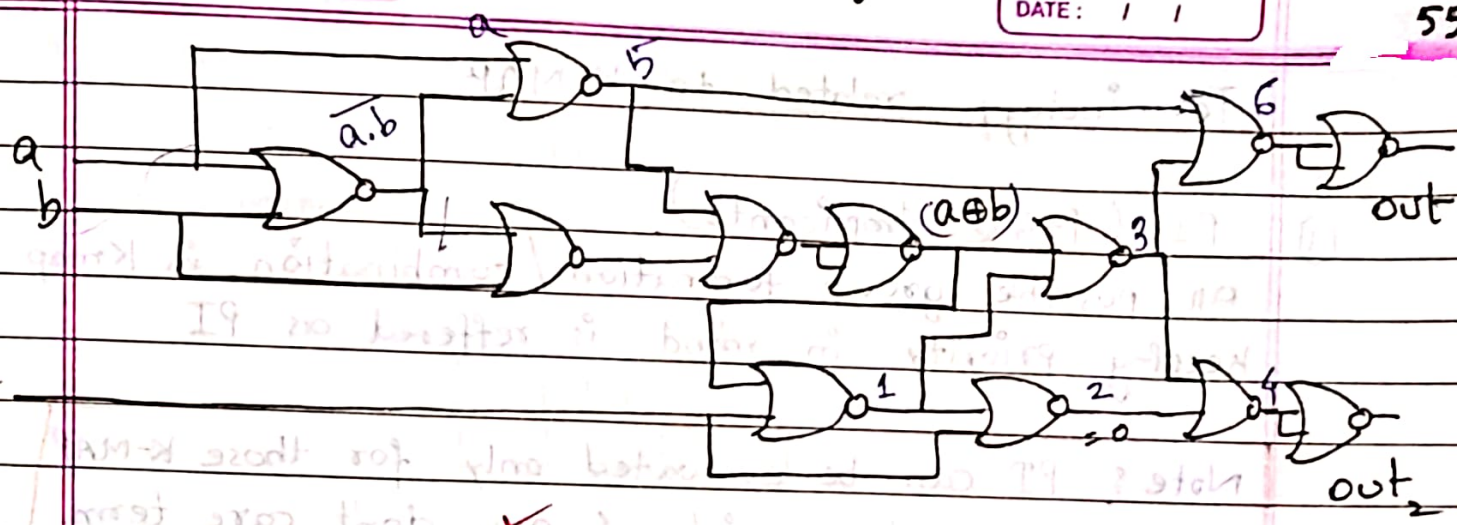




$\overline{a.b}$ NAND

PAGE NO. :
DATE : / /

55



1 : $(a\oplus b)\cdot c = \cancel{(a\oplus b)+c}$ $\quad a\oplus b + c = \overline{a\oplus b}\cdot\bar{c}$ ✓

2 : $\cancel{\overline{(\overline{(a\oplus b)}\cdot c)}\cdot c} = \cancel{((a\oplus b)\cdot c)+\bar{c}}$

$\overline{a\oplus b}.\bar{c} + c = \cancel{\bar{c}+(a\oplus b)} = \cancel{0}$

$= \overline{a\oplus b + c} = (a\oplus b).\bar{c}$ ✓

3 : $(a\oplus b)+\overline{(a\oplus b)}\cdot\bar{c} = \cancel{(a\oplus b)[\overline{a\oplus b}+\bar{c}]}$ $\quad A+\bar{A}B = A+B$

$= \overline{a\oplus b}.c$ ✓ $\quad = \cancel{(a\oplus b)\cdot\bar{c}}$

out_2 $\boxed{4} = 2+3 = \cancel{\bar{c}+(a\oplus b)+(a\oplus b)\cdot\bar{c}}$

difference $= \overline{a\oplus b}.c = \cancel{(a\oplus b)\cdot\bar{c}} = a\bar{b}\bar{c} + \bar{a}b\bar{c}$

$+2$ $\quad + abc + \bar{a}\bar{b}c$ ✓

$5 = \overline{a.\overline{a.b}} = a.(\bar{a}+\bar{b}) = a+\bar{b} = \overline{\bar{a}.b}$

$= \bar{a}.b$ ✓

borrow

out_1 $\boxed{6} = \bar{a}.b + \cancel{(a\oplus b)\cdot\bar{c}}$ $\quad \overline{a\oplus b}.c$

$\bar{a}.b + \bar{a}\bar{b}c + \bar{a}bc$ ✓

Full subtractor using NOR Gates.

PAGE NO. :
DATE : / /

Terminology related to K-MAP

① **PI (Prime Implicants)**

All possible group formation / combination in Kmap keeping priority in mind is reffered as PI

Note : PI can be evaluated only for those K-MAP which does not consist of any don't care term.

a \ bc	00	01	11	10
0		1		1
1		1	1	1

4 PI

x \ yz	01	01	11	10
0	1	1		1
0		1	1	

4 PI

ab \ c	0	1
00		1
01	1	1
11	1	
10	1	1

6 PI

ab \ cd	00	01	11	10
00	1	1		
01		1	1	
11			1	1
10				1

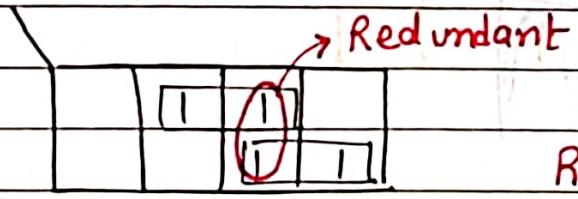
6 PI

	00	01	11	10
00	1			
01		1	1	1
11		1	1	
10	1		1	

4 PI

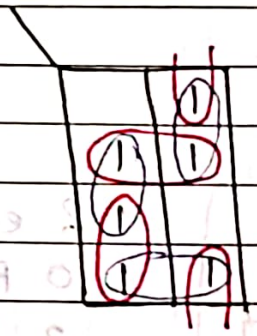
② Redundant prime implicant :

Unwanted Group formed in K-MAP, removal of which still makes the K-MAP to be completed



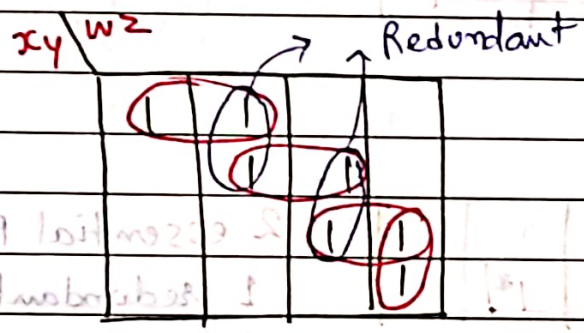
PI = 3
Redundant = 1.
Essential = 2

Ques Find number of RPI for the given K-Map.



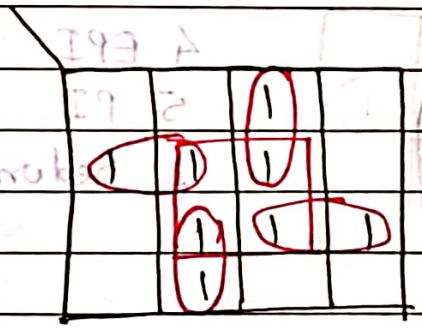
PI = 6
Essential = 0
Redundant = 3

Ques



2 essential
2 redundant
6 total.

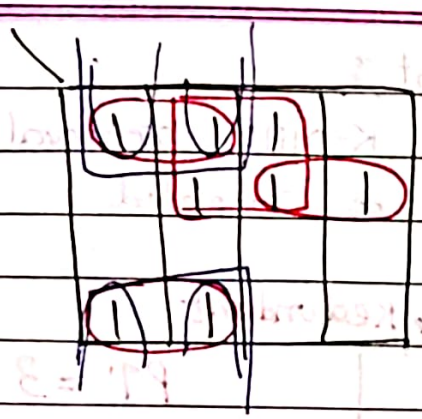
Ques Find number of RPI and PI for given K-Map



1 redundant PI
5 PI
4 essential.

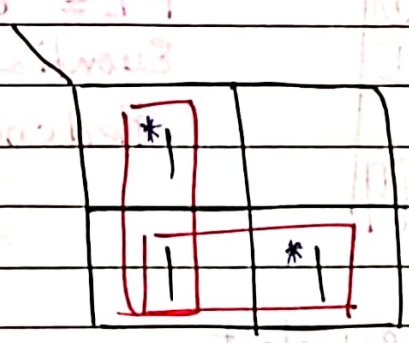
PAGE NO. :
DATE : / /

Ex

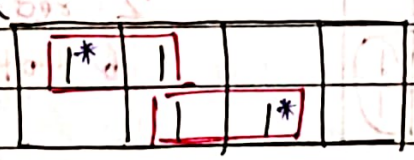


3 essential.
0 redundant
3 PI

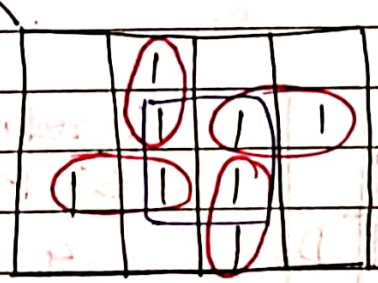
Essential Prime implicant (EPI):
unique group formed in K-MAP considering priority. And the uniqueness is defined by presence of atleast a singe 1 which is forming group in a single pattern.



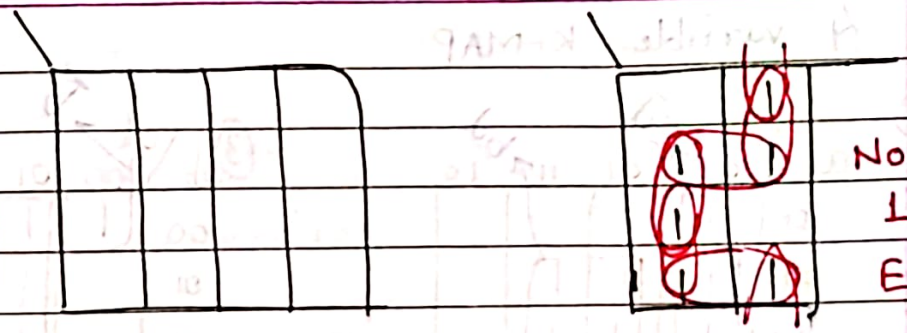
2 essential PI
0 Redundant
2 PI



2 essential PI
1 redundant
3 PI



4 EPI
5 PI
1 Redundant



No unique 1,
EPI = "0"

Ex Find the compliment of given Boolean function:

$$f = ab + bc + ac = \Sigma_m(6, 7, 3, 5)$$

$$f = (\bar{a}+\bar{b}) \cdot (\bar{b}+\bar{c}) \cdot (\bar{a}+\bar{c}) \Rightarrow \Sigma_m(0, 1, 2, 4)$$

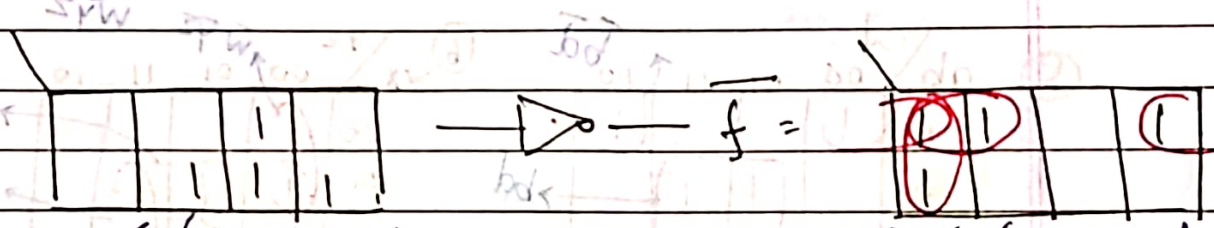
Ex

$$f = \bar{a}b + a\bar{b}$$

$$\bar{f} = (a+\bar{b}) \cdot (\bar{a}+b)$$

$$= \bar{a}\bar{b} + ab. \checkmark$$

$f =$



$\Sigma(3, 5, 6, 7) \longrightarrow \Sigma(0, 1, 2, 4)$

$\Pi(0, 1, 2, 4) \longrightarrow \Pi(3, 5, 6, 7)$

$$f' = \bar{b}\bar{c} + \bar{a}\bar{c} + \bar{a}b$$

Note: No of different function (boolean) which can be formed by n variable input.

a	b	f_1	f_2	f_3	f_4	f_5	f_6	....	f_{5}
0	0	1	0	0	0	1	0		1
0	1	0	1	0	0	1	1		1
1	0	0	0	1	0	0	1		1
1	1	0	0	0	1	0	0		1

2^{2^n}

2 - variable $\rightarrow$ 2^2 16 different functions

PAGE NO. :
DATE : / /

4-variable K-MAP

①

ab \ cd	00 ($\bar{c}\bar{d}$)	01	11 (bd)	10
00	1			
01	1	1	1	
11	1	1	1	
10	1			

③

ab \ cd	00 ($\bar{b}$)	01	11 (d)	10
00	1	1	1	1
01		1	1	
11		1	1	
10	1	1	1	1

②

ab \ cd	00	01 ($\bar{b}d$)	11	10
00		1		
01	1	1		
11	1	1	1	1
10		1		

$b\bar{c}$ ab

④

WX \ YZ	00 ($\bar{W}\bar{Y}\bar{Z}$)	01	11 (XYZ)	10
00	1			
01	1		1	
11		1	1	1
10		1		1

$\bar{W}\bar{Y}Z$ WYZ

⑤

ab \ cd	00	01	11	10 ($\bar{b}\bar{d}$)
00	1			1
01		1	1	
11		1	1	
10	1			1

bd

⑥

WX \ YZ	00 ($W\bar{Y}\bar{Z}$)	01	11	10
00	1			
01	1	1	1	
11			1	
10		1		1

$\bar{W}XZ$ $XY\bar{Z}$ $W\bar{X}Y\bar{Z}$ $W\bar{X}\bar{Y}Z$

Ex Simplify $f = \Sigma_m(1, 2, 4, 7, 13, 14, 8, 11)$

WX \ YZ	00	01	11	10
00		1		1
01	1		1	
11		1		1
10	1		1	

$W \oplus X \oplus Y \oplus Z$

apoorv135@gmail.com

Ex Find the number of min term for the given boolean function

$$f = a \oplus b \oplus c \oplus d \oplus e \oplus f \oplus g \oplus h.$$

n variable 2^{n-1} minterms.

* Maximum no of EPI

- n - variables

$\boxed{2^{n-1} \text{ maximum EPI}}$

2^{n-1} maximum minterm or maxterm.

(only when it is X-OR or X-NOR)

a \ b	
	1
1	

$a \oplus b$

a \ bc			
	1		1
1		1	

$a \oplus b \oplus c$

Imp 2004
Ex Which are EPI of the following boolean function

$f(a,b,c) = a'c + ac' + b'c = \Sigma m(1,3,4,6,5)$

(a) $a'c + ac'$
(b) $a'c + b'c$
(c) $a'c$ only
(d) ac' & bc'

a \ bc	00	01	11	10
0			1	1
1	1	1		1

a \ bc	00	01	11	10
0		1	1*	
1	1	1		1*

$\bar{a}c$

$a\bar{c}$

- For the given example, $a'c$, ac', $b'c$ represent implicants of a given boolean function.

PAGE NO. :
DATE : / /

minterm of the given boolean function is
$f = \Sigma_m(1, 3, 4, 5, 6)$

Ex The minterm expansion of
$f(P, Q, R) = PQ + Q\bar{R} + P\bar{R}$.
$= \Sigma_m(6, 7, 2, 4)$

(a) $m_2 + m_4 + m_6 + m_7$
(b) $m_0 + m_1 + m_3 + m_5$
(c) $m_0 + m_1 + m_6 + m_2$
(d) $m_2 + m_3 + m_4 + m_5$

2012 **Ex** Simplify K-MAP

cd \ ab	00	01	11	10
00	1	X	X	1
01	X			1
11				
10	1			X

$\bar{c}\bar{b}$

$\bar{d}\bar{b}$

Consider boolean function f. The equivalent simplification of f is ?

$$F(P, Q) = \left((1 \oplus P) \oplus (P \oplus Q)\right) \oplus \left[(P \oplus Q) \oplus (Q \oplus 0)\right]$$

$$\left[\bar{P} \oplus (P \oplus Q)\right] \oplus \left[(P \oplus Q) \oplus Q\right]$$

$$= \left[\bar{P}(P \odot Q) + P(P \oplus Q)\right] \oplus \left[(P \odot Q)Q + (P \oplus Q)\bar{Q}\right]$$

$$= \left[\bar{P}(\bar{P}\bar{Q} + PQ) + P(P\bar{Q} + \bar{P}Q)\right] \oplus \left[(\bar{P}\bar{Q} + PQ)Q + (P\bar{Q} + \bar{P}Q)\bar{Q}\right]$$

$$= (\bar{P}\bar{Q} + P\bar{Q}) \oplus (\bar{P}\bar{Q} + PQ + P\bar{Q})$$

$$\bar{Q} \oplus (PQ + \bar{Q})$$

$$= \cancel{Q(PQ + \bar{Q}) + \bar{Q}(\bar{P} \cdot Q)}$$

$$= \cancel{PQ} \quad PQ \quad \times \quad \text{[use associative law]}$$

PAGE NO.:
DATE: / /

Ex The literals count of the boolean expression is the sum of number of times each literal appear in the expression. For example, the literal count of $(xy + xz)$ is 4. What are the minimum possible literal count of POS and SOP boolean function for the given K-MAP.

xy \ zw	00	01	11	10
00	X	1	0	1
01	0	1	X	0
11	1	X	X	0
10	X	0	0	X

SOP = 2 + 3 + 3 = 8

POS = 2 + 2 + 1 + 1 = 2 + 3 = 9

(9, 8) ✓

Ex find the simplified expression for given K-MAP.

ab \ cd	00	01	11	10
00			1	
01	1	1	1	
11		1	1	1
10		1		

$\bar{a}cd$

$\bar{a}b\bar{c}$

abc

$a\bar{c}d$

PAGE NO. :
DATE : / /

Concensus Theorem or Removal of redundancy theorem

Not required

$\bar{a}b + bc + ac = \bar{a}b + ac$

$xy + \bar{y}z + zx = \bar{y}z + xy$

$pq + qr + \bar{r}p = \bar{r}p + rq$

$(\bar{a}+b)(b+c).(a+c) = (\bar{a}+b)(c+a)$

$(x+y)(\bar{y}+z)(x+z) = (\bar{y}+z)(x+y)$

DUALITY: while applying duality property AND converts to OR and vice versa.

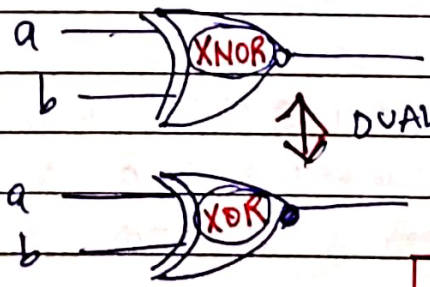
$\cdot \rightleftarrows +$

Duality property converts positive logic System to negative logic system.

(+v) PLS $\rightleftarrows$ NLS (-v)

Ex Find the dual of given logic gate.

(1)



$\boxed{f = \bar{a}\bar{b} + ab}$ (PLS) $\equiv (\bar{a}+\bar{b}).(a+b)$ (NLS).

$\boxed{f_D = \bar{a}b + a\bar{b}}$

$\boxed{a \rightarrow \bar{a}}$

stays same

PAGE NO. :
DATE :

(0,7) (1,6) (2,5) (3,4)

$$\oplus \rightleftarrows \odot$$

Ex Find the dual of the function $f = ab + ac + ca$.

$$f_D = \cancel{(\bar{a}+\bar{b})(\bar{a}+c)} \quad (a+b)(a+c)(c+a)$$
$$= ab + ac + ca.$$
$$= f.$$

$\therefore$ if $f = f_D$ then it is self-dual.

$$\bar{f} = \bar{a}\bar{b} + \bar{b}\bar{c} + \bar{c}\bar{a}$$
$$\bar{f}_D = (\bar{a}+\bar{b})(\bar{b}+\bar{c})(\bar{a}+\bar{c})$$
$$= (\bar{a}+\bar{b}\bar{c})(\bar{b}+\bar{c})$$
$$\bar{f}_D = \bar{a}\bar{b} + \bar{b}\bar{c} + \bar{a}\bar{c}$$

$\bar{f} = \bar{f}_D$ $\therefore$ Compliment of ~~self~~ self dual is also self dual

Characteristics of Self dual function:

$$f = ab + bc + ac = \Sigma_m(3, 5, 6, 7).$$

011 101 110 111

100 010 001 000

(4) (2) (1) (0)

unfilled.

a \ bc	00	01	11	10
0			1	
1	1	1	1	1

"Half filled".

$$\bar{f} = \bar{a}\bar{b} + \bar{b}\bar{c} + \bar{a}\bar{c} = \Sigma_m(0, 1, 2, 4).$$

"Half filled"

7 6 5 3

unfilled.

a \ bc	00	01	11	10
0	1	1		1
1	1			

PAGE NO. :
DATE : / /

a \ b	0	1
0		1 → 01
1	1 → 10	

Not empty.

Half filled

a \ bc	00	01	11	10
0		1	1	
1		1	1	

a	b	c	
0	0	0	
0	0	1	(0, 7)
0	1	0	(1, 6)
0	1	1	(2, 5)
1	0	0	(3, 4)
1	0	1	
1	1	0	
1	1	1	

Mutually exclusive term

→ From all above example, the necessary condition for a function to be self dual

(i) It should be a neutral function, a half-filled K-MAP. i.e No of minterms is equal to no of max terms.

(ii) Now the sufficient condition for a function to be self dual, that it should not contain mutually exclusive terms.

1		1	1	0
			1	1

Ex Identify the given function to be neutral or self dual or both.

① $f = \Sigma m(0, 7, 1, 2)$ → Neutral Not-self-Dual

② $f = \Pi M(0, 1, 5, 3)$ → Neutral, self dual

③ $f = \Sigma m(7, 6, 2, 4)$ → Neutral, self dual

④ $f = \Pi M(7, 1, 2, 5)$ → Neutral, Not SD

⑤ $f = \Sigma m(2, 5, 1, 4)$ → Neutral, Not SD

⑥ $f = \Sigma m(0, 1, 3)$ → Not N, Not SD

⑦ $f = \Sigma m(1, 2, 4, 7)$ → N, SD.

Number of neutral functions possible for 2 variable function = 6.

Number of neutral functions possible for n variable functions = ${}^{2^n}C_{2^{n-1}}$

Total possibility of self dual function for 3 variable, $2^{2^{3-1}} = 16$.

No. of self dual functions possible for n variable $= 2^{2^{n-1}}$.

PAGE NO. :
DATE : / /

Neutral

Self Dual

$$2^{2^n} > {}^{2^n}C_{2^{n-1}} > 2^{2^{n-1}}$$

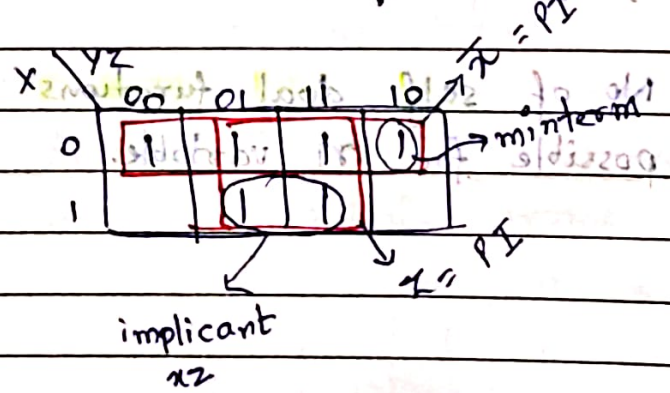
- 2^{2^n} → Total No. of function using n-variables
- ${}^{2^n}C_{2^{n-1}}$ → No of Neutral functions for n variables
- $2^{2^{n-1}}$ → No of self dual functions for n-variable.

- A self dual function is always neutral. But all neutral function cannot be a self dual function.

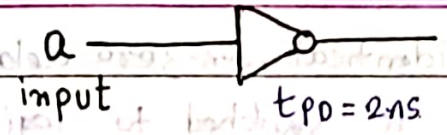
Homework

Ex Let $f(x, y, z) = \bar{x} + \bar{y}z + xz$ be a switching function then which of the following is true?

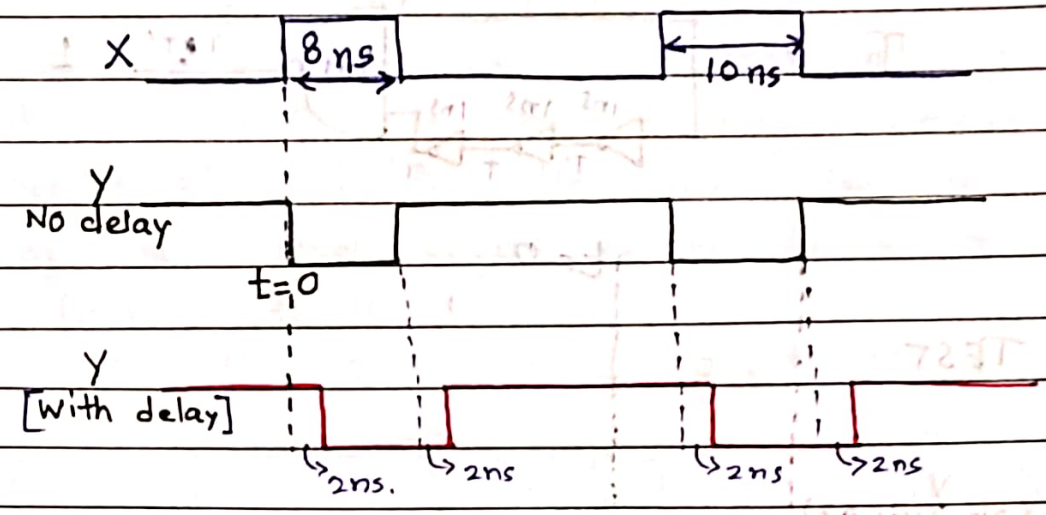
(a) $\bar{y}x$ is a PI of f
(b) xz is a minterm of f
✓(c) xz is an implicant of f
(d) y is a PI of f.

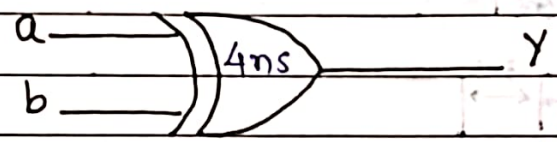


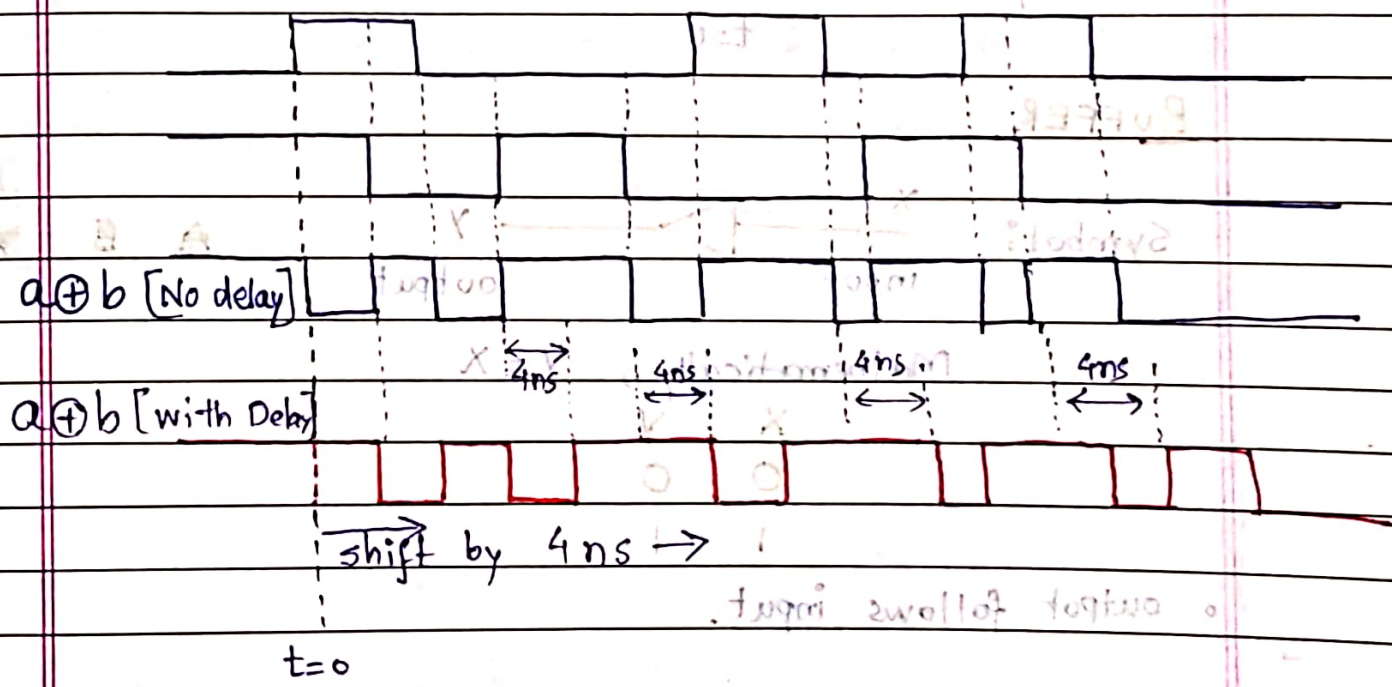
DELAYS.

Q.) 

Draw the output waveform of Y.

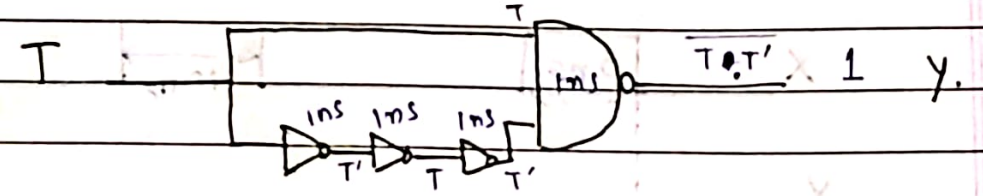


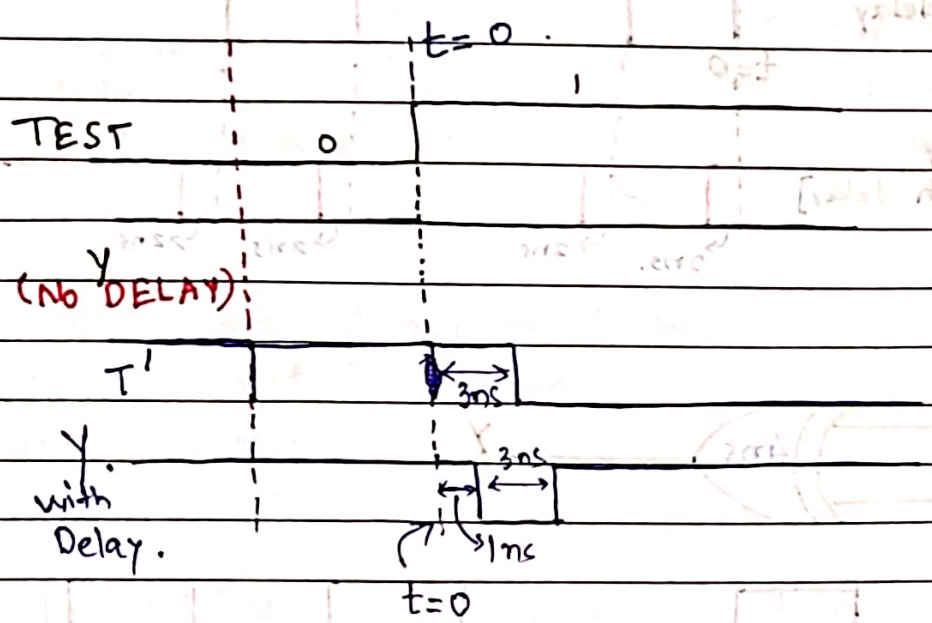
Ex 



PAGE NO. :
DATE : / /

Ex All gates in figure have identical non-zero delay. TEST, T which was at low logic is switched to logic high and maintained at logic high.





BUFFER

Symbol:

A B Y

Mathematically, $Y = X$

X	Y
0	0
1	1

- output follows input.

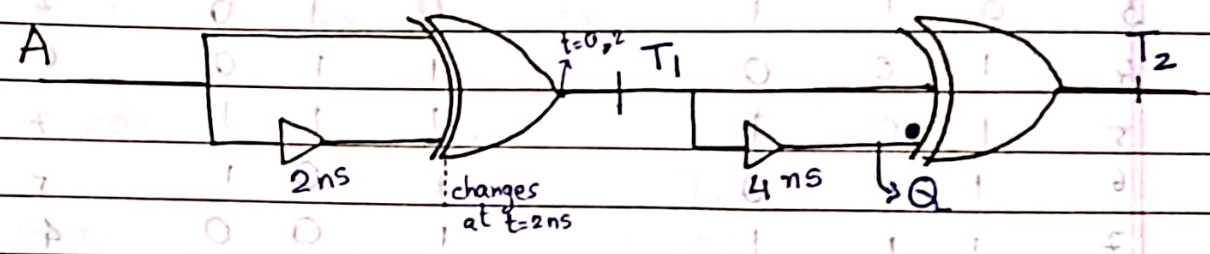
PAGE NO. :
DATE : / /

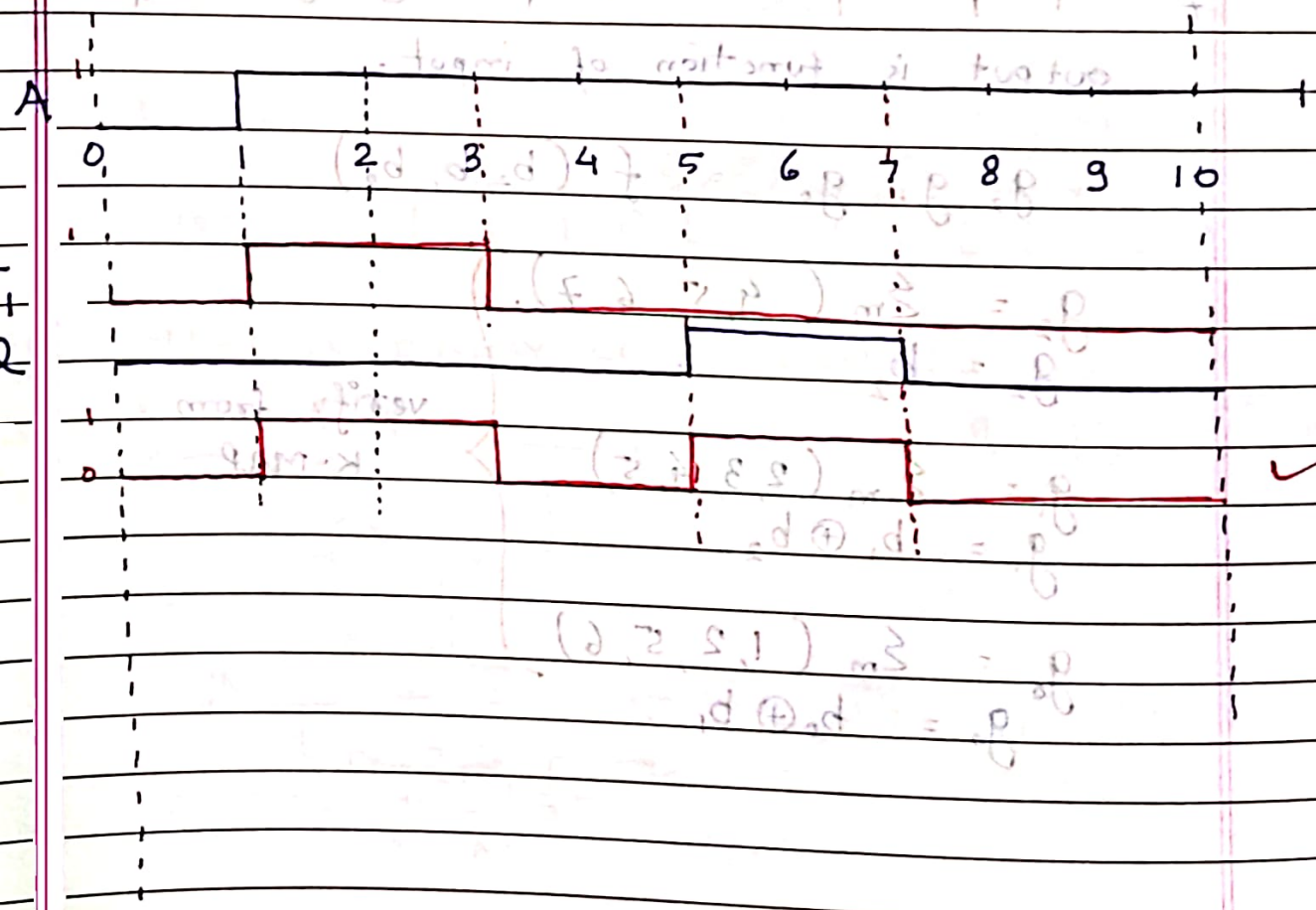
71

IMP

Q.) Consider a following circuit composed of non-inverting buffer and X-OR gate. Buffers have delay of $\delta_1 = 2ns$ and $\delta_2 = 4ns$ as shown in figure. Both XOR gate and all the wires have zero delay. Assume that all gates input / output and wire are stable at logic zero at time $t=0$. If the following waveform is applied at input A, How many transitions (change of logic level occurs at B during the interval from 0 to 10 ns?

(a) 1 (b) 2 (c) 3 (d) 4.





PAGE NO. :
DATE : / /

BINARY TO GREY CODE CONVERTER.

- Consider 3 bit ~~Grey~~ binary code and corresponding grey code.

	b_2	b_1	b_0	g_2	g_1	g_0	
0	0	0	0	0	0	0	
1	0	0	1	0	0	1	1
2	0	1	0	0	1	1	3
3	0	1	1	0	1	0	2
4	1	0	0	1	1	0	6
5	1	0	1	1	1	1	7
6	1	1	0	1	0	1	5
7	1	1	1	1	0	0	4

output is function of input.

$$g_2\, g_1\, g_0 = f(b_2, b_1, b_0)$$

$$g_2 = \Sigma m(4, 5, 6, 7)$$
$$g_2 = b_2$$

$$g_1 = \Sigma m(2, 3, 4, 5)$$
$$g_1 = b_1 \oplus b_2$$

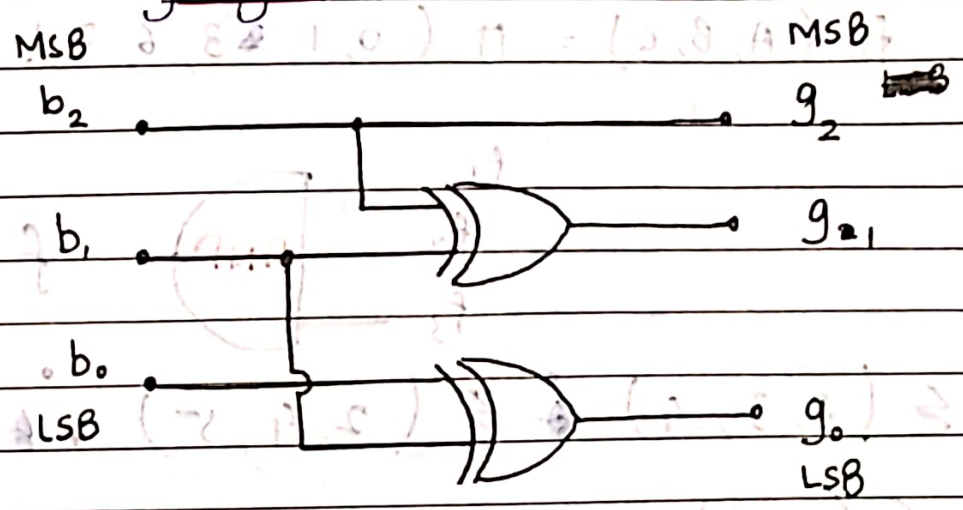
$$g_0 = \Sigma m(1, 2, 5, 6)$$
$$g_0 = b_0 \oplus b_1$$

verify from K-MAP.

PAGE NO. :
DATE : / /

73

Circuit Designing :



Convert Binary to Grey:-

~~Binary~~ ~~1 0 1 1 0 0 1 1 0 1 0 1 1~~

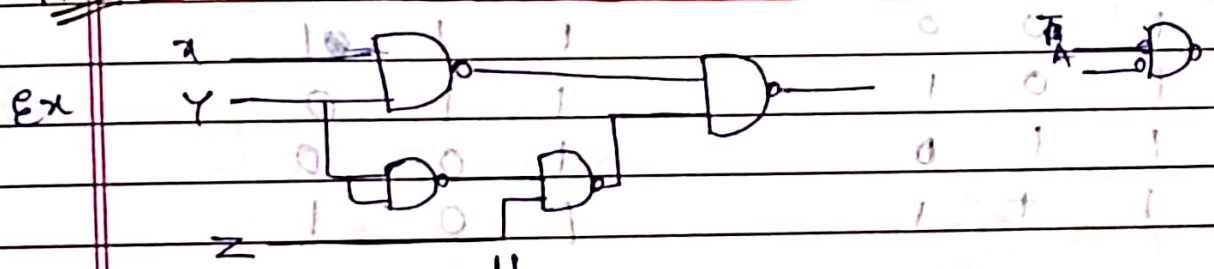
~~Grey~~ ~~1 1 0 1 1 1 0 1~~

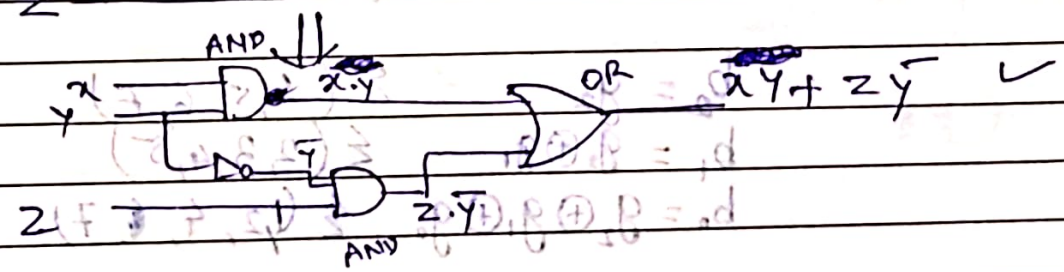
Binary	1	0	1	1	0	0	1	1	0	1	0	1	1
Grey	1	1	1	0	1	0	1	0	1	1	1	1	0

HW GREY TO BINARY CODE CONVERSION

$\overline{\bar{A}.\bar{B}} = A+B$

Ex

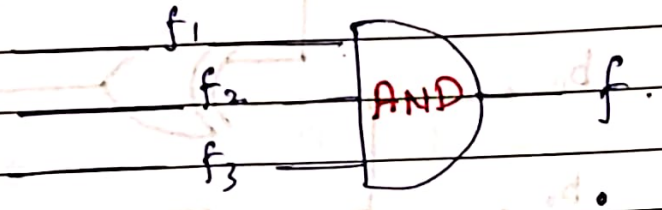




PAGE NO. :
DATE : / /

$f_1(A,B,C) = \Sigma(2,3,4)$

$f_2(A,B,C) = \Pi(0,1,3,6,7)$



$\Sigma(2,3,4) \cdot \Sigma(2,4,5) \cdot \Sigma(?)$

$\Sigma(2,4) \cdot f_3 = 0$

$\Sigma(\underbrace{0,1,3,5,6,7}_{\text{6 minterms}})$ ✓

⇒ Gray to Binary code Conversion

g_2	g_1	g_0	b_2	b_1	b_0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1

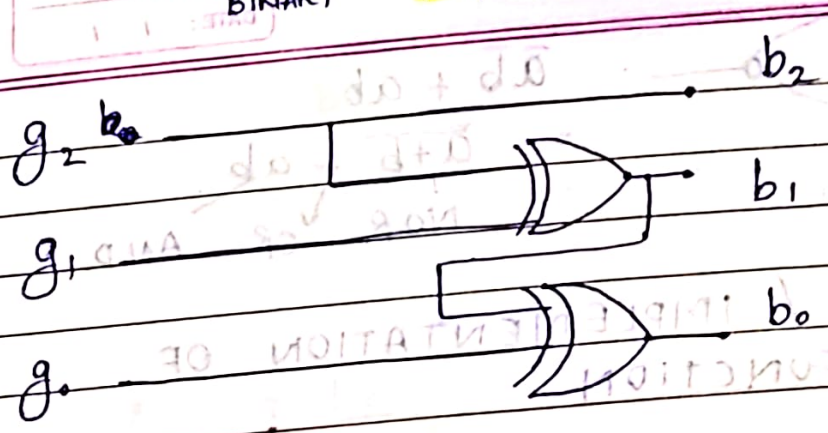
$b_2 = g_2$ $\quad \Sigma(4,5,6,7)$

$b_1 = g_2 \oplus g_1$ $\quad \Sigma(2,3,4,5)$

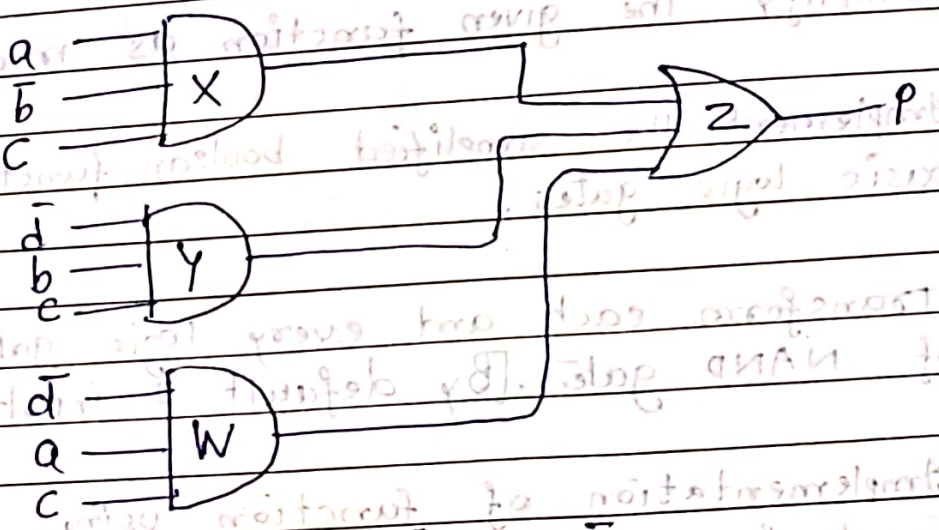
$b_0 = g_2 \oplus g_1 \oplus g_0$ $\quad \Sigma(1,2,4,7)$

GRAY 1 0 1 1 0 1

BINARY 1 1 0 1 1 0



Ex



$P = \underset{1\,0\,1}{a\bar{b}c} + \underset{1\,0\,1\,0}{\bar{a}bc\bar{d}} + \underset{1\,1\,1\,0}{acd\bar{d}}$

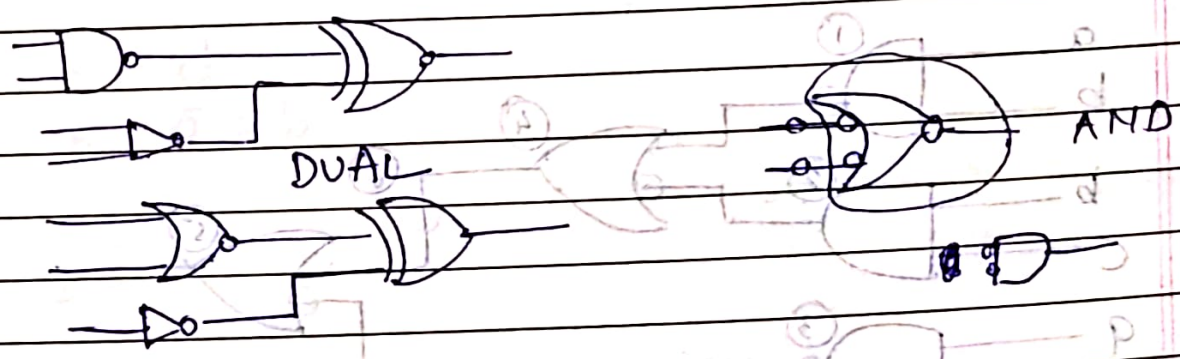
Redundant

Ans. W

ab \ cd	00	01	11	10
00				1
01				1
11			1	1
10				

RPI

Ex



PAGE NO. :
DATE : / /

CLASS-19

Ex

$\bar{a}\bar{b} + ab$

$= \overline{a+b} + ab$

NOR OR AND

DESIGNING / IMPLEMENTATION OF BOOLEAN FUNCTION

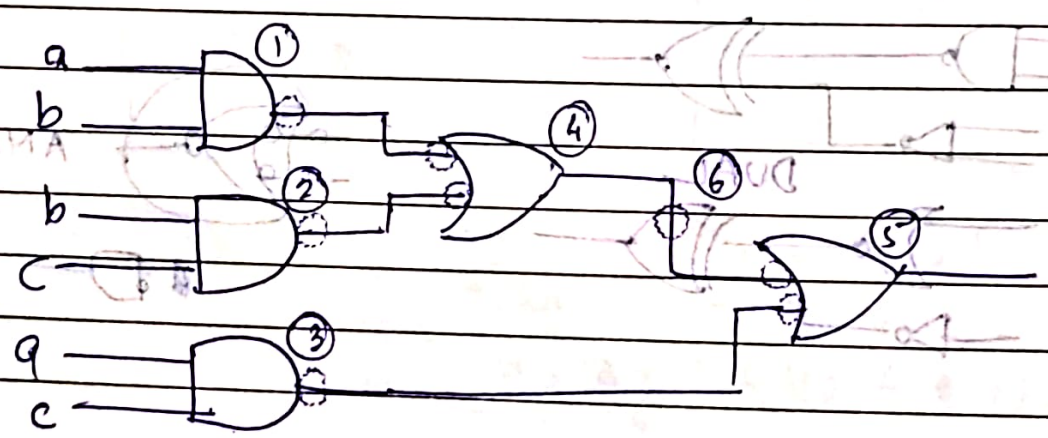
(i) Simplify the given function as much as we can.

(ii) Implement the simplified boolean function using basic logic gates.

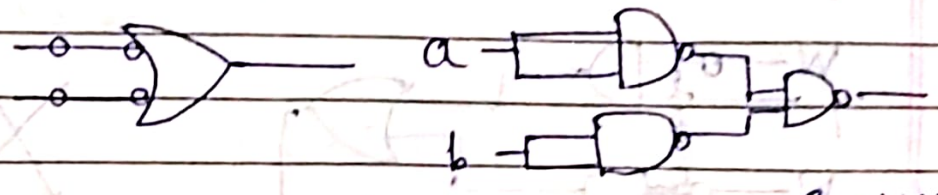
(iii) Transform each and every logic gate in terms of NAND gate. [By default 2 input logic Gate]

(iv) Implementation of function using NAND emphasize towards boolean function to be expressed in SOP form.

Ex Find min number of 2 input Nand gate to design given Boolean function $AB + BC + CA$

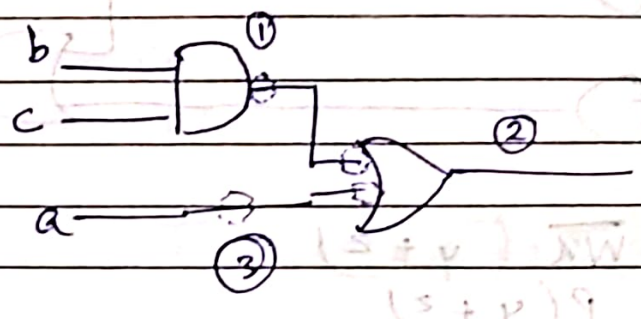


Ex $f = a + b$.

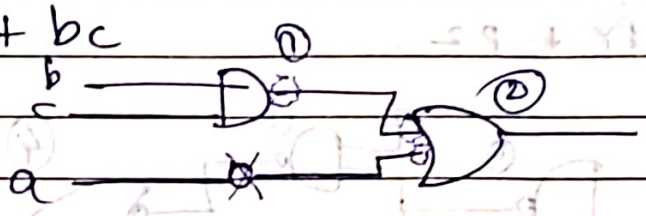


3 NAND

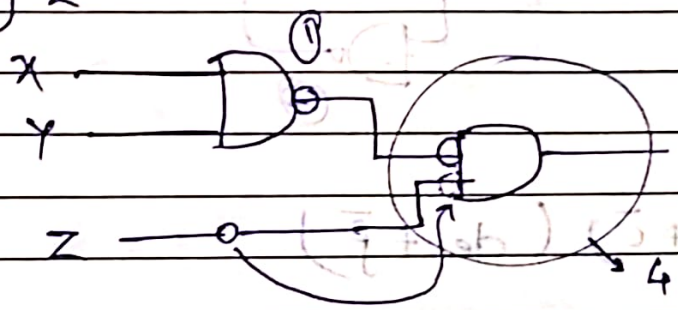
Ex $f = a + bc$

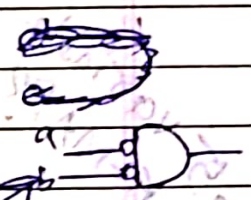


Ex $\bar{a} + bc$



Ex $x y \bar{z}$



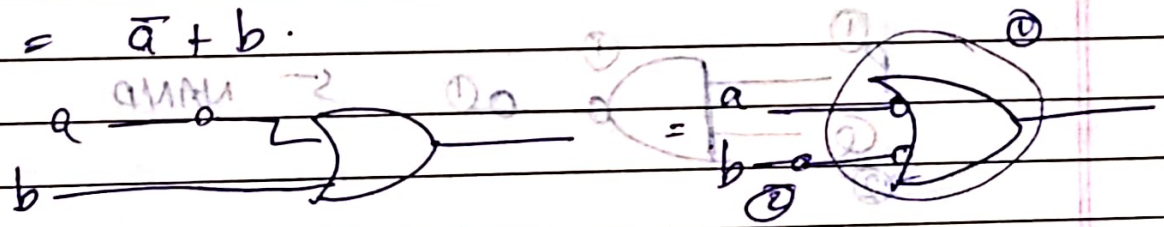


$\bar{a} . \bar{b}$ $\overline{a+b}$

4 NANDS + 1 NAND

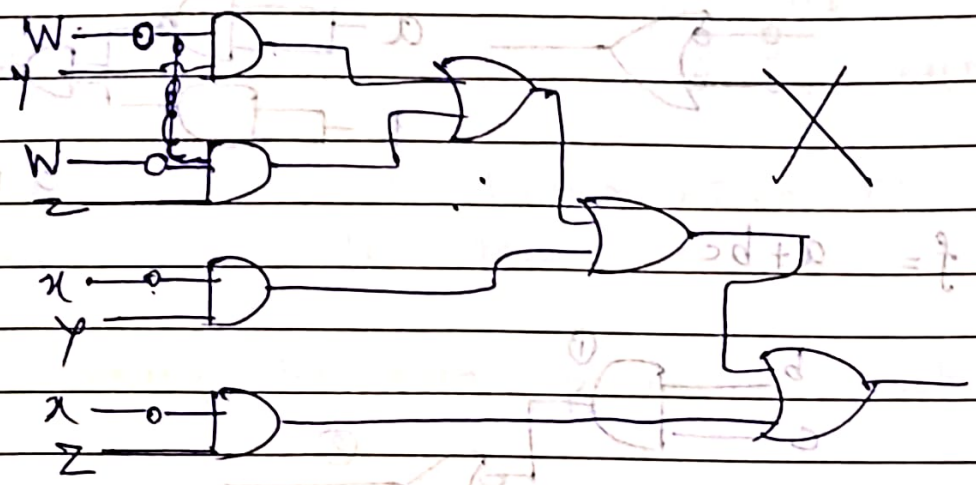
Ex $\bar{a} + ab$

$= \bar{a} + b$.

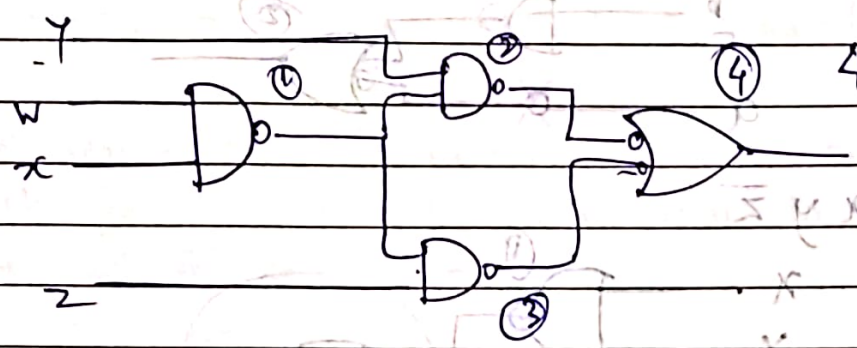


PAGE NO. :
DATE : / /

$$f = \bar{w}y + \bar{w}z + \bar{x}y + \bar{x}z$$



$$f = \overline{wx}\,(y+z)$$
$$= p(y+z)$$
$$= py + pz$$

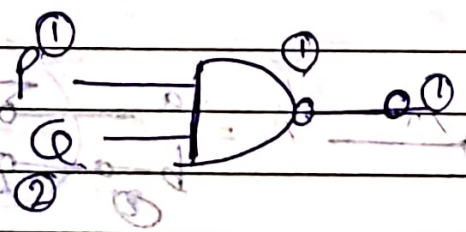


4 NAND

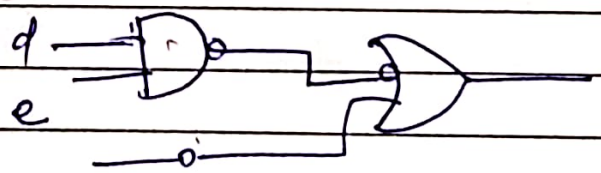
5 variable K-MAP?

Ex

$$f = (\bar{b}+\bar{c})(de+\bar{f})$$
$$= \underbrace{\overline{bc}}_{P} \cdot \underbrace{(de+\bar{f})}_{Q}$$



5 NAND



PAGE NO. :
DATE : / /

7

IMP

Ex If $A = 0$ in the logic expression Given, and expression is

$$Z = [A + EF + \bar{B}C + D].[A + D\bar{E} + \bar{B}.C + \bar{D}\bar{F}]$$

then,

(a) $Z = 0$

(b) $Z = 1$

(c) $Z = \bar{B}C$

(d) $Z = B\bar{C}$

$$\cancel{Z = [\bar{A}.(\bar{E}+\bar{F}).(\bar{B}+\bar{C}).\bar{D}]\bar{A}+D}$$

$$Z = (EF + (\bar{B}C) + D)(D\bar{E} + (\bar{B}C) + \bar{D}F)$$

$$Z = EF.\bar{B}C + (\bar{B}C).D\bar{E} + (\bar{B}C)\bar{D}F + D\bar{E}$$

$$Z = EF.\bar{B}C + D\bar{E} + \bar{B}C\,\bar{D}F$$

$$Z = \bar{B}C\,(EF + \bar{D}\bar{E}) + D\bar{E}$$

$$Z = \bar{B}C$$

Ex $f = \bar{a} + b\bar{c} + c\bar{d}$

$b\bar{c}$: XIOX, $c\bar{d}$: XXIO1 mandatory

ab \ cd	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1		1
10				1

PAGE NO. :
DATE : / /

Ex Implementation using NOR :

① $f = a + bc$

② $f = a + b$

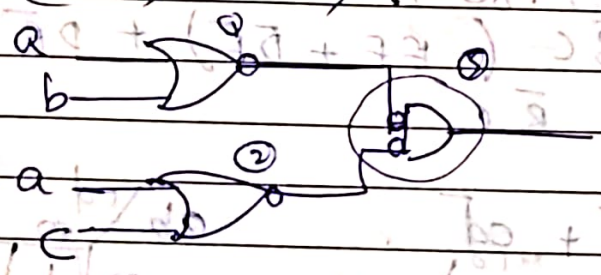
③ $f = \bar{a} b$

④ $f = a \bar{b} c$

⑤ $f = (a+b)(c+d)$

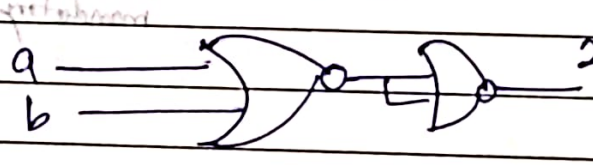
For NOR implementation, function must be expressed in POS form.

① $f = (a+b).(a+c)$



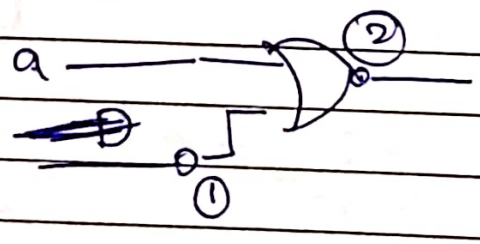
3 NOR

② $f = a + b$



2 NOR

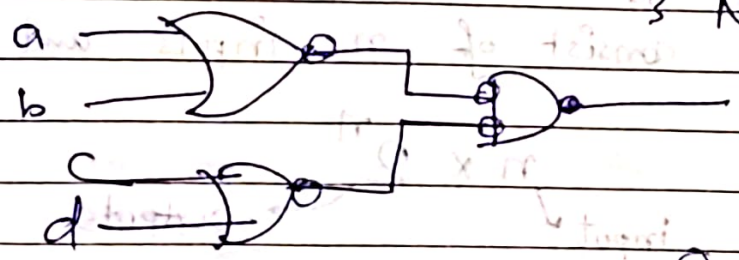
③ $f = \bar{a} b = \overline{a + \bar{b}}$



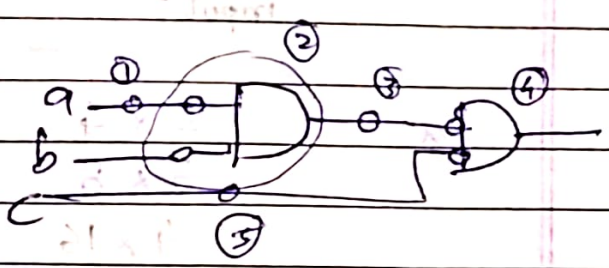
2 NOR

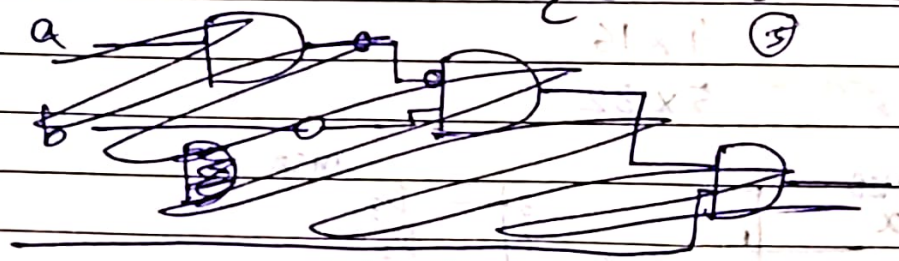
(5) $f = (a+b)(c+d)$.

3 NOR



(4) $f = a \cdot \bar{b} \cdot c$





2017 EX

Consider the K-MAP given below:
Assume all input (a, b, c, d) and there respective compliment are also available. Above logic is implemented using 2 input NOR Gate only.

dc \ ab	00	01	11	10
00	0	X	X	0
01		0	0	X
11		0	0	
10	0	X	X	0

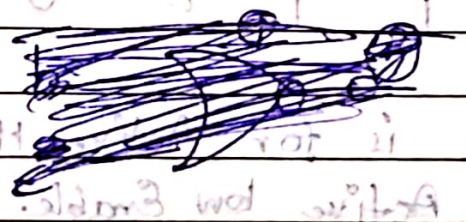
$\rightarrow \bar{c}$

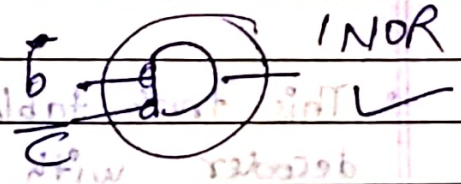
$\rightarrow \bar{b}$

$\bar{b} \cdot c$

POS

Minimum No of gate required is ____ ?





INOR

PAGE NO. :
DATE : / /

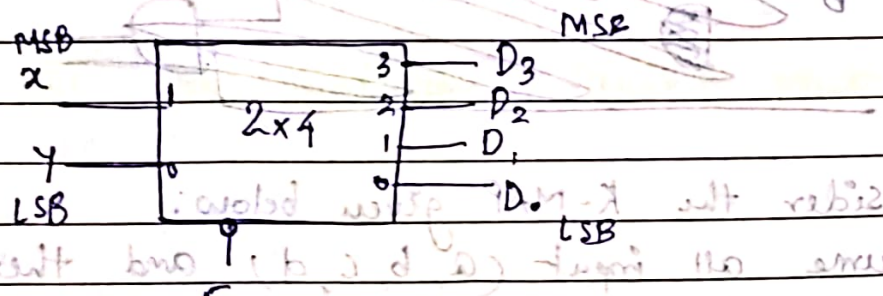
DECODER CIRCUIT

- Decoder is a kind of Combinational circuit which consist of n inputs and 2^n output.

Format : $n \times 2^n$

input → n, outputs → 2^n

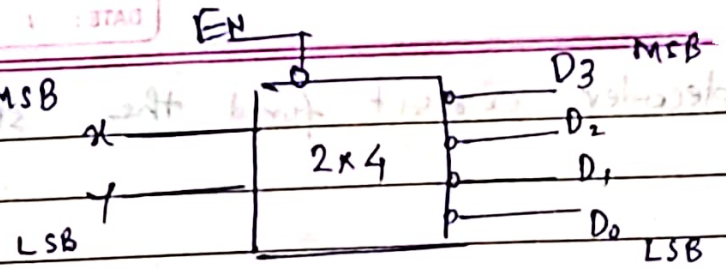
Ex
2×4
3×8
4×16
5×32



Truth Table : (2x4 Decoder with active low E_N)

	E_N	x	y	D_3	D_2	D_1	D_0	SOP
CKT Inactive	L	X	X	X	X	X	X	
CKT Active	0	0	0	0	0	0	1	$\rightarrow \bar{x}\bar{y}\bar{E_N}$
	0	0	1	0	0	1	0	$\rightarrow \bar{x}y\bar{E_N}$
	0	1	0	0	1	0	0	$\rightarrow x\bar{y}\bar{E_N}$
	0	1	1	1	0	0	0	$\rightarrow xy\bar{E_N}$

- This truth table is for Active High 2x4 decoder with Active low Enable.



Active low Decoder with Active low Enable.

Active High Decoder – SOP

Active Low Decoder – POS

* Similarily we can design for Active low decoder with Active high enable.

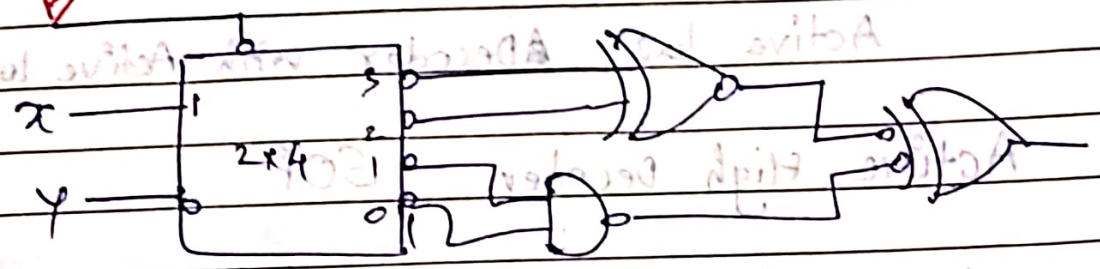
	EN	x	y	D3	D2	D1	D0	
	0	x	x	1	1	1	0	Active low output.
Active High	1	0	0	1	1	0	1	
	1	0	1	1	0	1	1	
	1	1	0	0	1	1	1	
	1	1	1					

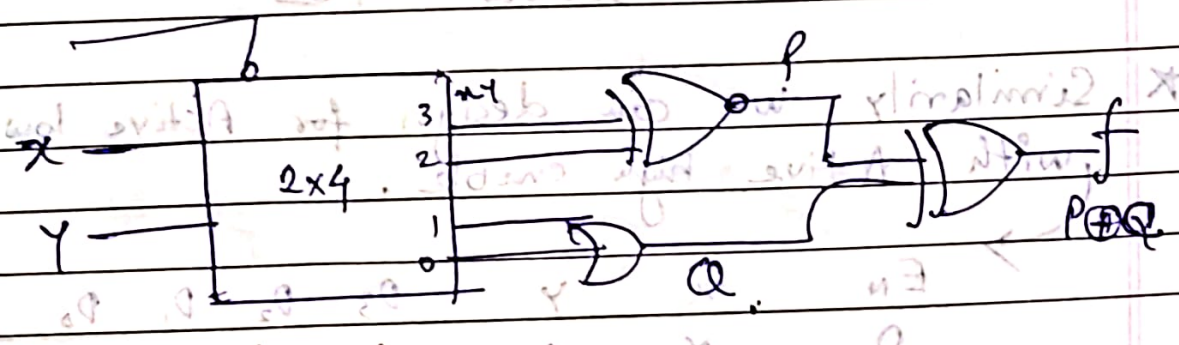
POS

$$D_0 = (\overline{E_N} + x + y)$$
$$D_1 = (\overline{E_N} + x + \overline{y})$$
$$D_2 = (\overline{E_N} + \overline{x} + y)$$
$$D_3 = (\overline{E_N} + \overline{x} + \overline{y})$$

PAGE NO. :
DATE : / /

Q) for the decoder circuit find the simplified output



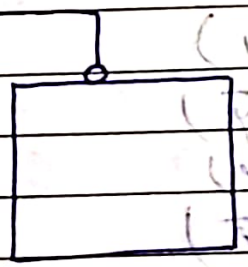


Simplified $P = \overline{x}$

Simplified $Q = \overline{x}$.

$\therefore P \oplus Q = 0$.

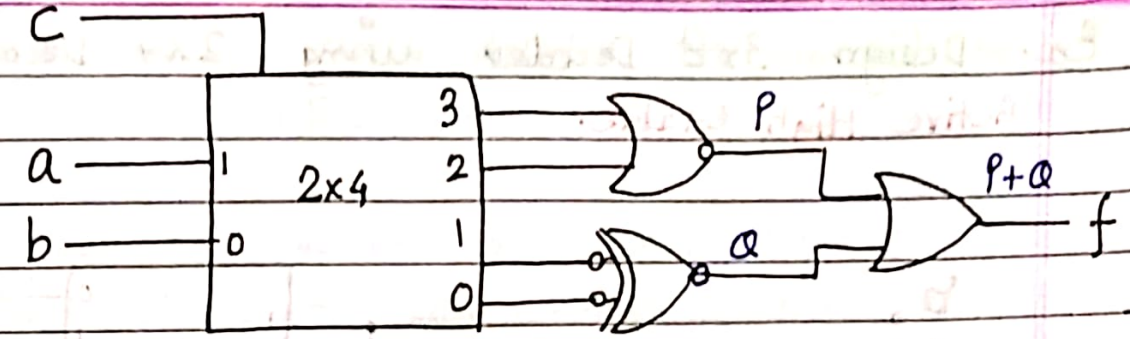
TEN = a = "0" or $\overline{a}$



"Active low" enable

PAGE NO. :
DATE : / /

Ex



Find simplified output.

$$P = \overline{(ab + a\bar{b})} = \overline{a}$$

$$Q = \overline{\bar{a}b \oplus \bar{a}\bar{b}} = \overline{\bar{a}b\,\bar{a}\bar{b} + \bar{a}b\,\overline{\bar{a}\bar{b}}}$$

$$= \overline{(a+\bar{b})(\bar{a}\bar{b})} + \bar{a}b\,(a+b)$$

$$= \bar{a}\bar{b} + \bar{a}b$$

$$= \bar{a}$$

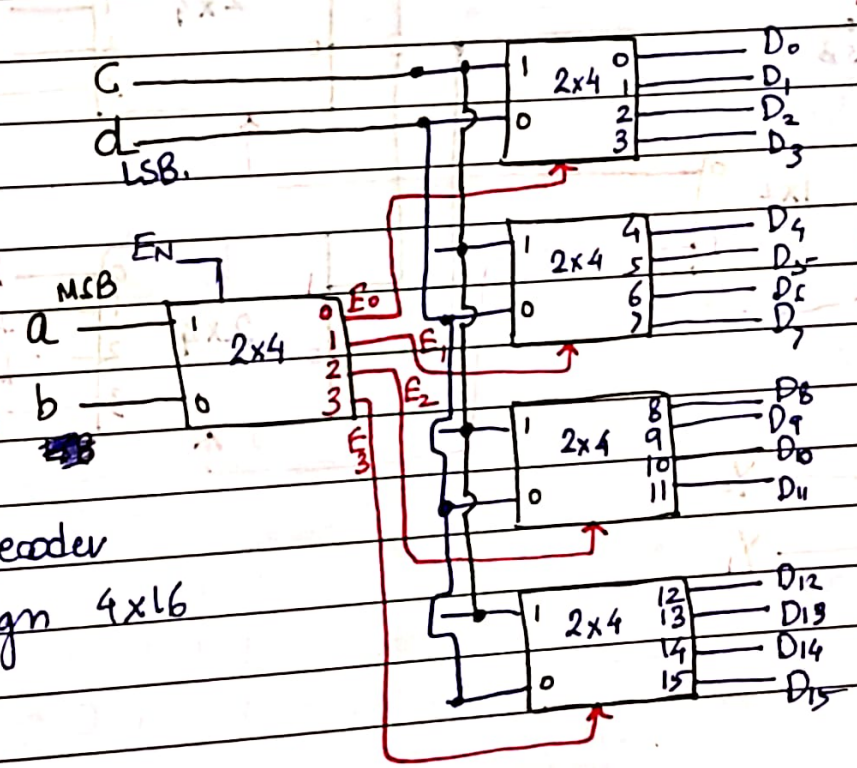
$$P + Q = 1$$

$$f = C \cdot 1$$

$$\boxed{f = C}$$

Ex Implement 4x16 Decoder using 2x4 Decoder.

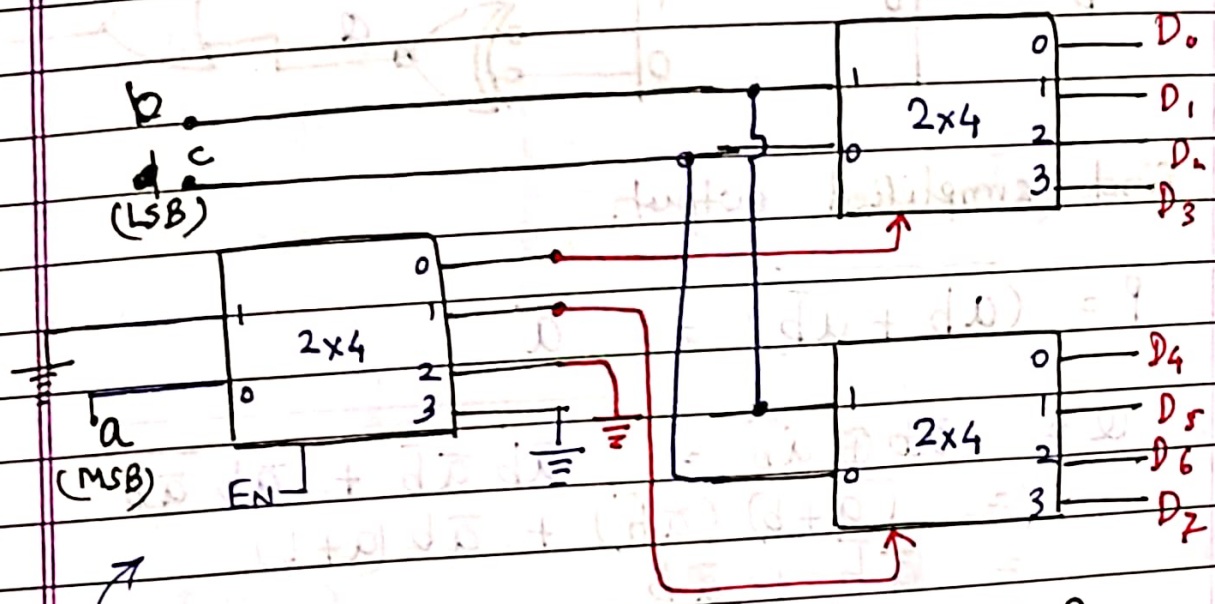
Active High Enable.



We need 5 no of 2x4 Decoder ~~using~~ to design 4x16 Decoder

PAGE NO. :
DATE : / /

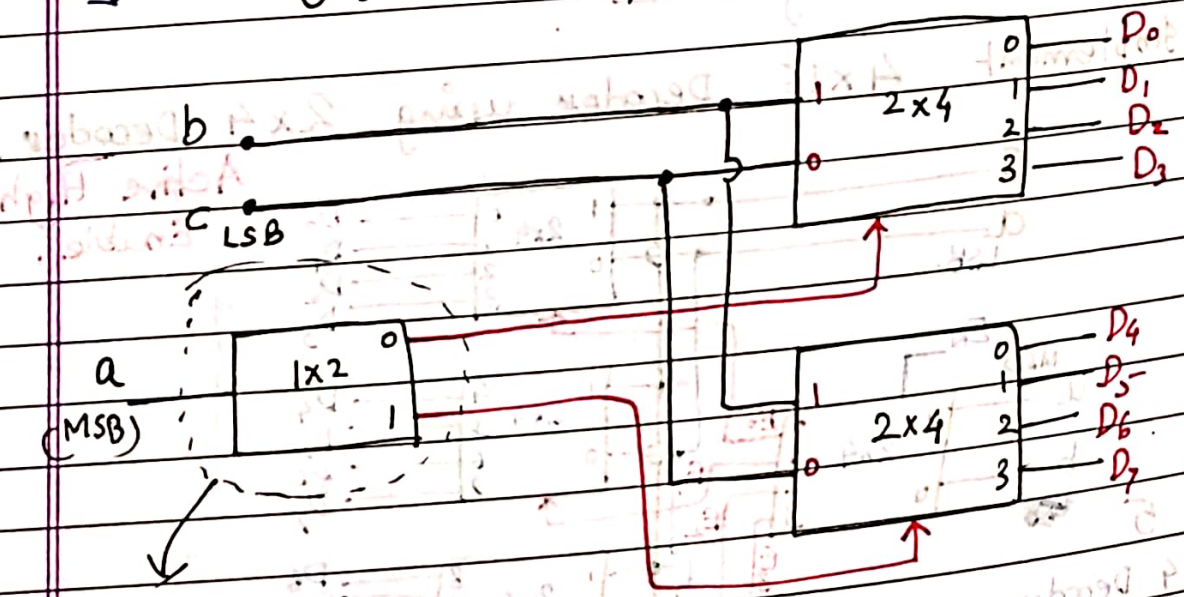
Ex Design 3x8 Decoder using 2x4 Decoder.
Active High enable.

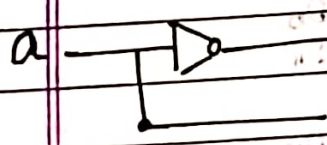


3x8 DECODER

Both are Equivalent

0abc	
0101	$- D_5$
0011	$- D_3$
0111	$- D_7$



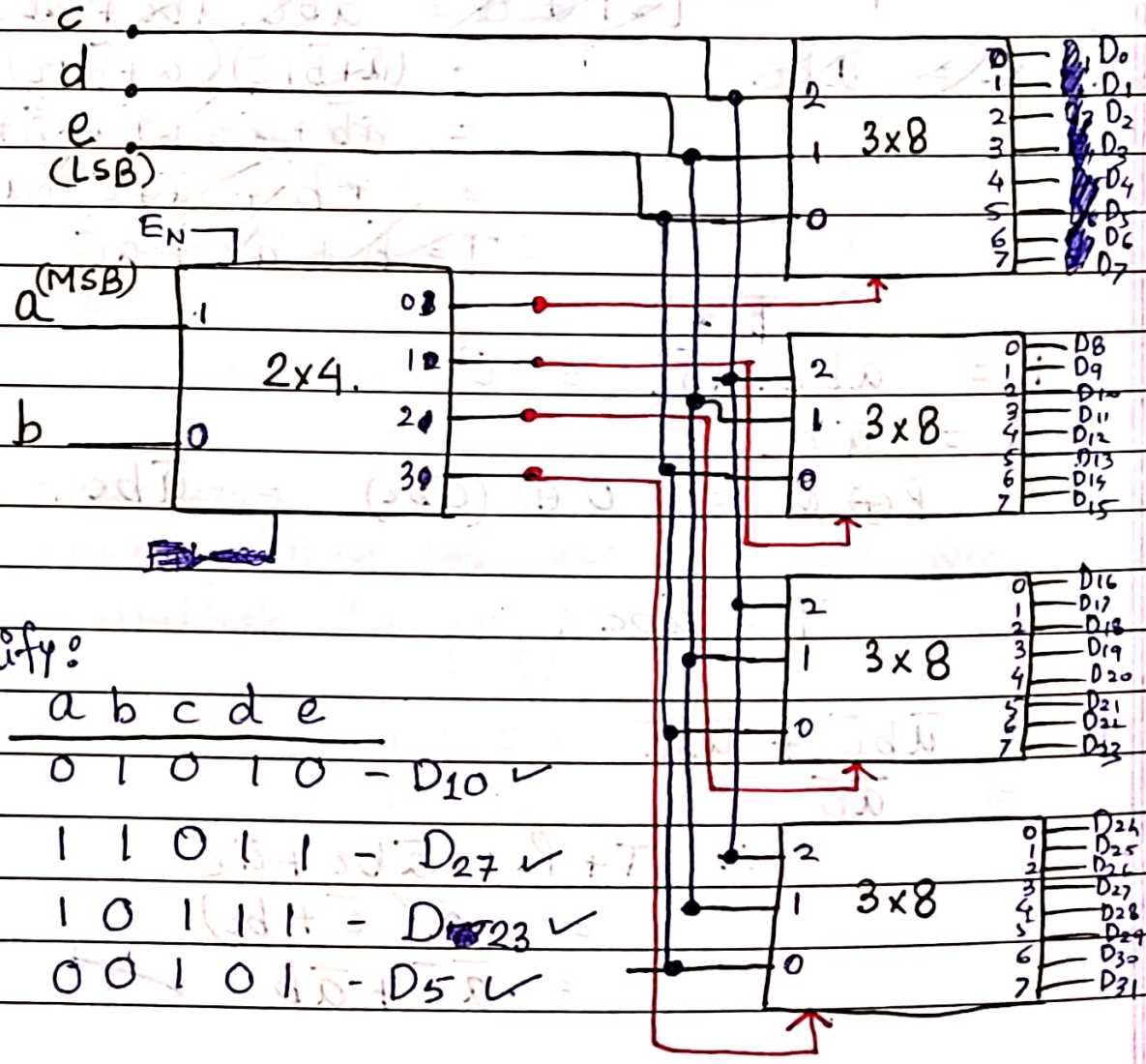


PAGE NO. :
DATE : / /

Ex How many 4x16 decoder are needed to design 8x 256 Decoder? 17

- We need 16 number of 4x16 decoder at the output stage to make overall output pin = 256.
- Combine all the respective MSB and LSB pins of 4x16 decoder. Now consider one 4x16 Decoder at the input stage, to make all output decoder as enable. Hence Ans is 16+1 = 17 ✓

Ex Implement 5x32 Decoder using minimum no of 2x4 and 3x8 decoder. Find the number of IC.
Active High Enable, Active High Decoders (5 ICs)

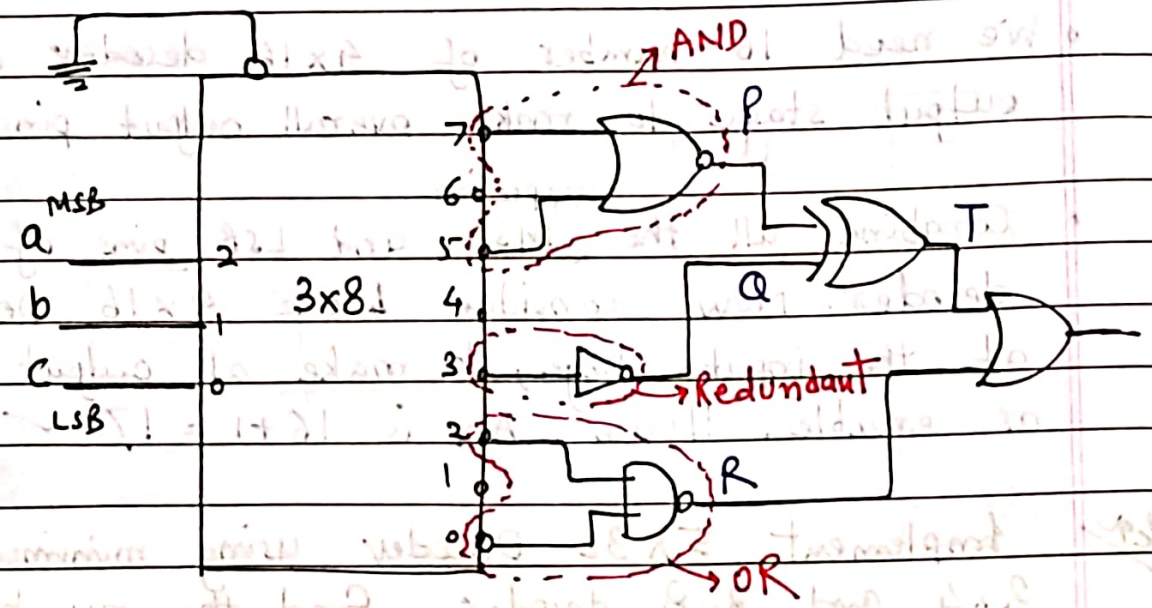


verify:

a	b	c	d	e	
0	1	0	1	0	- D_{10} ✓
1	1	0	1	1	- D_{27} ✓
1	0	1	1	1	- D_{23} ✓
0	0	1	0	1	- D_5 ✓

PAGE NO. :
DATE : / /

Ex. Simplify the boolean function present at the output of 3x8 Decoder. [Active Low Decoder]



$\cancel{R = \overline{abc}}$

Silly Mistake

$\cancel{Q = \overline{abc}}$

$\cancel{T = P \oplus Q = abc.\overline{a}bc + \overline{abc}.\overline{abc}}$

$\cancel{= (\overline{a}+\overline{b}+\overline{c})(a+b+c)}$

$\cancel{= \overline{a}\overline{b} + \overline{a}\overline{c} + \overline{b}a + \overline{b} + \overline{b}c}$

$\cancel{= \overline{b} + (\overline{a}+\overline{c})(a+c)}$

$\cancel{T = \overline{b} + \overline{a}c + a\overline{c}}$

$P = abc.\overline{a}bc = 0$

$Q = \overline{a}bc$

$P \oplus Q = 0 \oplus (\overline{a}bc) = \overline{a}bc.$

$T = \overline{a}bc.$

$R = \overline{a}b\overline{c} + \overline{a}\overline{b}\overline{c}$

$= \overline{a}\overline{c}$

$\therefore T + R = \overline{a}bc + \overline{a}\overline{c}$

$= \overline{a}(\overline{c} + bc)$

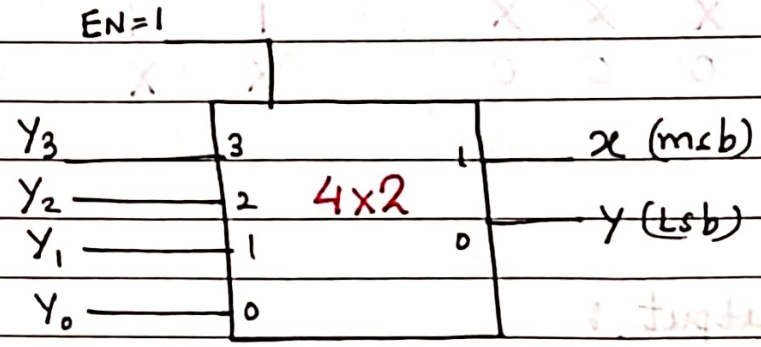
$= \overline{a}\overline{c} + \overline{a}b$ ✓

ENCODER CIRCUIT

Format : $\underbrace{2^n}_{\text{Input}} \times \underbrace{n}_{\text{Output}}$.

- Kind of combinational circuit which perform encoding.

Truth table for 4x2 encoder circuit.



MSB Y_3	Y_2	Y_1	LSB Y_0	x	y
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

Disadvantage :

- unknown output for below inputs when there are multiple 1's or all zeros.

0 0 0 0
0 0 1 1
1 1 0 0
1 0 1 0
1 1 1 1
1 0 1 1

Gives unknown output.

etc

PAGE NO. :
DATE : / /

Disadvantage is removed in priority ~~Enc~~ Encoder circuit.

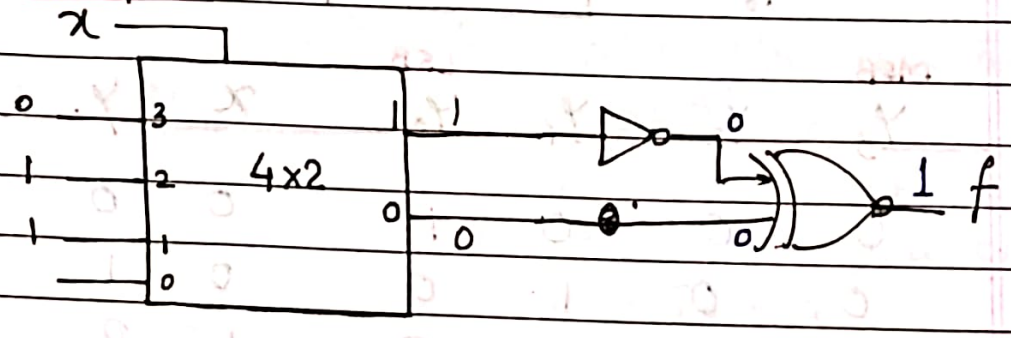
MSB Y_3	Y_2	Y_1	LSB Y_0	MSB x	LSB y
0	0	0	1	0	0
0	0	1	X	0	1
0	1	X	X	1	0
1	X	X	X	1	1
0	0	0	0	X	X

{0010, 0011}

{0100, 0101, 0110, 0111}

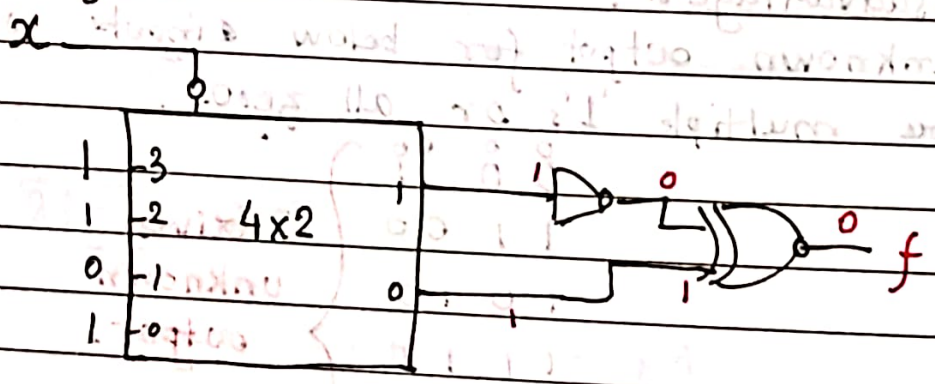
1000, 1001, ⋮, 1111

Ques Find output :



$$\boxed{f = x}$$

Ques Find output :



$$f = 0.\bar{x} = 0$$

PAGE NO.: _____
DATE: / /

01

$Y_3Y_2 \backslash Y_1Y_0$	00	01	11	10
00	X	0	0	0
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$\rightarrow Y_2$

$\rightarrow Y_3$

$$X = Y_2 + Y_3$$

$Y_3Y_2 \backslash Y_1Y_0$	00	01	11	10
00	X	0	1	1
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

$\rightarrow Y_1\bar{Y}_2$

$\rightarrow Y_3$

$$Y = Y_1\bar{Y}_2 + Y_3$$

Test 1 Ques 17 Ex

$WX \backslash YZ$	00	01	11	10
00				
01		1	1	
10	1	1	1	
11			1	

WXY' WYZ

Mandatory terms.

PAGE NO. :
DATE : / /

IMP

RIPPLE CARRY ADDER
(Binary Parrallel Adder)

- Consider 4 bit Binary parallel Addition.

```
  1   1 1 1
      1 1 0 1
    + 1 0 1 1
  ---------------
Carry 1 0 0 0
```

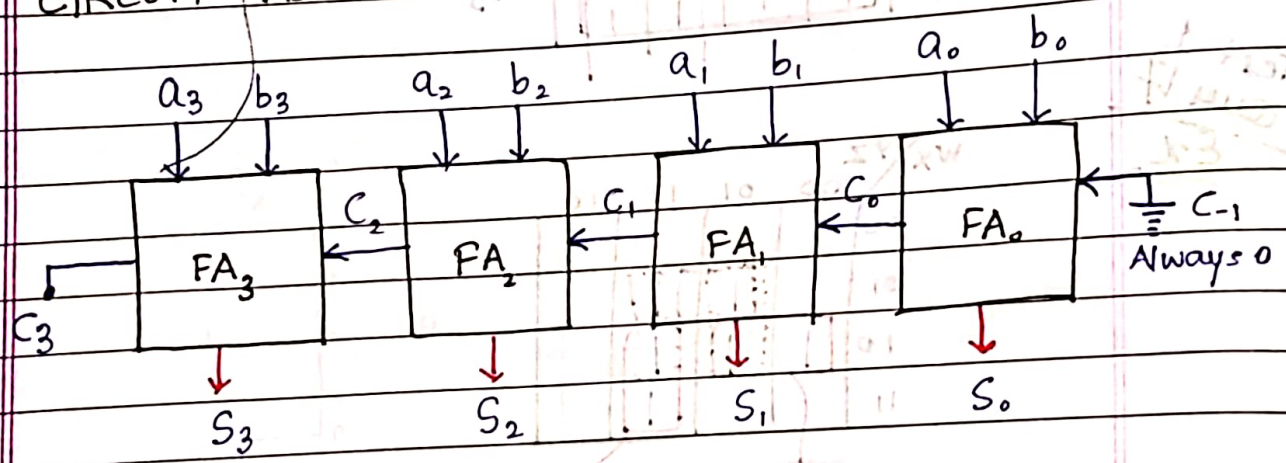
4 bit sum

C_3 → final carry.

$C_2 \; C_1 \; C_0$
$a_3 \; a_2 \; a_1 \; a_0$
$b_3 \; b_2 \; b_1 \; b_0$
$S_3 \; S_2 \; S_1 \; S_0$ — sum

$C_{-1} = 0$ → Initial carry.

CIRCUIT DESIGN



- Above ckt has longest carry propogation. (longest latency.
- n-bit binary parrallel adder requires "n" Full Adders.

IMP

OR (n-1) FA + 1 Half Adder
OR (2n-1) HA + (n-1) or Gate.

E.g. for 4-bits,
4 Full Adders
OR 3 FA + 1 HA
OR (2×4)-1 HA + (4-1) OR
7 HA + 3 OR Gate.

PAGE NO. :
DATE : / /

Q2

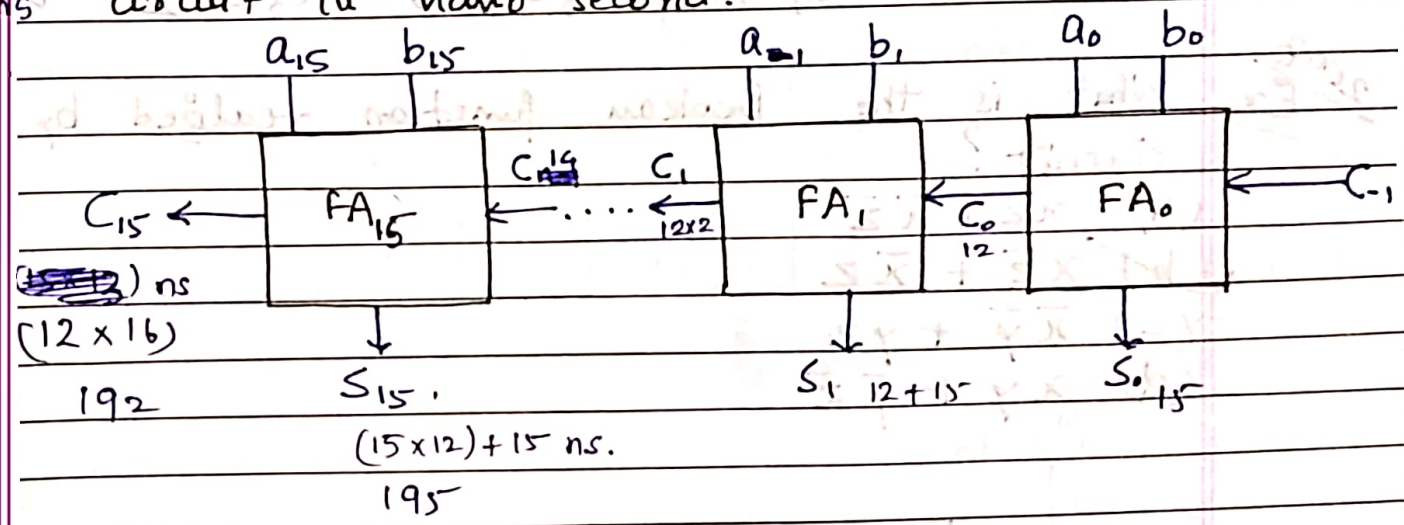
For a 16 bit Binary Parallel Adder circuit constructed using identical FA, The full adder generates carry after 12 ns and sum after 15 ns.

195 ns ← (i) What is the total delay in the generation of final sum?

maximum delay in ckt

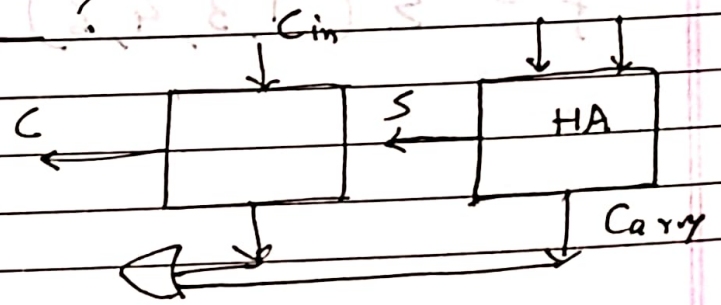
195 ns ← (ii) What is the worst case delay in the circuit?

192 ns ← (iii) What is the longest latency for the given circuit in nano second.

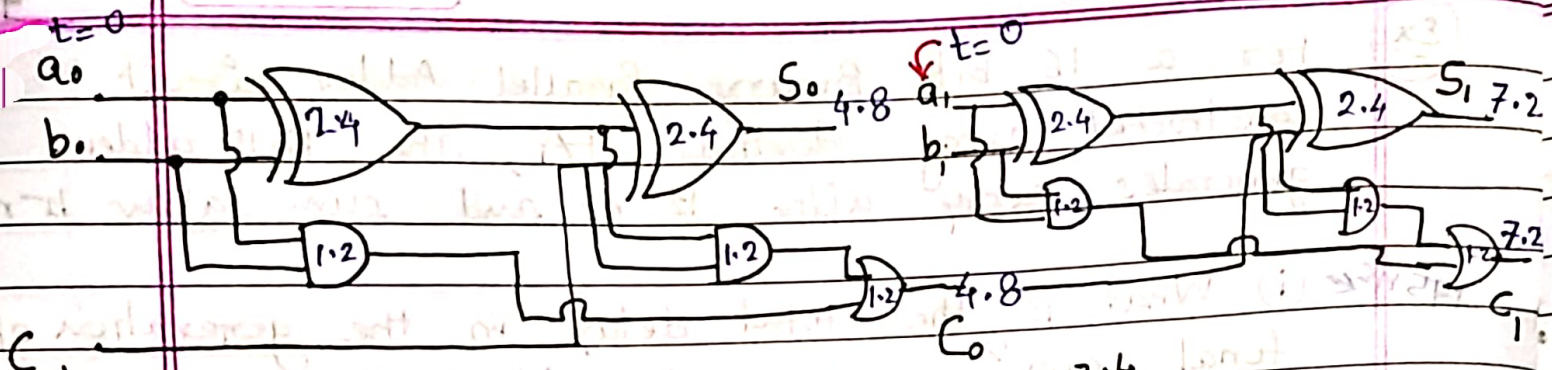


V.V.I

Half Adder is implemented with XOR and AND gate. A FA is implemented with 2 HA and 1 OR gate. The propogation delay of XOR-gate is twice that of AND / OR gate. Propogation delay of AND/OR is 1.2 ms. A 4 bit ripple carry binary adder is implemented using 4 full Adder. The total propogation time of this 4 bit binary adder in microsecond. is ____ ?



PAGE NO. :
DATE : / /



$S_0 = 4.8$ $\xrightarrow{+2.4}$ $S_1 = 7.2$ $\xrightarrow{+2.4}$ $S_2 = 9.6$ $\xrightarrow{+2.4}$ $S_3 = 12$ ✓

$C_0 = 4.8$ $\quad C_1 = 7.2$ $\quad C_2 = 9.6$ $\quad C_3 = 12$ ✓

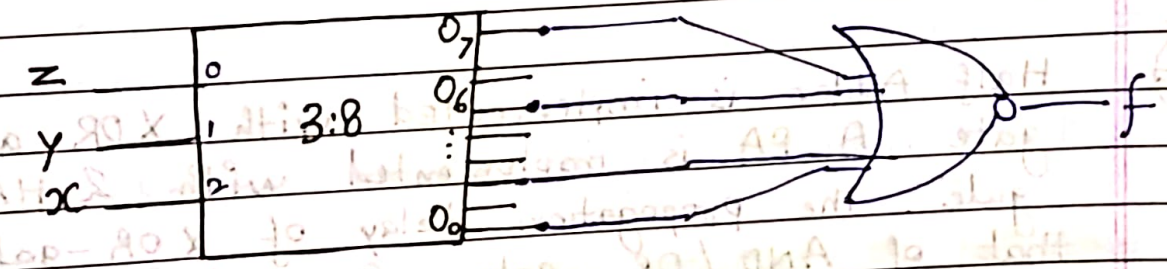
2008 Ex What is the Boolean function realized by the circuit?

(a) $xz + \bar{x}\bar{z}$

(b) $x\bar{z} + \bar{x}z$ ✓

(c) $\bar{x}\bar{y} + yz$

(d) $xy + \bar{y}\bar{z}$



$f = \sum(0, 2, 5, 7)$

$f = \sum(1, 3, 4, 6)$.

A \ BC	00	01	11	10
0		1	1	
1	1			1

$\bar{A}C + A\bar{C}$ ✓

PAGE NO. :
DATE : / /

95

12.

$f = \Sigma(5, 6, 13)$

$f_1 = \Sigma(0, 1, 2, 3, 5, 6, 8, 9, 10, 11, 13)$.

$f = f_1 \cdot \overline{f_2}$

(11) Total possible functions of f_2 is ?

(12) Minimal value of f_2 is ?

AB \ CD				
		1		1
		1		

f

AB \ CD				
	1	1	1	1
		1		1
		1		
	1	1	1	1

f_1

AB \ CD				
	X	1	X	1
	X	1	X	X

$\overline{f_2}$

AB \ CD				
	1	1	1	1
	X		X	
	X		X	X
	1	1	1	1

f_2.

2^5 different function

$\overline{B}$ minimized.

PAGE NO. :
DATE : / /

MULTIPLEXER

- It is a multiplexer is a combinational circuit that performs multiplexing of input signal, and with combination of select line, it generates single output.

- using multiplexer, we can design any boolean function / any logic gate. Hence MUX is reffered as universal Logic Gate. (Functionally complete set).

- MUX is also reffered as data Selector.

- Based on select line, it select one input at a time.

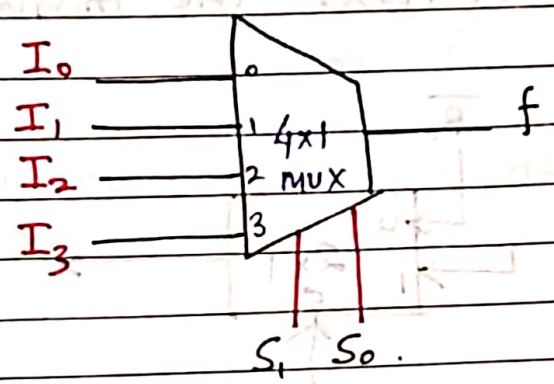
- Multiplexer is also reffered as parallel to ~~series~~ serial converter.

Format : $\boxed{2^n \times 1}$ n : no of select lines

No of select lines	order of MUX
1	2×1
2	4×1
3	8×1
4	16×1
5	32×1

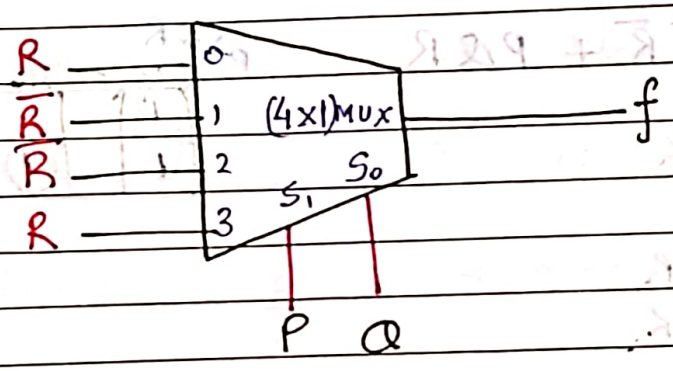
PAGE NO. :
DATE : / /

97



$$f = \bar{S}_1\bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1\bar{S}_0 I_2 + S_1 S_0 I_3$$

2010 Ex



(a) $\overline{P \oplus Q \oplus R}$

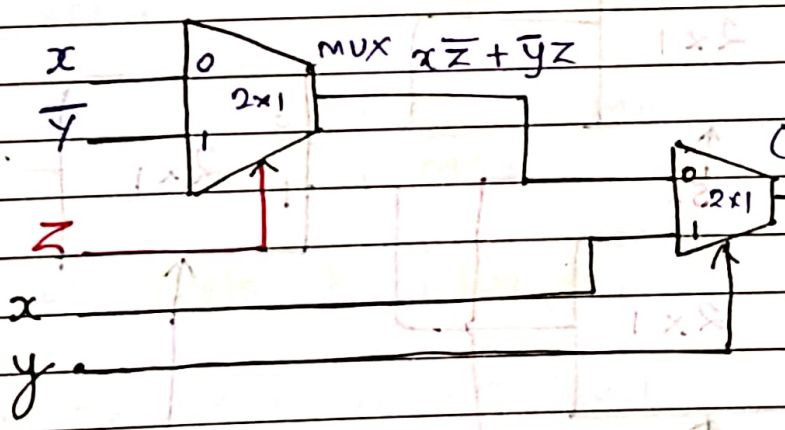
✓(b) $P \oplus Q \oplus R$

(c) $P + Q + R$

(d) $\overline{P + Q + R}$

$$f = \bar{P}\bar{Q}R + \bar{P}Q\bar{R} + P\bar{Q}\bar{R} + PQR$$
$$= \Sigma(1, 2, 4, 7).$$
$$f = P \oplus Q \oplus R$$

2006 Ex Find output $f(x, y, z)$

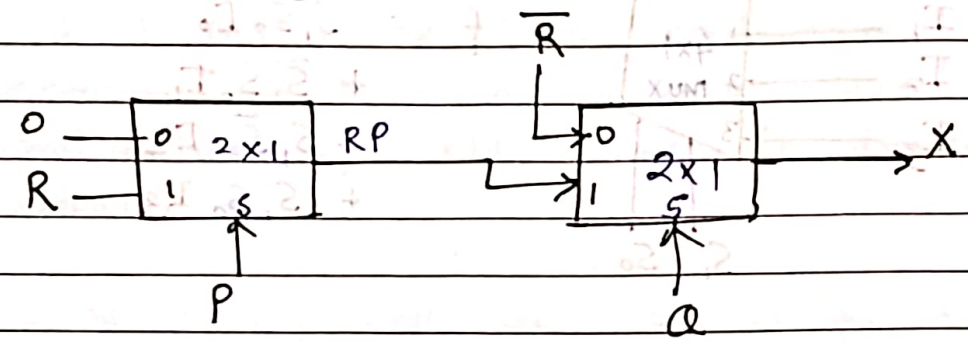


$(x\bar{z} + \bar{y}z)\bar{y} + x \cdot y$

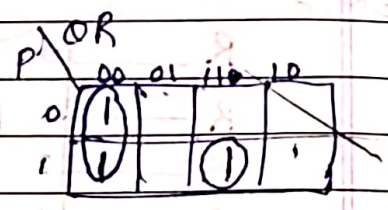
$= x\bar{z} + xy + \bar{y}z$

PAGE NO. :
DATE : / /

Ex Consider cascaded 2x1 MUX. The minimal SOP at the output



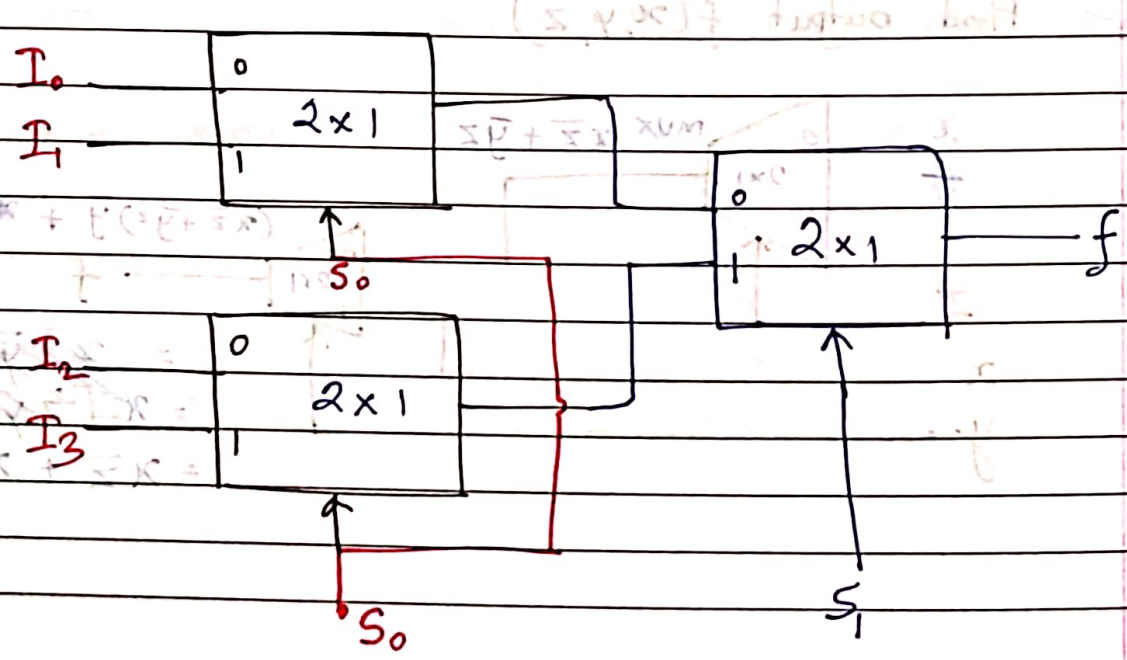
$$X = \overline{Q}\,\overline{R} + PQR$$



(a) $\overline{P}\,\overline{Q} + PQR$
(b) $\overline{P}Q + QR$
(c) $PQ + \overline{P}\,\overline{Q}R$
(d) $\overline{Q}\,\overline{R} + PQR$

Ex Implement 4x1 mux using 2x1 Mux.

Ex. Find number of 2x1 mux to design 32x1 mux.



PAGE NO. :
DATE : / /

aa

No of stages = 2

No of MUX => 2+1 = 3.

Ex No of MUX (4x1) needed to design 64x1 MUX

16 + 4 + 1 = 21 ✓

⇒ No of mux (2x1) needed to design 32x1 MUX.

Level 1 $\frac{32}{2}$ = 16 MUX.

Level 2 $\frac{16}{2}$ = 8 MUX

level 3 $\frac{8}{2}$ = 4 MUX

Level 4 $\frac{4}{2}$ = 2 MUX.

level 5 $\frac{2}{2}$ = 1 MUX.

∴ 16 + 8 + 4 + 2 + 1 = 31 MUX.

In General, N x 1 MUX using M x 1 MUX requires,

$$\sum_{i=1}^{k} \left\lceil \frac{N}{M^i} \right\rceil \text{ MUX.}$$

No of levels $k = \lceil \log_M N \rceil$

No of MUX in k^{th} level $= \left\lceil \frac{N}{M^k} \right\rceil$

PAGE NO. :
DATE : / /

How many 4x1 MUX needed to design 128x1 Multiplexer?

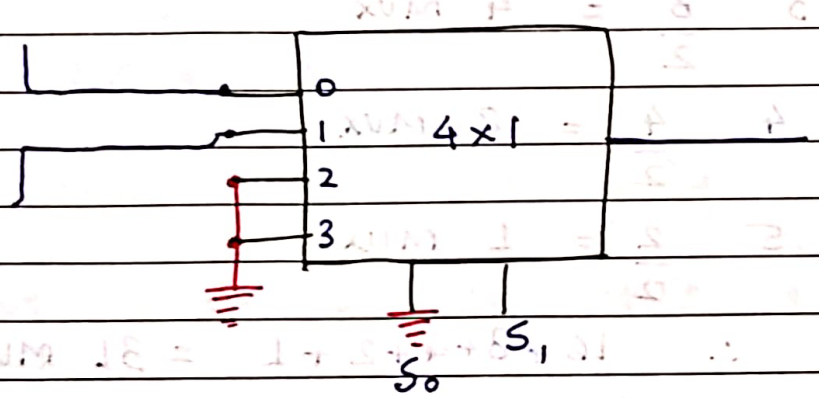
$\frac{128}{4} = 32$ mux — Level 1

$\frac{32}{4} = 8$ mux — level 2

$\frac{8}{4} = 2$ mux Level 3

∴ "42" 4x1 MUX + "1" 2x1 MUX needed.

If only 4x1 MUX to be used then 2x1 can be converted as 4x1 MUX as below.



Ex Find No of 8x1 MUX needed to design, 256x1.

$\left\lceil \frac{256}{8} \right\rceil = 32$ Level

$\left\lceil \frac{32}{8} \right\rceil = 4$ level 2.

$\left\lceil \frac{4}{8} \right\rceil = 1$ Level 1

37 Ans ✓

PAGE NO. :
DATE : / /

101

A 2 bit binary multiplier circuit can be implemented using.

(a) 2 input AND Gate only.

✓(b) Six 2 input AND Gate & 2 XOR Gate

(c) 2 input NOR Gate and 1 XNOR Gate.

(d) XOR Gate and shift register.

a_1	a_0	b_1	b_0	f_4	f_3	f_2	f_1	
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	0	2
0	0	1	1	0	0	0	0	3
0	1	0	0	0	0	0	0	4
0	1	0	1	0	0	0	1	5
0	1	1	0	0	0	1	0	6
0	1	1	1	0	0	1	1	7
1	0	0	0	0	0	0	0	8
1	0	0	1	0	0	1	0	9
1	0	1	0	0	1	0	0	10
1	0	1	1	0	1	1	0	11
1	1	0	0	0	0	0	0	12
1	1	0	1	0	0	1	1	13
1	1	1	0	0	1	1	0	14
1	1	1	1	1	0	0	1	15

1 ~~AND~~

Short cut:-

$a_1 \; a_0$

$b_1 \; b_0$

$a_1.b_0 \quad a_0.b_0$

$a_1b_1 \quad a_0b_1 \quad \times$

$S_1 \quad S_0 \quad a_0.b_0$

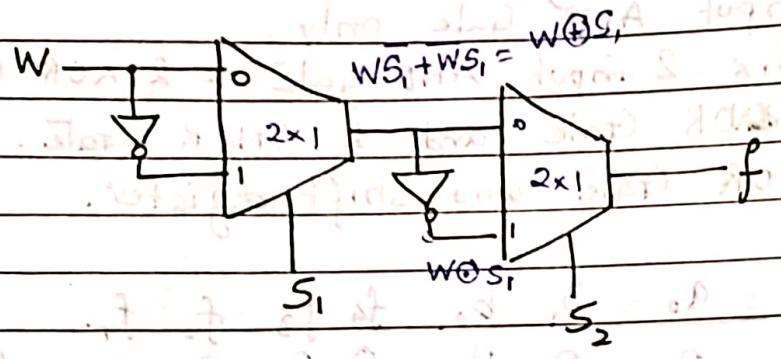
$S_1 \rightarrow$ HA, $S_0 \rightarrow$ HA

∴ 4 AND + 2(1 XOR, 1 AND)

= 6 AND, 2 XOR.

PAGE NO. :
DATE : / /

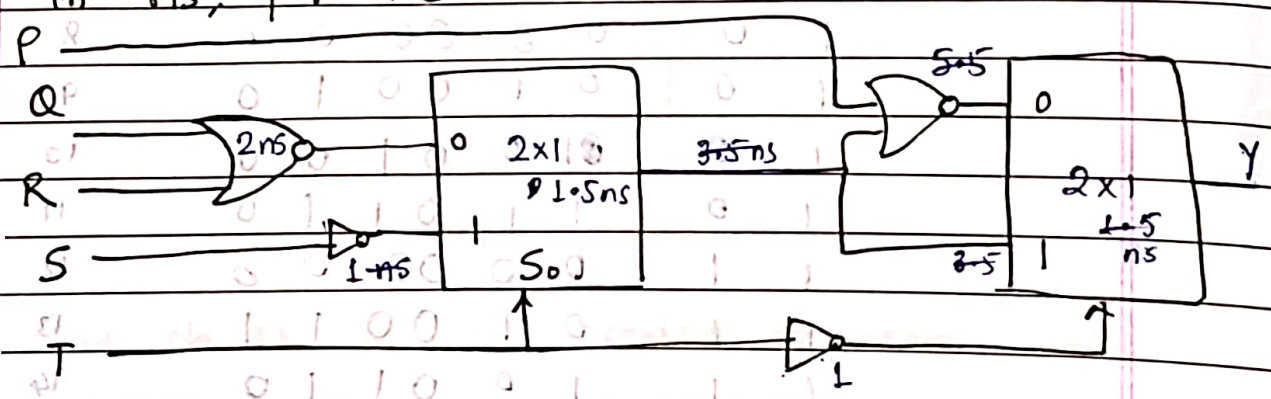
Ex Find output :



$f = W \oplus S_1 \oplus S_2$

V. imp

Ex For the circuit shown, delay of NOR gates, MUX and inverters are 2ns, 1.5ns and 1ns respectively. If all input P,Q,R,S,T are applied at same time instant, the max propagation delay in ns, for the circuit is ?

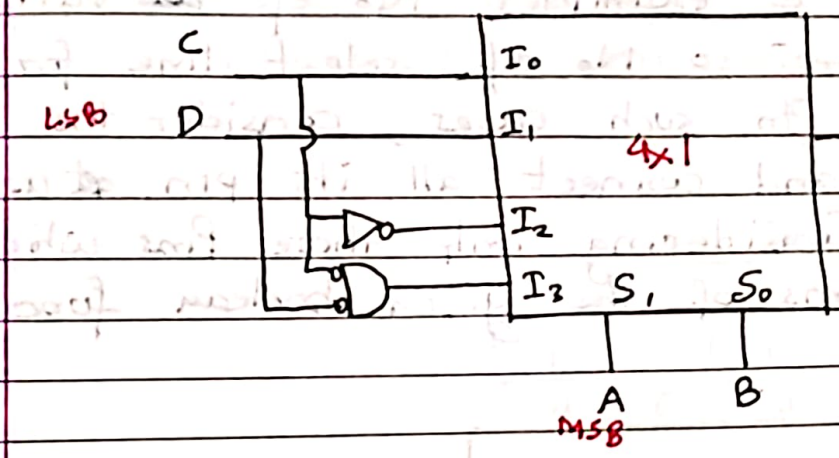


Sol

In case T = 0, Y = 5 ns
T = 1 Y = 6 ns.

PAGE NO. :
DATE : / /

2010 Ex



$$f = \bar{A}\bar{B}C + \bar{A}BD + A\bar{B}\bar{C} + AB(\overline{C+D})$$

$$AB\bar{C}\bar{D}.$$

CD ~~AB~~ as ~~input~~ select lines

AB ~~CD~~ as ~~inp~~ select lines.

AB \ CD	00	01	11	10
00			1	1
01		1	1	
11	1			
10	1	1		

CD \ AB	00	01	11	10
00			1	1
01		1		1
11	1	1		
10	1			
	I_0	I_1	I_3	I_2

$$f = \Sigma(2, 3, 5, 7, 8, 9, 12).$$

Ex (i) Design the given function using 8x1 MUX.

$$f = \Sigma_m(1, 2, 4, 7)$$

(ii) Design using 4x1 MUX

$$f = \Sigma_m(0, 1, 3)$$

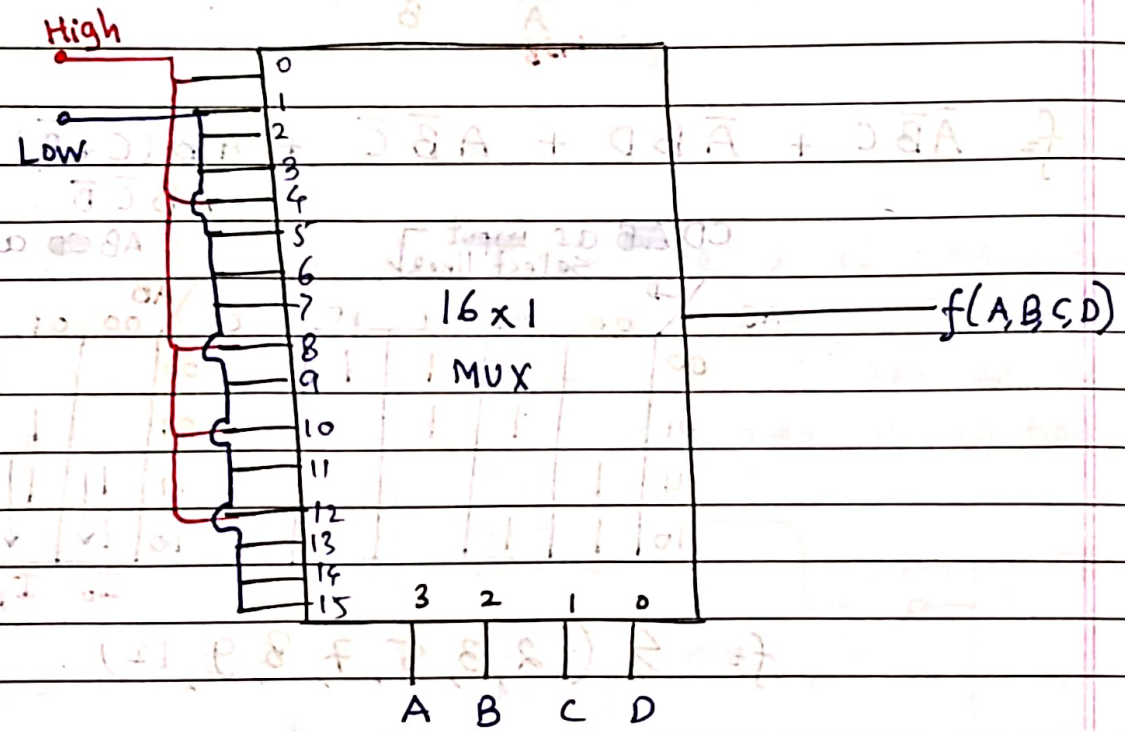
(iii) Design using 16x1 MUX.

$$f = \Sigma_m(0, 1, 4, 8, 10, 12)$$

PAGE NO. :
DATE : / /

For all cases & examples, No of ~~bo~~ variable in boolean func^n = No of select line for given MUX. In such cases, consider the MUX given and connect all its pin ~~at~~ as high logic. Considering only those pins which are min terms of the given boolean function

(iii)



Ex Design following function :

No of var = 3 $2^{3-1} \times 1$ MUX.

(i) $f = \Sigma_m (1, 2, 4, 7)$ using 4x1 MUX.

(ii) $f = \Sigma_m (0, 1, 3)$ using 2x1 MUX

(iii) $f = \Sigma_m (0, 1, 4, 8, 10, 12)$ using 8x1 MUX.

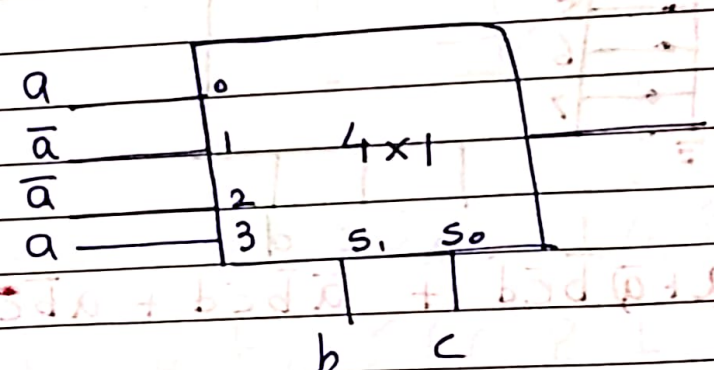
(No of variable − 1) = No of select lines.

PAGE NO. :
DATE : / /

(i) $f = \Sigma m(1, 2, 4, 7)$ using 4x1.

$f(a,b,c) \rightarrow$ considering bc as select lines
a as input.

a \ bc	I_0	I_1	I_2	I_3
0		1		1
1	1		1	
	a	$\bar{a}$	a	$\bar{a}$

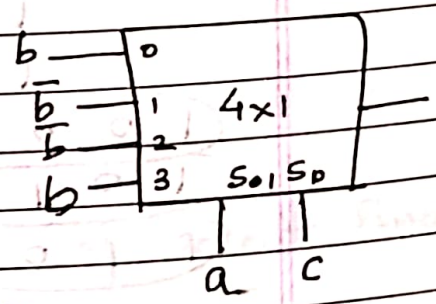


verify : $a\bar{b}\bar{c} + \bar{a}\bar{b}c + \bar{a}b\bar{c} + abc$

$f(a,b,c) \rightarrow$ considering b as input and ac as select lines.

b	a	c		a	b	c	
0	0	0		0	0	0	
0	0	1	✓	0	0	1	✓
1	0	0	✓	0	1	0	✓
1	0	1		0	1	1	
0	1	0	✓	1	0	0	✓
0	1	1		1	0	1	
1	1	0		1	1	0	
1	1	1	✓	1	1	1	✓

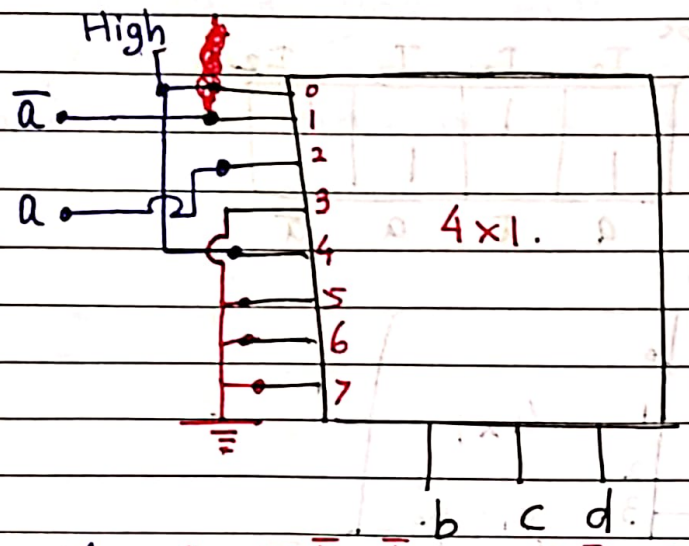
b \ ac	I_0	I_1	I_3	I_2
0		1		1
1	1		1	



No change in min terms.
as its $a \oplus b \oplus c$.

PAGE NO. :
DATE : / /

a \ bcd	I_0	I_1	I_3	I_2	I_6	I_7	I_5	I_4
0	1	1						1
1	1			1				1



verify: $(a+\bar{a})\bar{b}\bar{c}\bar{d} + \bar{a}\bar{b}\bar{c}d + a\bar{b}\bar{c}\bar{d} + (a+\bar{a})b\bar{c}\bar{d}$

(ii) using c as input and a b d as selecting.

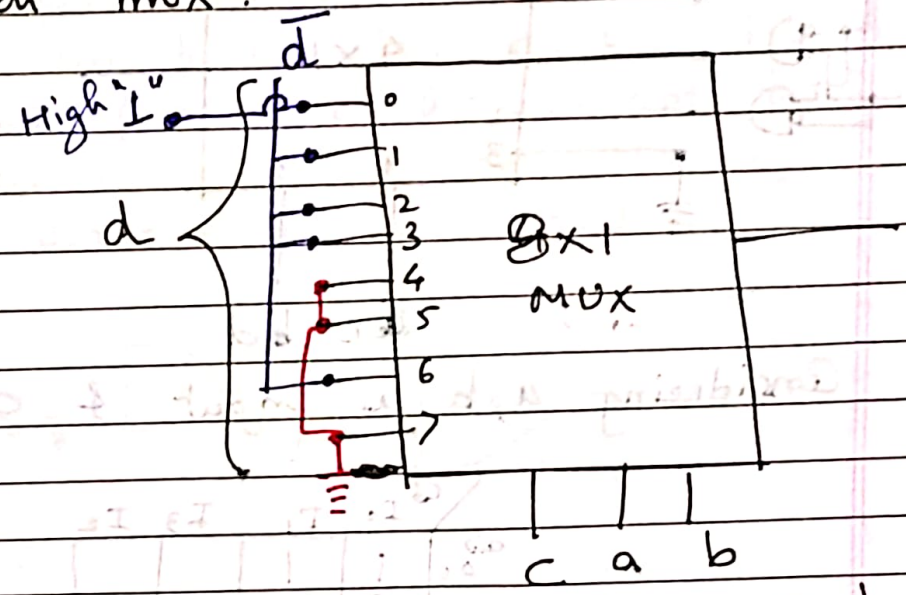
a b c d	c a b d
0 0 0 0	0 0 0 0
0 0 0 1	0 0 0 1
0 0 1 0	
0 0 1 1	
0 1 0 0	0 0 1 0
0 1 0 1	
0 1 1 0	
0 1 1 1	
1 0 0 0	0 1 0 0
1 0 1 0	1 1 0 0
1 1 0 0	0 1 1 0

$f(c,a,b,d)$
$\Sigma_m(0,1,2,4,6,12)$

c \ abd								
0	1	1		1	1			1
1								1

PAGE NO. :
DATE : / /

→ Find the connecting pin from I_0 to I_7 for given mux.



$f(a, b, c, d) = \Sigma_m(0, 1, 4, 8, 10, 12)$.

$f(d, c, a, b) = \Sigma_m(0, 8, 1, 2, 6, 3)$.

d \ cab	I_0	I_1	I_3	I_2	I_6	I_7	I_5	I_4
0	1	1	1	1	1			
1	1							
	1	$\bar{d}$	$\bar{d}$	$\bar{d}$	$\bar{d}$	⏚	⏚	⏚

$2^{n-1} \times 1$ may or may not need an inverter

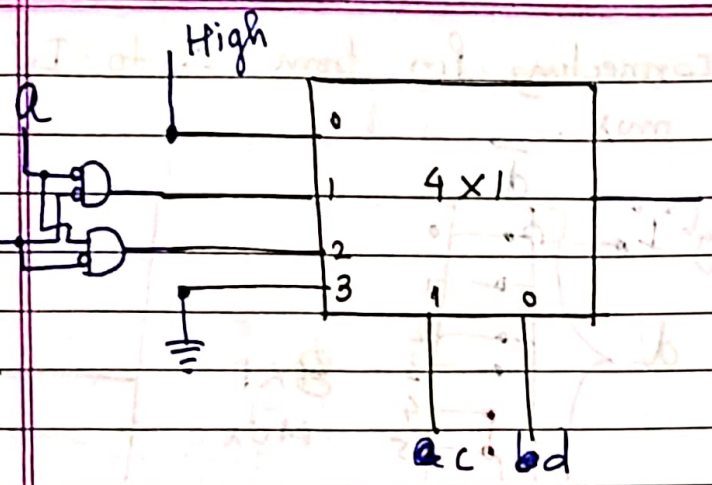
→ $f = \Sigma_m(0, 1, 4, 8, 10, 12)$.

use $2^{n-2} \times 1$ mux

4 variable − 2 = No of select lines.

PAGE NO. :
DATE : / /

Ex



Considering a, b as input & c, d as select line

ab \ cd	I_0	I_1	I_3	I_2
00	1	1		
01	1			
11	1			
10	1			1

$I_0 = 1$

$I_1 = \bar{a}.\bar{b}$

$I_3 = 0$

$I_2 = a.\bar{b}$

Considering $f(a,b,c,d) = \Sigma_m(0,1,4,7,10,12,15,11)$
ab as input and CD as select lines.

$I_0 = \bar{a}+b$

$I_1 = \bar{a}\bar{b}$

$I_2 = a\bar{b}$

$I_3 = a+b$

ab \ cd	I_0	I_1	I_3	I_2
00	1	1		
01	1		1	
11	1		1	
10			1	1

~~$\bar{a}.\bar{b}$ $\bar{a}+\bar{b}$ $(a+b)$ $(a\bar{b})$~~

~~$\bar{a}+\bar{b}$~~

~~I_0 = A NAND B~~

~~I_1 = A NOR B~~

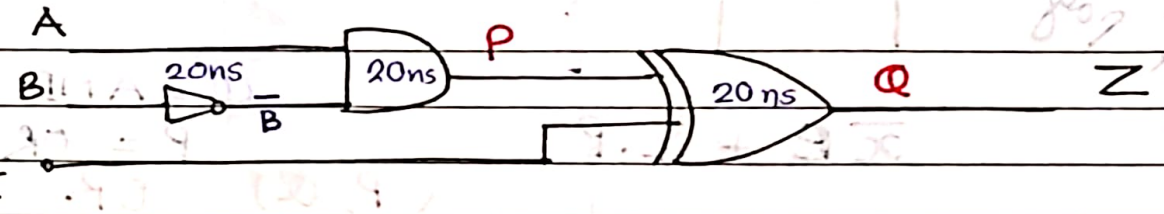
~~I_2 = A AND $\bar{B}$~~

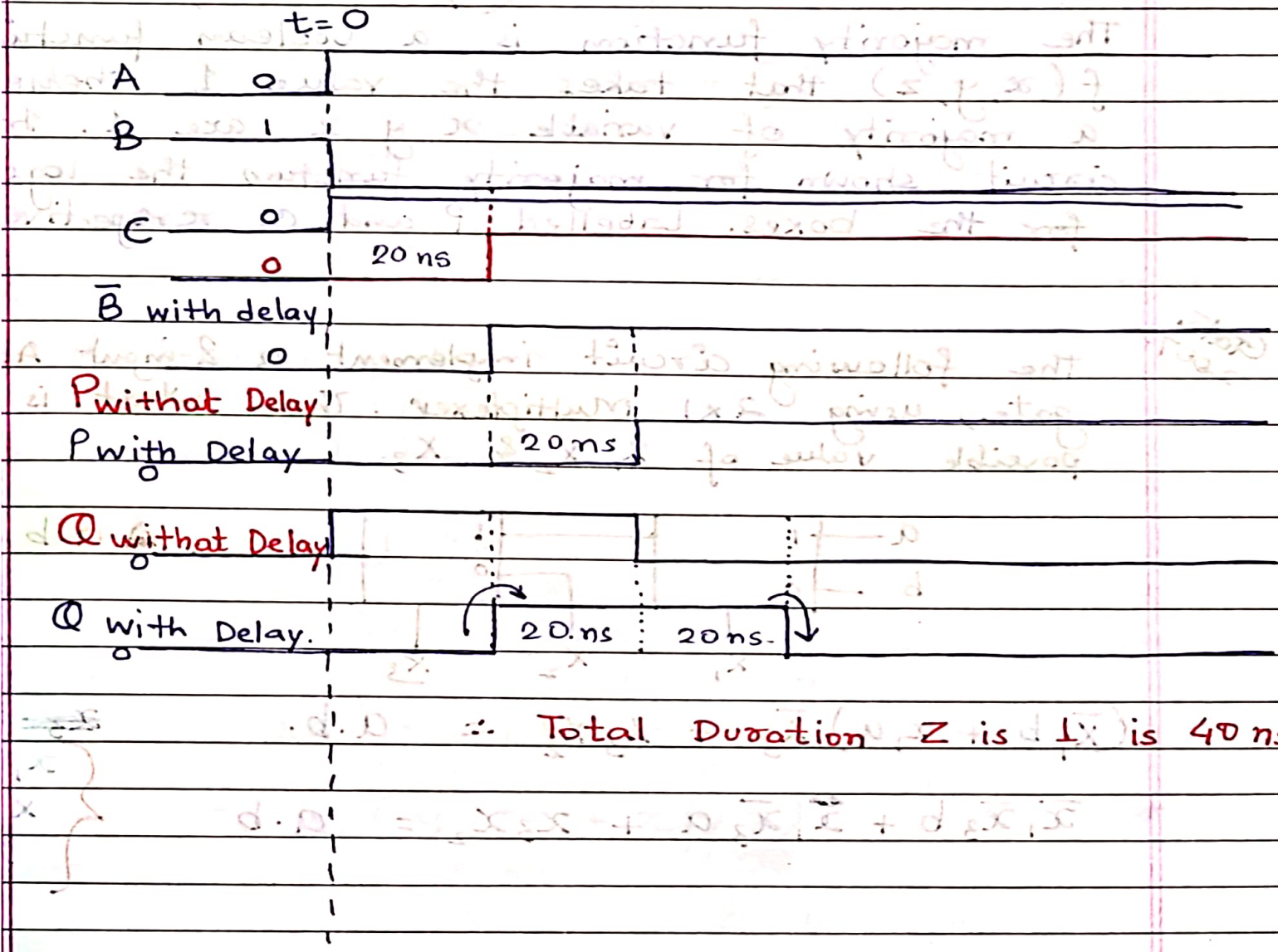
~~I_3 = A OR B~~

Work

PAGE NO. :
DATE : / /

If all logic gate shown in figure are having finite propogation delay of 20 ns each. Let $a = c = 0$ and $b = 1$. For $t \leq 0$. At time $t = 0$, input flip. (ie $a = c = 1$ and $b = 0$) and remain in that state only. The output $Z = 1$ for the duration in nanosecond — ?





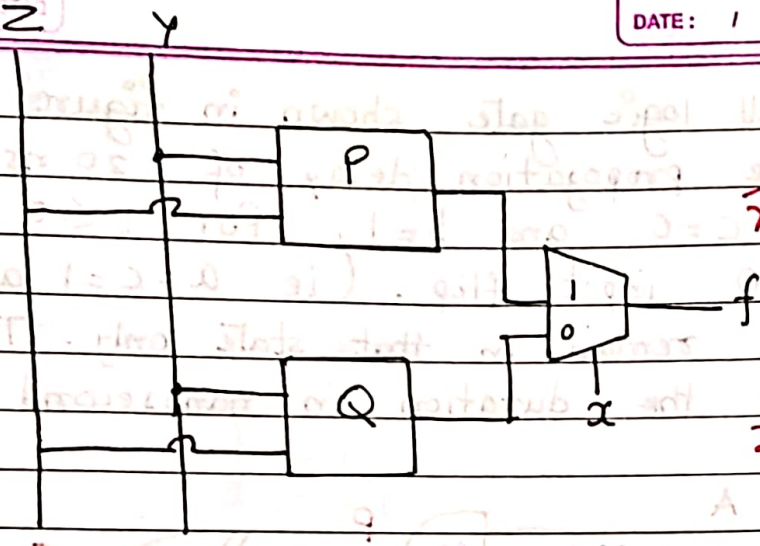
∴ Total Duration Z is 1 is 40 ns

PAGE NO. :
DATE : / /

Gate 2006

Solve using K-Map Homework

Done, see right page



x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$\bar{x}$; x

$\bar{x}\,Q + x.P$

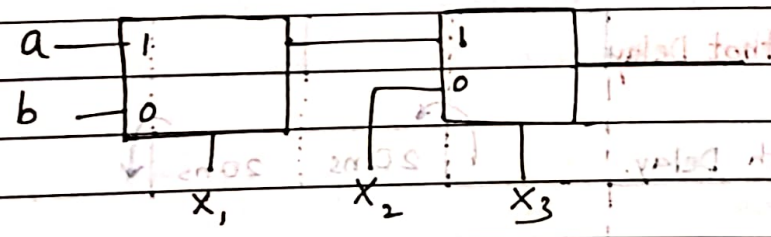
Q = AND
P = OR

(P, Q) OR, AND

The majority function is a boolean function $f(x, y, z)$ that takes the value 1 whenever a majority of variable x y z are 1. In the circuit shown for majority function the logic gate for the boxes. Labelled P and Q respectively.

Gate 2007

The following circuit implement a 2-input AND gate, using 2×1 Multiplexer. Then what is the possible value of X_1, X_2 & X_3.



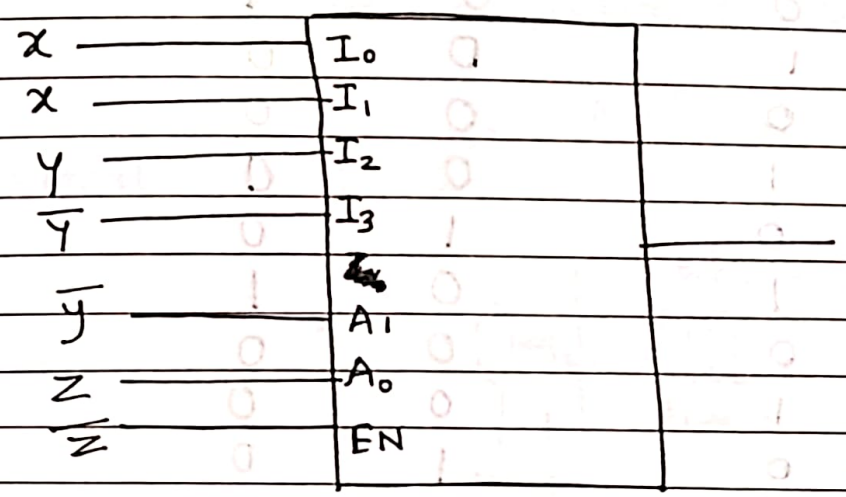
$(\bar{X}_1 b + X_1 a)\bar{X}_3 + X_3 X_2 = a.b.$

$\bar{x}_1 \bar{x}_3 b + \bar{x}_1 \bar{x}_3 a + x_3 x_2 = a.b$

$x_1 = b$
$x_2 = 0$
$x_3 = a$

PAGE NO.: _____
DATE: / /

Ex 02 find output f for the given MUX, where EN represent enable input.



$$f = \bar{z}\left[\bar{z}y.x + yzx + \bar{y}\bar{z}y + \bar{y}z\bar{y}\right]$$
$$= xy\bar{z} + \bar{y}z\bar{z}$$
$$f = xy\bar{z}$$
$$f = \Sigma_m(6)$$

Homework

Gate 2006.

x \ yz	00	01	11	10
0			1	
1		1	1	1

$$f = xy + yz + xz$$
$$f = x(y+z) + yz$$
$$f = x(y+z) + (\bar{x}+x)yz$$
$$= x(y+z) + \bar{x}yz + xyz$$
$$= x\underbrace{[(y+z)+yz]}_{P} + \bar{x}\underbrace{yz}_{Q}$$
$$= x(y+z) + \bar{x}(yz)$$

~~AND~~ OR ~~OR~~ AND

PAGE NO. :
DATE : / /

2-BIT Magnitude Comparator.

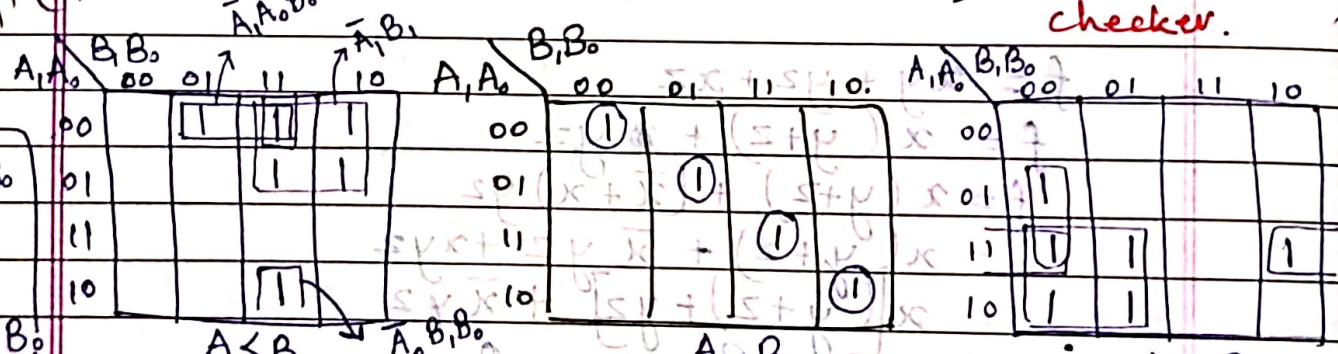
	A_1	A_0	B_1	B_0	$A_1A_0 > B_1B_0$	$A = B$	$A_1A_0 < B_1B_0$
0	0	0	0	0	0	1	0
1	0	0	0	1	0	0	1
2	0	0	1	0	0	0	1
3	0	0	1	1	0	0	1
4	0	1	0	0	1	0	0
5	0	1	0	1	0	1	0
6	0	1	1	0	0	0	1
7	0	1	1	1	0	0	1
8	1	0	0	0	1	0	0
9	1	0	0	1	1	0	0
10	1	0	1	0	0	1	0
11	1	0	1	1	0	0	1
12	1	1	0	0	1	0	0
13	1	1	0	1	1	0	0
14	1	1	1	0	1	0	0
15	1	1	1	1	0	1	0

for $A = B$, logically, when $A_1 = B_1$ "&" $A_0 = B_0$.

$\therefore (A_1 \odot B_1) \cdot (A_0 \odot B_0)$. equivalence checker.

$\bar{A}_1B_1 + (A_1 \odot B_1)\bar{A}_0B_0$

$\bar{A}_1\bar{A}_0B_0 + \bar{A}_1B_1 + \bar{A}_0B_1B_0$



Hw Find expression for < and >.

$A > B$: $A_1\bar{B}_1 + A_0\bar{B}_1\bar{B}_0 + A_1A_0\bar{B}$

$A_1\bar{B}_1 + (A_1 \odot B_1)A_0B_0$

Note : $a \oplus b \oplus c \neq a \odot b \odot c$.

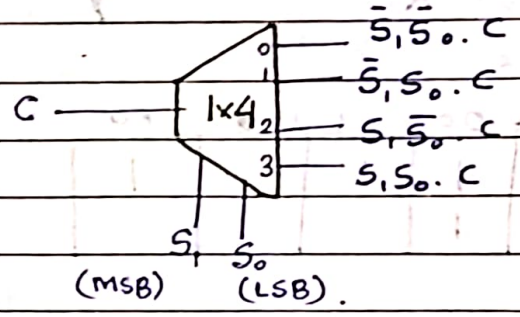
Even variable → $\odot$ is same as $\oplus$.

PAGE NO.:
DATE: / /

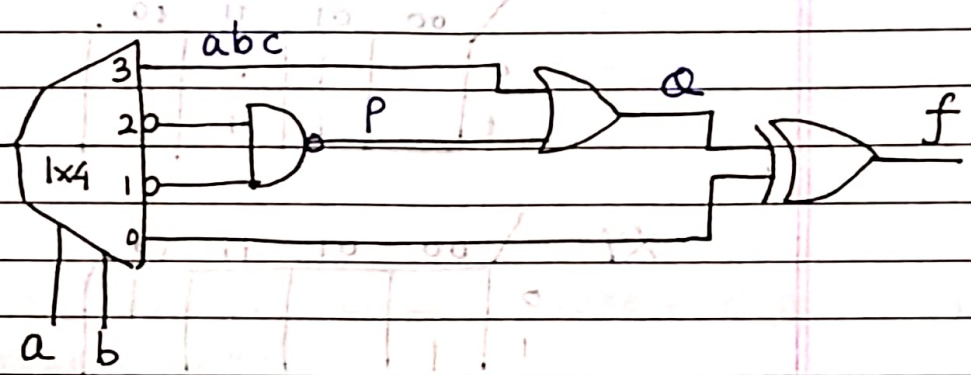
DEMULTIPLEXER

- Performs inverse operation on multiplexing.
- Also reffered as serial to parrallel Converter circuit.

Format 1×2^{n} → No of select lines



Ques



$$P = \bar{a}b.c + a\bar{b}c = (a \oplus b).c.$$

$$Q = abc + \bar{a}b.c + a\bar{b}c.$$

$$= c\,(a \oplus b + ab).$$

$$f = \bar{a}\bar{b}c \oplus c\,(a \oplus b + ab)$$

$$f = c\,(\cancel{(a \oplus b) + a \oplus b}).$$

$$f = \bar{a}\bar{b}c \oplus (a+b)c.$$

$$= \overline{a+b}\,c \oplus (a+b)\,c.$$

$$= \bar{X}C \oplus \bar{X}C$$

$$= \overline{\bar{X}C}.\bar{X}C + \overline{XC}.\overline{\bar{X}C}$$

$$= (\bar{X}+\bar{C})\bar{X}C + XC(X+\bar{C})$$

$$= \bar{X}C + XC = C$$

PAGE NO. :
DATE : / /

Ex. A 3 input majority gate defined by a function $M(a, b, c) = ab + bc + ca$. which one of the following Gate is represented by the function ?

$$M(\underbrace{\overline{M(a,b,c)}}_{X}, \underbrace{M(a,b,\bar{c})}_{Y}, \underbrace{c}_{Z}) = ?$$

K-MAP Method

X

	00	01	11	10
0	1	1		1
1	1			

Y

	00	01	11	10
0				1
1	1		1	1

Z

	00	01	11	10
0		1	1	
1		1	1	

Normal Method ⇒ Solved on Back Page ✓

XY

	00	01	11	10
0				1
1	1			

YZ

	00	01	11	10
0				
1			1	

XZ

	00	01	11	10
0		1		
1				

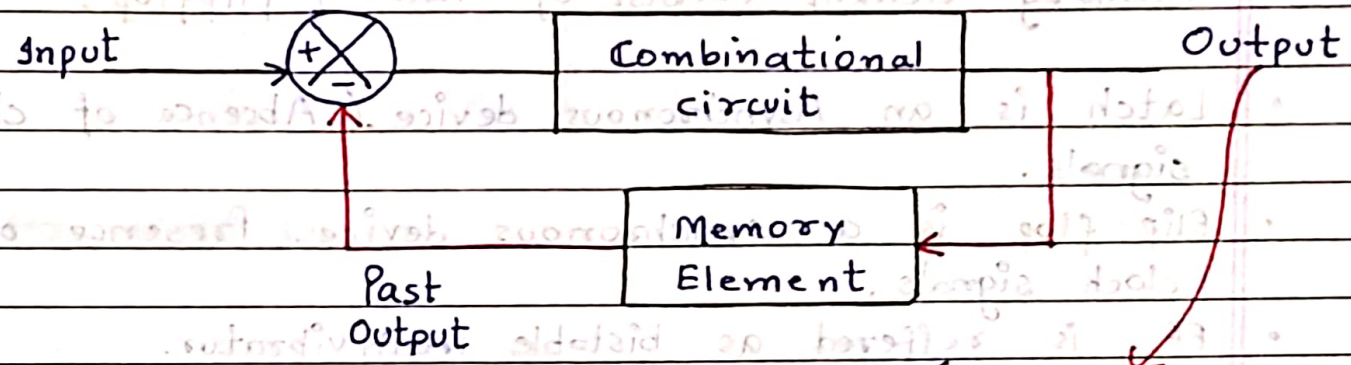
$f = \Sigma m(1,2,4,7)$ SOP

∴ 3 input XOR Gate. ✓

* M is not a 3 variable function. It is an operator

PAGE NO. :
DATE : / /

SEQUENTIAL CIRCUITS



f(Present Input and Past output).

Memory Element → Latches (Asynchronous) CLOCK absent
↓
Flip-Flops (Synchronus) CLOCK Present.

- Output of combinational circuit purely depends on input only. (Present input)
- Output of sequential circuit depend on present input as well as past output.
- Combination is an example of open loop system (No feed back).
- Sequential is an example of closed loop system, (with feedback).

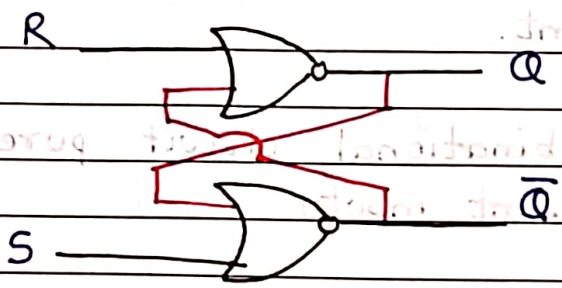
⇒ Feedback: Portion of output connecting input.

PAGE NO. :
DATE : / /

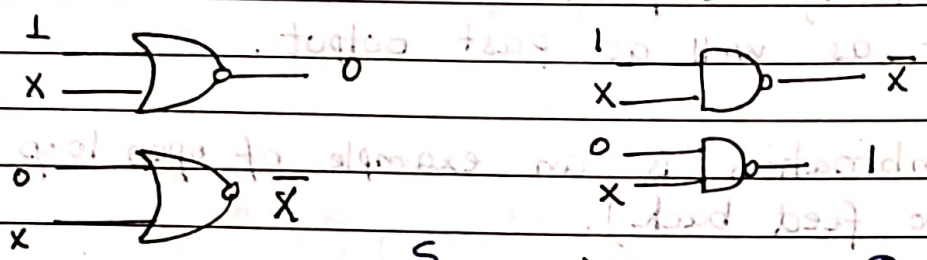
- Sequential circuit consists of combinational circuit and memory element.
- Memory element consist of latch / flipflop.
- Latch is an Asynchronous device. (Absence of clock signals.
- Flip-flop is a synchronous device. Presence of clock signals.
- FF is reffered as bistable multivibrator.
- FF / Latch is a 1 bit storage device.
- Latch is a basic fundamental unit of FF
- FF consist of two stable stages.

LATCH (Temporary Storage)

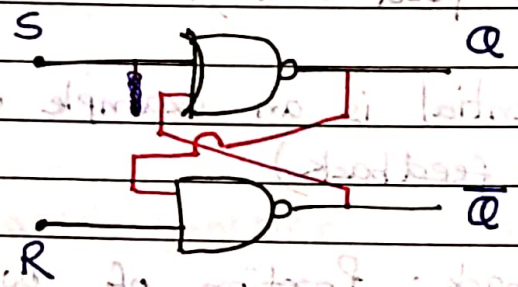
NOR - LATCH



S	R	Q_n	$\overline{Q}_n$	
0	0	Q_n	$\overline{Q}_n$	"Hold"
0	1	0	1	OFF/RESET
1	0	1	0	ON/SET
1	1	X	X	prohibited (oscillation)



NAND - LATCH



PAGE NO. :
DATE : / /

TTL → Wired AND
ECL → Wired OR

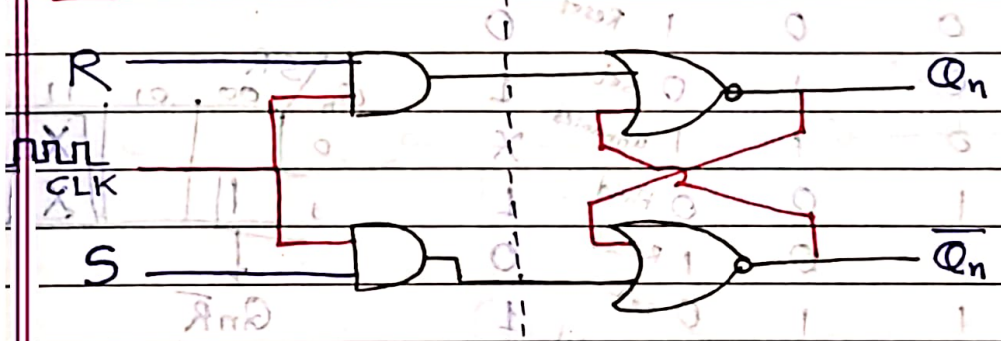
AOI → AOI } POS
OAI → OAI }

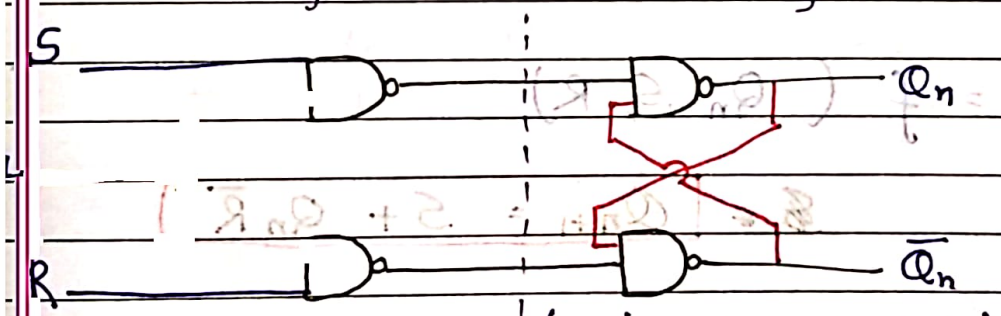
For NAND LATCH,

S	R	Q_n	$\overline{Q_n}$	
0	0	X	X	→ Prohibited } oscillation.
0	1	1	0	→ Set
1	0	0	1	→ Reset
1	1	Q_n	$\overline{Q_n}$	→ Hold

For SR latch using NOR, we cannot apply both inputs as 1 1. It is reffered as prohibited input which leads to oscillation.

S-R FF (using NOR Latch)





(using NAND Latch)

PAGE NO. :
DATE : / /

Any value

CLK	S	R	Q_n	$\overline{Q_n}$	
0	X	X	Q_n	$\overline{Q_n}$	Hold
1	0	0	Q_n	$\overline{Q_n}$	→ Hold
1	0	1	0	1	→ Reset /OFF
1	1	0	1	0	→ set / ON
1	1	1	X	X	} oscillating

Truth tabe is same for Both NOR and NAND implementation shown in previous page.

Characteristic Equation:

Characteristic Table : In this table, we determine upcoming output / next output for present input and past output.

past output	Present Input			Next output
Q_n	S	R		Q_{n+1}
0	0	0	Hold	0
0	0	1	Reset	0
0	1	0	set	1
0	1	1	unwanted	X
1	0	0	Hold	1
1	0	1	Reset	0
1	1	0	set	1
1	1	1	unwanted	X

Q_n \ SR	00	01	11	10
0			X	1
1	1		X	1

$Q_n\overline{R}$ $\quad$ S

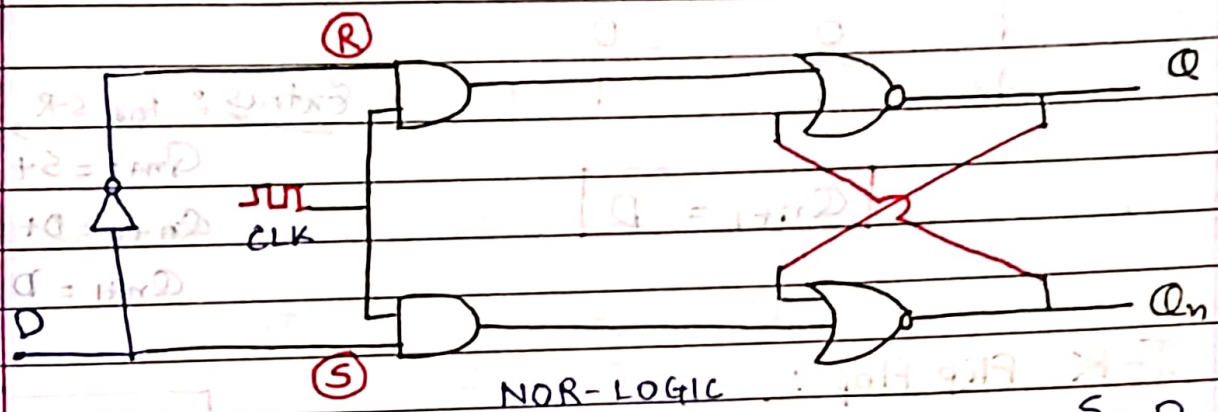
$$Q_{n+1} = f(Q_n, S, R)$$

$$\boxed{Q_{n+1} = S + Q_n\overline{R}}$$

PAGE NO. :
DATE : / /

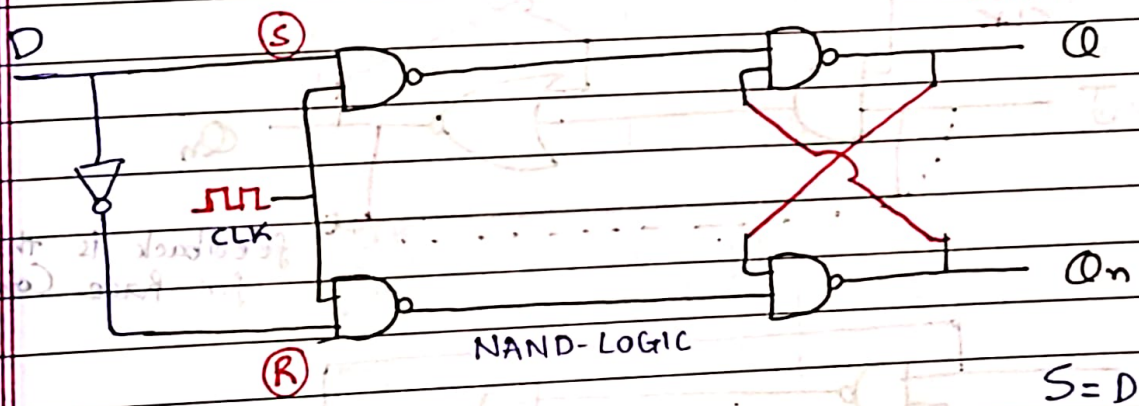
D- Flip flop : (Delay Flip Flop)

- It is used in data transmisson.
- It is reffered as transparent latch.
- It is also reffered as data transmission flip-flop.



NOR- LOGIC

$S = D$
$R = \overline{D}$



NAND- LOGIC

$S = D$
$R = \overline{D}$

CLK	D	Q_n	Q_{n+1}	
0	X	Q_n	$\overline{Q_n}$	Hold
1	0	0	1	Hold
1	1	1	0	

PAGE NO. :
DATE : / /

Characteristic Table :

Past output Q_n	Present input D	next output. Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

$$\boxed{Q_{n+1} = D}$$

Extras : for S-R,

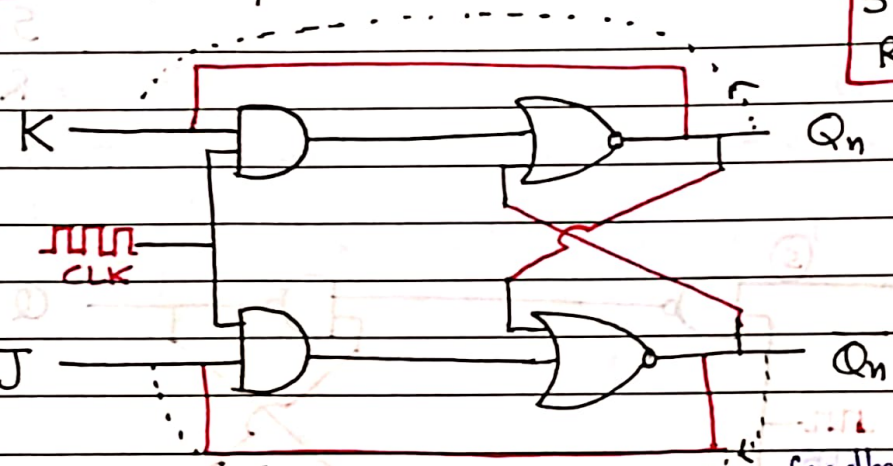
$Q_{n+1} = S + Q_n \overline{R}$

$Q_{n+1} = D + Q_n \overline{D}$

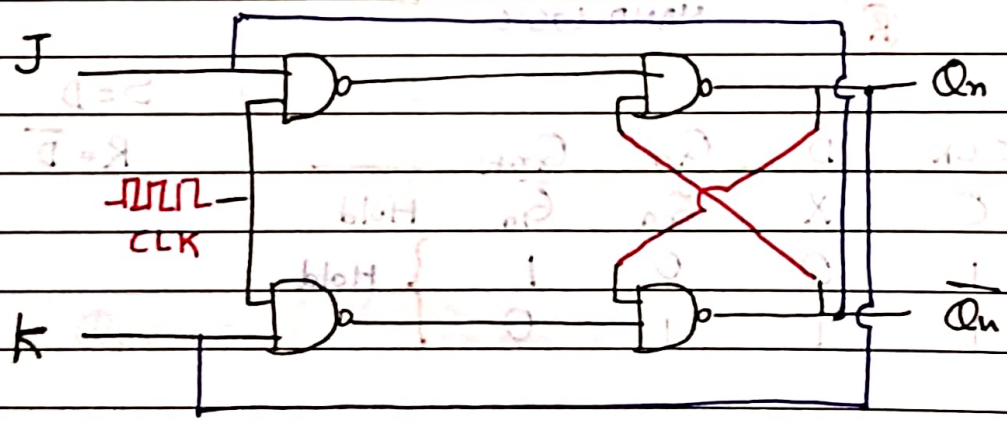
$Q_{n+1} = D$

J-K Flip Flop :

$$\boxed{\begin{aligned} S &= J\overline{Q_n} \\ R &= K Q_n \end{aligned}}$$



feedback is the reason for Race Condition



PAGE NO. :
DATE : / /

Truth Table.

CLK	J	K	Q_n	$\overline{Q_n}$	
0	X	X	Q_n	$\overline{Q_n}$	Hold
1	0	0	Q_n	$\overline{Q_n}$	Hold
1	0	1	0	1	Reset
1	1	0	1	0	set
1	1	1	$\overline{Q_n}$	Q_n	compliment

characteristic Table :

Q_n	J	K	Q_{n+1}	
0	0	0	0	Hold
0	0	1	0	Reset
0	1	0	1	set
0	1	1	1	compliment
1	0	0	1	Hold
1	0	1	0	Reset
1	1	0	1	set
1	1	1	0	Compliment

Q_n \ JK	00	01	11	10
0			1	1
1	1			1

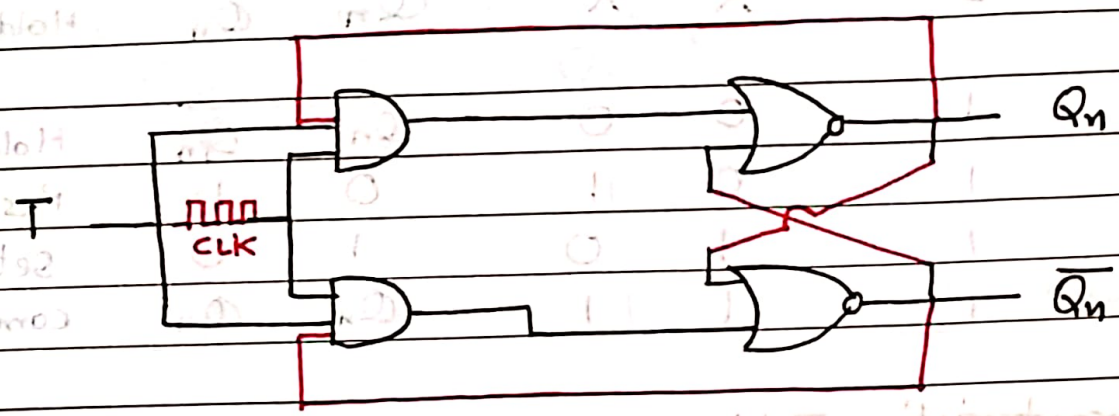
$$\boxed{Q_{n+1} = Q_n\overline{K} + \overline{Q_n}J}$$

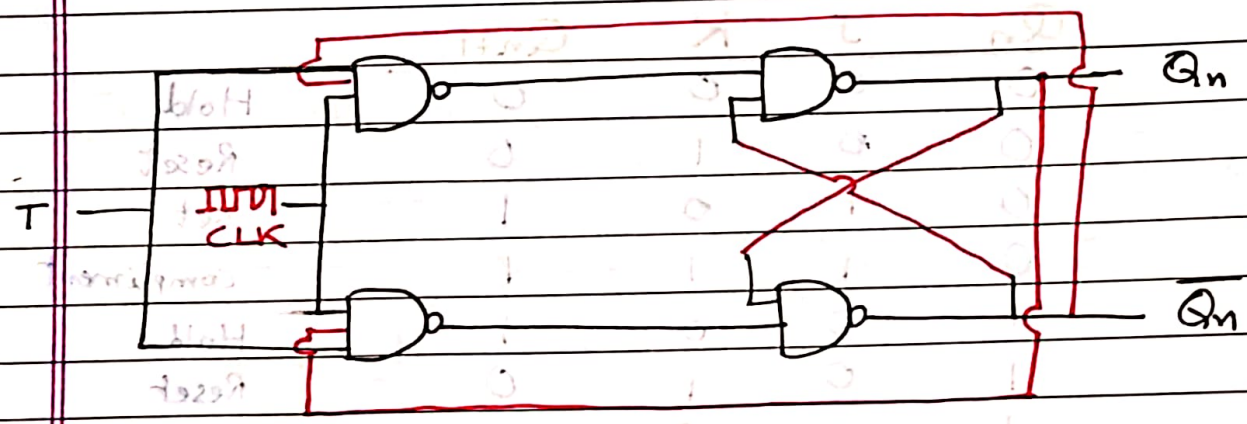
Extra

$$Q_{n+1} = S + Q_n\overline{R}$$
$$= J\overline{Q_n} + Q_n\left[\overline{K \cdot \overline{Q_n}}\right]$$
$$= J\overline{Q_n} + Q_n(\overline{K} + \overline{Q_n})$$
$$= J\overline{Q_n} + \overline{K}Q_n.$$

PAGE NO. :
DATE : / /

T-Flip Flop : $\boxed{J = K = T}$





Truth Table :

CLK	T	Q_n	$\overline{Q_n}$	
0	X	Q_n	$\overline{Q_n}$	Hold
1	0	Q_n	$\overline{Q_n}$	Hold.
1	1	$\overline{Q_n}$	Q_n	compliment OR ~~TOGGLE~~

characteristic Table.

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

$$\boxed{Q_{n+1} = T \oplus Q_n}$$

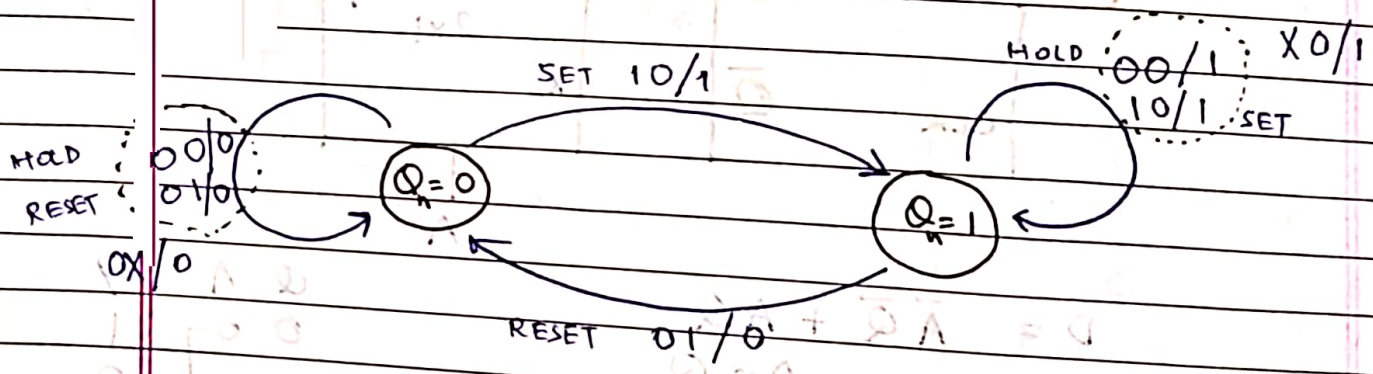
Extra:
$Q_{n+1} = \overline{Q_n}J + Q_n\overline{K}$
$= \overline{Q_n}T + Q_n\overline{T}$
$= Q_n \oplus T$

PAGE NO. :
DATE : / /

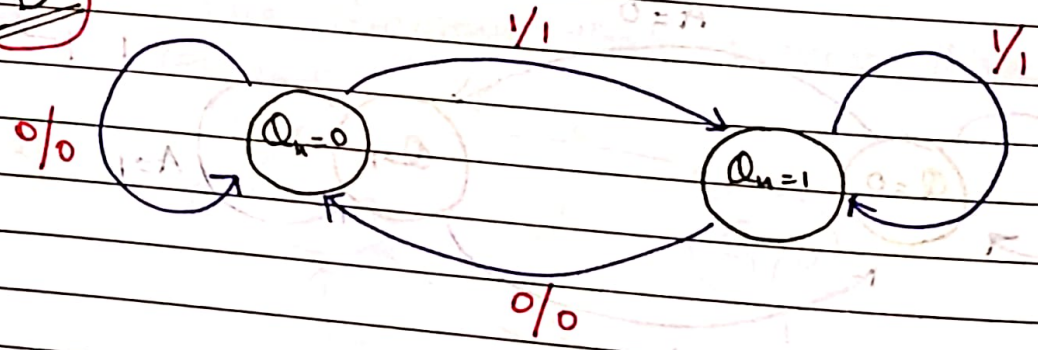
State Transition Diagram
OR
Vector Diagram

format $\boxed{\text{Input / output}}$

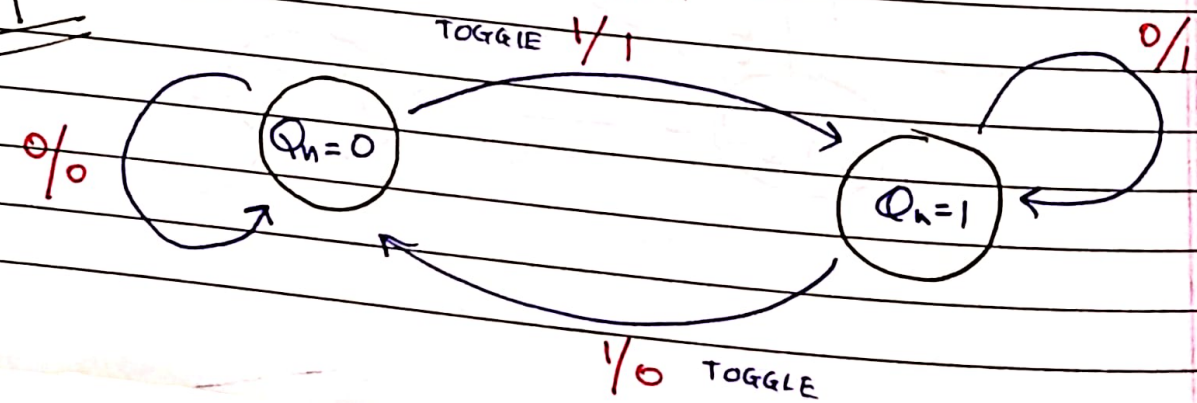
SR / Q_{n+1}
JK / Q_{n+1}
D / Q_{n+1}
T / Q_{n+1}



D

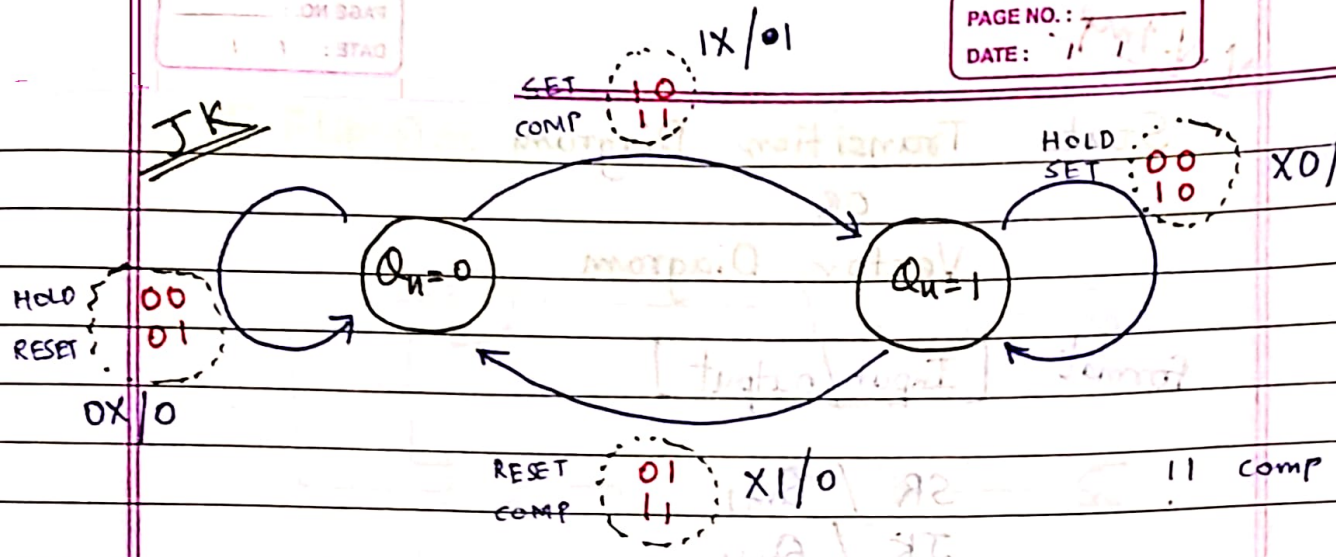


T

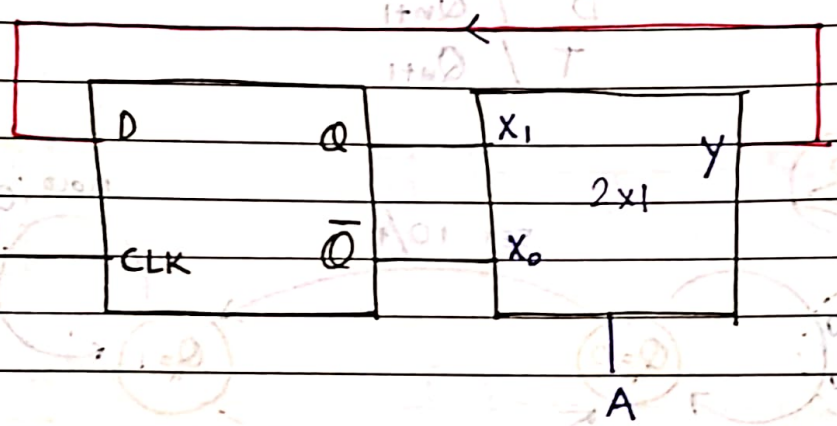


PAGE NO. :
DATE : / /

JK



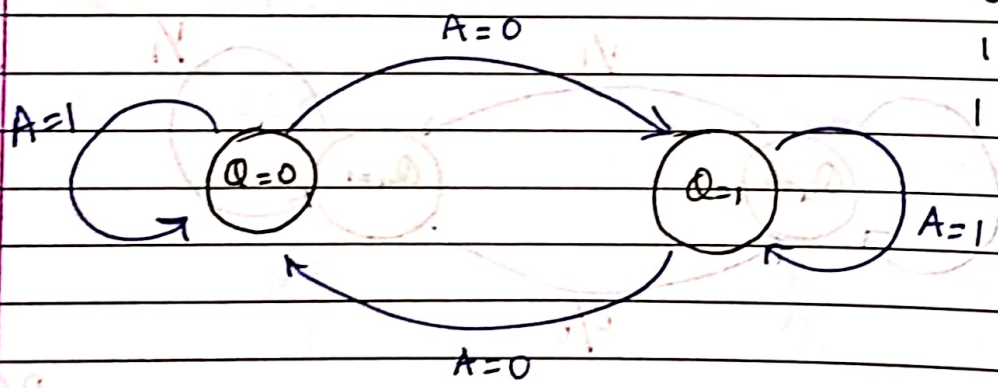
Ex



$D = \bar{A}\bar{Q} + AQ$

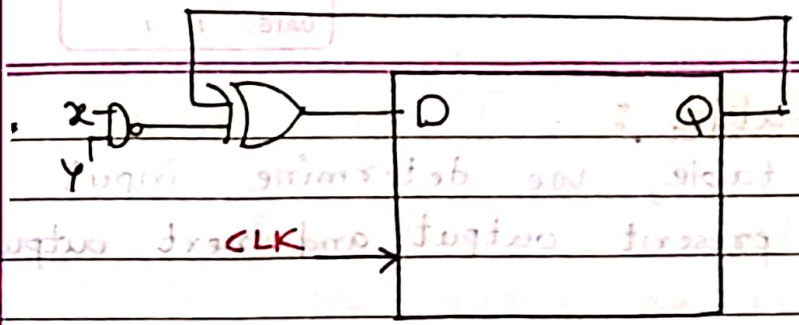
$D = A \odot Q$

Q	A	y
0	0	1
0	1	0
1	0	0
1	1	1

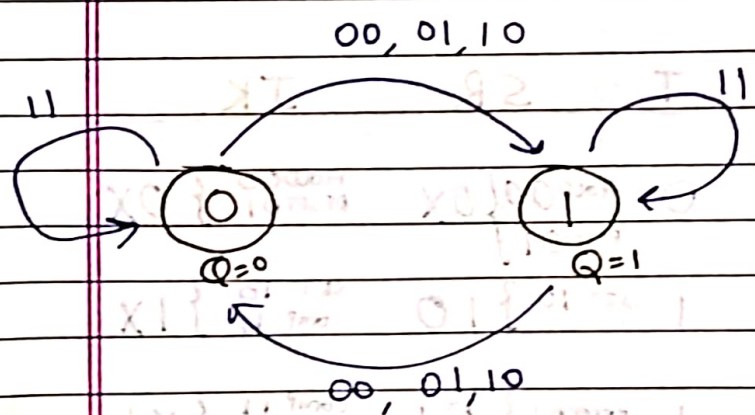


PAGE NO. :
DATE : / /

Ex.



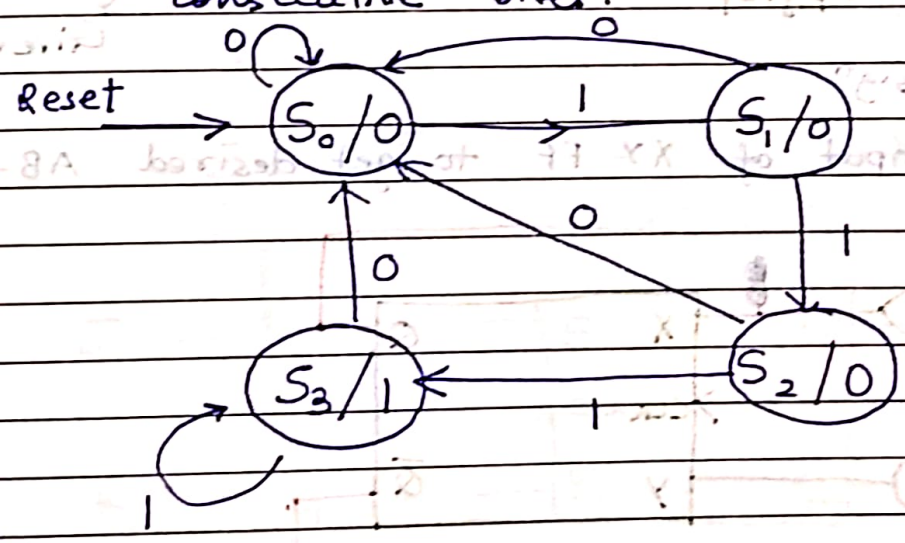
$$Q_{n+1} = D = Q_n \oplus (\overline{xy})$$



Q_n	x	y	Q_{n+1}
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Q.59 Homework.

State diagram that detects three or more consecutive ones.



PAGE NO. :
DATE : / /

Excitation Table :

- In excitation table, we determine input condition for present output and next output.

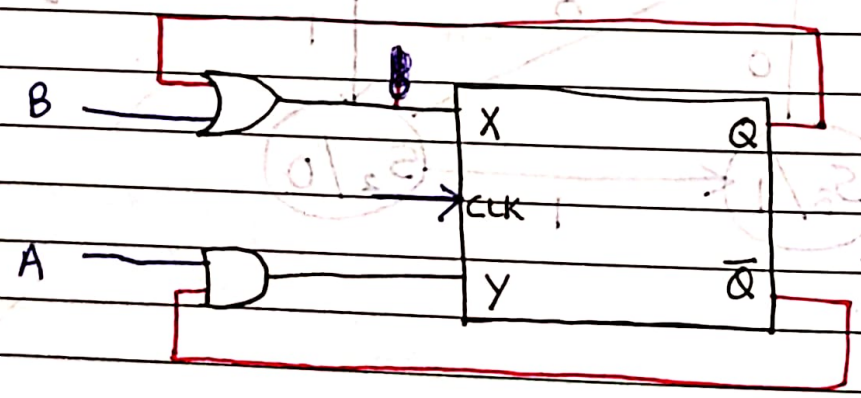
- using excitation table we can do, conversion of flip-flop. Ex. using Excitation table we can convert T-FF to JK-FF.

present output Q_n	next output Q_{n+1}	D	T	SR	JK
0	0	0	0	HOLD 00, RESET 01 } 0X	HOLD 00, RESET 01 } 0X
0	1	1	1	SET 10 } 10	SET 10, COMP 11 } 1X
1	0	0	1	RESET 01 } 01	COMP 11, RESET 01 } X1
1	1	1	0	HOLD 00, SET 10 } X0	SET 10, HOLD 00 } X0

Ex. A modal representing conversion of (XY) flip flop to (AB) Flip flop

(AB) → To design.
(XY) → Given

- Modify input of XY-FF to get desired AB-FF



PAGE NO. :
DATE : / /

Convert SR-FF to J.K-FF

- The given ff is SR-FF and we need to design JK FF, that means we need to modify the input of, SR FF, to get JK Flip Flop.

Q_n	J	K	S	R
0	0	0	0	X
0	0	1	0	X
0	1	0	1	0
0	1	1	1	0
1	0	0	X	0
1	0	1	0	1
1	1	0	X	0
1	1	1	0	1

$S = f(Q_n, J, K)$.

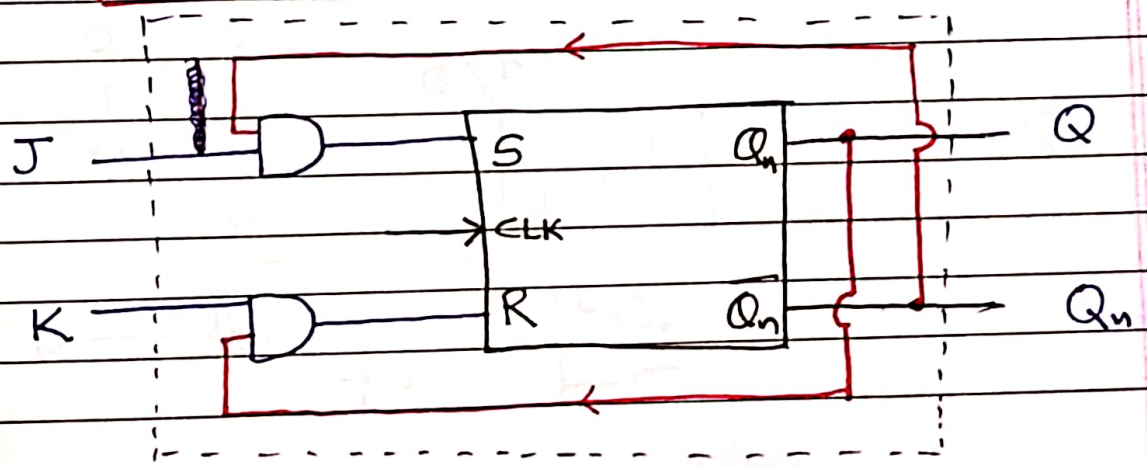
Q_n \ JK	00	01	11	10
0	0	0	1	1
1	X	0	0	X

$\boxed{S = J\overline{Q_n}}$

$R = f(Q_n, J, K)$

Q_n \ JK	00	01	11	10
0	X	X	0	0
1	0	1	1	0

$\boxed{R = K.Q_n}$



PAGE NO. :
DATE : / /

Ex Convert SR to D ff

- Given ff is SR ff and we need to design D-ff.

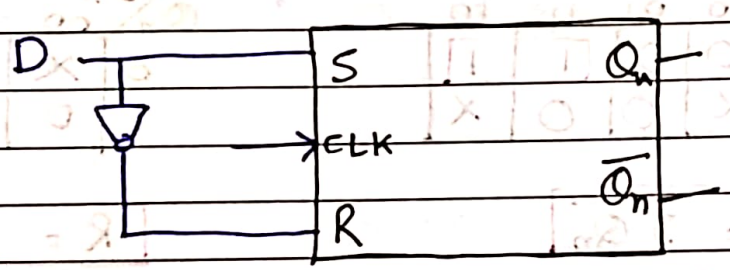
Q_n	D	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

$S = f(Q_n, D)$ $\qquad$ $R(Q_n, D)$

$Q_n \backslash D$	0	1 → D
0	0	1
1	0	X

$Q_n \backslash D$	0 → $\overline{D}$	1
0	X	0
1	1	0

$S = D$ $\qquad$ $R = \overline{D}$



PAGE NO. :
DATE : / /

Ex Convert D to T ff.

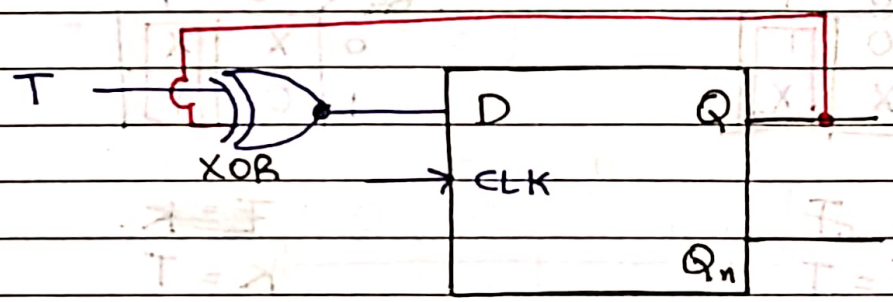
- Given ff is D-ff and we need to design T-ff.

Q_n	T	D
0	0	0
0	1	1
1	0	1
1	1	0

$D = f(Q_n, T)$

Q_n \ T	0	1
0	0	1
1	1	0

$D = T \oplus Q_n$.



H.W.

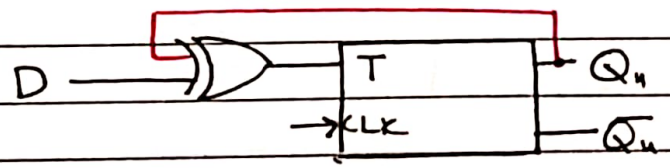
Ex. Convert T-ff to D-ff.

Q_n	D	T
0	0	0
0	1	1
1	0	1
1	1	0

$T = f(Q_n, D)$

Q_n \ D		
		1
	1	

$T = D \oplus Q_n$.



PAGE NO. :
DATE : / /

Ex Convert J-K to T

- Given ff is J-K, desired ff is T.

Q_n	J	K
0	0	0
0	0	
0	1	
0	1	
1	0	
1	0	
1	1	
1	1	

Q_n	T	J	K
0	0	0	X
0	1	1	X
1	0	X	0
1	1	X	1

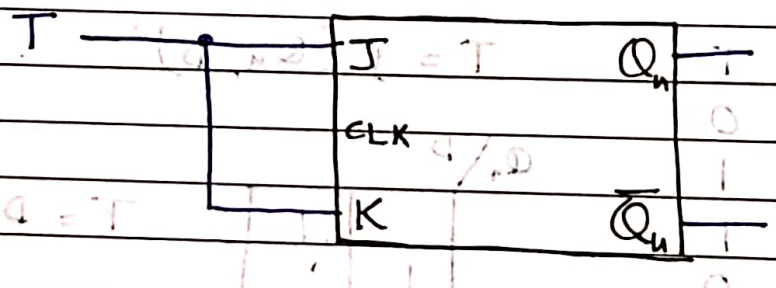
$J = (Q_n, T)$ $K = (Q_n, T)$

Q_n \ J	0	1
0	0	1
1	X	X

Q_n \ K	0	1
0	X	X
1	0	1

$T = J$
$J = T$

$K = T$.



PAGE NO. :
DATE : / /

Ex Convert T to JK.

- Given ff is T, we need to modify input of T to get J K.

Q_n	J	K	T
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

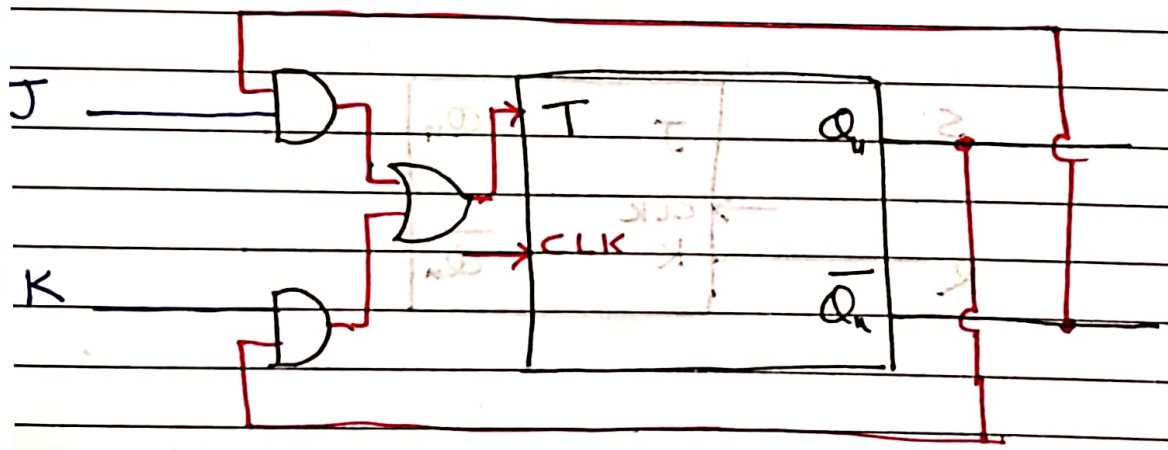
$T = f(Q_n, J, K)$

Q_n \ JK	00	01	11	10
0	0	0	1	1
1	0	1	1	0

$J\overline{Q_n}$

$K.Q_n$

$$\boxed{T = J\overline{Q_n} + K.Q_n}$$



PAGE NO. :
DATE : / /

Ex Convert J-K to SR.

- Given ff is JK, we need to convert input of J-K to get SR.

Q_n	S	R	J	K
0	0	0	0	X
0	0	1	0	X
0	1	0	1	X
0	1	1	X	X
1	0	0	X	0
1	0	1	X	1
1	1	0	X	0
1	1	1	X	X.

Q_n \ SR	00	01	11	10
0	0	0	X	1
1	X	X	X	X

S

Q_n \ SR	00	01	11	10
0	X	X	X	X
1	0	1	X	0

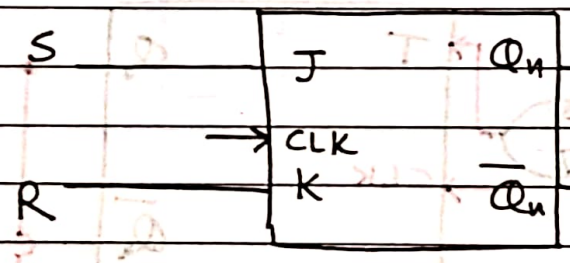
R.

SR

JK

$J = S$ $K = R$

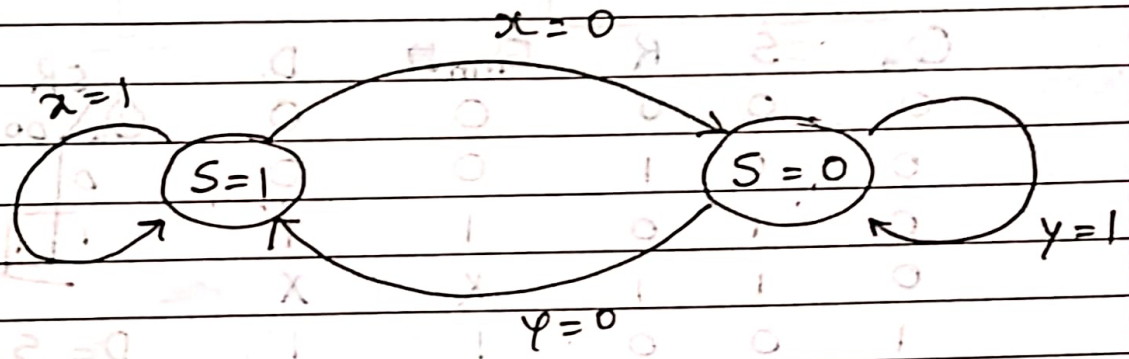
- JK ff itself behaves as SR-ff.



PAGE NO. :
DATE : / /

Q8. Ex

For a state machine with following state diagram, the expression for the next state S^+ in terms of current state S and the input variable X and Y is :-



(a) $S^+ = S'y' + Sx$
(b) $S^+ = Sxy' + Syx'$
(c) $S^+ = xy'$
(d) $S^+ = S'y + Sx'$

Ans :)

S	x	y	S^+
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

S \ xy	00	01	11	10
0	1	0	0	1
1	0	0	1	1

$S = S'y' + Sx$

PAGE NO. :
DATE : / /

H.W

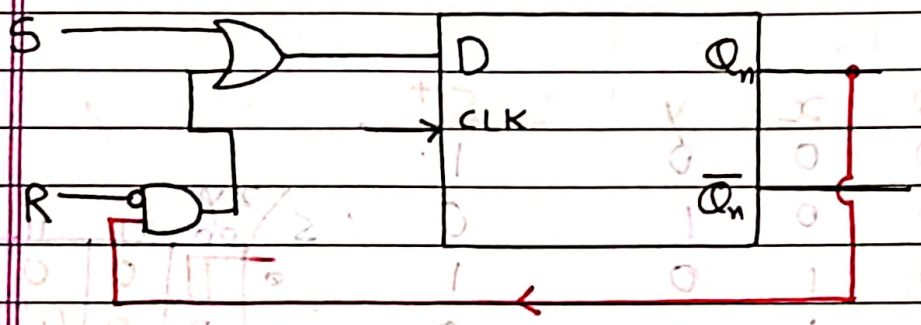
Ex Convert D to SR flip flop.

Given FF is D, we need to modify input of D to get SR.

Q_n	S	R	Q_{n+1}	D.
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	X	X
1	0	0	1	1
1	0	1	0	0
1	1	0	1	1
1	1	1	X	X

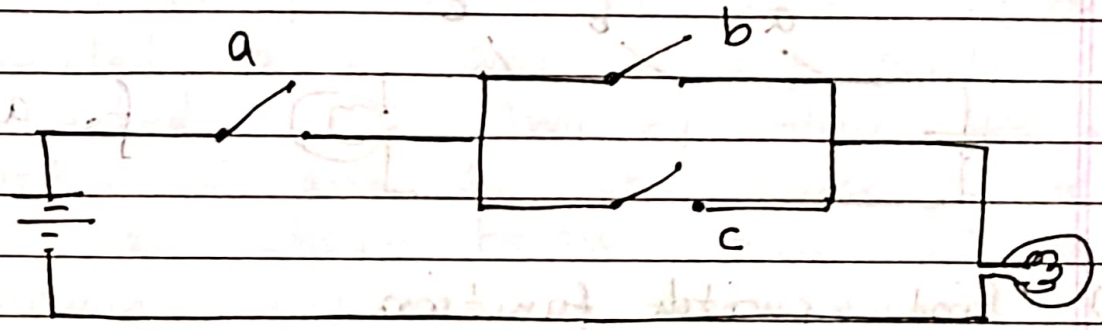
$Q_n \backslash SR$	00	01	11	10
0			X	1
1	1		X	1

$D = S + Q_n \overline{R}$



PAGE NO. :
DATE : / /

(Q) Find the switching function for given circuit

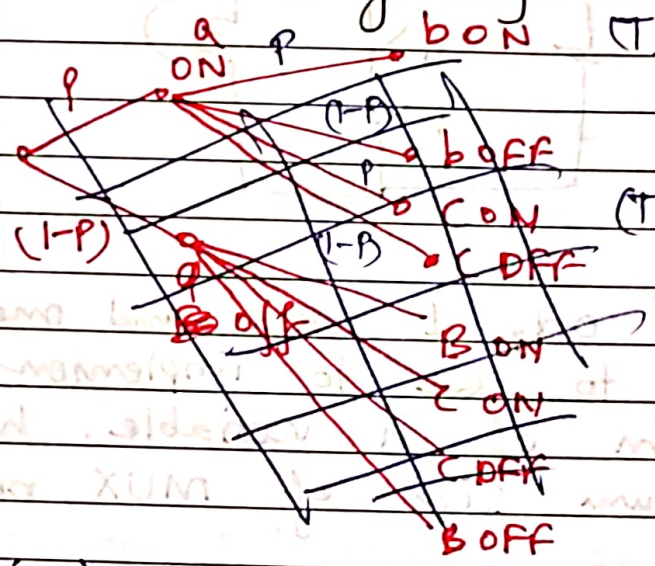


Incondescent Bulb.

$f = a.(b+c)$.

$f = ab + ac$.

(Q) Find the switching function for given ckt switching probability of all the switches is p then find the probability that the bulb is in glowing condition.



$\cancel{p(p)} + \cancel{p(p)}$

$\cancel{= 2p^2}$.

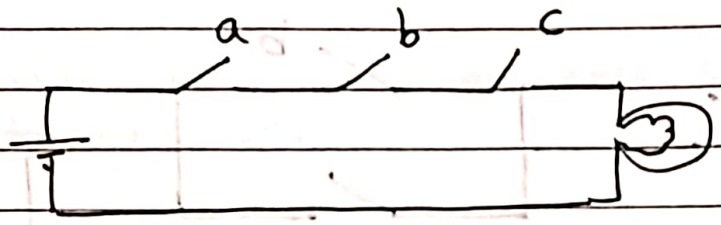
$p.p.(1-p) + p.p.(1-p) + p.p.p$

$= 2p^2 - p^3 - p^3 + p^3$.

$= 2p^2 - p^3$ ✓

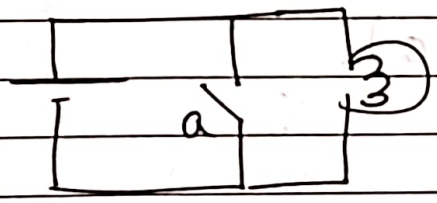
PAGE NO. :
DATE : / /

(Q.) Find switch function.



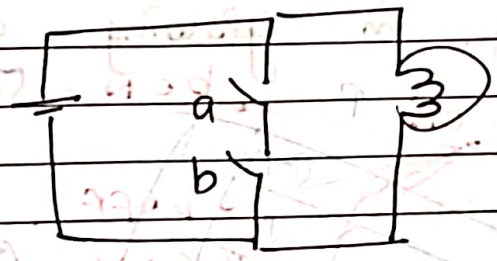
$f = a.b.c.$

(Q) Find switch function



$f = \bar{a}$

(Q.) Find switch function.



$f = \overline{a.b}$

Ex Suppose only 1 mux and one inverter are allowed to use to implement any boolean function of n variable. What is the minimum size of MUX needed _____

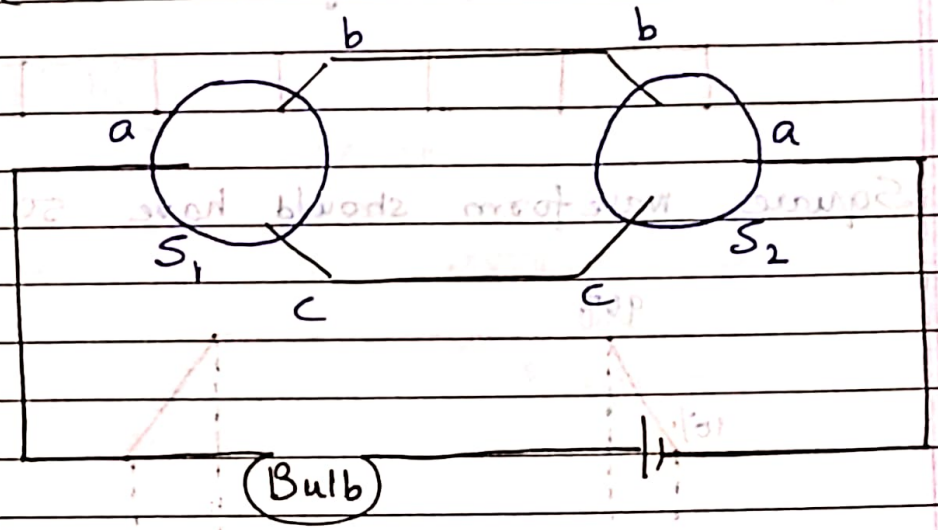
(a) 2^n line to 1 line
(b) 2^{n+1} line to 1 line
✓(c) 2^{n-1} line to 1 line
(d) 2^{n-2} line to 1 line.

PAGE NO. :
DATE : / /

2005
Ex

A two way switch has 3 terminal a, b and c. In on position (logic value 1), a is connected to b, and in off position a is connected to c. Two of these two way switches S_1 and S_2 are connected to a bulb as shown below. Which of the following expression if true will always result in the lightning of bulb?

(a) $S_1 \bar{S}_2$
(b) $S_1 + S_2$
(c) $\overline{S_1 \oplus S_2}$
(d) $S_1 \oplus S_2$



$S_1 \cdot S_2 + \bar{S}_1 \cdot \bar{S}_2$

(b) If P is the probability of switch in on condition (closed), then find the probability that the bulb is on.

$$P^2 + (1-P)^2 = P^2 + P^2 - 2P + 1$$
$$= \cancel{(1-2P)}\ 2P^2 - 2P + 1$$

PAGE NO. :
DATE : / /

TYPES OF CLOCK SIGNAL

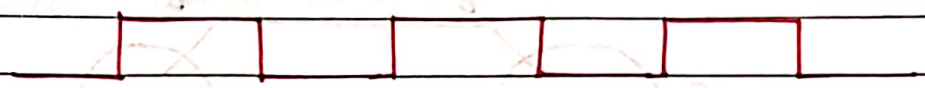
- A clock is used for synchronization purpose.
- We consider square wave form as clock signal
- A square wave form is characterized by duty cycle.

Duty cycle :

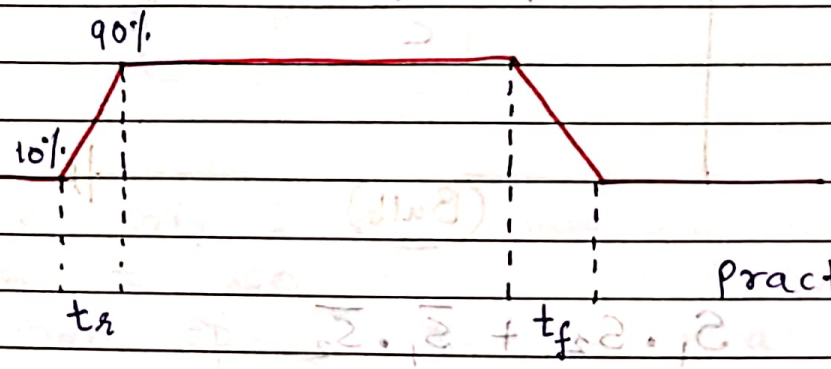
$$\% D = \frac{T_{ON}}{T_{ON} + T_{OFF}} \times 100 \%$$

$$= \frac{T_{ON}}{T} \times 100 \%$$

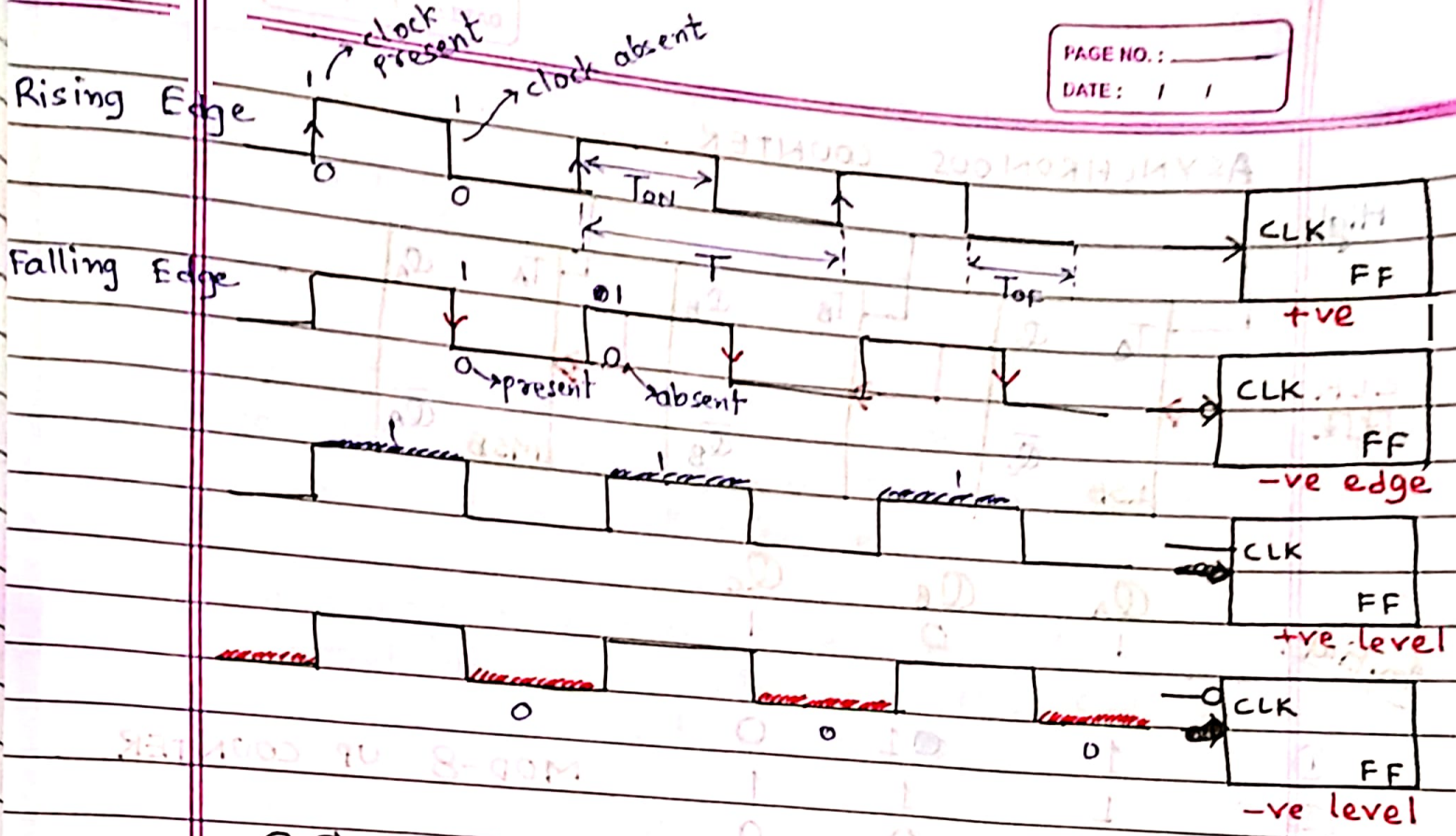
- for the ideal square wave form, we consider 0 rize time, and zero fall time.



- Square waveform should have 50 % duty cycle.



Practical



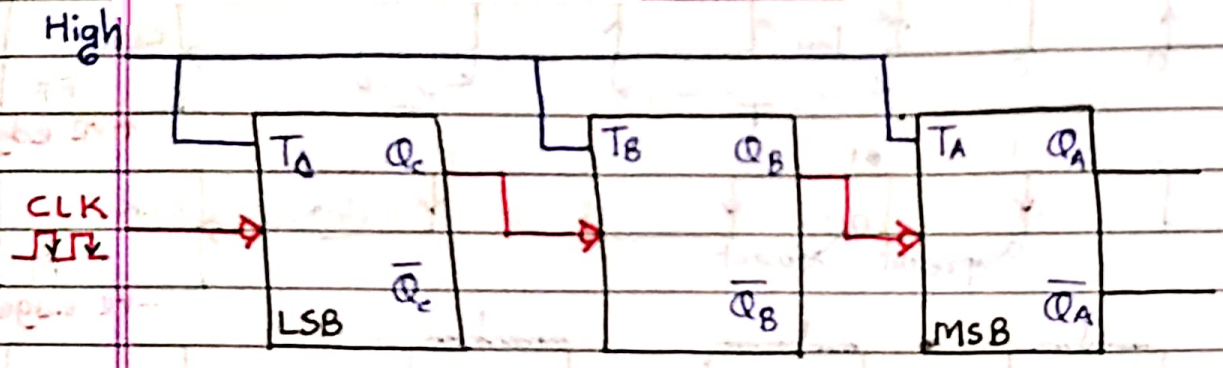
COUNTER

SLOWER → Asynchronous OR SERIES OR RIPPLE

FASTER → Synchronous OR PARALLEL

PAGE NO. :
DATE : / /

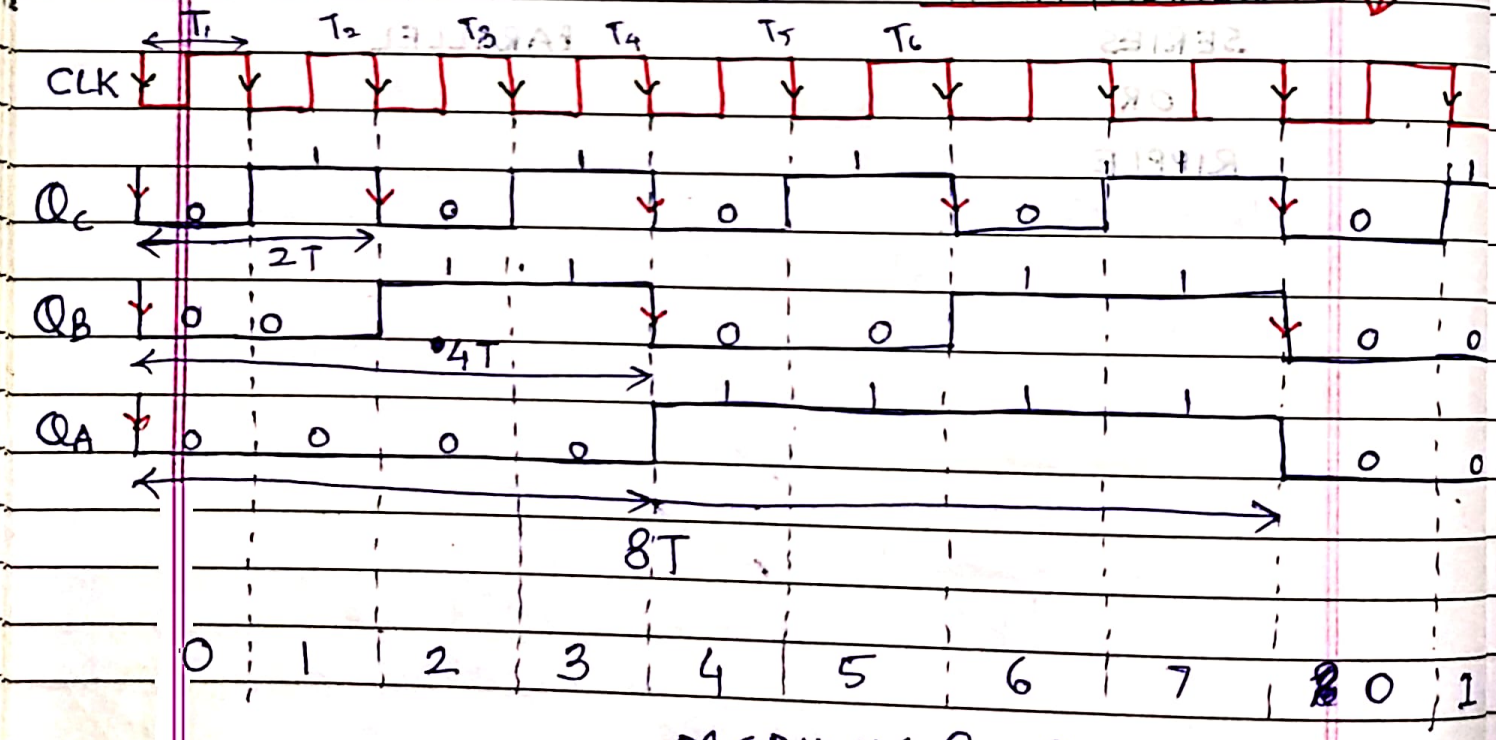
ASYNCHRONOUS COUNTER.



	Q_A	Q_B	Q_C
initial	1	0	1
1	1	1	0
2	1	1	1
3	0	0	0
4	0	0	1
5	0	1	0
6	0	1	1
7	1	0	0
8	1	0	1

MOD-8 UP COUNTER

TIMING DIAGRAM



MODULUS-8 UP Counter.

$$T_{out} = 8\,T_{IN}$$

$$f_{out} = \frac{f_{IN}}{M} = \frac{f_{IN}}{8}$$

- In Asynchronous counter, clock signal is provided to one of the flip-flop, and that flip-flop is considered as LSB flip-flop.

- up-coming ff / other ff will be driven, by the output of the previous flip-flop. And the last ff will be considered as MSB ff.

- By looking at the clock signal (Behaviour) rising edge / falling edge, we can identify it, that if it is up or down counter.

- Ripple counter is slower in operation compared to synchronous counter.

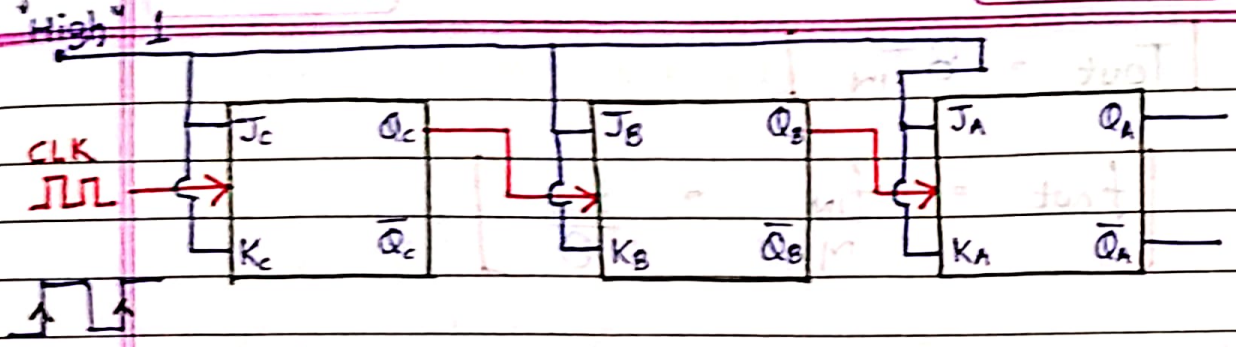
$$T_D = n \cdot t_{PD}$$

n → No of ff used ; t_{PD} → Propogation delay of each ff

- for designing of Asynchronous counter, only T and JK-ff are used.

- Modulus formula: $MOD \leq 2^n$

PAGE NO. :
DATE : / /

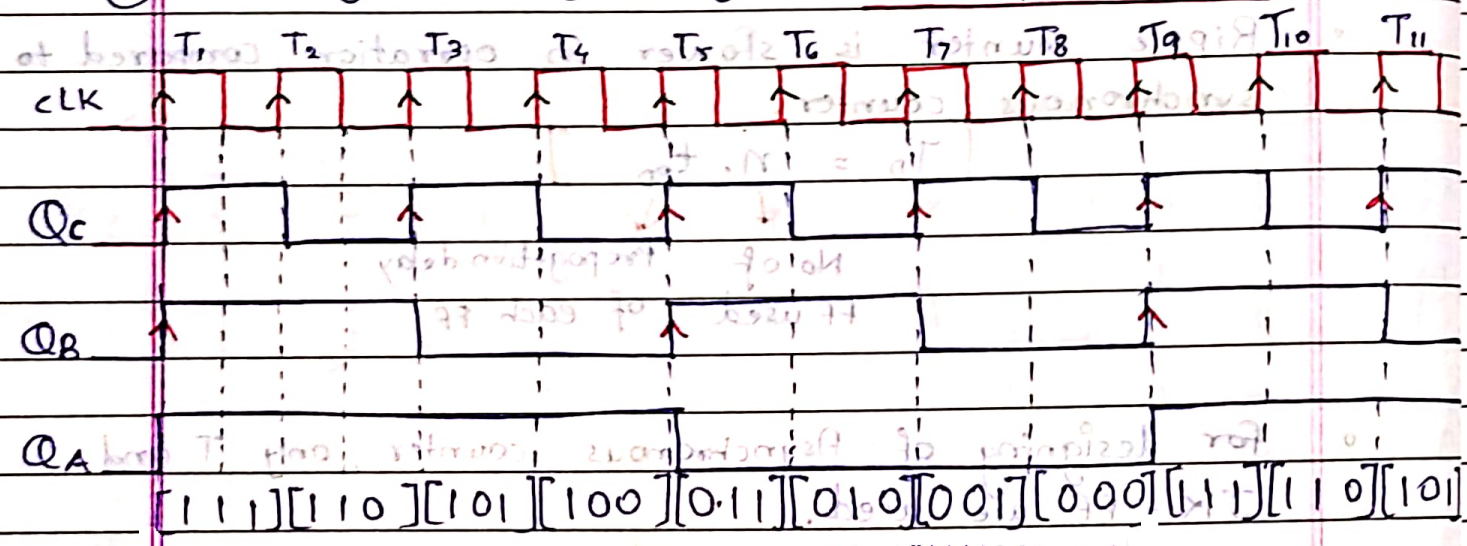


	Q_A	Q_B	Q_C
Initial	0	0	0
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1
8	0	0	0

MOD-8 DOWN COUNTER

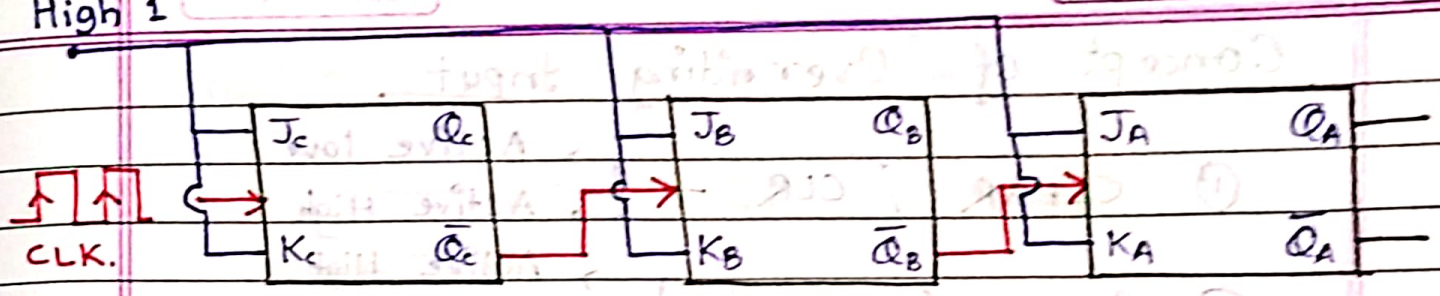
Homework

TIMING DIAGRAM



DOWN

"High 1"



a) This is MOD-8 up-counter.

b) This is MOD-8 down counter.

	Q_A	Q_B	Q_C	$\overline{Q_B}$	$\overline{Q_C}$
initial	0	0	0	1	1
1	0	0	1	1	0
2	0	1	0	0	1
3	0	1	1	0	0
4	1	0	0	1	1
5	1	0	1	1	0
6	1	1	0	0	1
7	1	1	1	0	0
8	0	0	0	1	1

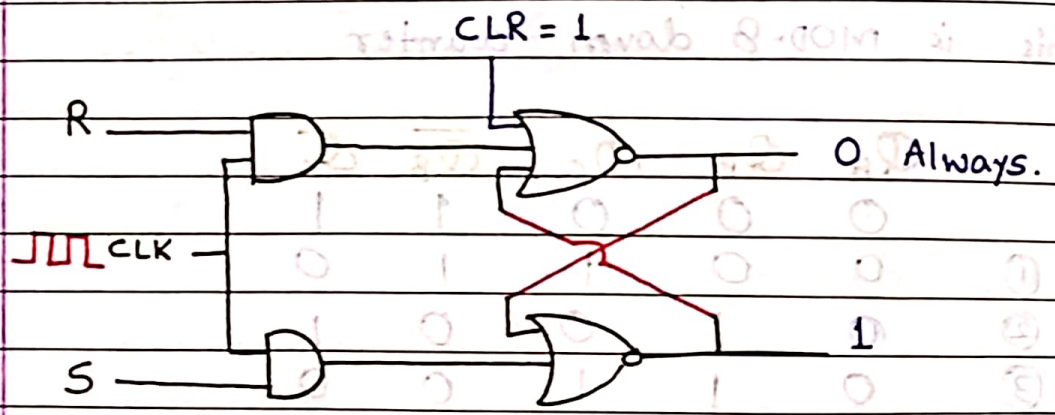
"UP COUNTER"

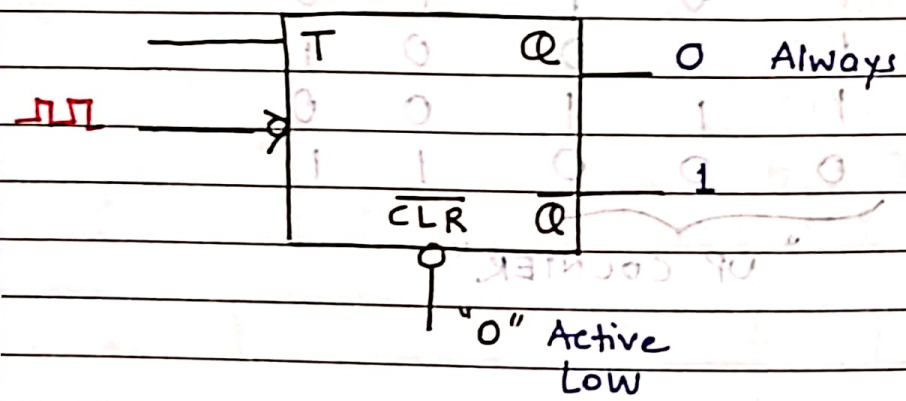
PAGE NO. :
DATE : / /

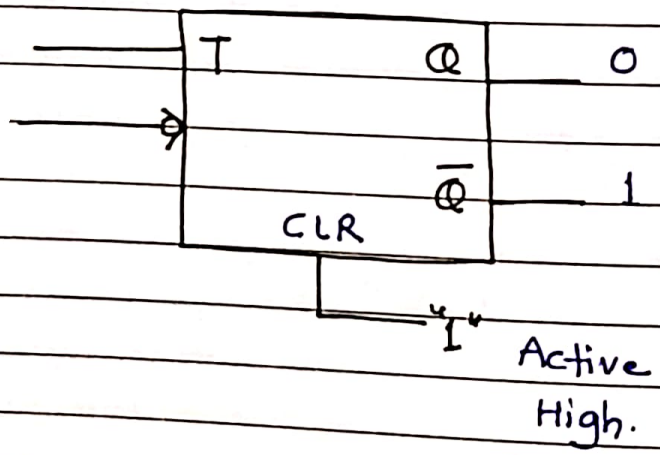
Concept of Overriding Input

① CLEAR / CLR → Active low / Active High

② PRESET / PRE → Active High / Active low.

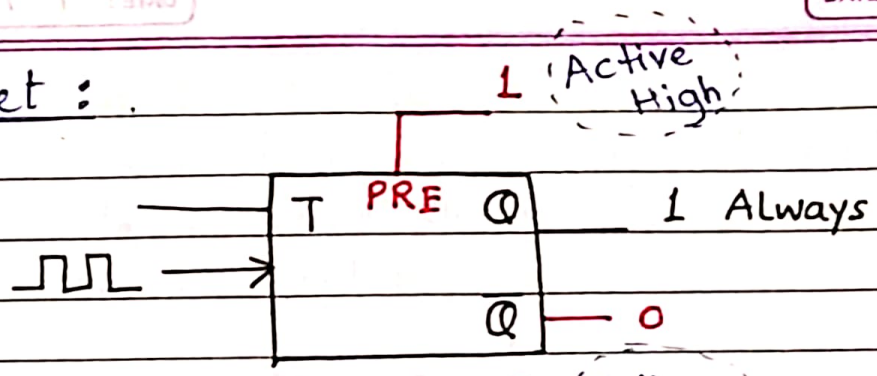


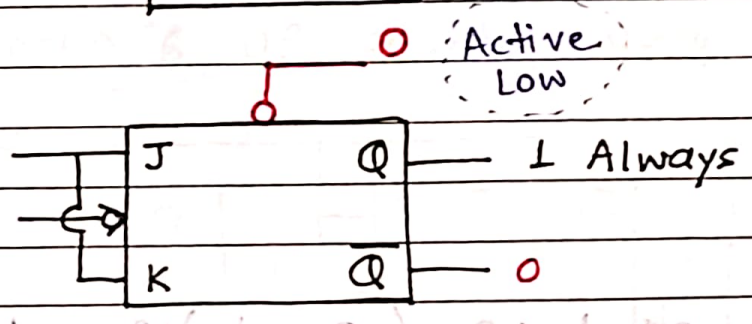


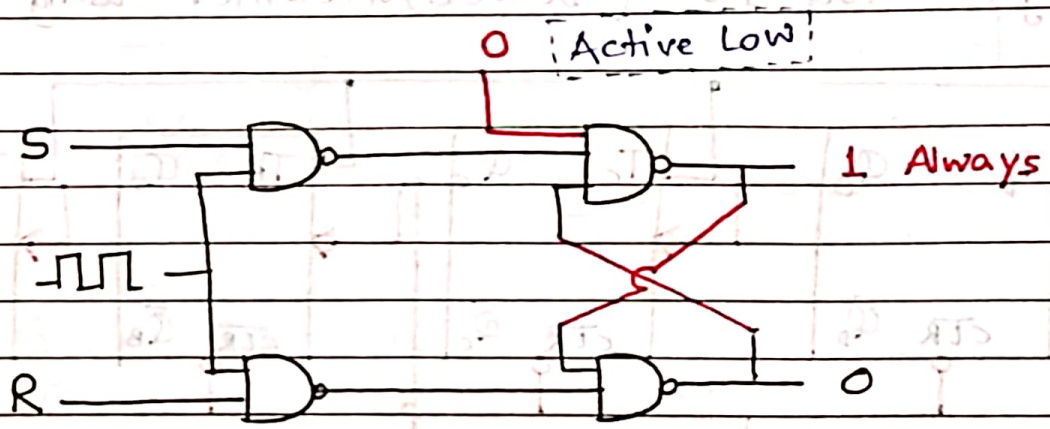


PAGE NO. :
DATE : / /

Preset :





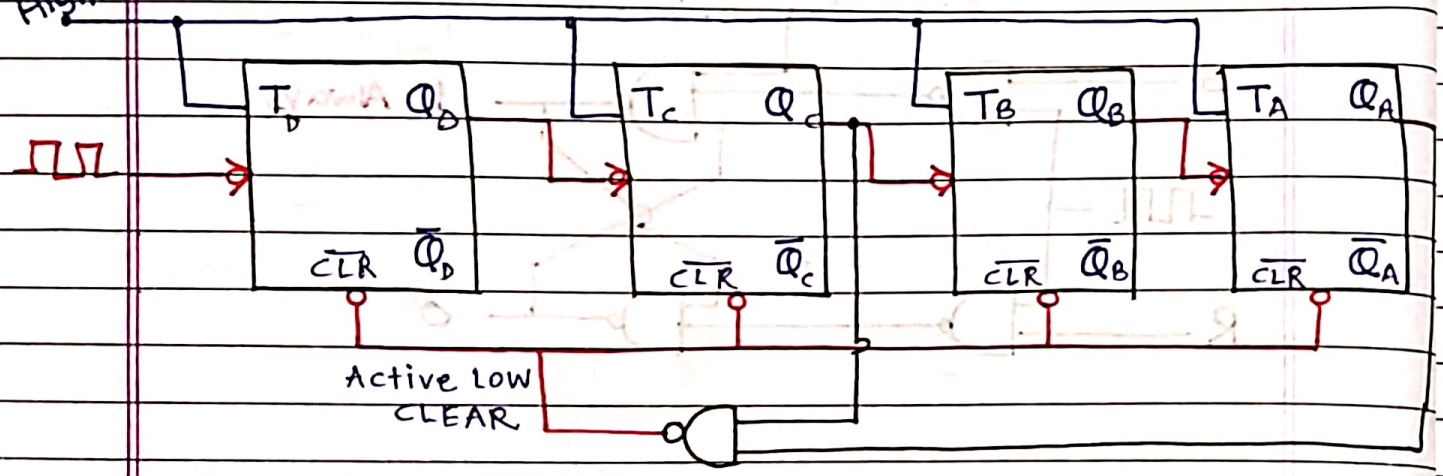


DESIGNING OF ASYNCHRONOUS COUNTER

- From the given data, find the modulus of the counter given.
- Determine the number of flip flop used.
- Write the desired sequence of the counter.
- Truncate / Break the sequence where ever needed using unique hardware design.

PAGE NO. :
DATE : / /

IMP Q.) Design Mod-10 (Decade) Upcounter using T-FF.



Initial

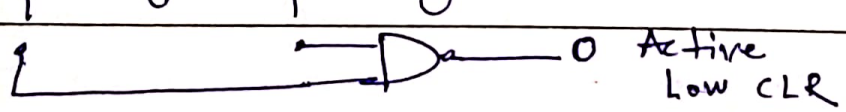
Q_A	Q_B	Q_C	Q_D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0

Desired Sequence.

V.V.IMP

IMP $f_{max} \leq \frac{1}{n.t_p + t_g + t_s}$

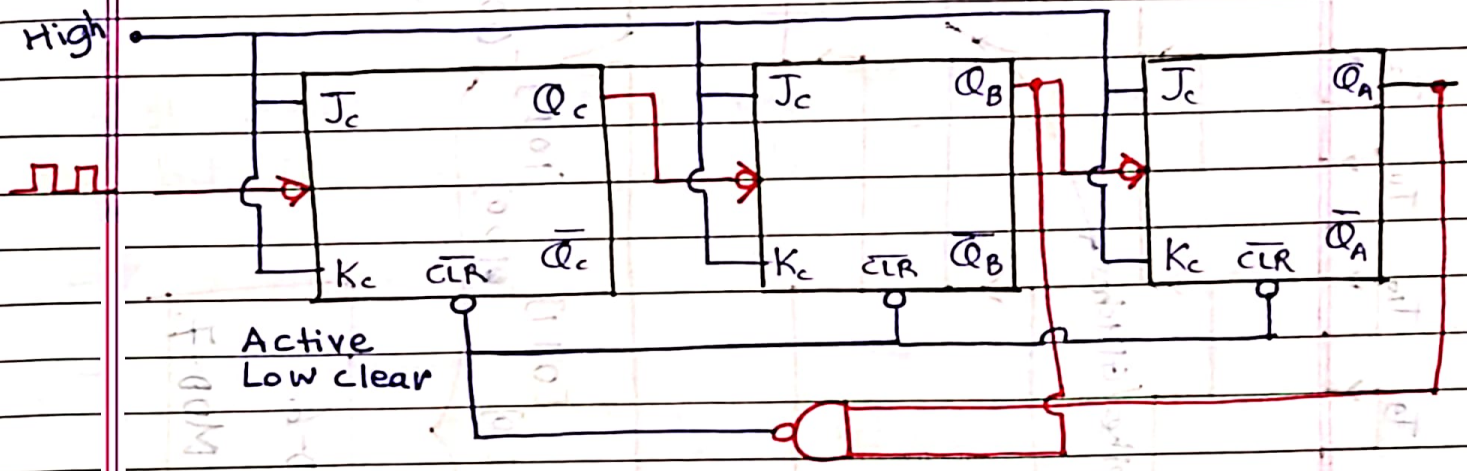
[Maximum clock frequency applied to the counter]



PAGE NO. :
DATE : / /

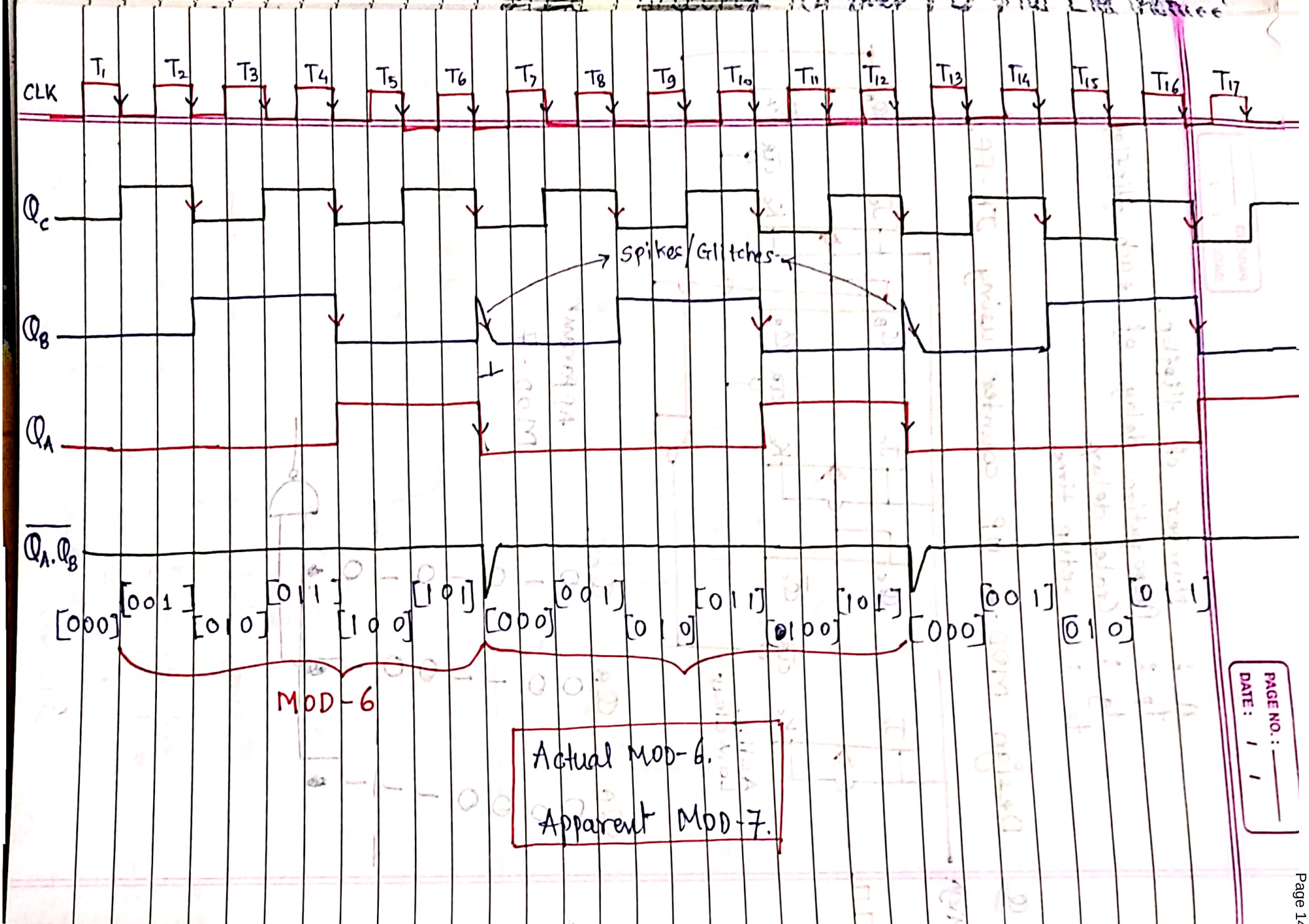
n : Number of flipflop.
t_p : Propogation delay of each flipflop.
t_g : Gate delay.
t_s : setup time

IMP Q Design MOD-6 UP counter using JK-FF.



	Q_A	Q_B	Q_C
Initial	0	0	0
	0	0	1
	0	1	0
	0	1	1
	1	0	0
	1	0	1
	1	1	0

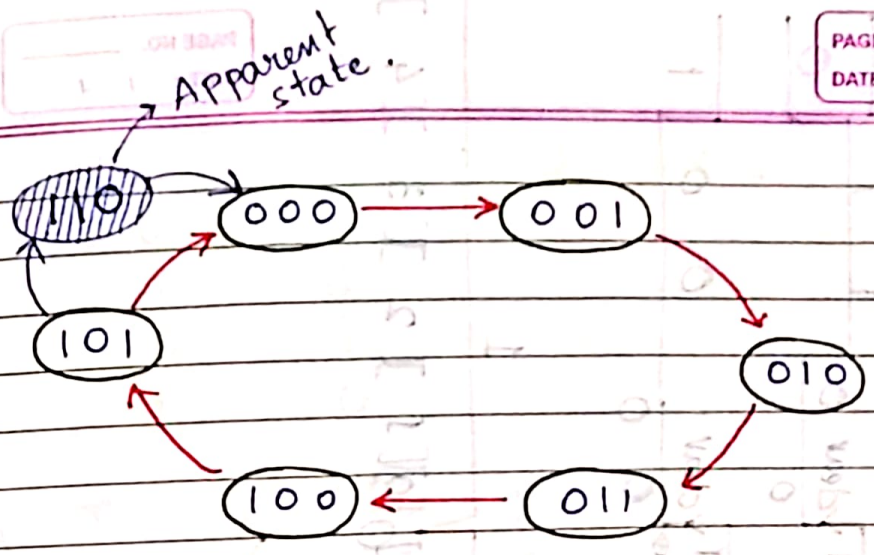
Apparant MOD-7.


CLK
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14 T15 T16 T17
Qc
QB
QA
Spikes/Glitches
[000] [001] [010] [011] [100] [101] [000] [001] [010] [011] [100] [101] [000] [001] [010] [011]
MOD-6
Actual MOD-6.
Apparent MOD-7.

PAGE NO. :
DATE : / /

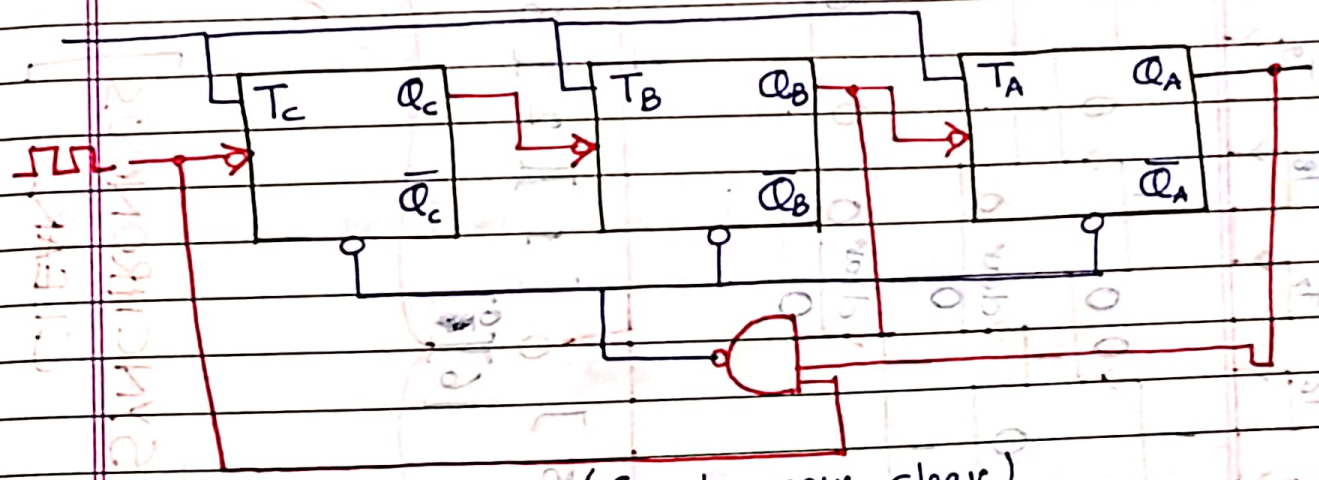
PAGE NO. :
DATE : / /

occuring for lesser time instant.



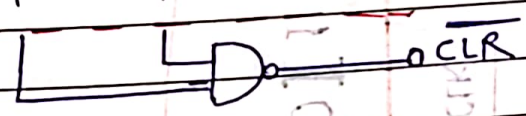
- It seems as if it is present in counter output but it occurs apparantly.

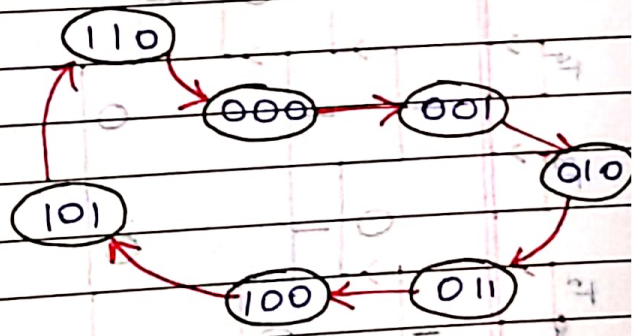
⇒ SYNCHRONOUS CLEAR, MOD-7 UP COUNTER.

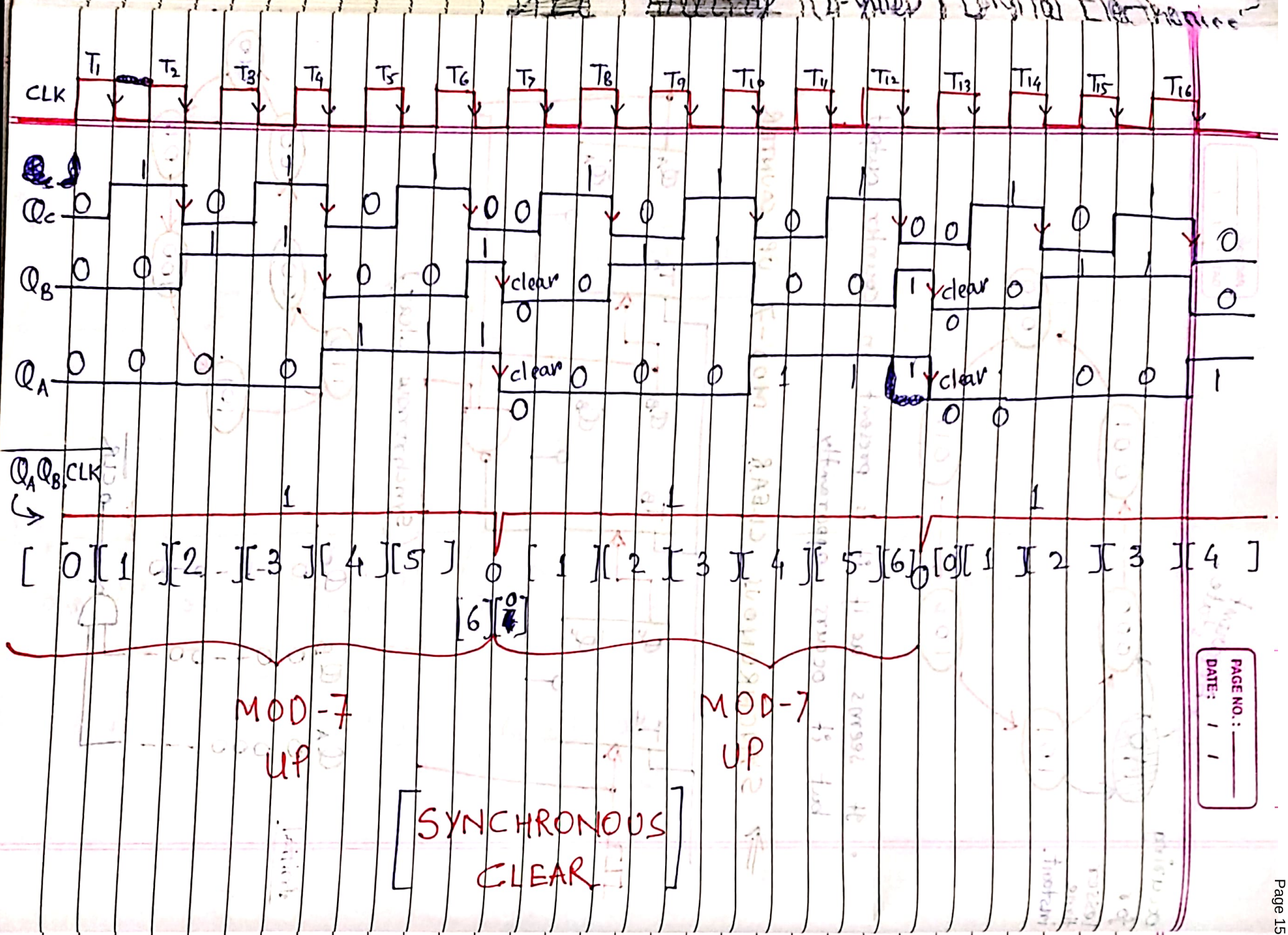


(Synchronous clear)

	Q_A	Q_B	Q_C
initial	0	0	0
	0	0	1
	0	1	0
	0	1	1
	1	0	0
	1	0	1
	1	1	0







Apoorv Panse, iGate Bhilai

apoorv135@gmail.com

PAGE NO. :
DATE : / /

Q

X Y	Q_{n+1}	J	K
0 0	1		
0 1	$\overline{Q_n}$		
1 0	Q_n		
1 1	0		

Q_n	J	K	Q_{n+1}	X	Y
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	0	1	1
1	1	0	1	0	0
1	1	1	0	0	1

For Q_{n+1}

Q_n \ XY				
	1	1	0	0
	1	0	0	1

$$Q_{n+1} = \overline{X}\,\overline{Q_n} + Q_n\overline{Y}$$

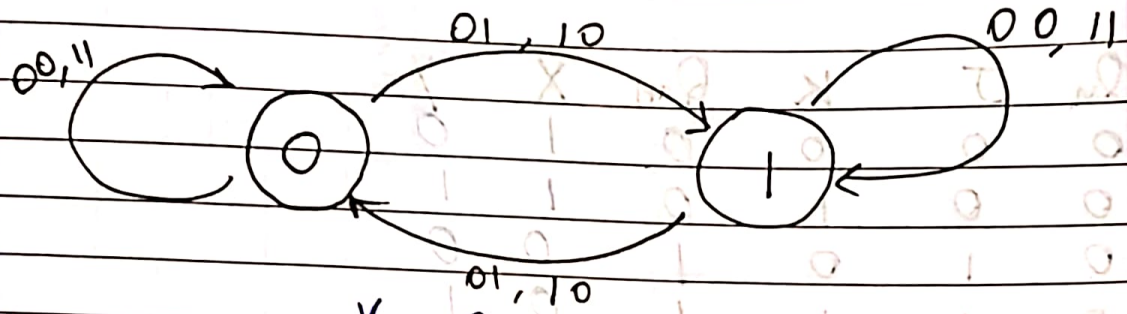
$$Q_{n+1} = J\,\overline{Q_n} + \overline{K}\,Q_n$$

$\therefore$ $J = \overline{X}$

$K = Y$.

PAGE NO. :
DATE : / /

Ex Consider the following state Diagram and its realization by JK flip flop. The combin-ational circuit generates J and K in terms of X, Y and Q. The boolean exp for J and K are.



Q_n	J	K	Q_{n+1}	X	Y
0	0	0	0	0	0
0	0	1	1	1	0
0	1	0	1	1	0
0	1	1	0	0	0
1	0	0	1	0	0
1	0	1	0	0	1
1	1	0	0	0	1
1	1	1	1	0	0

$JK \rightarrow XY$

for X

$Q_n \backslash XY$	00	01	11	10
0		1		1
1				

$J = Q_n(\overline{X}Y + X\overline{Y})$

for Y

$Q_n \backslash XY$	00	01	11	10
1		1		1

$K = Q_n(\overline{X}Y + X\overline{Y})$

$$\boxed{\begin{aligned} J &= X \oplus Y \\ K &= X \oplus Y \end{aligned}}$$

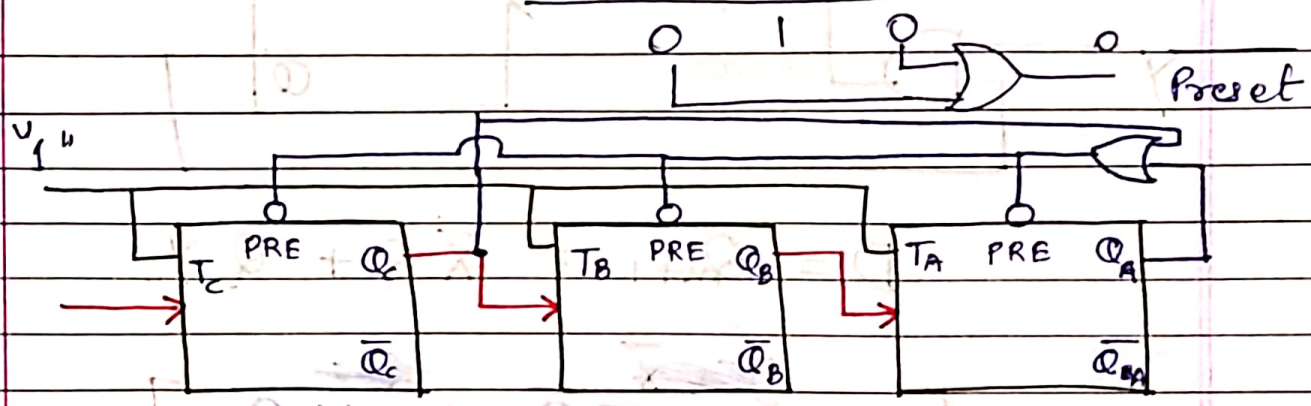
PAGE NO. :
DATE : / /

Ex Design MOD-5 Down Counter using T flipflop.

Desired output

MSB Q_A	Q_B	LSB Q_C
1	1	1
1	1	0
1	0	1
1	0	0
0	1	1
0	1	0

MOD-5



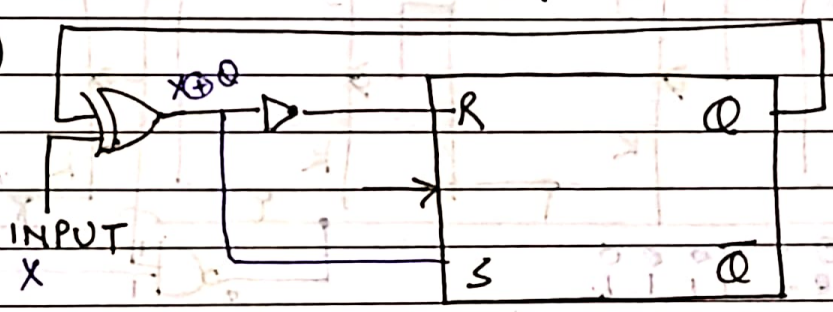
[MOD-5 DOWN with ASYNC PRESET.]

DLD Assignment Q.20 Homework

DLD

Which FF is this?

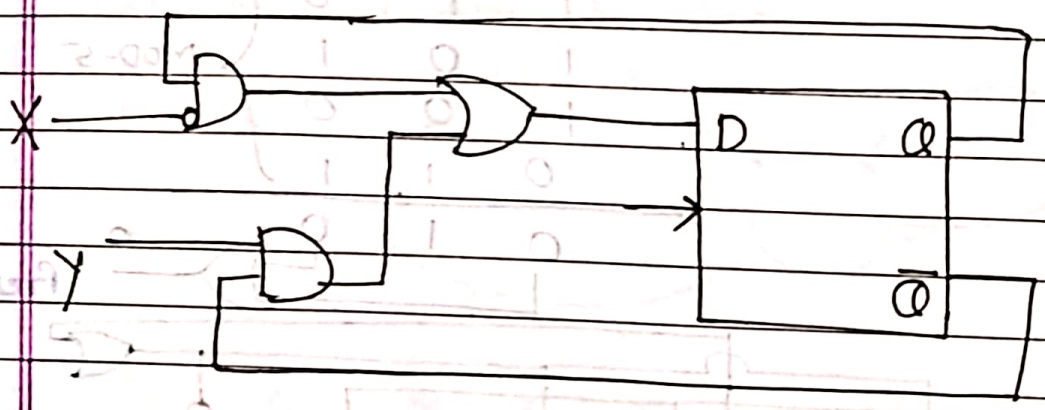
(Q)



$$Q_{n+1} = S + \overline{R}\, Q_n$$
$$= (X \oplus Q) + (X \oplus Q)\, Q_n$$
$$\Rightarrow X \oplus Q \quad \therefore \text{T-flip flop}$$

PAGE NO. :
DATE : / /

Q A seq circuit using D-FF and logic gates is shown in figure. XY are input, Z is output.

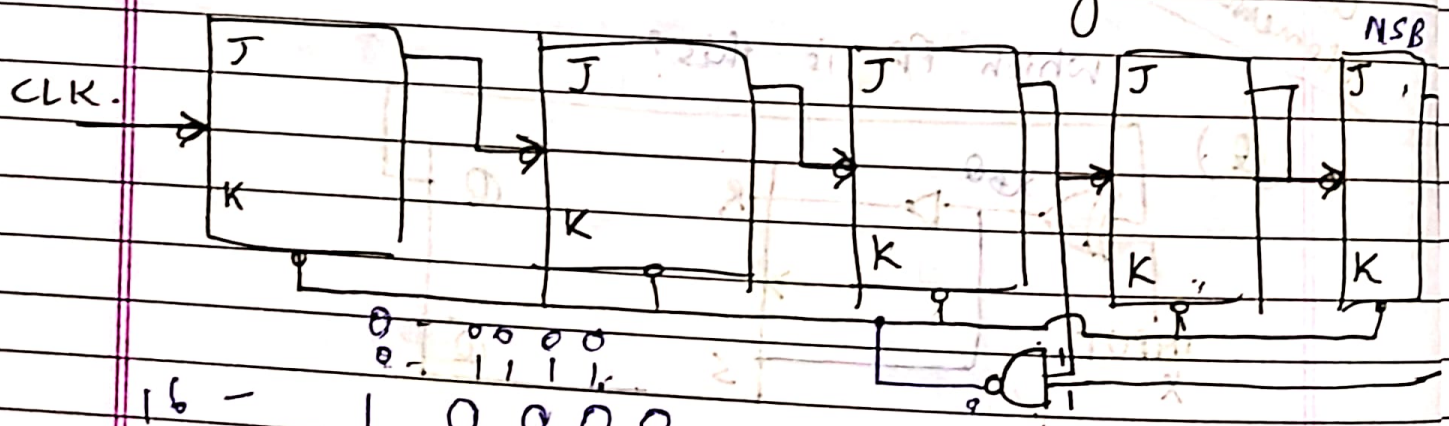


$$D = Q_{n+1} = \bar{X}Q + \bar{Q}Y$$

$$\boxed{Q_{n+1} = J\bar{Q}_n + K Q_n}$$

$J = Y \qquad K = X$ ✓

Q.2 Assume all J & K are High.



0 -	0	0	0	0	
8 -	1	1	1	1	
16 -	1	0	0	0	0
17	1	0	0	0	1
18 -	1	0	0	1	0
19 -	1	0	0	1	1
20 -	1	0	1	0	0 → Reset

0 to 19

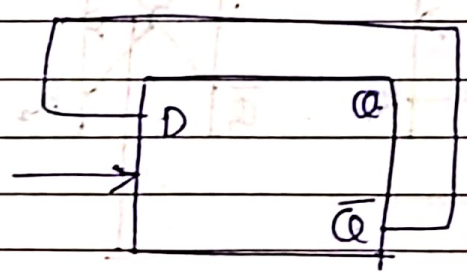
PAGE NO. :
DATE : / /

Q. Frequency of signal available at Q is 10 kHz. frequency of clock applied to rising edge triggered D-FF.

$$\frac{f_{clock}}{2} = f_{output}$$

2 → MOD

$$\therefore f_{clock} = 2 \times 10 = 20 \text{ kHz}$$



Truth table

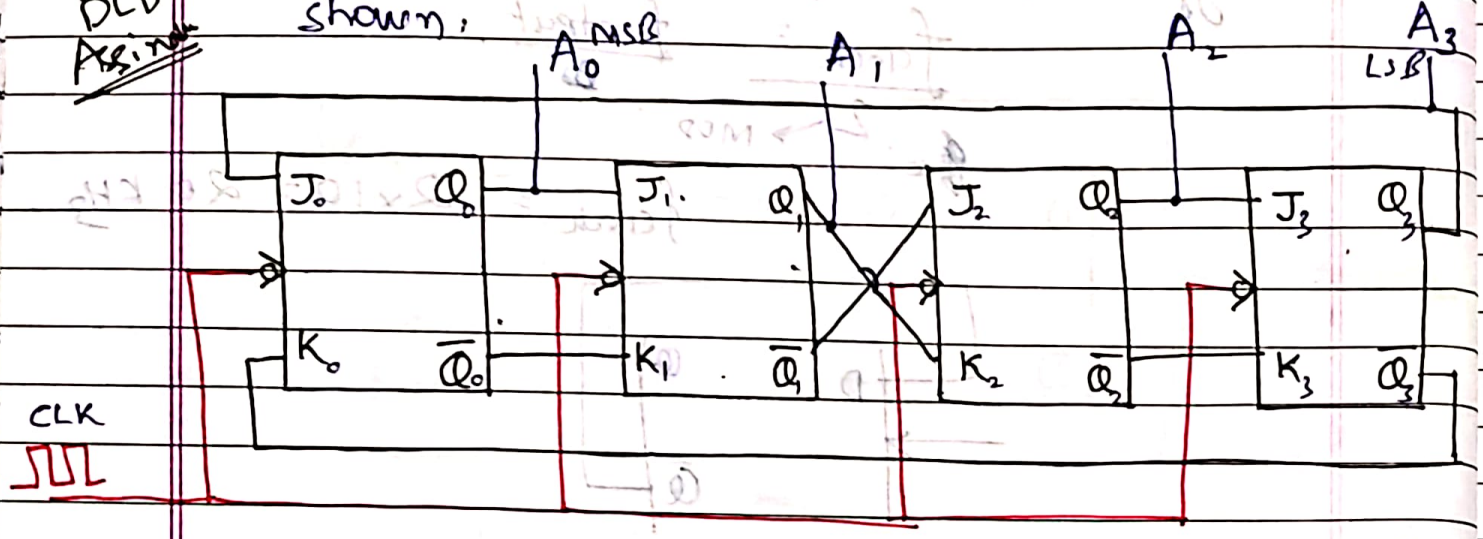
	Q	$\bar{Q}$	D	
Initial	1	0	0	} MOD-2
	0	1	1	
	1	0	0	
	0	1	1	

PAGE NO. :
DATE : / /

Ex Synchronous Counter

Q.65 DLD Assignment

A counter consist of 4 F-F connected as shown:



	A_0	A_1	A_2	A_3	$K_0=\bar{Q}_3$ $J_0=Q_3$	$K_1=\bar{Q}_0$ $J_1=Q_0$	$K_2=Q_1$ $J_2=\bar{Q}_1$	$K_3=\bar{Q}_2$ $J_3=Q_2$
Initial	0	1	1	0	01	01	01	10
0	0	0	0	1	10	01	10	01
2	1	0	1	0	01	10	10	10
3	0	1	1	1	10	01	01	10
4	1	0	0	1	10	10	10	01
5	1	1	1	0	01	10	01	10
6	0	1	0	1	10	01	01	01
7	1	0	0	0	01	10	10	01
8	0	1	1	0				

∴ MOD-8 Synchronous counter.

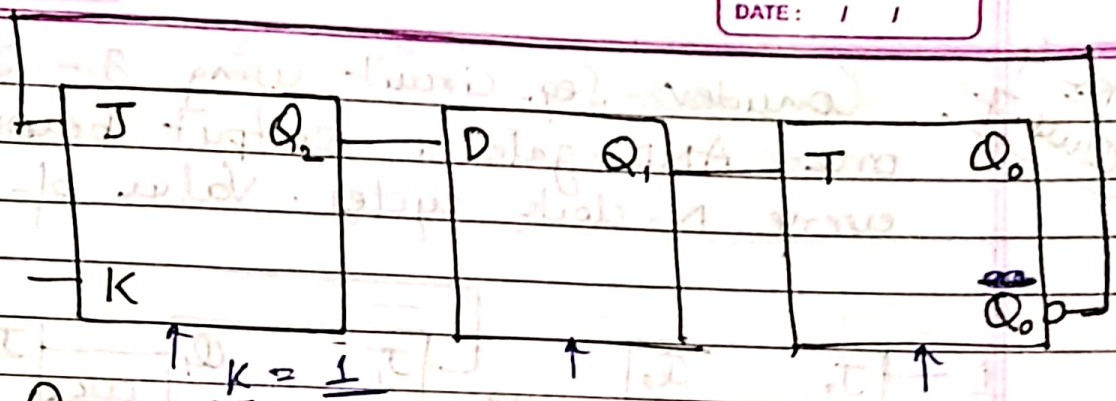
$$f_0 = \frac{f_{in}}{8}$$

output after 6th clock = 0101

output after $\underbrace{\text{next clock}}_{\text{after } 0110}$ = 0001

DLD-A

Q-25



$K = 1$

	Q_2	Q_1	Q_0	$J = Q_0$	$D = Q_2$	$T = Q_1$
Initial	0	0	0	11	0	0
1	1	0	0	11	1	0
2	0	1	0	11	0	1
3	1	0	1	01	1	0
4	0	1	1	01	0	1
5	0	0	0			

MOD-5 counter ✓

DLD-A

Q.24

Homework

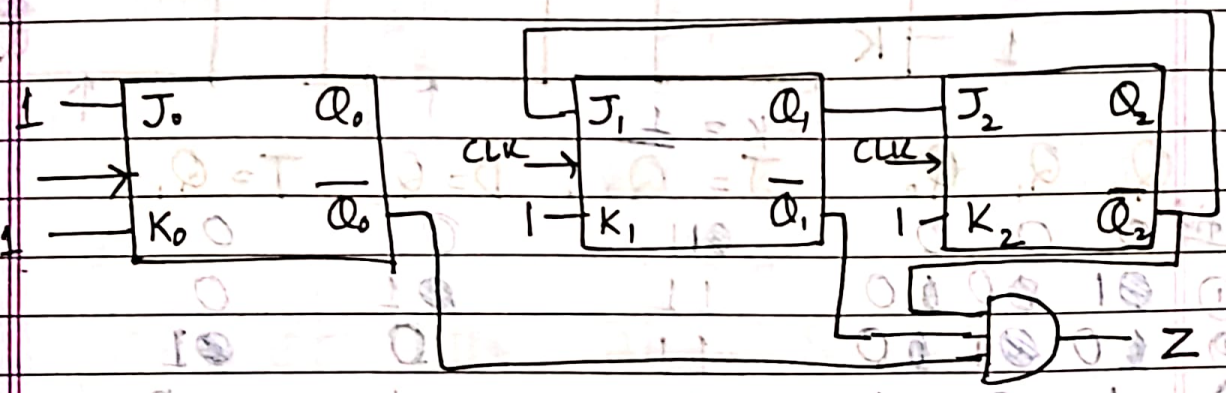
Q.) If a synch counter designed using J, K, D and T-FF having individual P.d of 25, 30 & 15 ns respectively. Then what is the Pd of the counter.

Ans 30

(Maximum of 3 values)

PAGE NO. :
DATE : / /

Ass 4
Ques. 7 Consider Seq. circuit using 3 - J.K FF and one AND gate. Output becomes 1 after every N-clock cycles. Value of N is.



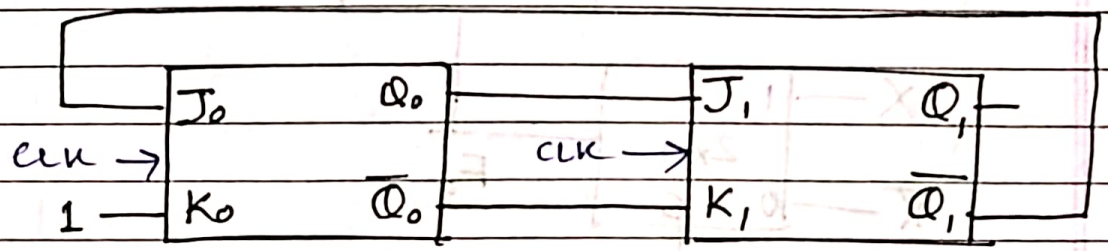
	Q_2	Q_1	Q_0	$K_0=1$ $J_0=1$	$K_1=1$ $J_1=\overline{Q_2}$	$K_2=1$ $J_2=Q_1$
initial	0	0	0	1 1	1 1	0 1
1	0	1	1	1 1	1 1	1 1
2	1	0	0	1 1	0 1	0 1
3	0	0	1	1 1	1 1	0 1
4	0	1	0	1 1	1 1	1 1
5	1	0	1	1 1	0 1	0 1
6	0	0	0			

MOD-6

After 6th clock N will be 1 ✓

PAGE NO. :
DATE : / /

Ass. 4 (11) Assume $Q_0 = Q_1 = 0$. then Q_0, Q_1 immediately after 33rd pulse are.



$K_0 = 1$ $K_1 = \overline{Q_0}$

	Q_0	Q_1	$J_0 = \overline{Q_1}$	$J_1 = Q_0$
Initial	0	0	1 1	0 1
1	1	0	1 1	1 0
2	0	1	0 1	0 1
3	0	0		

3rd clock – Repeat – MOD-3 counter.

∴ after 33rd pulse 00 ✓

4 Ass Q.13

4 Ass Q.12 A 4-bit mod-16 ripple counter uses J.K FF if P-delay of each FF is 50 ns, max clock freq = ?

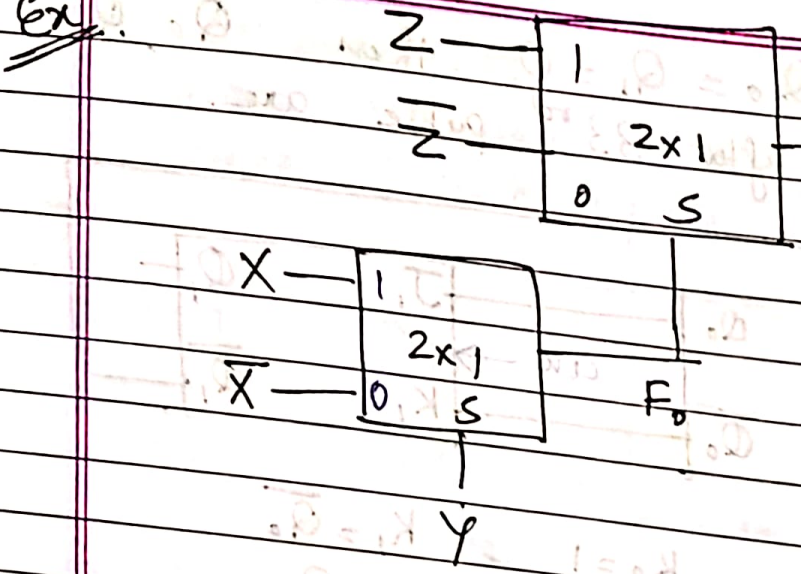
$$f_{max} = \frac{1}{4 \times 50 \times 10^{-9}} = \frac{1 \times 10^9}{200}$$

$$= 5 \times 10^6$$

5 MHz.

PAGE NO. :
DATE : / /

Ex.



$F_0 \; \overline{(X\bar{Y} + Y\bar{X})} = \overline{X \oplus Y}$.

$F_1 = \overline{(X \oplus Y)} \cdot \bar{Z} + \overline{(X \oplus Y)} Z$

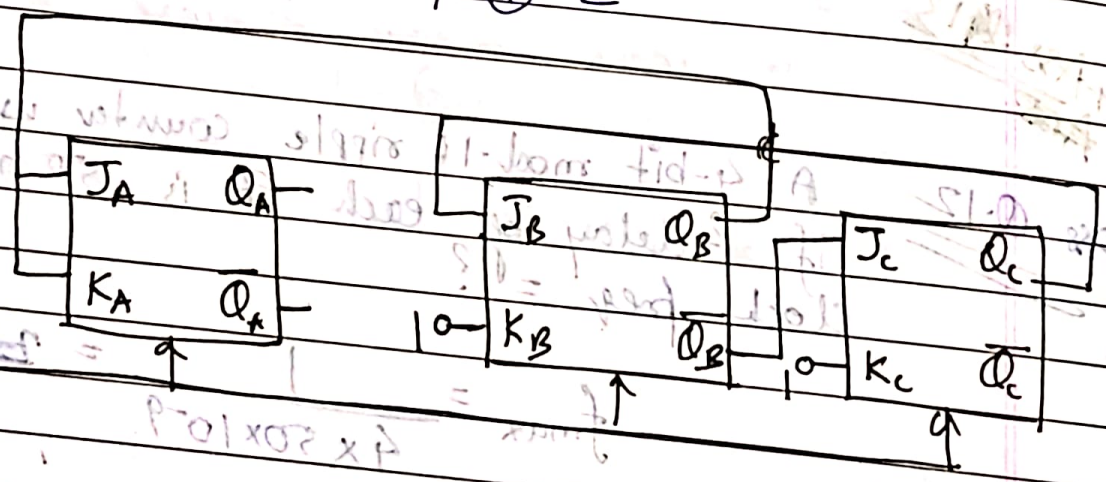
$F_1 = \cancel{X \oplus Y \oplus Z} \quad X \odot Y \odot Z$

$F_1 = \overline{X \oplus Y} \odot Z$

$F_1 = \overline{\overline{X \oplus Y} \oplus Z}$

DLD-A

Q-1



PAGE NO. :
DATE : / /

	Q_A	Q_B	Q_C	$J_A = K_A = Q_B$	$K_B = 1$, $J_B = Q_C$	$K_C = 1$, $J_C = \overline{Q_B}$
Initial	0	0	0	00	01	11
	0	0	1	00	11	11
	0	1	0	11	01	01
	1	0	0	00	01	11
	1	0	1	00	11	11
	1	1	0	11	01	01
	0	0	0			

Mod-6 ∴ 2 unused states

Notes wrt Synchronous Counter

- In synchronous counter, clock pulse is provided to each and every flip-flop.
- All flip flops work parallely.
- By looking at the behaviour of clock signal we cannot comment on its working (UP/DWN)
- Over all propogation Delay in parallel counter = propogation delay of single flip-flop.

$$T_{Delay} = n \cdot t_{p.D}$$

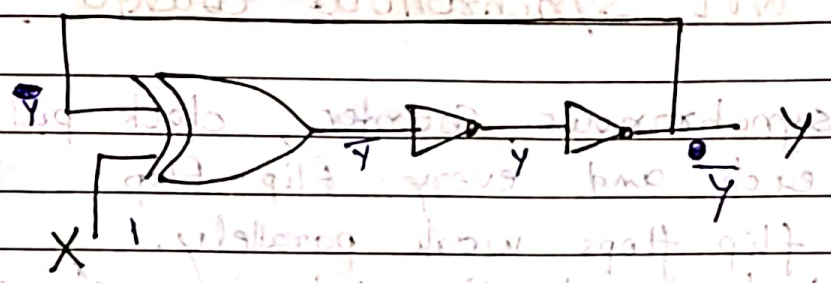
↳ Always 1.

PAGE NO. :
DATE : / /

Ex For Asynchronous counter consisting of 3-ff (JK, FF) and Pd of 30 ns. What is the Pd of counter

$$\therefore T_{Pd} = n \cdot t_{pd}$$
$$= 3 \times 30$$
$$= 90 \text{ ns}$$

Ex All gates have finite Pd. this can be used as clock generator.



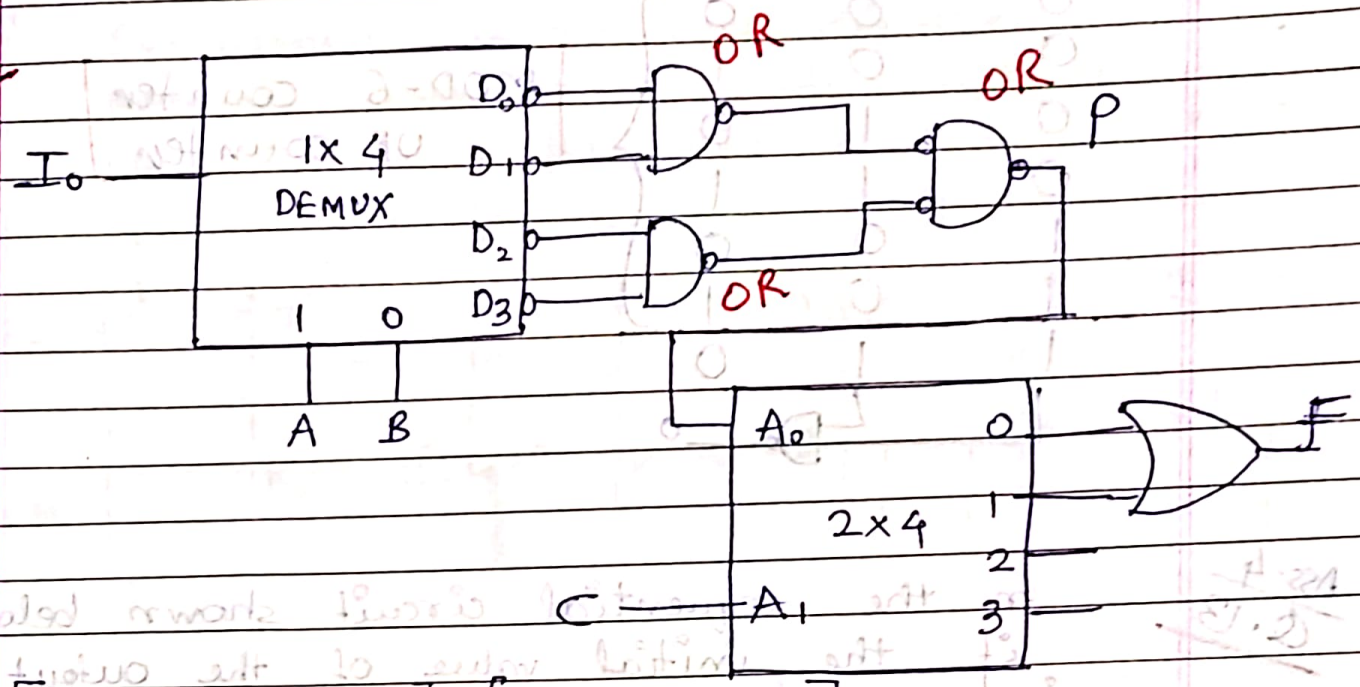
Considering X = 1 it is acting as clock, for other, it is acting as latch.

Ass. 3
Q. 10
Homework

PAGE NO. :
DATE : / /

Home Works

DLD-A
Q. 20



$P = [\bar{A}.\bar{B} I_0 + \bar{A} B I_0] + [A\bar{B} I_0 + A B I_0]$

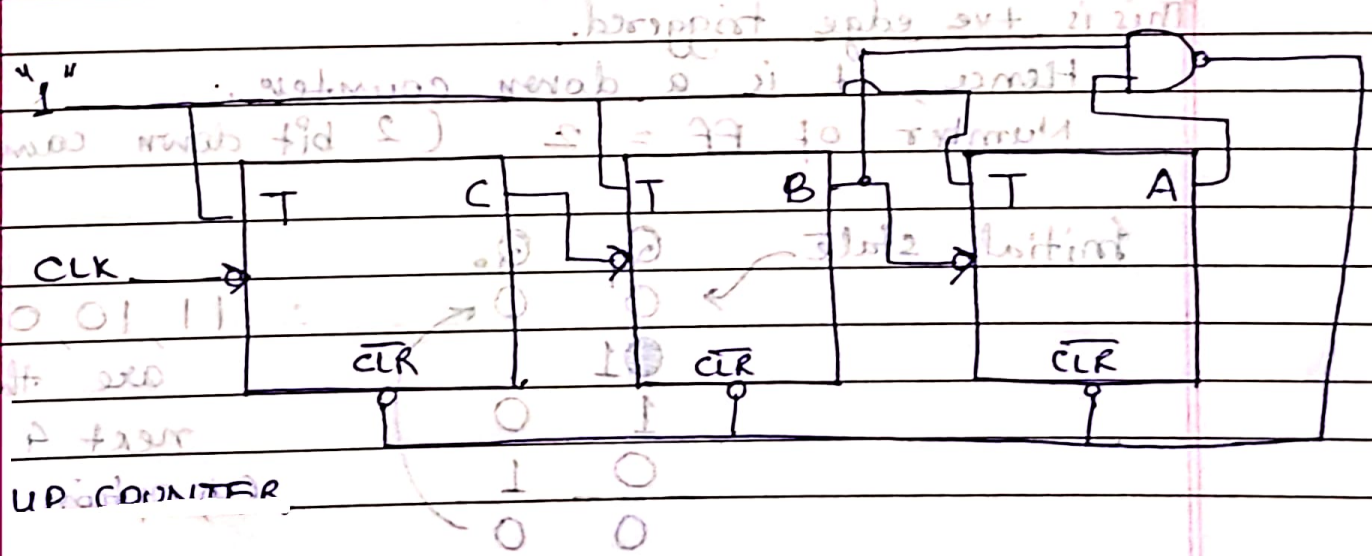
$P = I_0$

$F = \bar{C}\bar{A}_0 + \bar{C}A_0$

$\boxed{F = \bar{C}}$ ✓

∴ (a) option

DLD-A
Q. 24 Modulus value of below asynchronous counter is

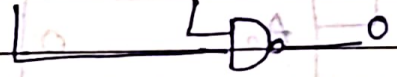


UP COUNTER

PAGE NO. :
DATE : / /

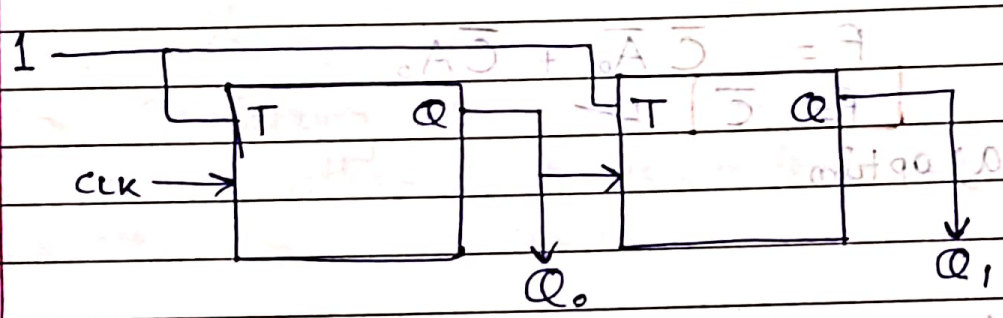
A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0

MOD-6 counter
UP counter



ASS-4
Q.13

In the sequential circuit shown below, if the initial value of the output Q_1Q_0 is 00 what are the next four values of Q_1Q_0 ?



This is +ve edge triggered.
Hence, it is a down counter.
Number of FF = 2 (2 bit down counter)

Initial state → Q_1 Q_0

Q_1	Q_0
0	0
1	1
1	0
0	1
0	0

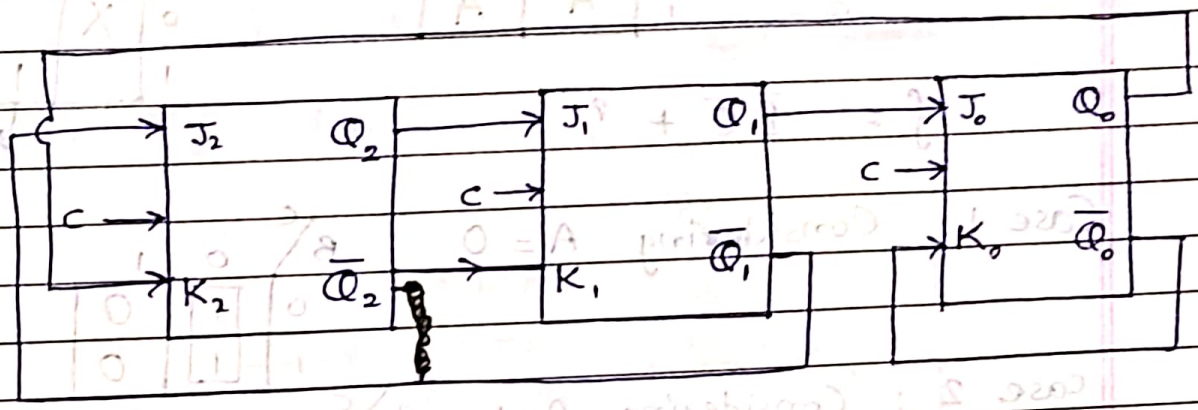
∴ 11, 10, 01, 00 are the next 4 states

(a) option

PAGE NO. :
DATE : / /

Ass. 2

Q. 10 Synchronous counter uses JK flip flops with ~~propagation delay~~ initial state $Q_2 Q_1 Q_0 = 000$. The state seq for next 3 clock cycles is.



	Q_2	Q_1	Q_0	$J_2 = \bar{Q}_1$, $K_2 = Q_0$	$J_1 = Q_2$, $K_1 = \bar{Q}_2$	$J_0 = Q_1$, $K_0 = \bar{Q}_0$
Initial	0	0	0			
1	1	0	0	10	01	01
2	1	1	0	10	10	01
3	1	1	1	00	10	11

∴ Ans. [Option C] 100, 110, 111.

PAGE NO. : _____
DATE : / /

Q. Find the simplified function for the given K-MAP.

B \ C	0	1
0	1	0
1	$\bar{A}$	A

B \ C	0	1
0	X	
1		1

B \ C	0	1
0	X	1
1		

$\bar{A}\bar{C}$

ABC

$f = \bar{B}\bar{C} + ?$

Case 1: Considering $A = 0$

B \ C	0	1
0	1	0
1	1	0

$\bar{A}.\bar{C}$

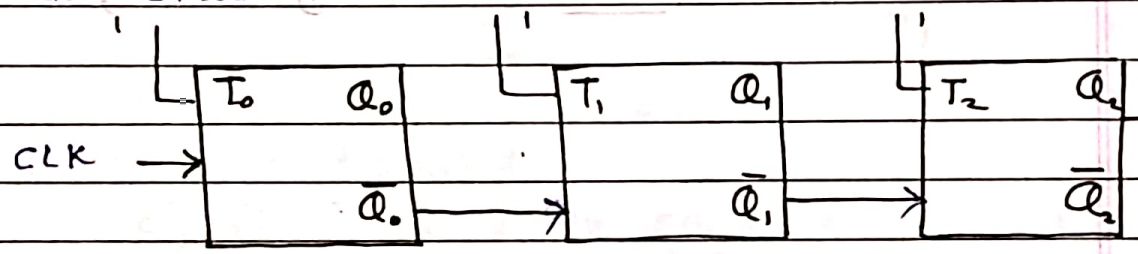
Case 2 : Considering $A=1$,

B \ C	0	1
0	1	
1		1

$A(\bar{B}\bar{C}+BC)$

$f = \bar{B}C + \bar{A}\bar{C} + ABC$ ✓

ASS-3 **Q.8** Figure shows a ripple counter using positive edge triggered ff. Present state $Q_2Q_1Q_0 = 011$ then next state is ?



Rising edge and $\bar{Q}$ ∴ UP counter.

(a) 010 (b) 100 (c) 111 (d) 101

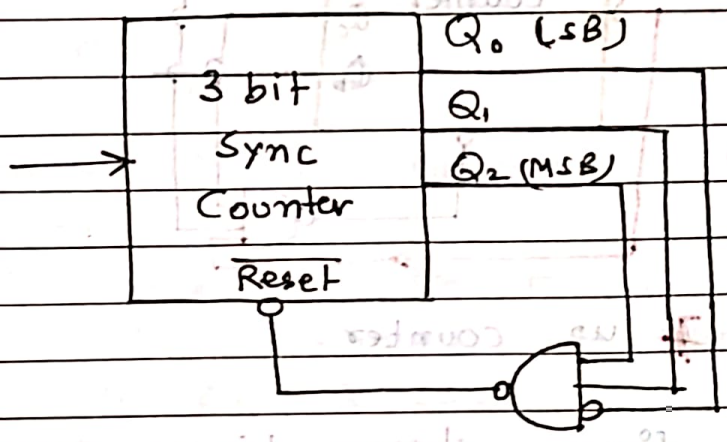
Very Good Ques

PAGE NO.:
DATE: / /

Q.) For a circuit shown in the figure, the delay of bubbled NAND gate is 2 ns and that the counter is assumed to be zero. If the clock frequency is 1 GHz. Then the counter behaves as.

(a) MOD-5 (b) MOD-6 (c) MOD-7 (d) MOD-8.

⇒ $f_c = 1 \times 10^9$ Hz. ∴ $t_c = 1$ ns. ∴



110.

Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	1
1	1	0
1	1	1

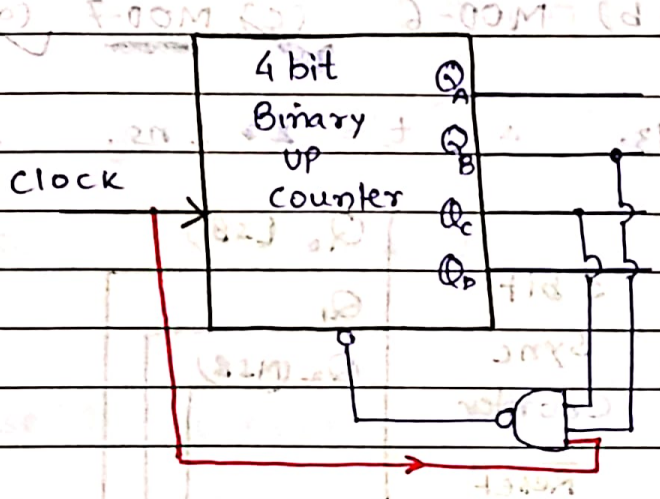
1ns

1ns

After 2ns

PAGE NO. :
DATE : / /

Ex The MOD-N counter using Sync - Binary UP counter, with synchronous - clear input shown in the figure the value of N is ?



Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0

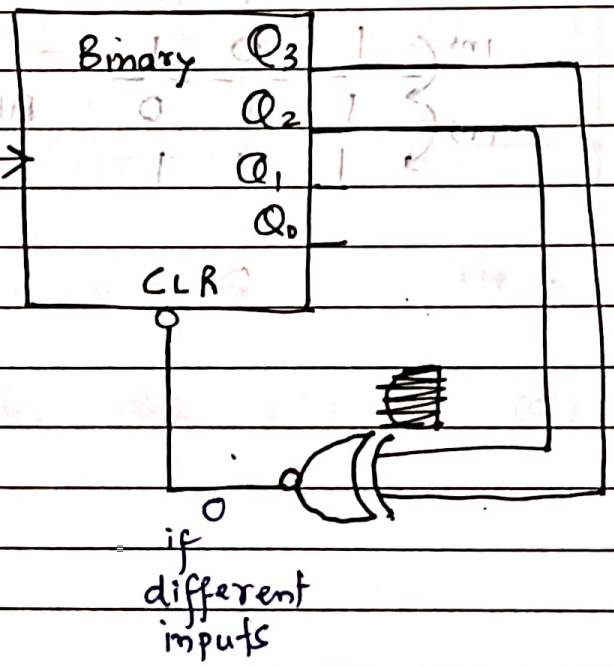
MOD-7 up counter.

Ex The figure shown binary counter with sync-clear input with the decoding logic shown. the counter works as.

(a) MOD-2 (b) MOD-4 (c) MOD-5 (d) MOD-6.

Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	1	1
0	1	0	0

4
-1
5



MOD-5

PAGE NO. :
DATE : / /

Ex A 4 bit ripple counter and 4 bit Sync counter are made using Propogation delay of 10 ns each. For the worst case delay in ripple counter and synch counter be R & S respectively. then

(a) R = 10 ns S = 40 ns
✓ (b) R = 40 S = 10
(c) R = 10 S = 30
(d) R = 30 S = 10.

Ex A pulse train with a frequency of 1 MHz is counted using modulo - 1024 ripple counter. Build using JK flipflop. For the proper operation of the counter the maximum permissible propogation delay per flip flop is ___ ns.

Ans 10 FF → 1 ms. → 10 ms → 100 ns

$$\boxed{f_c = \frac{1}{n\, t_p}}$$

Ex A 4-bit mod-16 ripple counter uses JK flip flop if the prop delay of each ff is 50 ns, the max clock frequency that can be used = ?

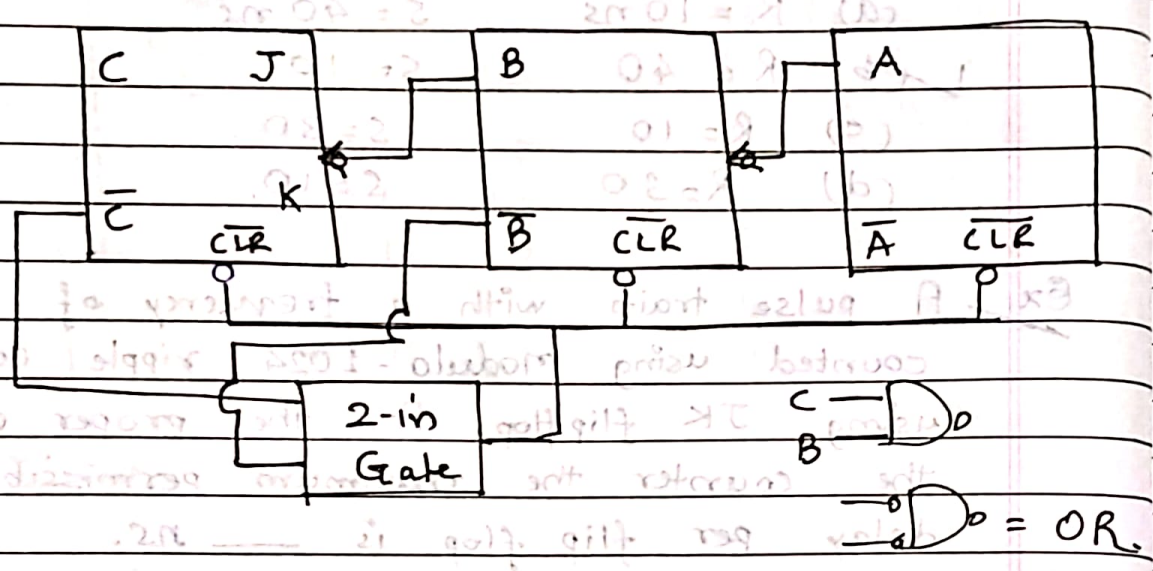
$$f_c = \frac{1}{200} \times 10^9 = 5 \times 10^6$$

$$f_c = 5\ MHz.$$ ✓

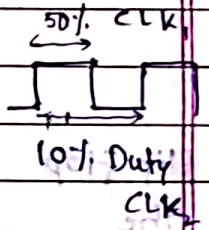
PAGE NO. :
DATE : / /

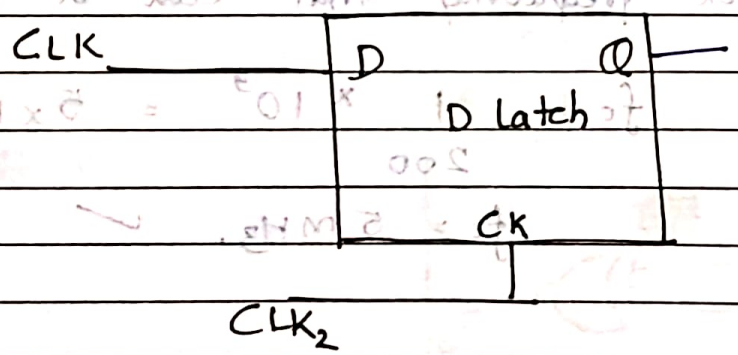
Ex In a mod-6 ripple counter shown in the figure below, the output of 2-input gate is used to clear the JK flip flop. The two input gate is ?

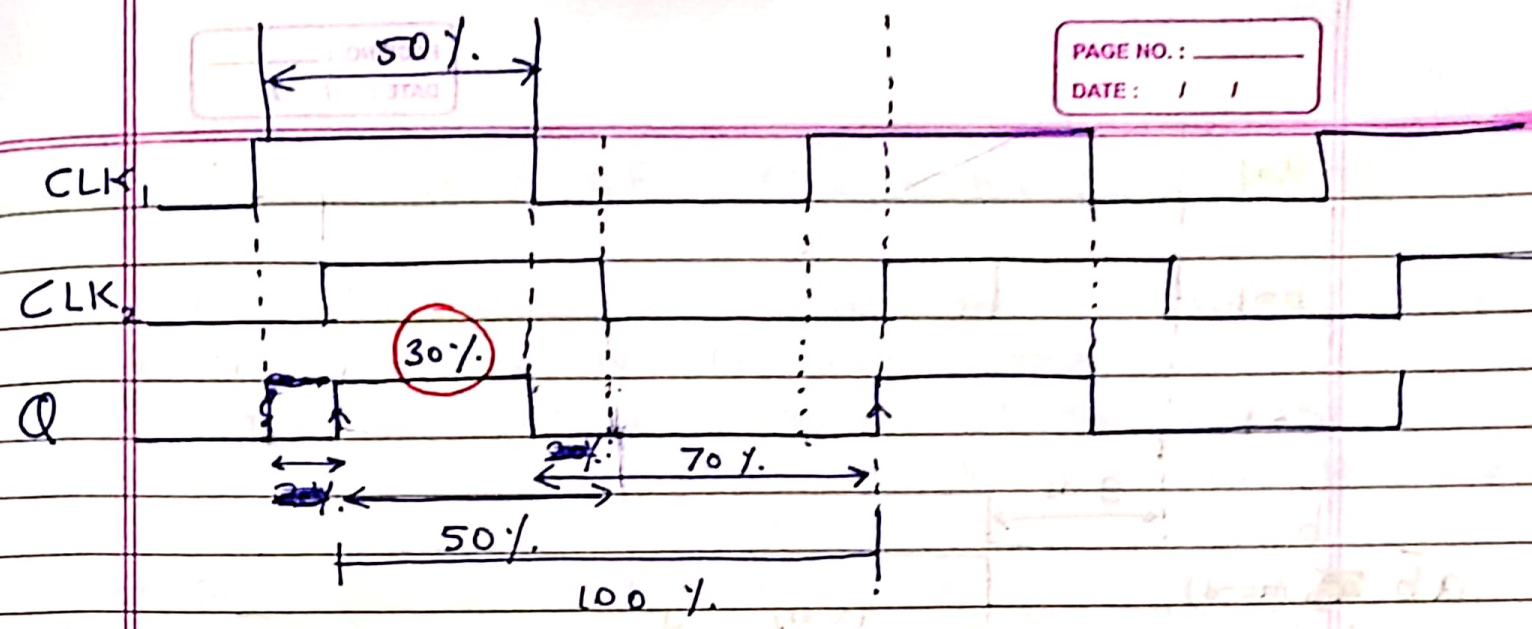
(a) NAND (b) NOR (c) OR (d) AND



Ex Consider the D-Latch shown in figure, which is transparent when its clock input clk is high, and has zero propogation delay. In the figure the clock signal, CLK, has 50% duty cycle. and CLK_2 is 1/5th period delay, version of CLK_1. The duty cycle at the output of the latch

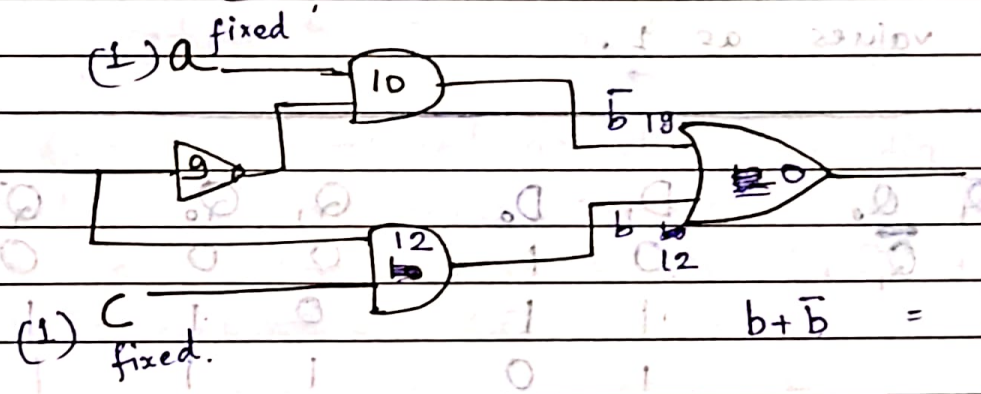






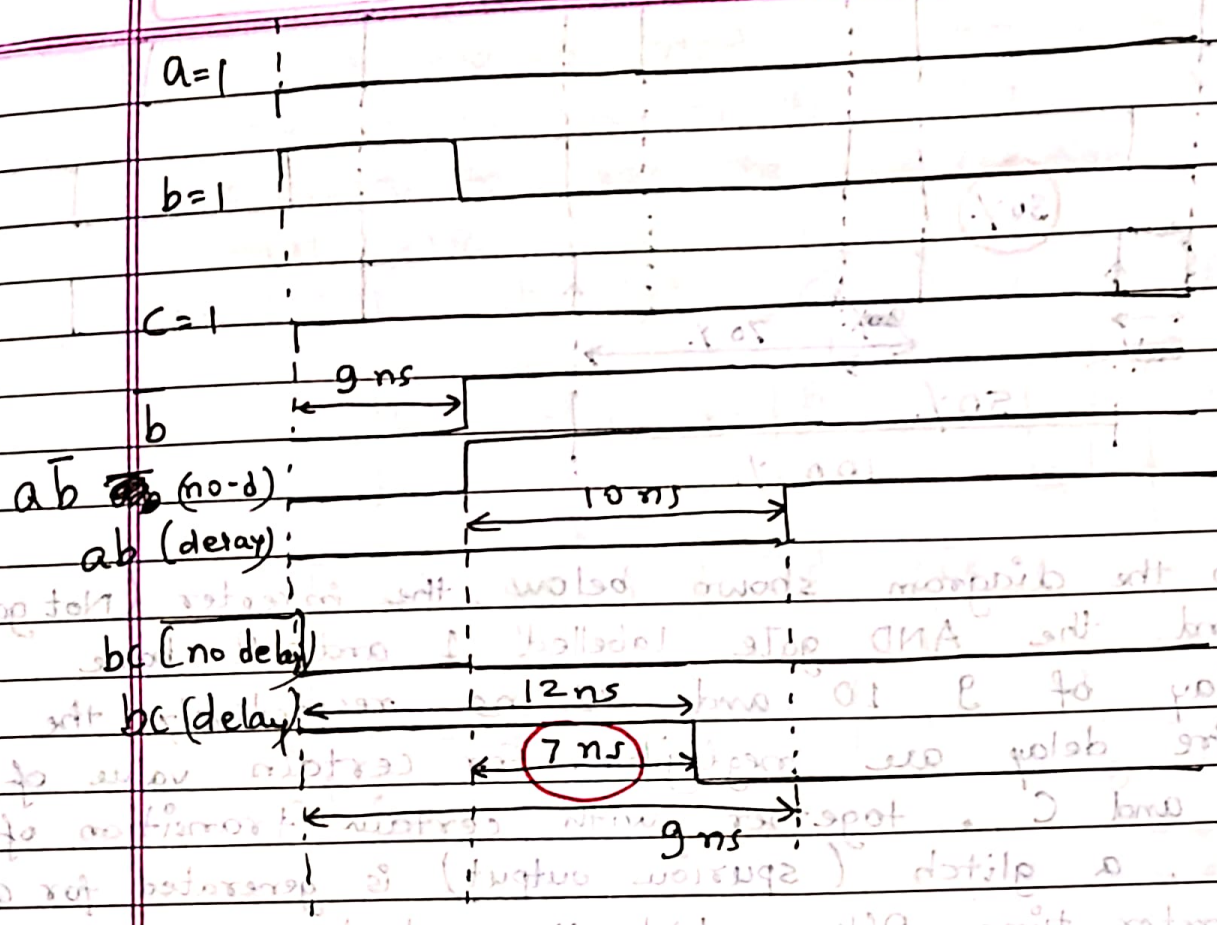
Ex In the diagram shown below, the inverter (Not gate) and the AND gate labelled 1 and 2 have delay of 9, 10 and 12 ns respectively, the wire delay are negligible. For certain value of A and C, together with certain transition of B, a glitch (spurious output) is generated for a shorter time. After which the output assume its correct value. The duration of the glitch is,

(a) 7ns (b) 9ns (c) 11ns (d) 13 ns



$b + \bar{b} = 1$

PAGE NO. :
DATE : / /



- If a & c are 0, output of OR gate is always zero (No Glitch)
- That means we need to consider a & c both values as 1.

(a) $\bar{Q}_1$ $\bar{Q}_0$ Q_0

(b) $\bar{Q}_0$ $\bar{Q}_1$

D_1	D_0	Q_1	Q_0	Q_1^+	Q_0^+
0	1	0	0	0	1
1	1	0	1	1	1
1	0	1	1	1	0
0	0	1	0	0	0

$Q_1 \backslash Q_0$	0	1
0	0	1
1	0	1

$D_1 = Q_0$

$Q_1 \backslash Q_0$	0	1
0	1	1
1		

$\bar{Q}_1$ Q_0

$D_0 = \bar{Q}_1$

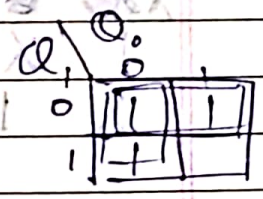
PAGE NO. :
DATE : / /

DESIGNING OF SYNCHRONOUS COUNTER

- From the Given data find the MODULUS of counter
- Find the No of FF used, ~~Write~~
- Write the present sequence of the counter.
- Parallel to this column, write the next sequence of the counter.
- Do mapping corresponding to given FF.

DLDA Ex Q.46 The next state table of a 2 bit saturating UP-counter is given below :

T_1	T_0	Q_1	Q_0	Q_1^+	Q_0^+
0	1	0	0	0	1
1	1	0	1	1	0
0	1	1	0	1	1
0	0	1	1	1	1

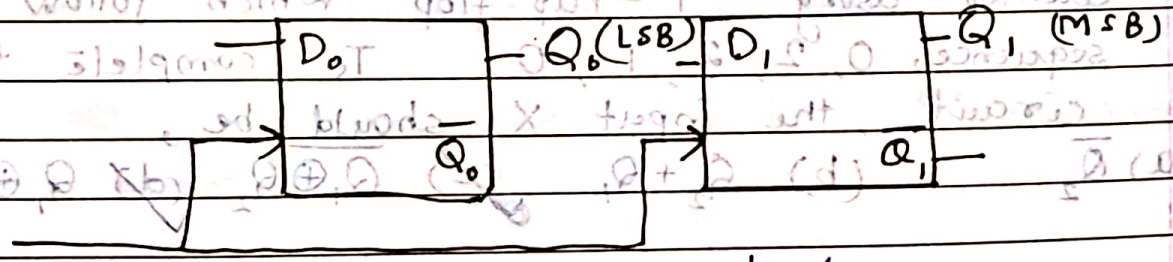


$$T_1 = \overline{Q_1}\, Q_0 \qquad T_2 = \overline{Q_0} + \overline{Q_1}$$

$\therefore$ option B is correct.

Ex. Two D flip-flop connected as shown in figure, Connected as synchronous counter that goes through the following sequence of $Q_1 Q_0$

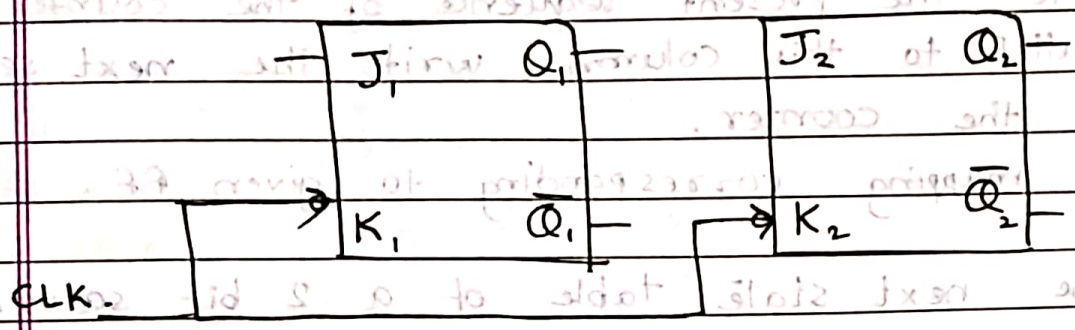
$00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00$



The in-put D_0 and D_1 respectively are.

PAGE NO. :
DATE : / /

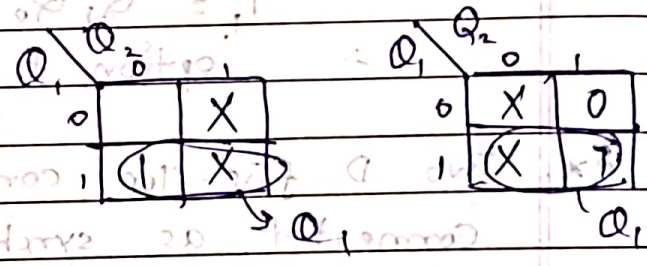
DLD-A Q. 68 A Synchronous counter using two JK ff that goes through the seq. Q_1Q_2 = 00 → 10 → 01 → 11 → 00 is required. To achieve this, inputs required are



J_1	K_1	J_2	K_2	Q_1	Q_2	Q_1^+	Q_2^+
1	X	0	X	0	0	1	0
X	1	1	X	1	0	0	1
1	X	X	0	0	1	1	1
X	1	X	1	1	1	0	0

$J_1 = 1$ $K_1 = 1$ $J_2 = Q_1$ $K_2 = Q_1$

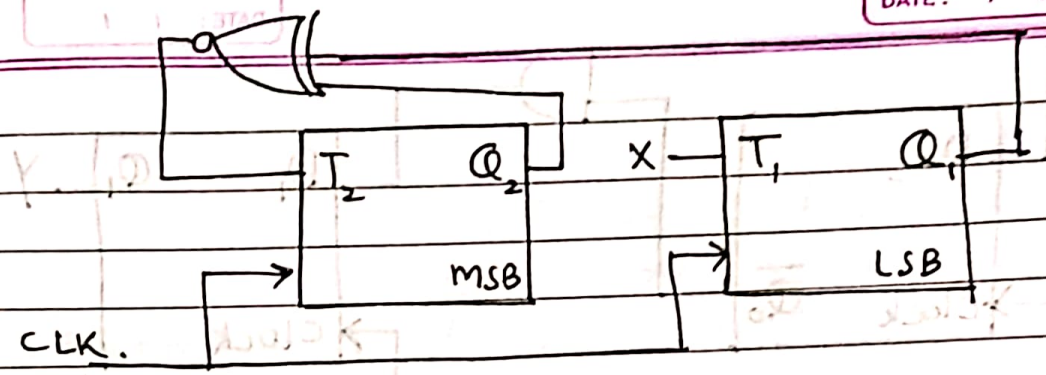
[option B]



Gate 2004 Consider the partial implementation of 2 bit counter using T-flip-flop. Which follow a sequence, 0, 2, 3, 1, 0 To complete the circuit, the input X should be,

(a) $\overline{Q_2}$ (b) $Q_2 + Q_1$ (c) $\overline{Q_1 \oplus Q_2}$ (d) $Q_1 \oplus Q_2$

PAGE NO. :
DATE : / /



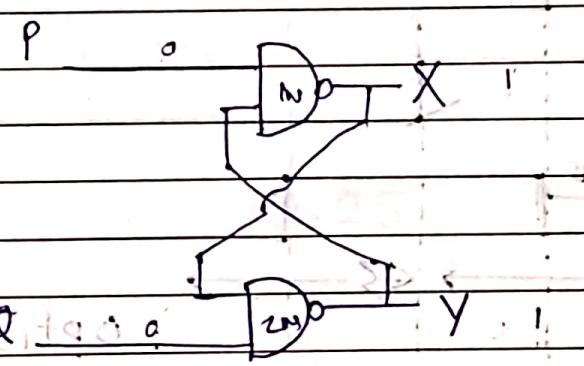
T_2	T_1	Q_2	Q_1	Q_2^+	Q_1^+
1	0	0	0	1	0
0	1	1	0	1	1
1	0	1	1	0	1
0	1	0	1	0	0

$T_1 =$

$Q_2 \backslash Q_1$	0	1
0	0	1
1	1	0

$= Q_1 \oplus Q_2$

Ex

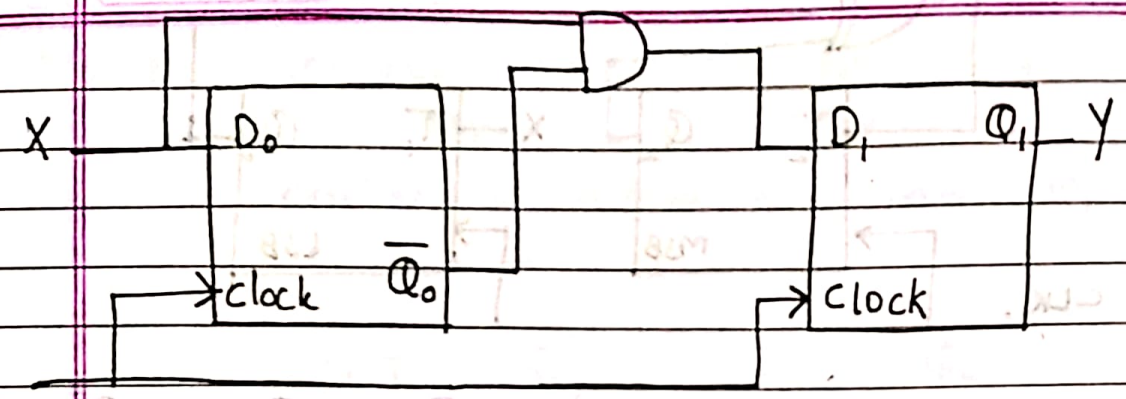


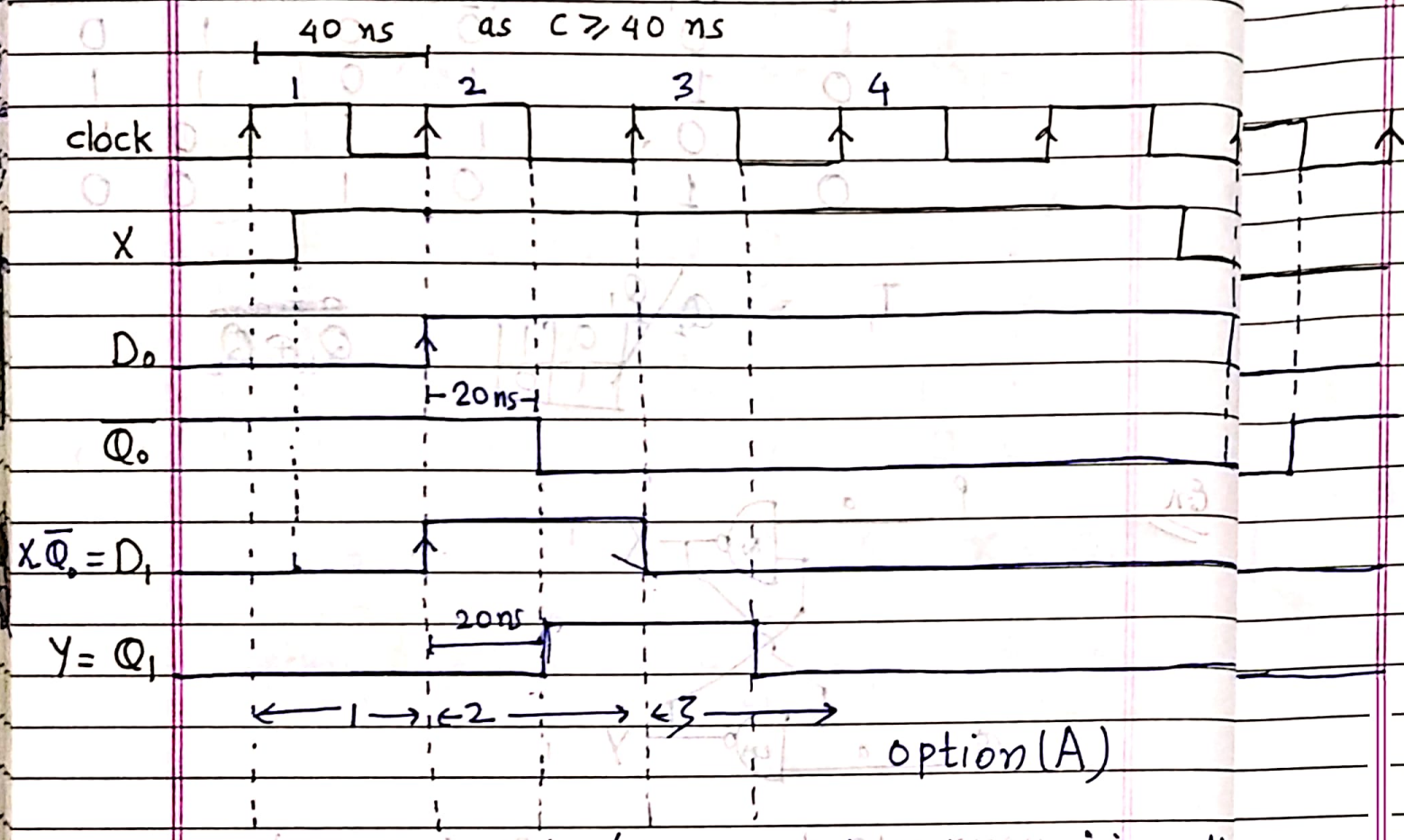
NAND gates have non-zero Pd: (unequal)

Initial $P = Q = 0$ If input is changed simultaneously to $P = Q = 1$ The outputs are

$\Rightarrow$ 0,0 input case is not stable as inputs are changed

PAGE NO. :
DATE : / /





option (A)

D_0 and D_1 works/changes state only on rising edge

$\overline{Q_0}$ is same as $\overline{D_0}$, but with 20ns delay
i.e shift $\overline{D_0}$ 20ns to right side

Q_1 is same as D_1, but with 20 ns delay.
i.e shift D_1 20 ns right side.

Also, $D_0 = X$
$D_1 = X \cdot \overline{Q_0}$

PAGE NO. :
DATE : / /

Two's compliment of Positive Number = same as binary value

2's compliment of 5 = 101

Two's compliment of negative number is 2's compliment of it's positive value.

Eg. 2's compliment of −5 will be 2's compliment of +5

101

2's compliment → 011

2's compliment of −5 is 011

0.25

Keep multiplying fraction part by 2

$0.25 \times 2 = \boxed{0}.50$ → .01 ✓

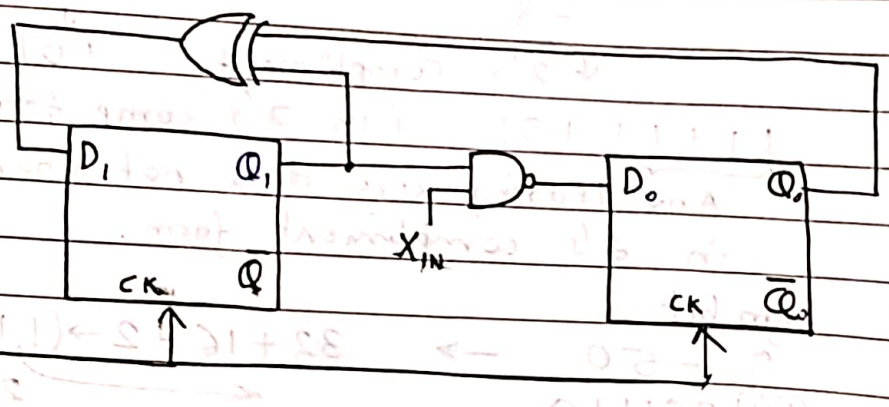
$0.50 \times 2 = \boxed{1}.00$

↓

we can stop as 00 is result.

Shift Register.

Ex



Q_1	Q_0	Q_1^+	Q_0^+	$D_1 = Q_0 \oplus Q_1$	$D_0 = \overline{Q_1 \cdot X_{IN}} = 1$
0	0	0	1	0	1
0	1	1	0	1	1
1	1	0	0	0	1
0	1	0	1	1	1
1	1				

For $X_{IN} = 0$

01 → 11 → 01 → 11 for $X = 0$.

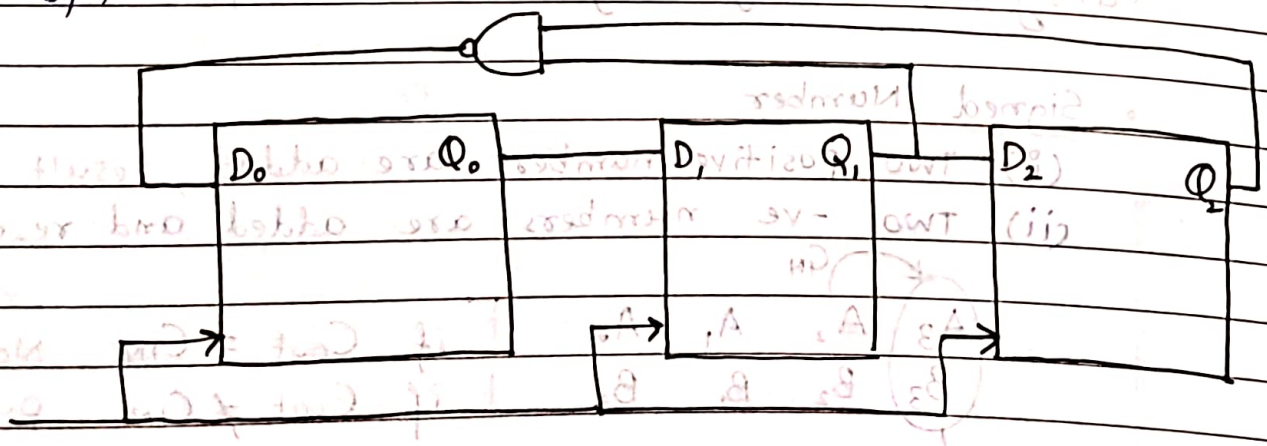
∴ D option,

only two of the four states if $X = 0$.

Homework

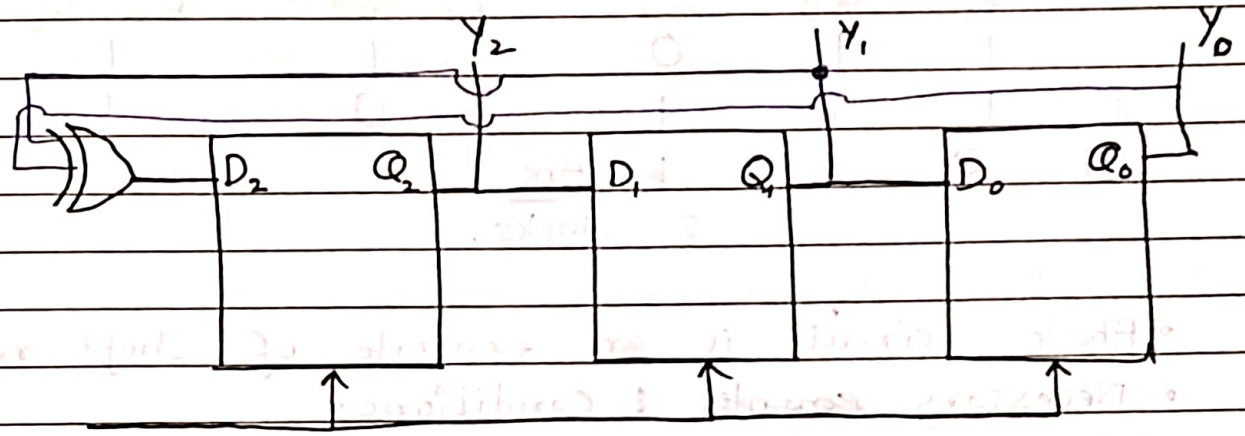
Approach - 2

Solve the same circuit using implementation of synchronous counter.



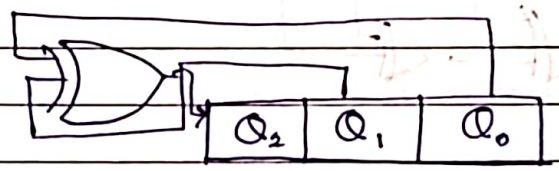
	Q_2	Q_1	Q_0	$D_2 = Q_1$	$D_1 = Q_0$	$D_0 = \overline{Q_1 \cdot Q_2}$
Initial	0	0	0	0	0	1
1	0	0	1	0	1	1
2	0	1	1	1	1	1
3	1	1	1	1	1	0
4th clk →	1	1	0			

DLD-A
Q.35



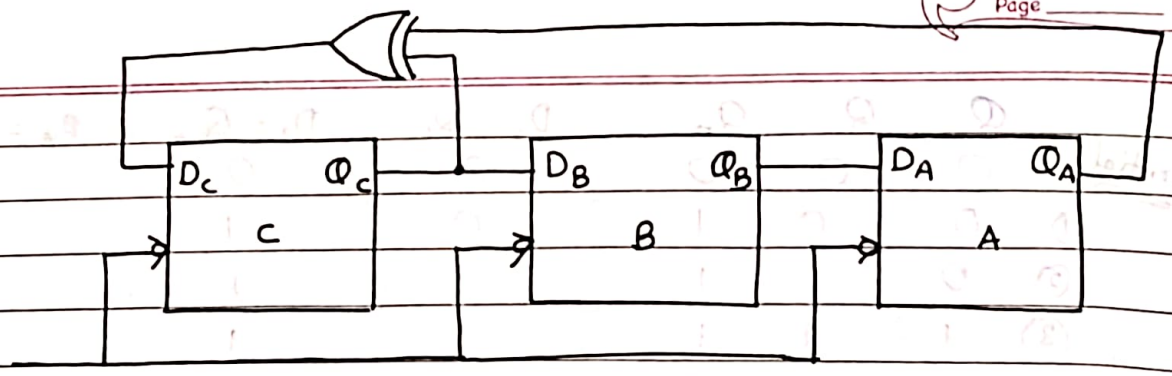
	Y_2	Y_1	Y_0	$D_2 = Q_1 \oplus Q_0$	$D_1 = Q_2$	$D_0 = Q_1$
	1	1	1	0	1	1
1	0	1	1	0	0	1
2	0	0	1	1	0	0
3rd →	1	0	0	0	1	0
	0	1	0			

Equivalent circuit



Only D flipflop is used in shift registers.

DLD-A
Q.12
Homework



	Q_C	Q_B	Q_A	$D_C = Q_C \oplus Q_A$	$D_B = Q_C$	$D_A = Q_B$
	1	1	0	1	1	1
①	1	1	1	0	1	1
②	0	1	1			

Ans

2 - clocks.

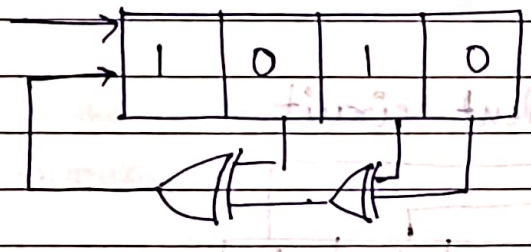
- Above circuit is an example of shift register.
- Necessary ~~counter~~ & conditions:

(1) It should be a synchronous counter.

sufficient condition:

(2) All the FF used in synchronous counter must be D flip flop. (or behave like a D-FF)

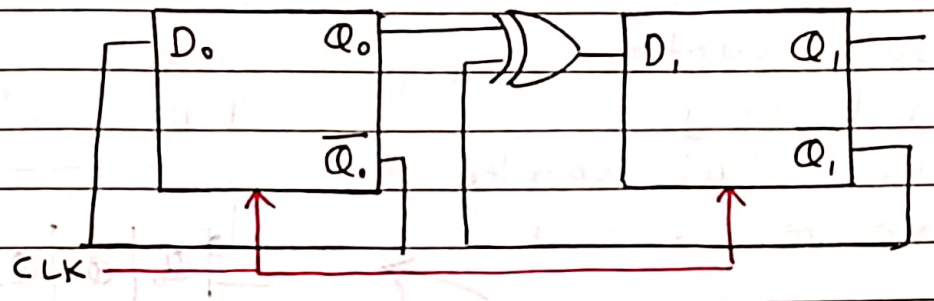
DLD-A Ex-7



Initial →	1 0 1 0
①	1 1 0 1
②	0 1 1 0
③	0 0 1 1
④	0 0 0 1
⑤	1 0 0 0
⑥	0 1 0 0
⑦	1 0 1 0

Shift Register.

CSE 2005



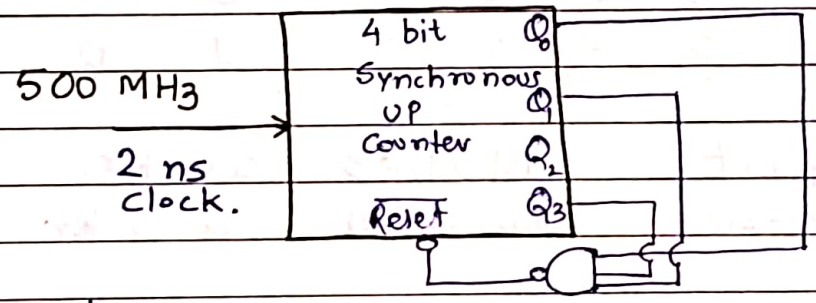
Consider above ckt, FF are +ve edge triggered D FF with 2 bit string. Q_0 and Q_1 initially 0, 0. The state transition sequence is

Q_0	Q_1	$D_0 = \overline{Q_0}$	$D_1 = Q_0 \oplus \overline{Q_1}$ (must be same)	
0	0	1	1	
1	1	0	1	
0	1	1	0	$Q_0 \oplus \overline{Q_1}$
1	0	0	0	$= Q_0 \odot Q_1$
0	0			

$\therefore$

$00 \rightarrow 11 \rightarrow 01 \rightarrow 10$

Ex In the circuit given below, propogation delay of NAND gate is 6 ns, and counter delay is assumed to be zero. Clock freq of 500 MHz is applied. Then the modulus of the counter is ____.



1001
1010
1011
1100

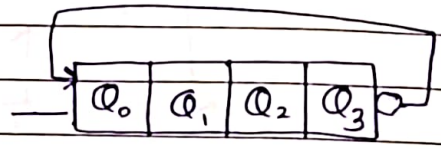
MOD - 14

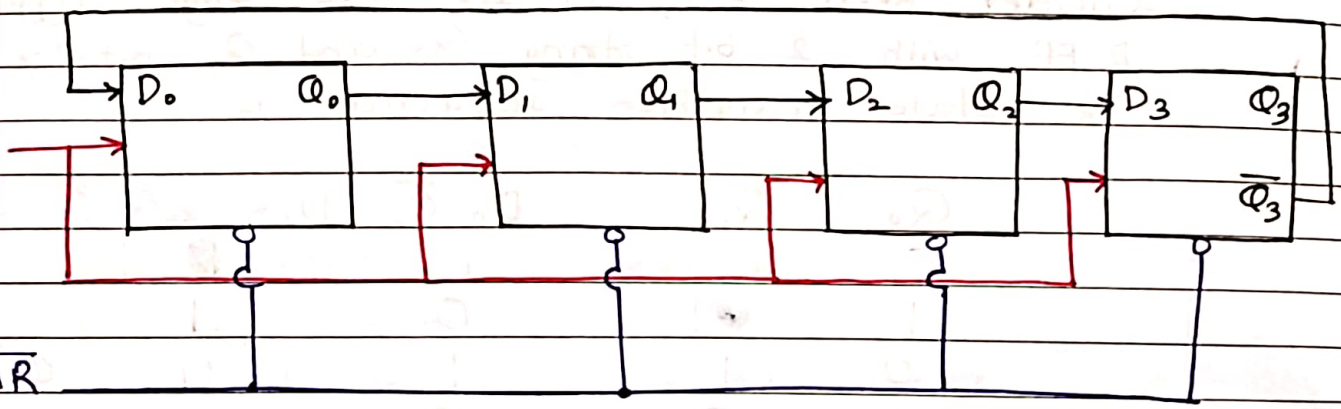
$$t_c = \frac{1}{500 \times 10^6} = 2 \text{ ns.}$$

Shift Register as Counter.

① Johnson Counter
Twisted Ring
switch tail counter
walk in counter

} "MOD = 2n".



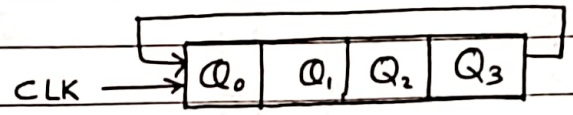


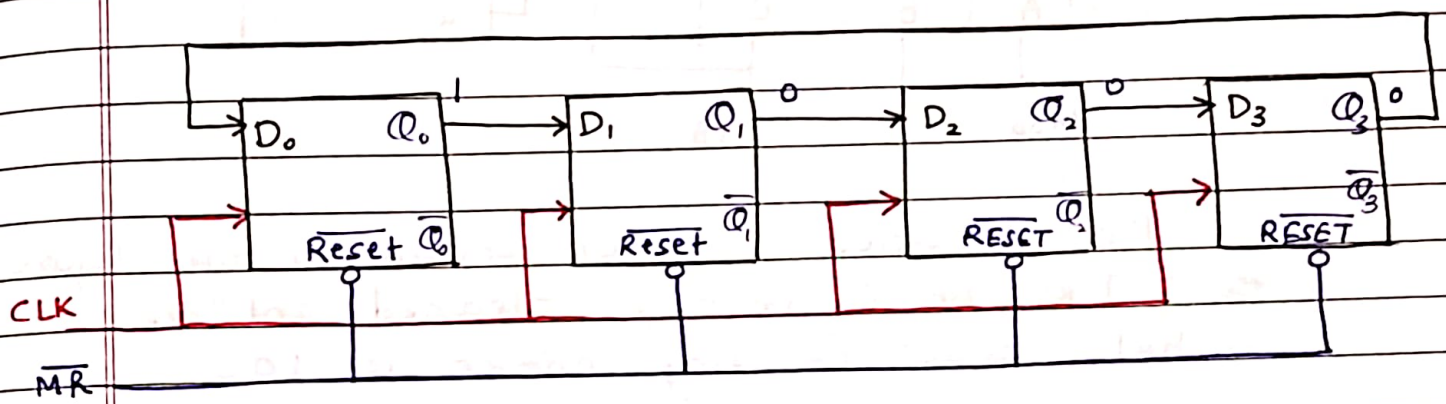
{ Master Reset }

	Q_0	Q_1	Q_2	Q_3	D_0	D_1	D_2	D_3
	0	0	0	0	1	0	0	0
①	1	0	0	0	1	1	0	0
②	1	1	0	0	1	1	1	0
③	1	1	1	0	1	1	1	1
④	1	1	1	1	0	1	1	1
⑤	0	1	1	1	0	0	1	1
⑥	0	0	1	1	0	0	0	1
⑦	0	0	0	1	0	0	0	0
⑧	0	0	0	0	1	0	0	0.

4-bit MOD-8 counter.
n-bit MOD-2n counter

② Ring Counter :



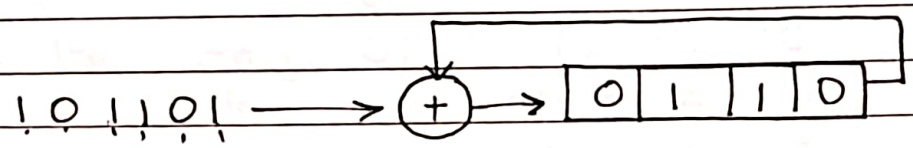


MOD-4

MOD-n

Q_0	Q_1	Q_2	Q_3	D_0	D_1	D_2	D_3
1	0	0	0	0	1	0	0
0	1	0	0	0	0	1	0
0	0	1	0	0	0	0	1
0	0	0	1	1	0	0	0
1	0	0	0	0	1	0	0

Gate 2007



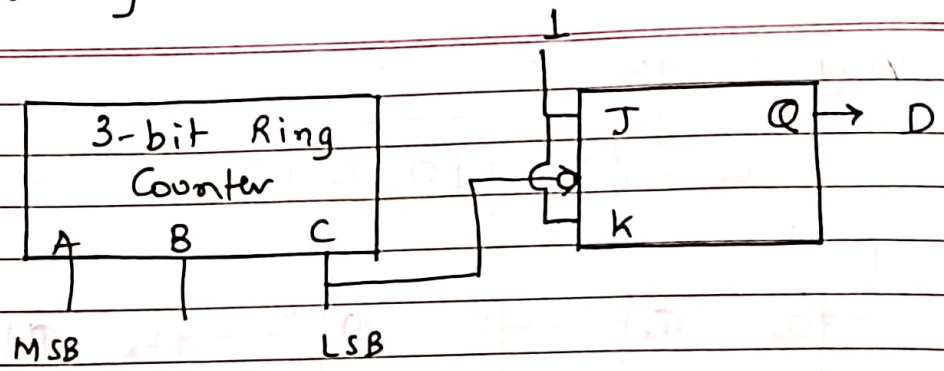
1 ⊕	0	1	1	0
0	1	0	1	1
1	1	1	0	1
1	0	1	1	0
0	1	0	1	1
1	1	1	0	1
	0	1	1	0

MOD-3 (Input dependent)

Cascading Counters

IMP

Ex

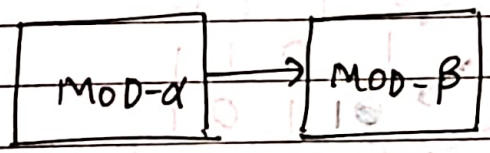


For the cascaded counter shown in the figure the J.K. FF is initialy cleared. and the initial value of ring counter is 100.

(a) Then find the modulus of the counter
(b) Draw the state transition sequence of the counter.

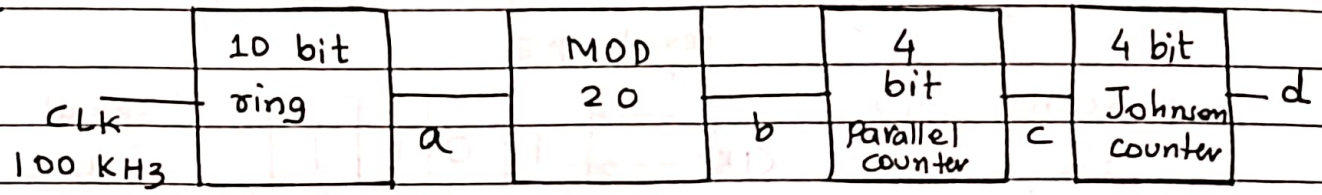
ring			JK
A	B	C	D
1	0	0	0
0	1	0	0
0	0	1	0
1	0	0	1
0	1	0	1
0	0	1	1
1	0	0	0

MOD-6

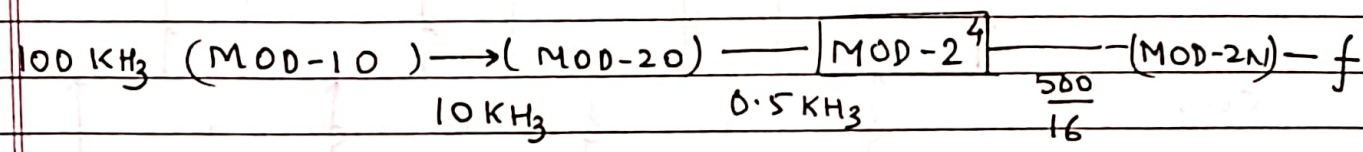


⇒ MOD-α.β.

V. Imp
DLD-A
Q. 51



$f_c = 100\ KHz \qquad t_c = \frac{1}{100 \times 10^3} = 10\ ms.$



$f = \frac{500}{16 \times 8} = 3.9\ Hz.$

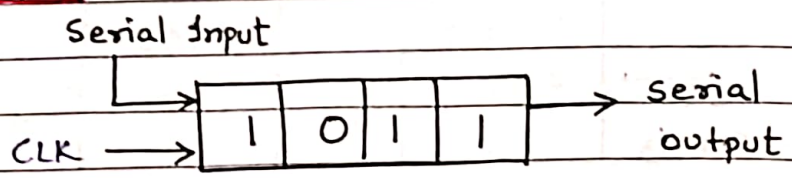
$\boxed{M \leq 2^n}$

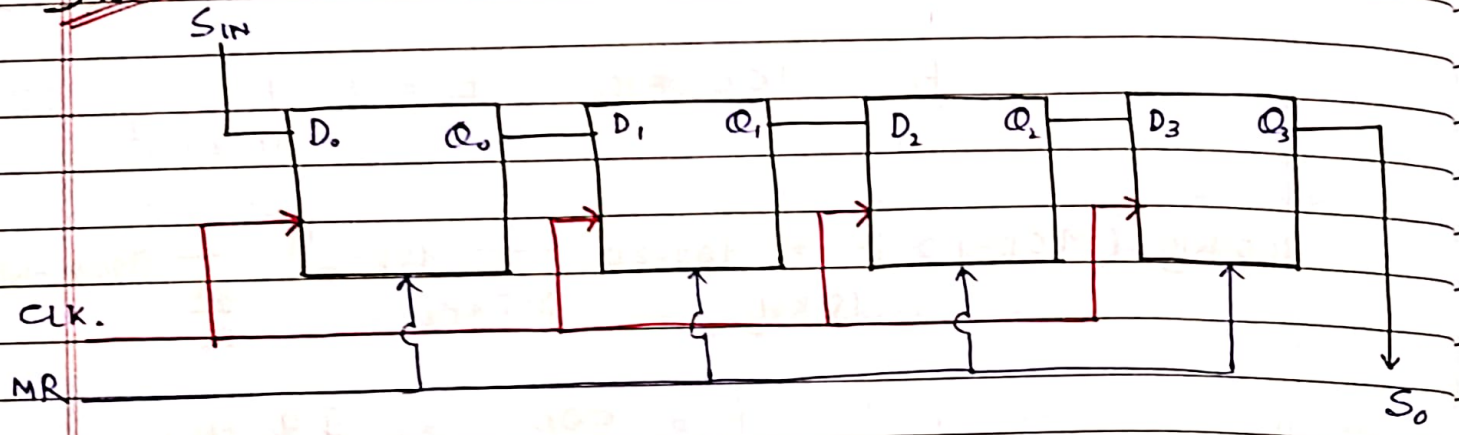
If $M = 2^n$ (Binary counter)
if $M < 2^n$ then Truncated sequence counter.

Ex Find the number of FF needed to design a counter which count upto 1024. MOD-11
consider 0000 to 1024 → 1025 states.

Shift Registers

① Serial Input
SISO





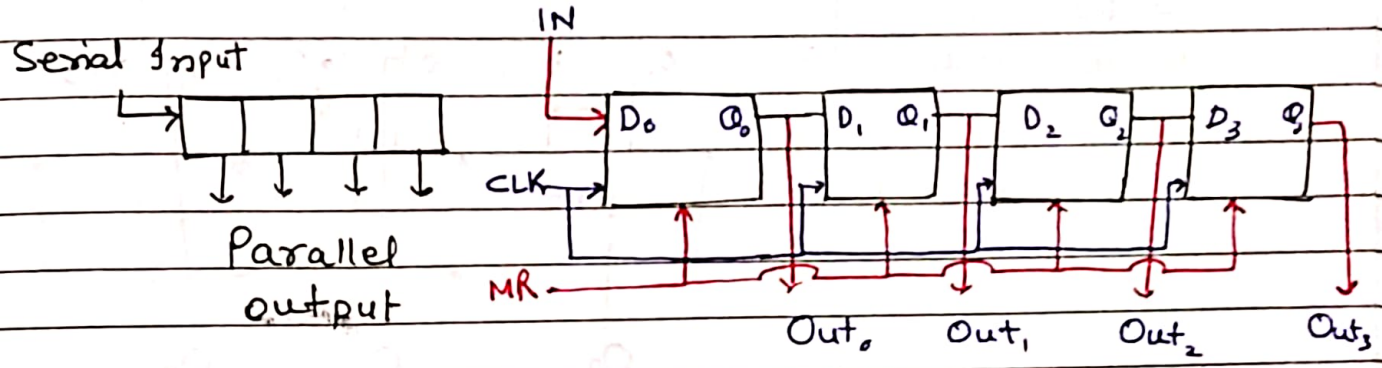
Ex. 0 1 0 1 ← 1 0 1 0 is input
0 will go in first.

Initial	1	0	1	1
CLK ①	0	1	0	1
CLK – 2	1	0	1	0
CLK – 3	0	1	0	1
CLK – 4	1	0	1	0 – 0
CLK – 5	X	1	0	1 – 1
CLK – 6	X	X	1	0 – 0
CLK – 7	X	X	X	1 – 1

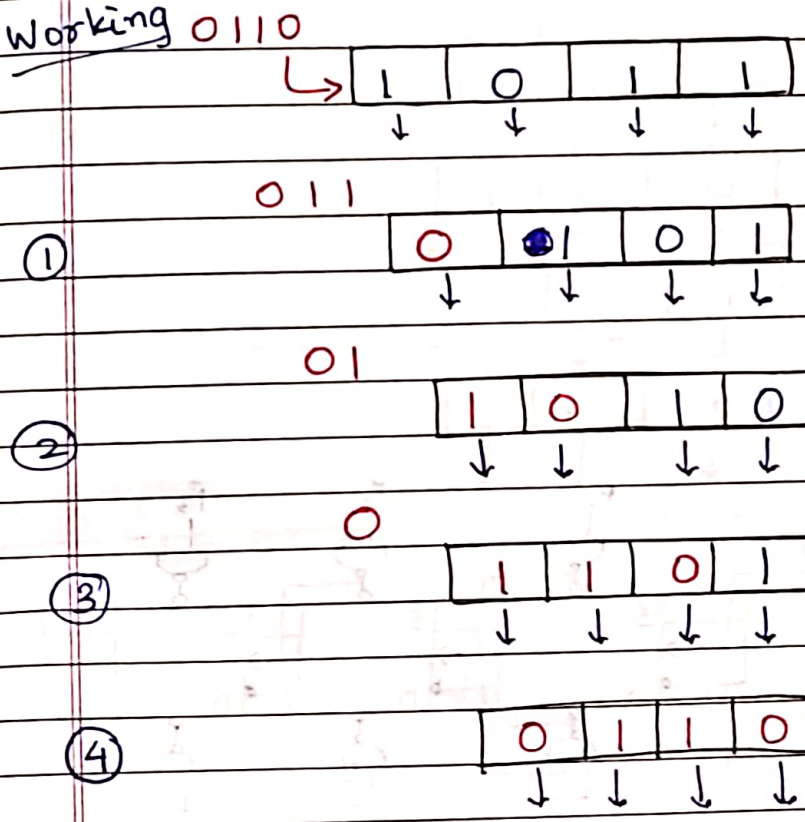
Desired output 1 0 1 0.

∴ After 2N–1 clock, we will get desired out.

② SIPO (Serial Input Parallel output)



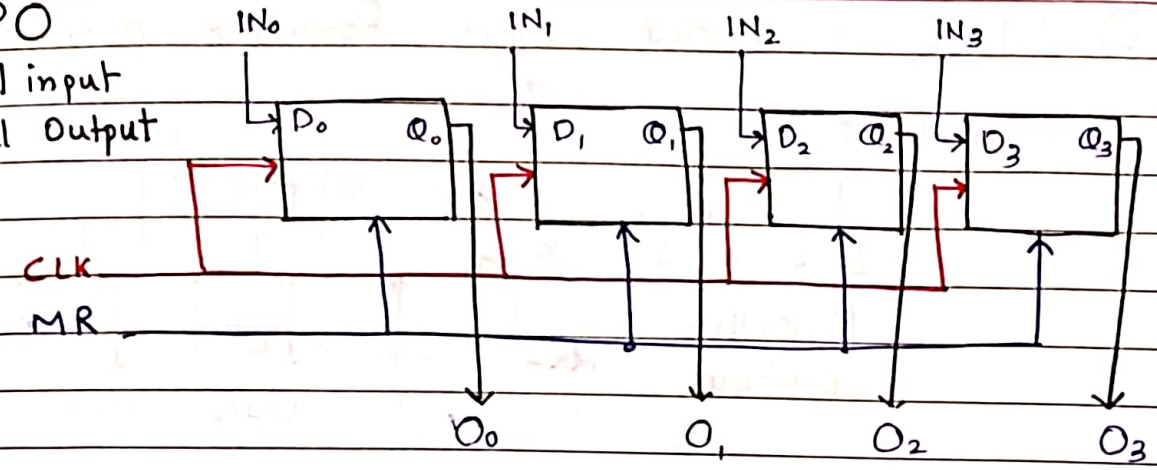
Working 0110



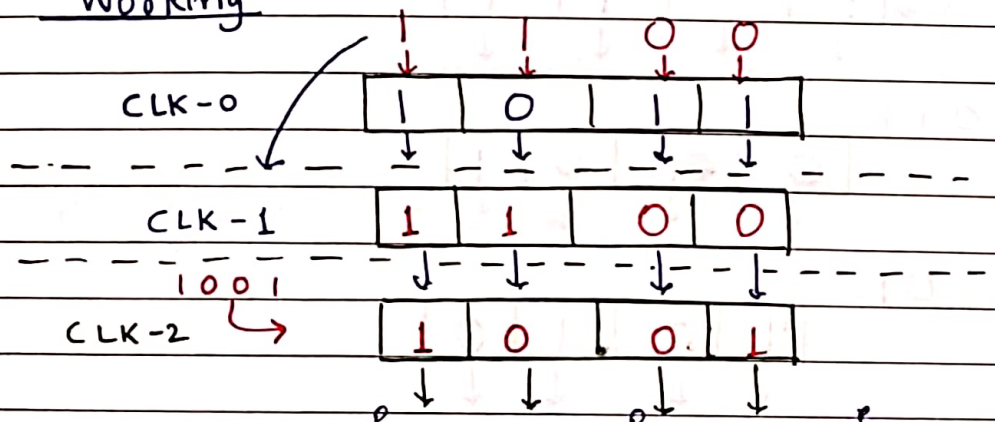
classmate
Date
Page

③ PIPO

Parallel input
Parallel Output



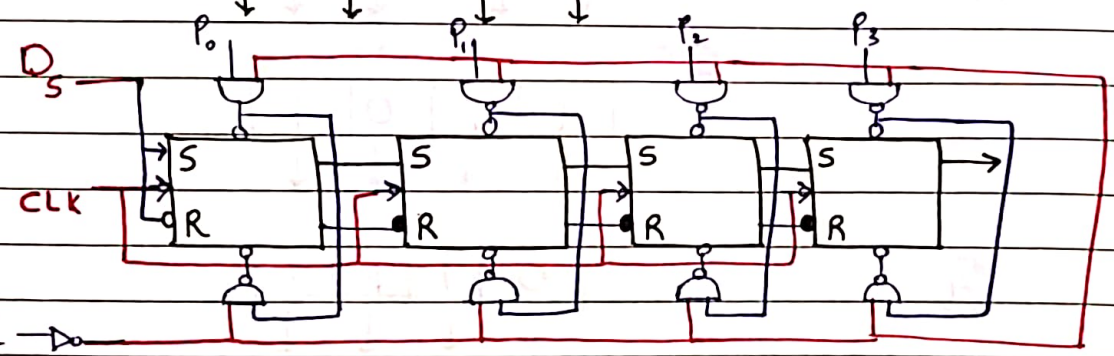
Working



Imp

④ PISO

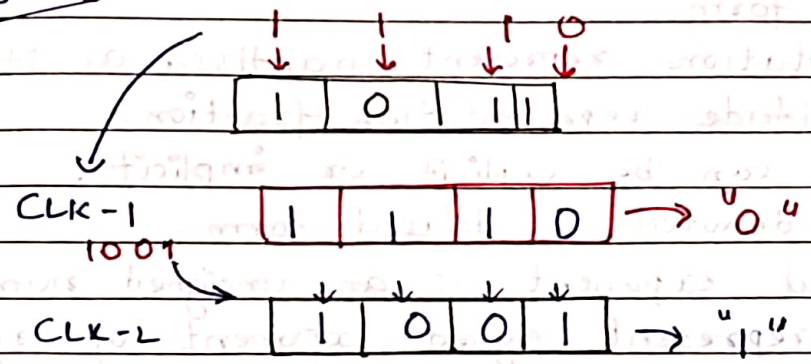
Parallel to Serial Out



- It actually has both serial data entry via D_S, and asynchronous parallel data entry. The only accessible output flipflop is Q_3 and $\bar{Q}_3$.
- All FF are clocked SR responds to NGT (Negative gate trigger
- Each FF has Asynch input. Preset and clear.

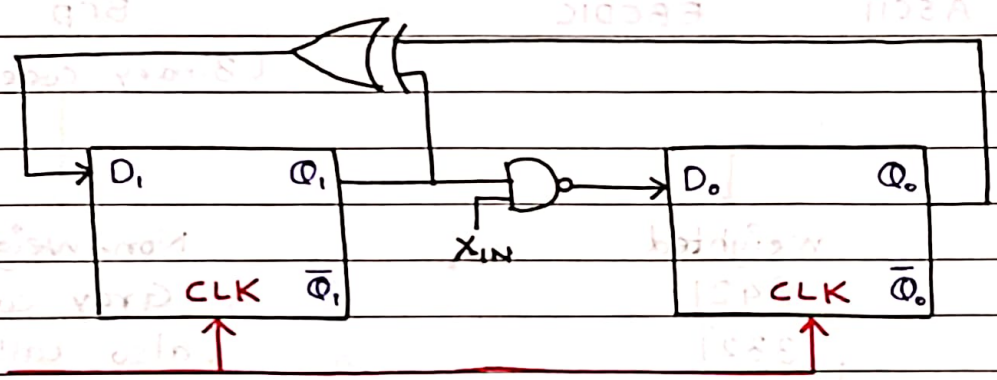
- This shift register can be used for parallel data entry when $\overline{PL}$ goes low.

Working



Home Work

⇒ Approach 2 [Designing a synchronous counter using D - FF. To count (0, 0) → (0, 1) → (1 1) → (0 1) → (1 1) Mod-2 using D-FF.



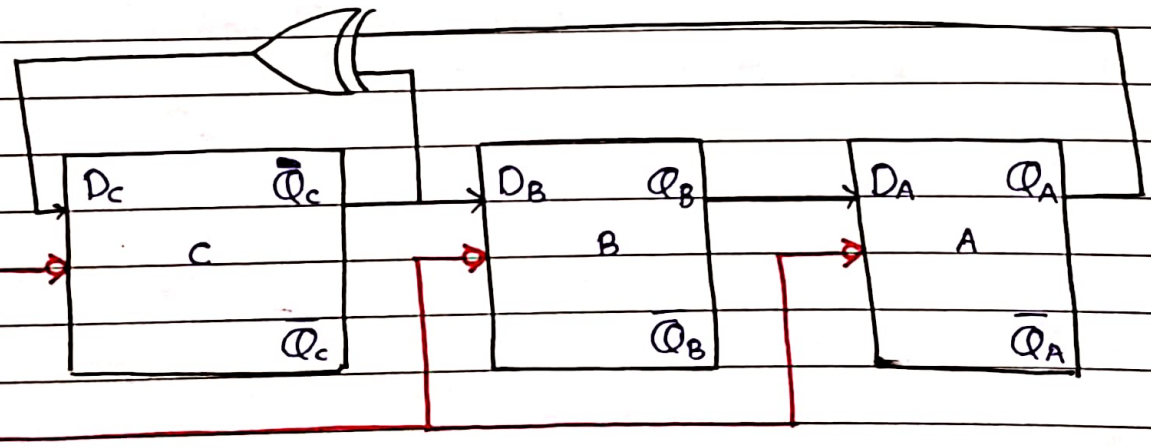
Q_1	Q_0	Q_1^+	Q_0^+	D_1	D_0
0	0	0	1	0	1
0	1	1	1	1	1
1	0	1	1	1	1
1	1	0	1	0	1

must Go to (1,1) for D_1 to be $Q_0 \oplus Q_1$

[as D_0 needs to be always 1, X_{IN} must be 0 always]

$\therefore X_{IN} = 0$.

DLD-A Q.12



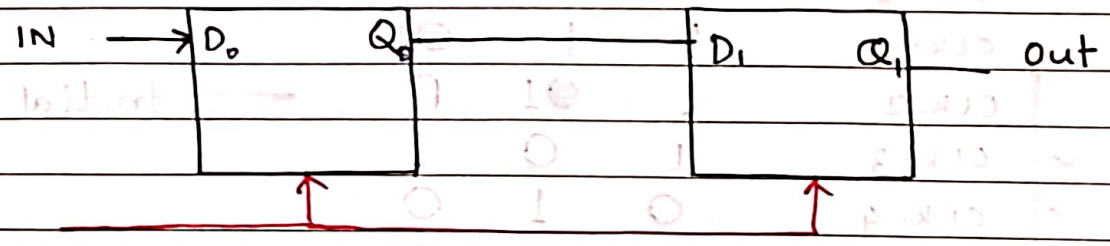
The digital circuit is designed with three D-FF and one EX-OR gate as shown. If Initial value of $Q_A Q_B Q_C$ was 110 then minimum number of clock pulses required to get $Q_A Q_B Q_C$ as 011.

		$Q_A = Q_B$	$Q_B = Q_C$	$Q_C = Q_A \oplus Q_C$	
	CLK-0	0	1	1	
	CLK-1	1	1	1	
	CLK-2	1	1	0	← Initial value 110
After 5 clocks we get 011. ✓	CLK-3	1	0	1	
✓	CLK-4	0	1	0	
✓	CLK-5	1	0	0	
✓	CLK-6	0	0	1	∴ 5 clocks Ans
✓	CLK-7	0	1	1	← Desired value 011

2018

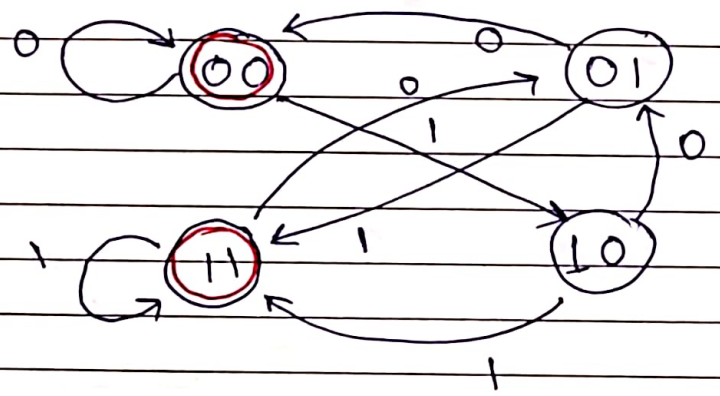
Ex Consider the sequencial circuit, where both FF used are +ve edge triggered D-FF the number of states in transition diagram of the circuit that have the transition back to the same state, on some value of IN is :-

(serial in, serial out shift register).



IN = 0

Q_1	Q_0	$D_1 = Q_0$	$D_0 = 0$
→ 0	0	0	0
0	0	0	0
→ 0	1		



Q_1	Q_0	In	D_1	D_0
0	0	0		
0	0	1		
0	1	0		
0	1	1		

IMP

Ex The digital logic circuit shown in figure satisfy the given state diagram where Q_1 is connected to A of the XOR gate. Suppose XOR is replaced by XNOR Gate then which of the following option preserve the state diagram.

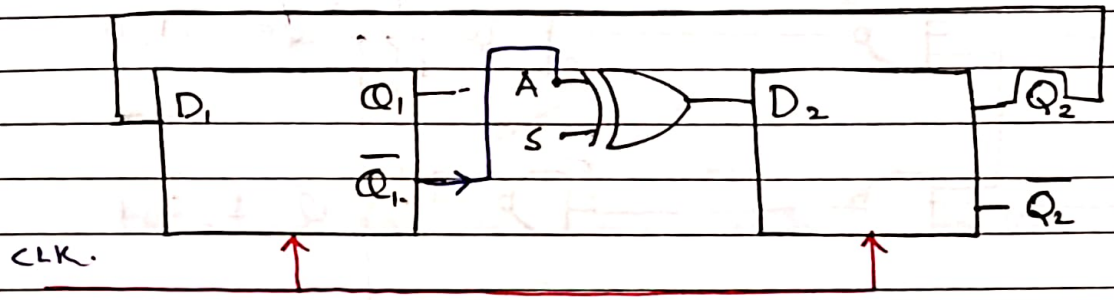
(a) Input A is connected to $\overline{Q_2}$

X-OR

(b) Input A is connected to Q_2

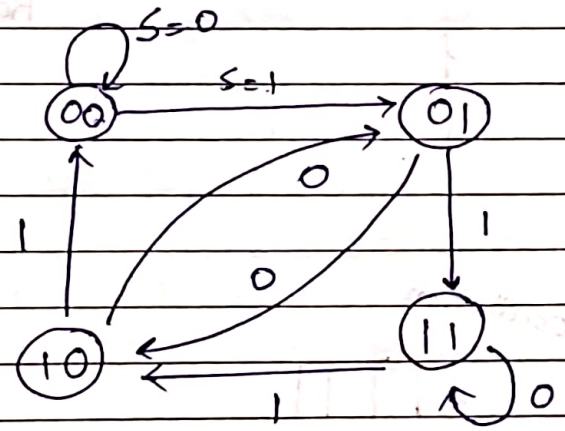
(c) Input A is connected to $\overline{Q_1}$ and S is complimented.

(d) Input A is connected to $\overline{Q_1}$.



Homework

draw state transition diagram of original circuit

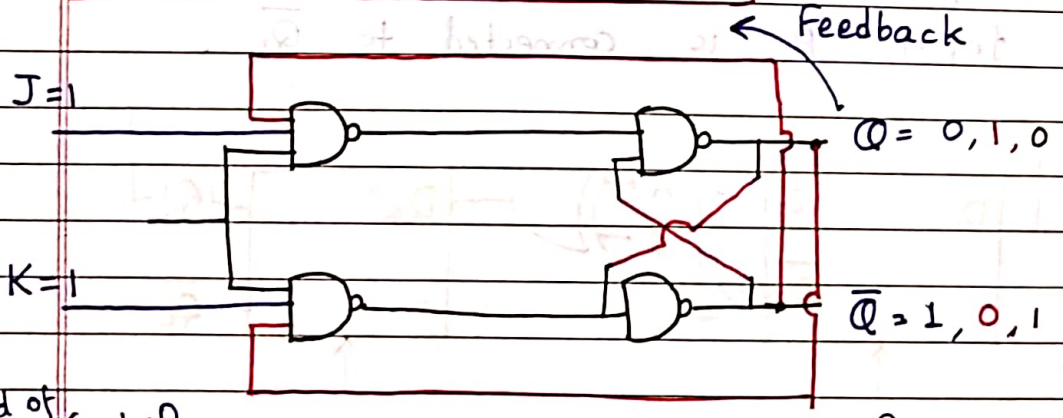


Note: Counters are also reffered as frequency divider circuit. Modulus of a counter is also reffered as divide by M counter.

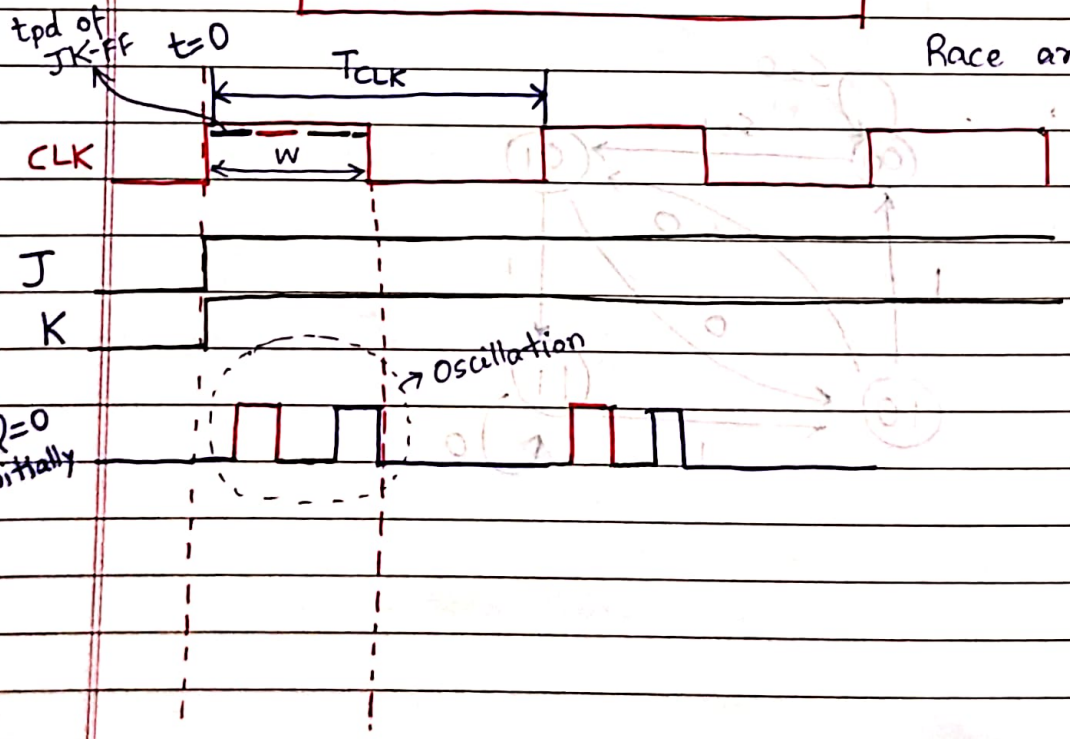
$$f_{out} = \frac{f_{IN}}{M}$$

(Q) If the output frequency of a circuit is 1/12th of the input frequency then find the no of FF used. 4-FF Ans.

Master Slave FLIP-FLOP



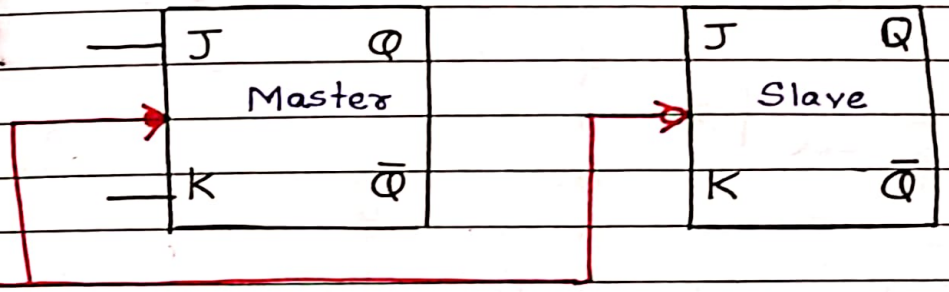
Race around condition



leads to unpredictable output.

- Race around condition is removed in MS-FF.

Master +ve edge Trigger — Slave -ve edge Trigger



Condition :

① level triggered JK-FF $J = K = 1$

② when propogation delay is less than pulse width of the clock.

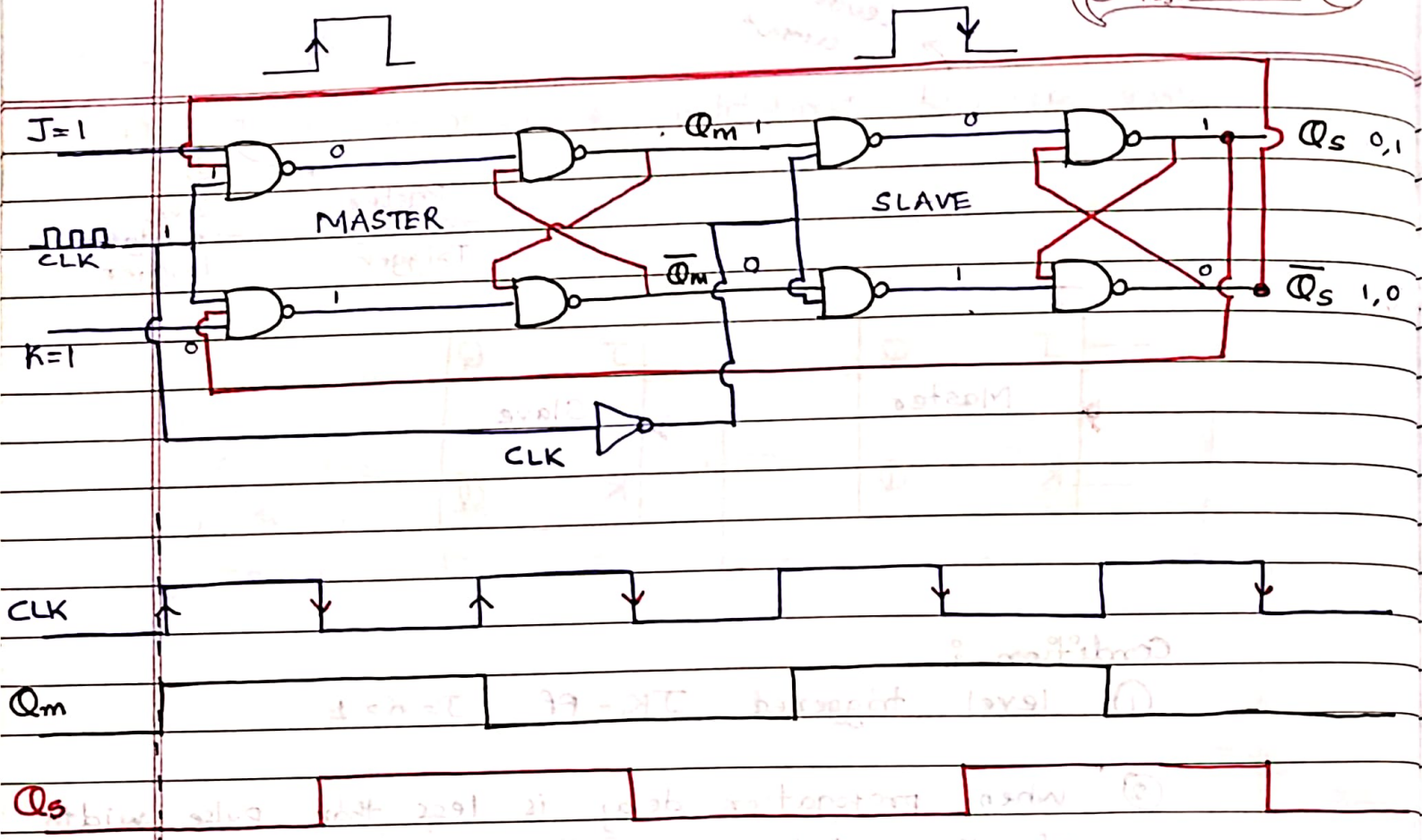
$$t_{pD} < W \quad \text{or} \quad \frac{T_{CLK}}{2}$$

Ex $f_{CLK} = 1\ MHz$ $t_{CLK} = 1\ \mu sec.$

$$\boxed{t_{pD} < \frac{T_{CLK}}{2}} \quad \therefore t_{pD} < 0.5\ \mu sec.$$

Note : Race around condition occurs in JK Flipflop (level triggered JK flip flop) when $J = K = 1$ and propogation delay of the FF is less than the pulse width of the clock signal. It leads to unpredictable output (0, 1)

★ The feedback from output to input is the main reason behind race around condition. (Every time generated output is used at input)



- Master Slave FF consist of two stages J.K Flipflop. First stage of input is reffered as master flipflop. Second stage (output is reffered as slave flip flop.

- Master FF is a positive edge triggered flip flop. Slave FF is a negative edge triggered Flip Flop.

- Master FF generates output for the rising edge of clock signal, and for the rising edge of clock signal, slave is in hold condition.

- For falling edge of clock signal, slave use the output generated by the master flip flop, while master remains in hold state. Hence, only due to falling edge, output of JKFF is changed.

5 bit Even Parity checker Circuit.

A	B	C	D	E	Y	
0	0	0	0	0	1	0
0	0	0	0	1	0	1
0	0	0	1	0	0	2
0	0	0	1	1	1	3
0	0	1	0	0	0	4
0	0	1	0	1	1	5
0	0	1	1	0	1	6
0	0	1	1	1	0	7
0	1	0	0	0	0	8
0	1	0	0	1	1	9
0	1	0	1	0	1	10
0	1	0	1	1	0	11
0	1	1	0	0	1	12
0	1	1	0	1	0	13
0	1	1	1	0	0	14
0	1	1	1	1	1	15
1	0	0	0	0	0	16
1	0	0	0	1	1	17
1	0	0	1	0	1	18
1	0	0	1	1	0	19
1	0	1	0	0	1	20
1	0	1	0	1	0	21
1	0	1	1	0	0	22
1	0	1	1	1	1	23
1	1	0	0	0	1	24
1	1	0	0	1	0	25
1	1	0	1	0	0	26
1	1	0	1	1	1	27
1	1	1	0	0	0	28
1	1	1	0	1	1	29
1	1	1	1	0	1	30
1	1	1	1	1	0	31

$$Y = \Sigma m(0, 3, 5, 6, 9, 10, 12, 15, 17, 18, 20, 23, 24, 27, 29, 30)$$

BC \ DE	00	01	11	10	10	11	01	00
	A=0				A=1			
00	1		1		1		1	1
01		1		1		1		1
11	1		1		1		1	
10		1		1		1		1

$$f = \bar{A} \cdot (B \odot C \odot D \odot E) + A \cdot \overline{(A \odot C \odot D \odot E)}$$

Date
Page

Carry Look Ahead Adder

x	y	C_{in}	C_{out}
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

carry propogated → $(x \oplus y)C_{IN}$

carry generated → $x.y$

$$C_{out} = P \cdot C_{IN} + G$$

$$C_n = P_n C_{n-1} + G_n$$

$$C_{out} = (x \oplus y) C_{in} + x.y$$

Considering $n = 0$,

$$C_0 = P_0 C_{-1} + G_0$$ stage 1

$n = 1$,

$$C_1 = P_1 C_0 + G_1$$
$$= P_1 P_0 C_{-1} + P_1 G_0 + G_1$$

stage 2

$n = 2$,

$$C_2 = P_2 C_1 + G_2$$
$$= P_2 P_1 P_0 C_{-1} + P_2 P_1 G_0 + P_2 G_1 + G_2$$

stage 3

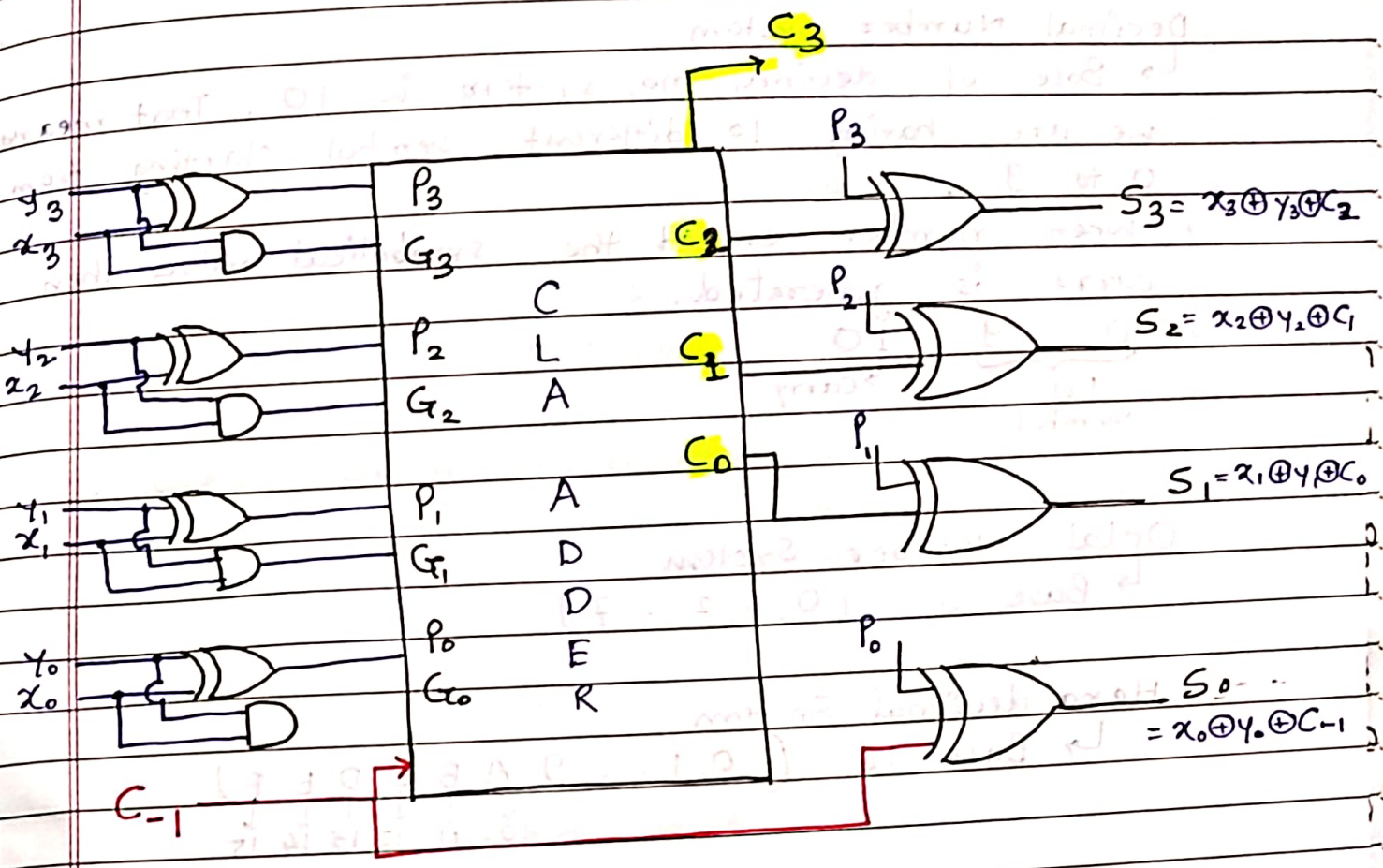
$n = 3$,

$$C_3 = P_3 C_2 + G_3$$
$$= P_3 P_2 P_1 P_0 C_{-1} + P_3 P_2 P_1 G_0 + P_3 P_2 G_1 + P_3 G_2 + G_3$$

stage 4

carry of nth stage is purely dependent on initial carry. Hence we have reduced the carry propogation delay.

- Carry look ahead adder is faster in operation compared to ripple carry adder.



Number System

Number system is characterized by its radix. (base)

Decimal Number System

↳ Base of decimal no. system is 10, That means we are having 10 different symbol starting from 0 to 9.

- When number exceed the symbolical value then carry is generated.
- $\underbrace{0 \ldots 9}_{\substack{10 \\ \text{Symbols.}}}$, $\underset{\text{carry.}}{10}$

Octal Number System

↳ Base - 8 (0, 1, 2 ... 7)

Hexa decimal System

↳ Base - 16 (0, 1 .... 9, A, B, C, D, E, F)

A → 10, B → 11, C → 12, D → 13, E → 14, F → 15

Binary Number System

↳ Base - 2 (0, 1)

(Q) Convert decimal to Binary, octal, Hexa.

$(125)_{10} \rightarrow$

2	125	
2	62	1
2	31	0
2	15	1
2	7	1
2	3	1
2	1	1

$(1111101)_2$

1 111 101

$(7\ 5)_8$

1111 1101

$(7\ D)_{16}$

$(0.125)_{10} = (0.001)_2$

$0.125 \times 2 = 0.250$
$0.250 \times 2 = 0.5$
$0.5 \times 2 = 1.0$

$(0.0625)_{10} = (0.04)_8$

$0.0625 \times 8 = 0.5$
$0.5 \times 8 = 4.0$

Convert octal to Binary

$(1\ 7\ 6)_8$ → 001 111 110

$(1111110)_2$

$(2\ 5\ 4)_8$ → 010 101 100

$(10101100)_2$

$(742.63)_8$ → 111 100 010 . 110 011

$(111100010.110011)_2$

Binary to octal :

$(11001010)_2 = (312)_8$

$(010011010111111101)_2 = (232775)_8$

$(10010101.010111)_2 = (225.27)_8$

Hexadecimal to Binary

A 1010
B 1011
C 1100
D 1101
E 1110
F 1111

$(78B)_{16} = (0111\ 1000\ 1011)_2 = (3612)_8$

$(A95D)_{16} = (1010\ 1001\ 0101\ 1101)_2$

$(B5.6E.FE)_{16} = (10110101\ 0110\ 1110.11111110)_2$

$\Downarrow$

$(132556.774)_8$

(Q) Representation of the value of 16 bit unsigned integer X in hexadecimal Number system, BCA9 the representation of value of X in octal number system ___?

$(BCA9)_{16}$

$\underbrace{1011}\ \underbrace{1100}\ \underbrace{1010}\ \underbrace{1001}$

1 3 6 2 5 1

$(136251)_8$ ✓

(Q) $(123456)_8$ is equivalent to

(a) $A72E_{16}$ & $(22130232)_4$ (c) $A73E_{16}$ & $(22130232)_4$
(b) $A72E_{16}$ & $(22131122)_4$ (d) $A62E_{16}$ & $(22120232)_4$

2 2 1 3 0 2 3 2

$\underbrace{001\ 010}\ \underbrace{011\ 1}\ \underbrace{0010}\ \underbrace{1110}$

A 7 2 E

(Q) Find base / radix

$\frac{312}{20} = 13 \cdot 1$

let base $= r$,

$$\frac{3r^2 + r + 2}{2r} = r + 3 + \frac{1}{r}.$$

$$3r^2 + r + 2 = 2(r^2 + 3r + 1)$$

$$r^2 - 5r + 0 = 0.$$

$$r(r-5) = 0$$

$r = 0$ $\quad$ $r = 5$ ✓

Binary Coded Decimal

- 4-bit code
- Range of BCD $\quad$ 0 9
- 6 Don't care $\quad$ 10, 11, 12, 13, 14, 15 X

$$(7\ 6\ 9)_{10}$$

0111 $\quad$ 0110 $\quad$ 1001

3

Byte 4 $\quad$ Byte 3 $\quad$ Byte 2 $\quad$ Byte 1

(Q) $(1\ 2\ 3\ 4\ 5\ 6\ 7)_{10}$

while expressing this number 1234567 in BCD form how many bytes are consumed. 4 Ans

Ex Find r.

$$(\sqrt{224})_r = 13_r.$$

$$2r^2 + 2r + 4 = (r+3)(r+3).$$
$$2r^2 + 2r + 4 = r^2 + 6r + 9.$$
$$r^2 - 4r - 5 = 0$$
$$(r = 5)\ (r = -1).$$

Ex **Compliment Representation**

① Radix Compliment (r's comp) and Reduced radix compliment. $(r-1)$'s comp.

if base = 10, 10's & 9's comp.
if base = 8, 8's & 7's comp.
if base = 2, 2's & 1's comp.

Find the 10's comp of 3 ⇒ 10−3 = 7.
10's comp of 38 ⇒ 100 − 38 = 62
10's comp of 194 ⇒ 1000 − 194 = 806

$$r^n - N$$

9's comp of 3 ⇒ 9 − 3 = 6
9's comp of 38 ⇒ 99 − 38 = 61
9's comp of 194 ⇒ 999 − 194 = 805

$$r^n - N - 1$$

[r's compliment = $(r-1)$'s comp + 1]

Find 9's comp of 12345

$\Rightarrow$ 87654

$$\begin{array}{r} 99999 \\ -\ 12345 \\ \hline (87654 \quad +1) \end{array} \longrightarrow \begin{array}{r} {}^{9}1\,{}^{9}0\,{}^{9}0\,{}^{9}0\,{}^{10}0 \\ -\ 1\ 2\ 3\ 4\ 5 \\ \hline 8\ 7\ 6\ 5\ 5 \end{array}$$

- Find 8's comp of $(1247)_8$

$$\begin{array}{r} (7777)_8 \\ (1247)_8 \\ \hline 6530 \end{array} + 1 = (6531)_8 \checkmark$$

7's compliment.

Representation of +ve Number

- In signed magnitude representation, we use MSB bit for representing the number in either -ve or positive form.

- If MSB bit is 0, that reflect, number is a positive value.
- If MSB bit is 1 that reflects number is -ve.

+ve 0 to 7	0000	1000
	0001	1001
	0010	1010
	0011	1011
	0100	1100
	0101	1101
	0110	1110
	0111	1111
		-ve 0 to 7

Range of SM representation.

$$-(2^n - 1) \text{ to } (2^{n-1} - 1)$$

total Symbols $= \underbrace{2^n - 1}_{\text{as zero is represent-ed twice.}}$

1's Compliment Representation

- It is only used to represent -ve number.
- Find the 1's compliment form of :

$+(8)_{10} = 1000$

$+(10)_{10} = 1010$

$+(12)_{10} = 1100$

$(38)_{10} \Rightarrow ?$

$$(10100101)_2 \Rightarrow \begin{array}{r} 11111111 \\ -\ 10100101 \\ \hline (01011010)_2 \end{array} \rightarrow \text{1's comp.}$$

1's comp of (1000). $= 0111$

Range of 1's compliment,

$$-(2^n - 1) \text{ to } 2^{n-1} - 1$$

- Twice the 1's compliment of the number represents the same number in magnitude form.

2's compliment form : $\underbrace{-2^n \text{ to } -(2^n-1)}_{\text{Range.}}$

- 2's comp $= (2^n - N - 1) + 1$

  1's comp + 1.

Ex Find 2's comp of (−17)

append

$(\boxed{0}10001)_2 \rightarrow +17$ in 6 bits

101111 is 2's comp of −17.

Ex Find 2's comp of (−68) 64+4.

append

$(\boxed{0}1000100)_2$ +68

10111100 is 2's comp.

Ex Solve variety of Numerical from Tocci

Index
Introduction and Basics
- Basic Logic Gates
- Special Logic Gates
- Basics of Boolean Algebra
- K-Maps
- Redundant Prime Implicants
- Essential Prime Implicants
- Concensus Theorem
- Duality

Combinational Circuits
- Half Adder
- Half Subtractor
- Full Adder
- Full Subtractor
- Delays
- Binary to Gray converter
- Gray to Binary converter
- Designing and implementation of Boolean Function
- Decoder Circuit
- Encoder Circuit
- Ripple Carry Adder
- Multiplexer
- 2 Bit Magnitude Comparator
- Demultiplexer
- Parity Checker
- Carry Look Ahead Adder

Sequential Circuits
- Flip Flops

- SR FF
- D FF
- T FF
- JK FF
- Excitation Table
- Conversion from A to B
  - SR to JK
  - SR to D
  - D to T
  - JK to T
  - T to JK
  - JK to SR
  - D to SR
- Switching Circuits
- Types of Clock Signals
- Counters and Registers
  - Asynchronus Counter
  - Synchronus Counter
  - Designing of Synchronus Counter
  - Shift Register Example
  - Shift Register as a counter
  - Ring Counter
  - Shift Registers
    - SISO
    - SIPO
    - PIPO
    - PISO

Number System

- Complement Representation

1's Compliment

2's Compliment