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# 

# EDUCATION

**BHANU SAHITHYA VATT I KUTI** +1 (979)9858585

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# Texas A&M University College Station, Texas, USA Aug 2023 – Aug 2025(Expected)

* **Master of Science (MS) in Computer Engineering(VLSI)**
* **Coursework:** Hardware Verification, Computer Architecture, Digital IC Design.

# Amrita Vishwa Vidhyapeetam (3.52/4) Tamil Nadu, India July 2019 – June 2023

* **Bachelor of Technology in Electronics and Communication Engineering**, First Class Graduate (Distinction).
* **Coursework:** Digital electronics and System, VLSI Design, FPGA based system design, RISC

processor Design.

# PROJECTS

* **Verification for SPI:** Complete RTL Design and verification of the protocol using system Verilog with scoreboard, assertion checks.
* **Test volume reduction:** Automated the process of test volume generation for Atalanta and used ML models like SVM, mRMR and LDA for test pattern reduction with nominal fault coverage.(Paper accepted in conference)
* **8 bit Radix-4 MAC unit:**  Complete RTL design of an 8-bit MAC unit using booth encoding and compared the power, speed with existing MAC units.
* **2 player whack-mole game:** Implemented a 2-player game in a Basys 3 FPGA board using LFSR and Finite State Machine.
* **Animal Intrusion Device:** A Miniature Model of Security system using image processing algorithm like YOLO with ATmega328P microcontroller to alert people of wild animals.

# SKILLS

* **Programming:** Verilog, System Verilog, UVM, C, C++, Assembly language.
* **Tools:** Xilinx, Vivado HLS, Cadence Xcelium, Simvision, Intel Quartuz prime.
* **Scripting Languages:** Python(Intermediate). **Protocol:** SPI, I2C**,** UART, AHB.

# WORK EXPERIENCE(Internship)

**Embedded Engineer Intern |P M T Honeywell International.Inc Jan 2023 - Jun 2023**

* Participated in the design, development and testing of safety manager.
* Analyzed the communication protocols like Modbus, SPI, UART, Safenet.
* Bugs in the interrupts in safety-critical systems were resolved.
* Analyzed errors in the core of the system which involved debugging in assembly language.
* Troubleshooting of hardware components was done.

Tools: Coverity, wireshark, Safety Builder.

# CERTIFICATIONS

* System Verilog for verification
* Introduction to FPGA Design for Embedded Systems