Bryant Har bjh254

Q1 a)

N_3	N_2	N_1	N_0	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	X
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	X
1	1	0	0	0
1	1	0	1	X
1	1	1	0	X
1	1	1	1	0

b)

N_1N_0 \ N_3N_2	00	01	11	10
00	1	1	0	1
01	1	0	X	0
11	0	X	0	X
10	1	0	X	0

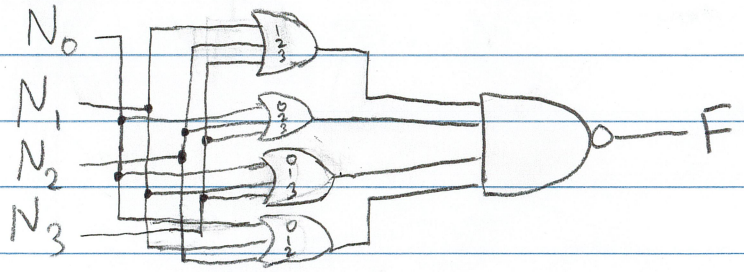
SOP: $N_1'N_2'N_3' + N_0N_2'N_3' + N_0'N_1'N_3' + N_0'N_1'N_2$

c)

N_1N_0 \ N_3N_2	00	01	11	10
00	1	1	0	1
01	1	0	X	0
11	0	X	0	X
10	1	0	X	0

POS: $(N_0'+N_1')(N_1'+N_2)(N_1+N_3)(N_0'+N_2)(N_2'+N_3')(N_0+N_3)$

d)



Q2 a)

i) P2: off P3: off N2: on N3: on

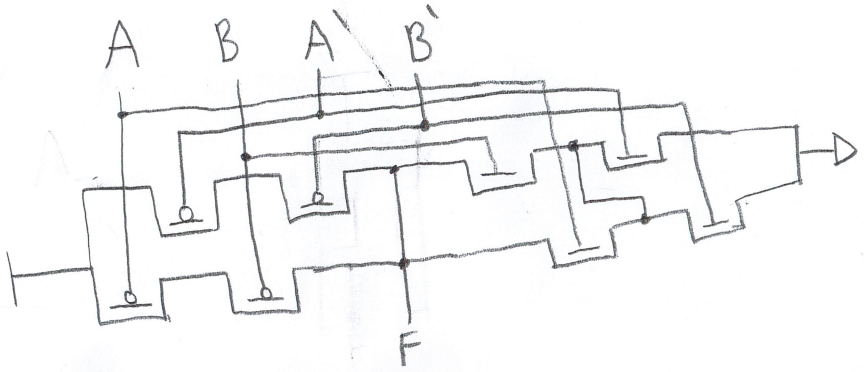
ii) P2: off P3: on N_2: off N3: on

b)

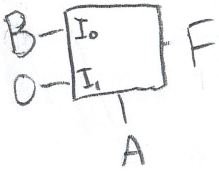
A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

Outputs XOR gate

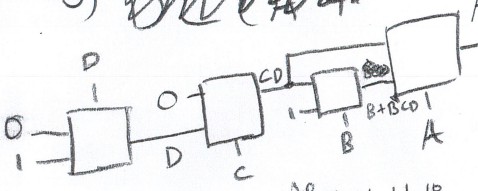
Q2 c)



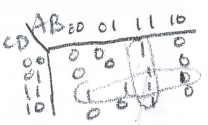
Q3 a)



b)



$F = A'CD + A(B + B'CD)$



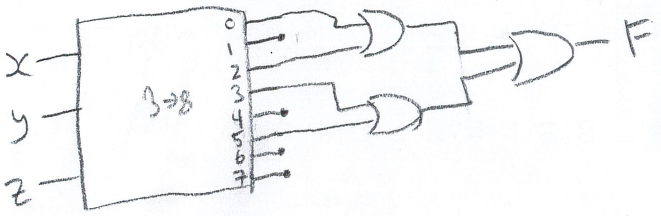
$\Rightarrow$ $F = AB + CD$

c)

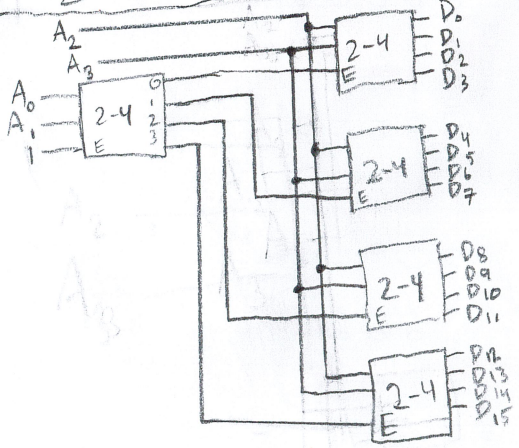
CD \ AB	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	1	1	1	1
10	0	0	1	0

$CD + AB$

Q4 $F = 0$ for xyz: 001, 100, 110, 111



Q5 a) 5 2-to-4 decoders at minimum



With enable pins

b) No enable pin. $\Rightarrow$ Min of 13 Encoders