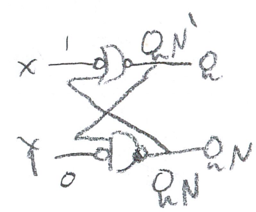
Bryant Har bjh254

Q1) a) Yes

$X=1$ $Y=0$

to hold state

X	Y	Q_n	Q_{n+1}	QN_{n+1}
1	0	Q	$QN' = Q$	QN



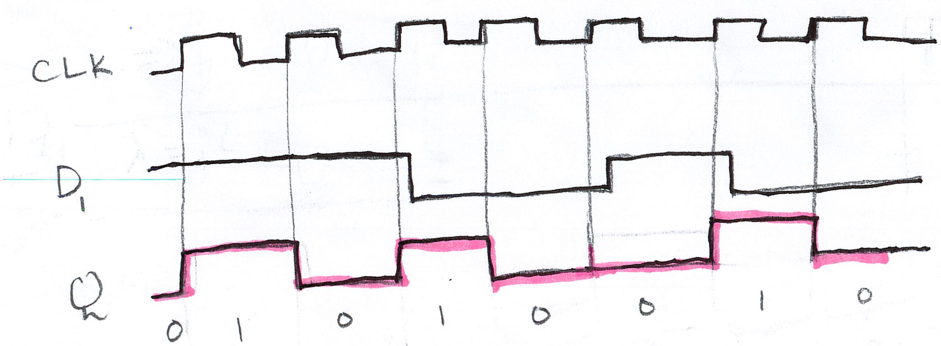
b) Yes

$X=0$ $Y=$ Don't Care

X	Y	Q_n	Q_f	QN_f
0	1	Q_n	0	1
0	0	Q_n	0	1

c) No. $X=0$ for Q_n to possibly be 1, and $Y=0$ for QN to possibly be 0. But even with these inputs, $Q=1$ for the NAND output QN to be 0, $Q_n=0$ will mean QN will be 1. In other words, no input can always set $Q_n=1$, $QN=0$ independent of the previous state.

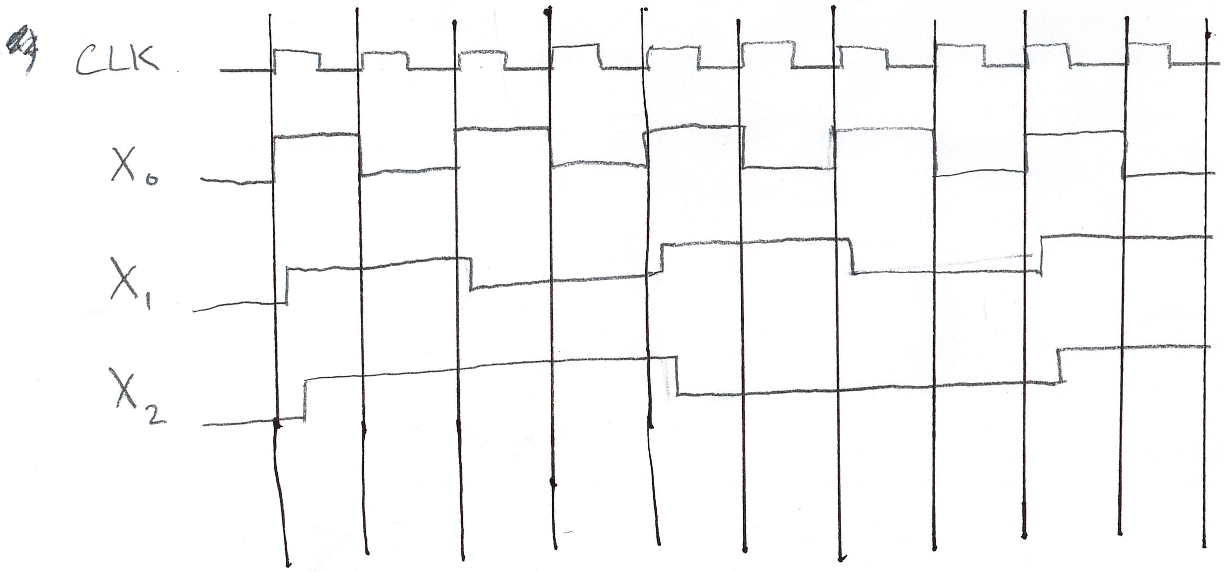
Q2)



Q3)

a)

Cycle	0	1	2	3	4	5	6	7	8	9	10
X0	0	1	0	1	0	1	0	1	0	1	0
X1	0	1	1	0	0	1	1	0	0	1	1
X2	0	1	1	1	1	0	0	0	0	1	1

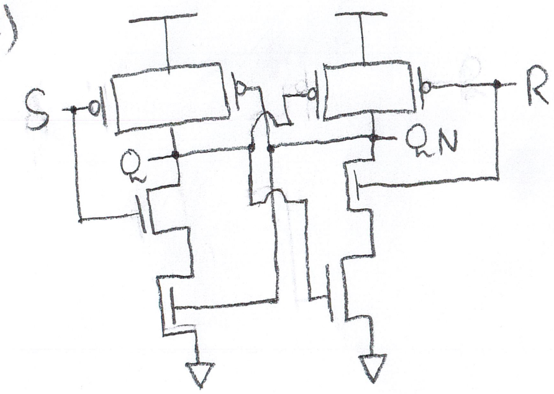


b) We made a down counter (counts in reverse)

c) Every X0, X1, X2 will now read from Q_n' instead of Q_n. So, it will go, starting with all Qs being 0 or all Q_nNs being 1: 111, 000, 001, 010, 011, 100,...

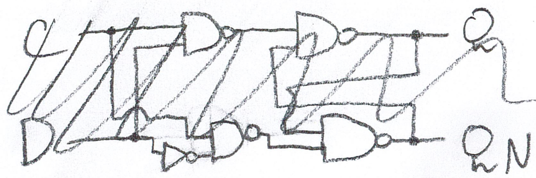
We have now made an up counter.

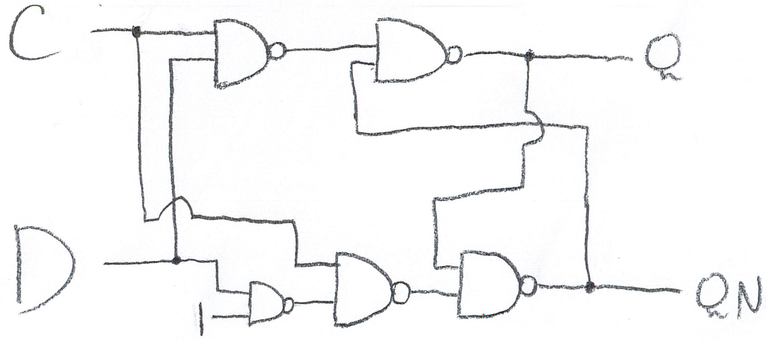
Q4| a)



b) C is Enable, so $C=0 \Rightarrow S=R=1$

If $C=1$ $\begin{cases} D=0: S=1, R=0 \\ D=1: S=0, R=1 \end{cases}$





Q5|

First ? ⇒ if i=1xxx, y=11. Otherwise, if i=x1xx, y=10.

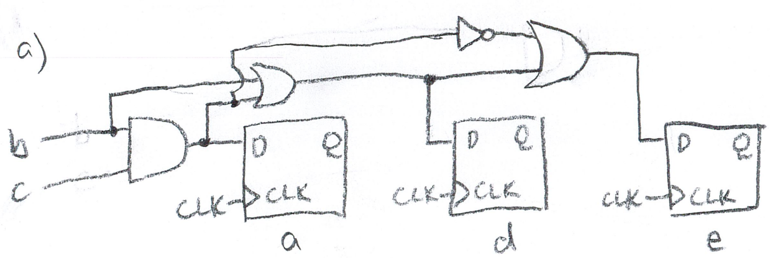
Otherwise, if i=xx1x, y=01. otherwise if i=xxx1, y=00.

i	y
xxx1	00
xx1x	01
x1xx	10
1xxx	11

This is clearly a $\boxed{\text{4-to-2 encoder}}$

Q6|

a)



b)