CMOS

OPEN ENDED

4:1 MULTIPLEXER USING 2:1 MULTIPLEXER

TEAM 21

Abhinav Shetti - 01FE19BEC263

Yash Mahale - 01FE19BEC265

Bharat Gunhalkar - 01FE19BEC274
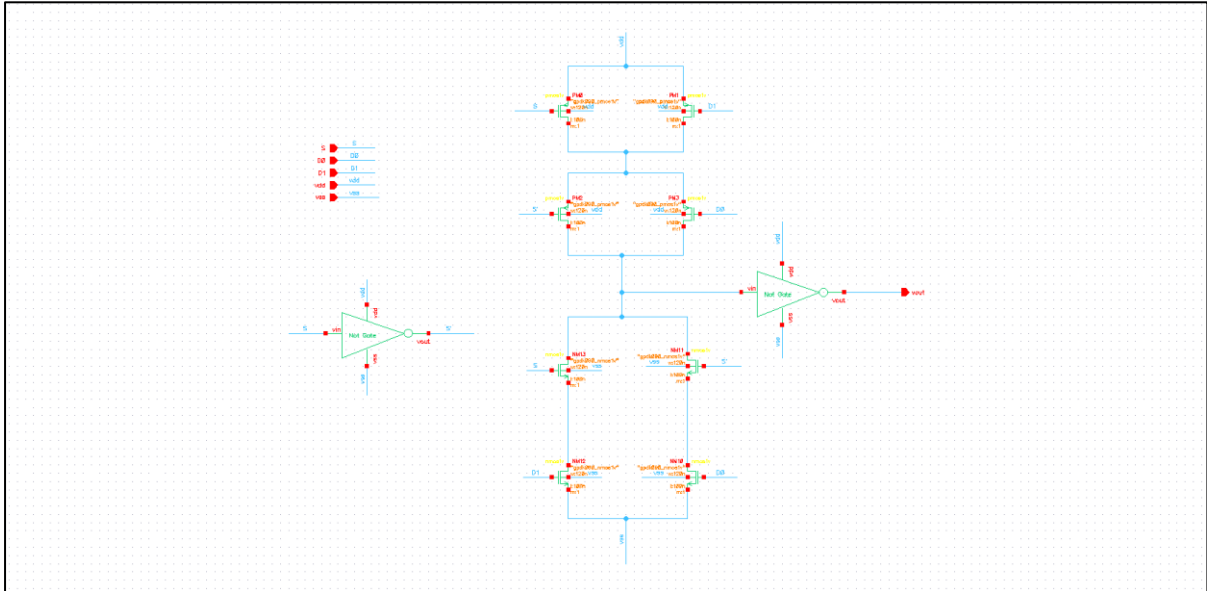
COMPLIMENTARY LOGIC:
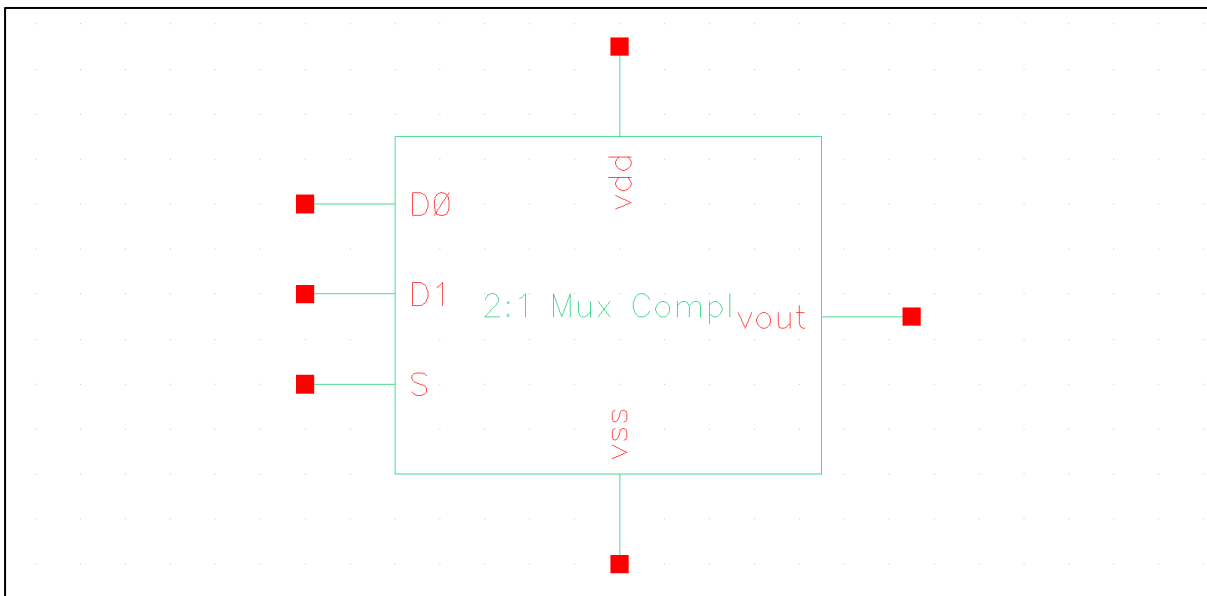
Figure a 2:1 MUX
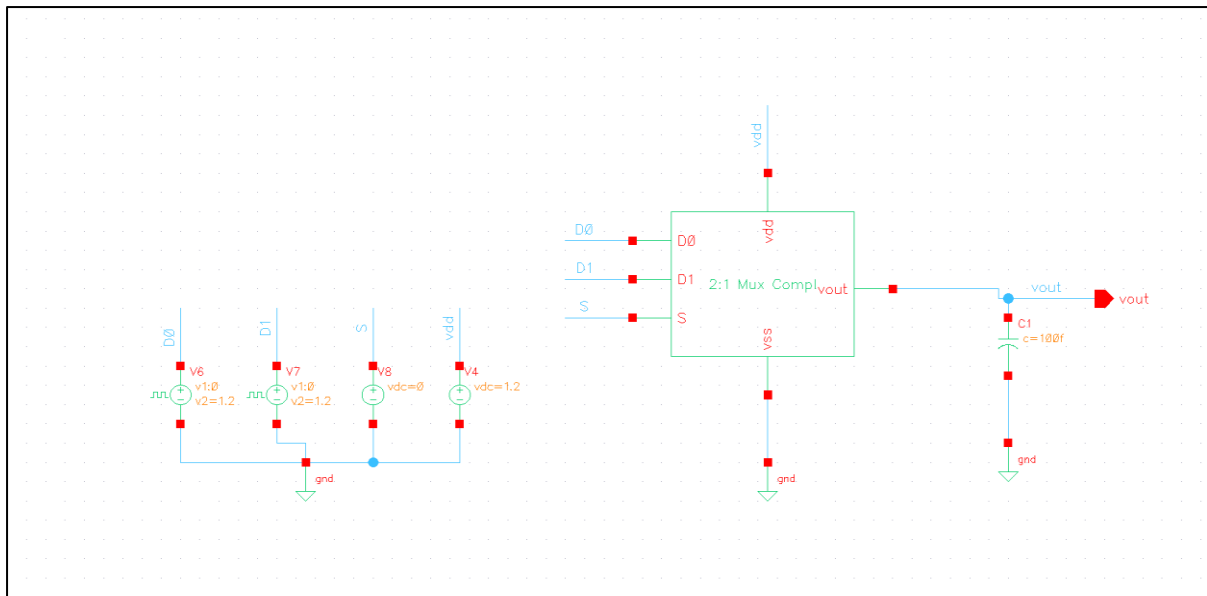

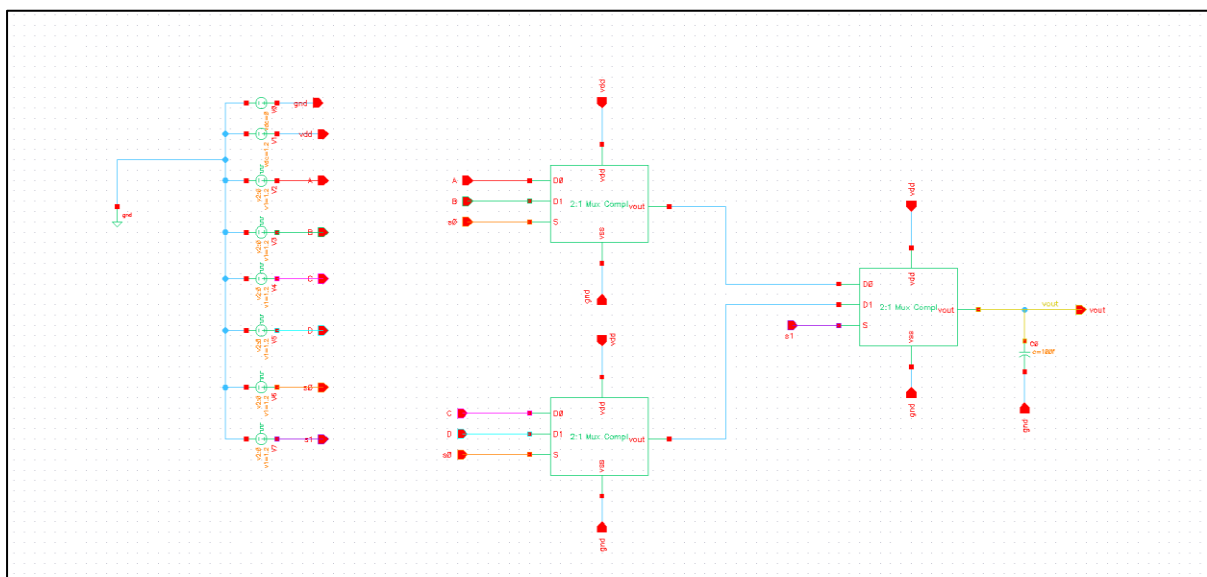*Figure b 2:1 MUX Symbol*

Figure c 2:1 MUX Test CIrcuit
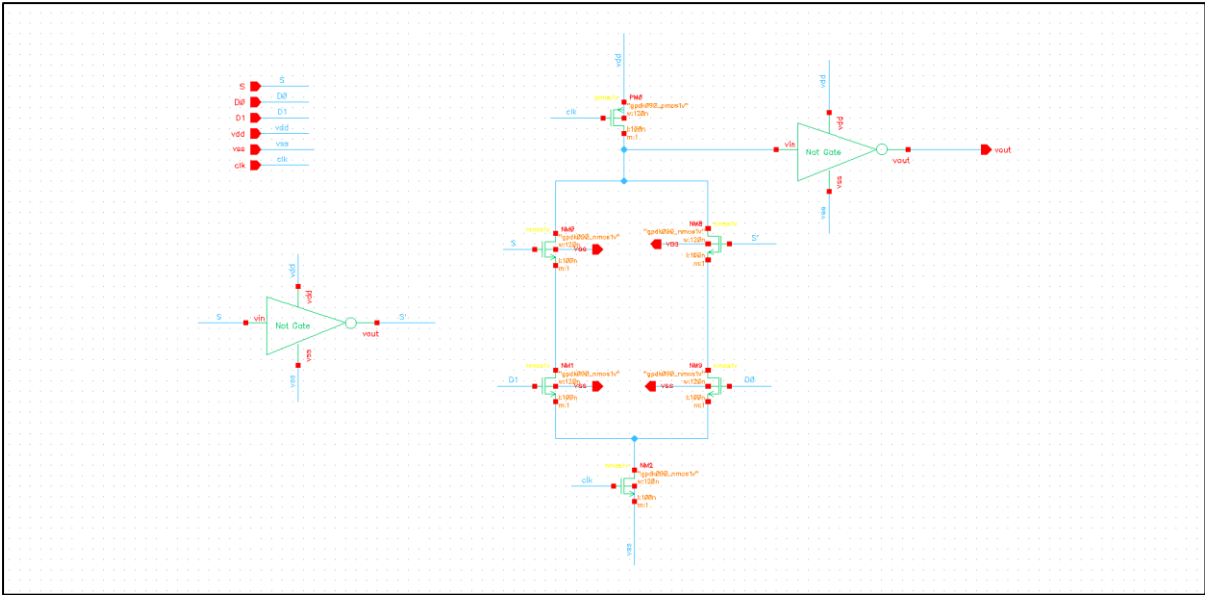
Figure d 4:1 MUX

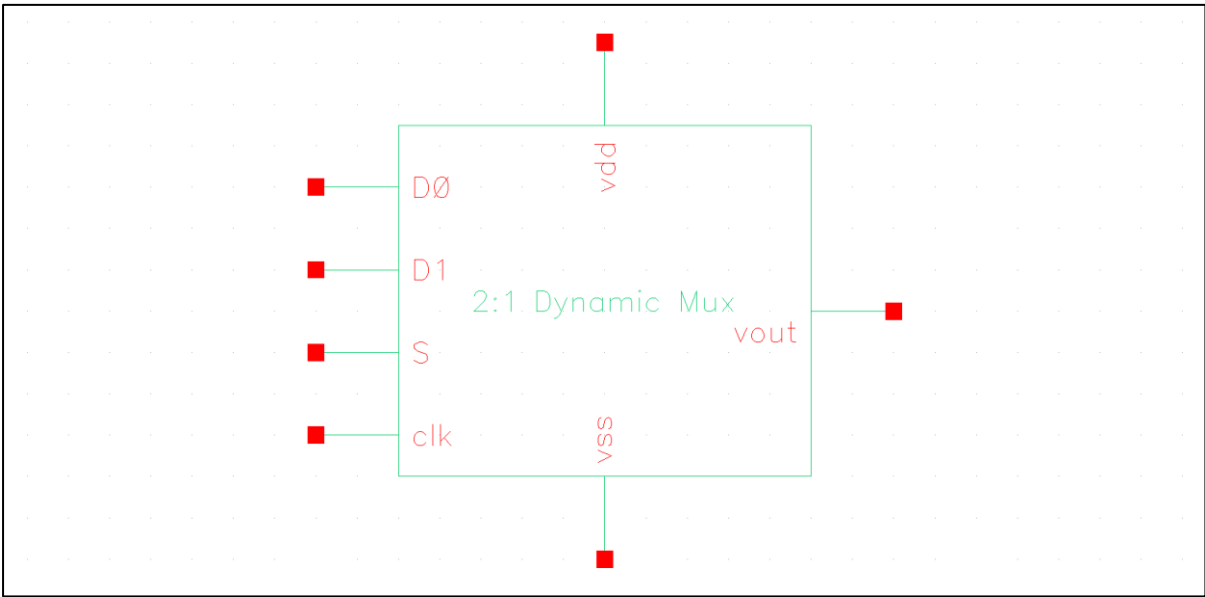# DYNAMIC LOGIC:

Figure e 2:1 MUX

Figure f 2:1 MUX Symbol
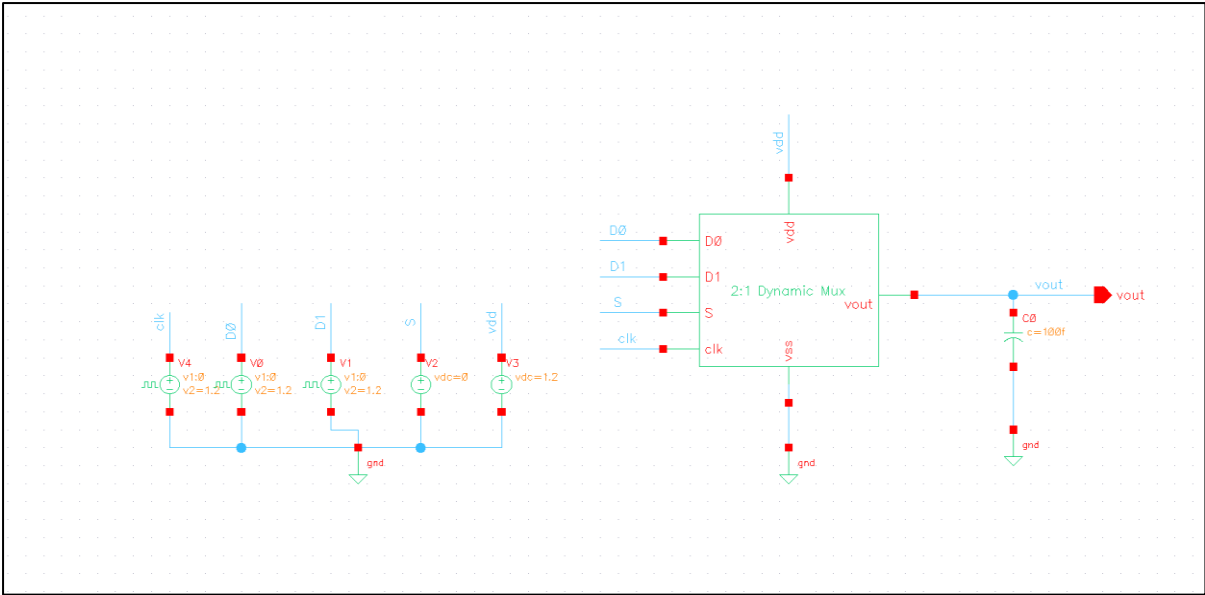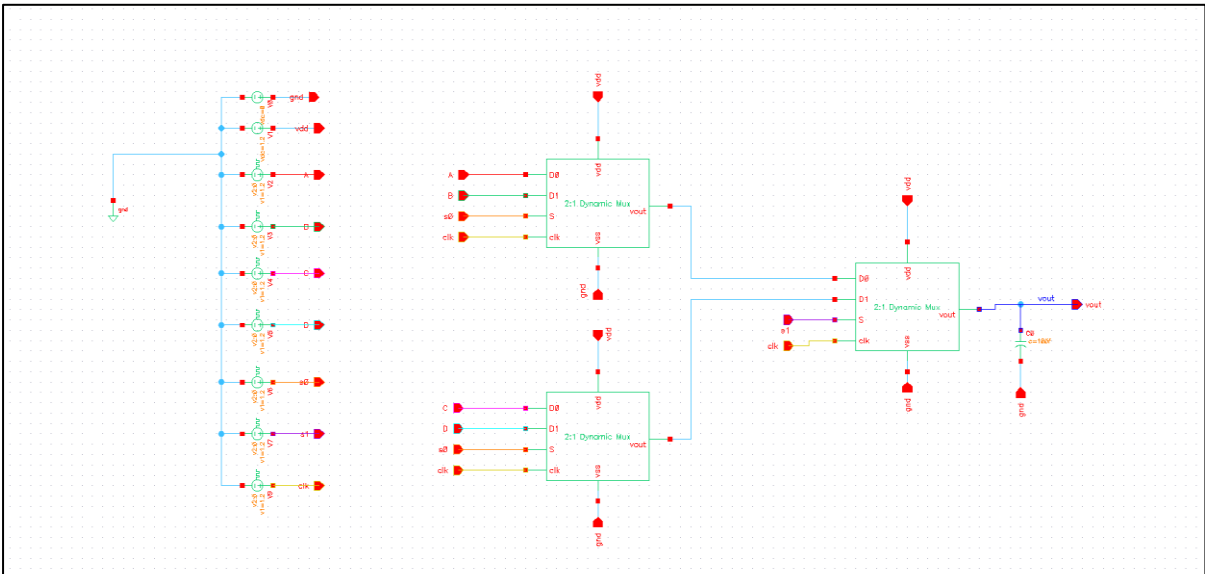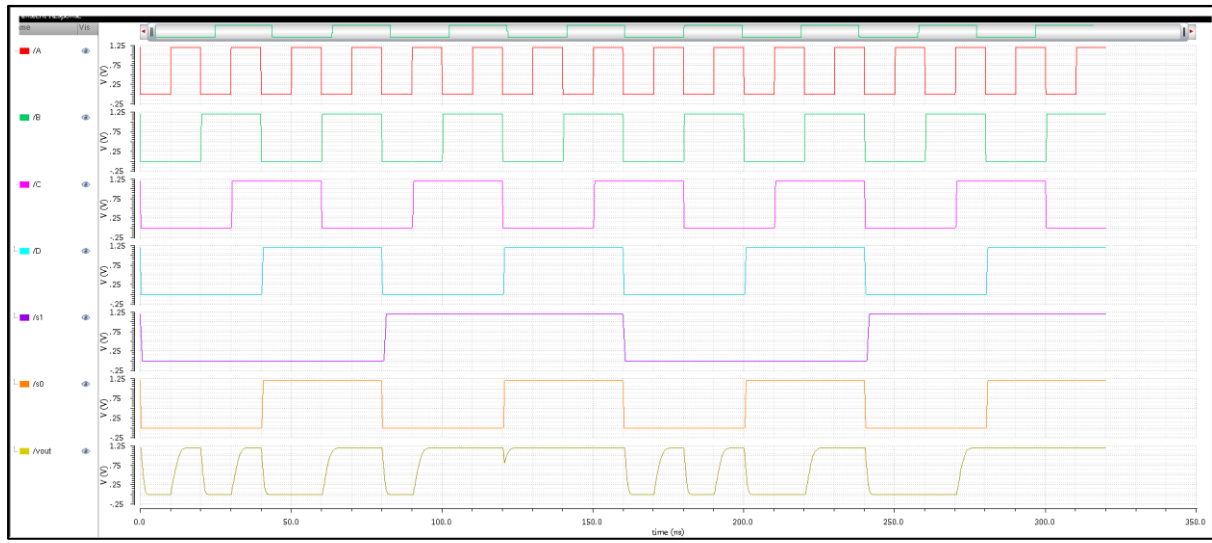
Figure g 2:1 MUX Test Circuit

Figure h 4:1 MUX

RESULTS:

- ## COMPLEMENTARY LOGIC:
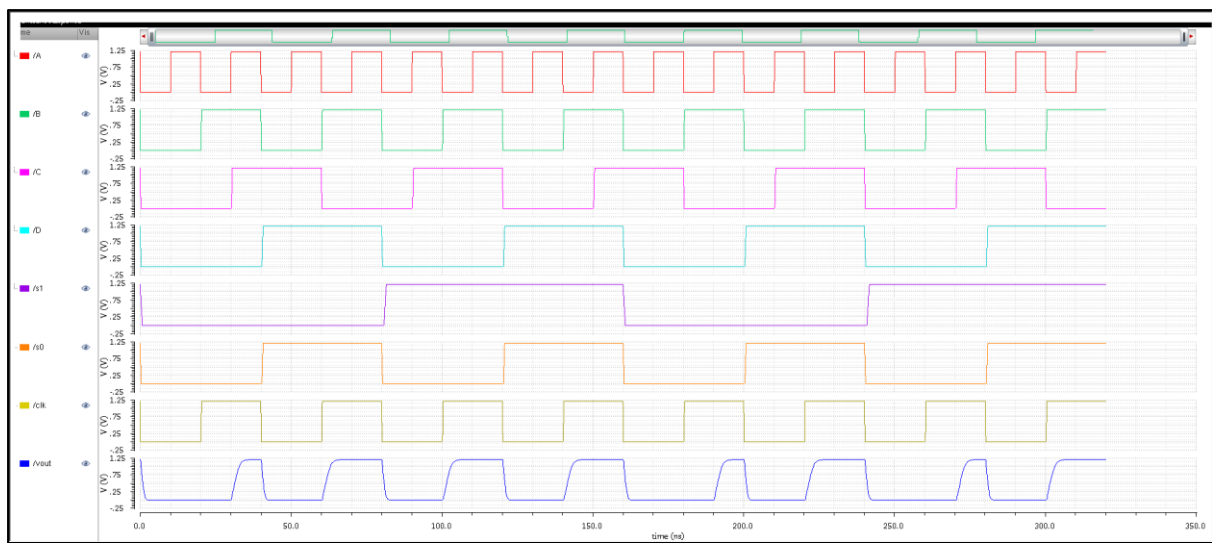
- ## DYNAMIC LOGIC:

CONCLUSION:

	COMPLEMENTARY LOGIC	DYNAMIC LOGIC
Rise Time (t_r)	2.901 ns	2.88 ns
Fall Time (t_f)	1.273 ns	1.27 ns
Area	4320 nm	3600 nm
Power	719.0 mW	455.3 mW