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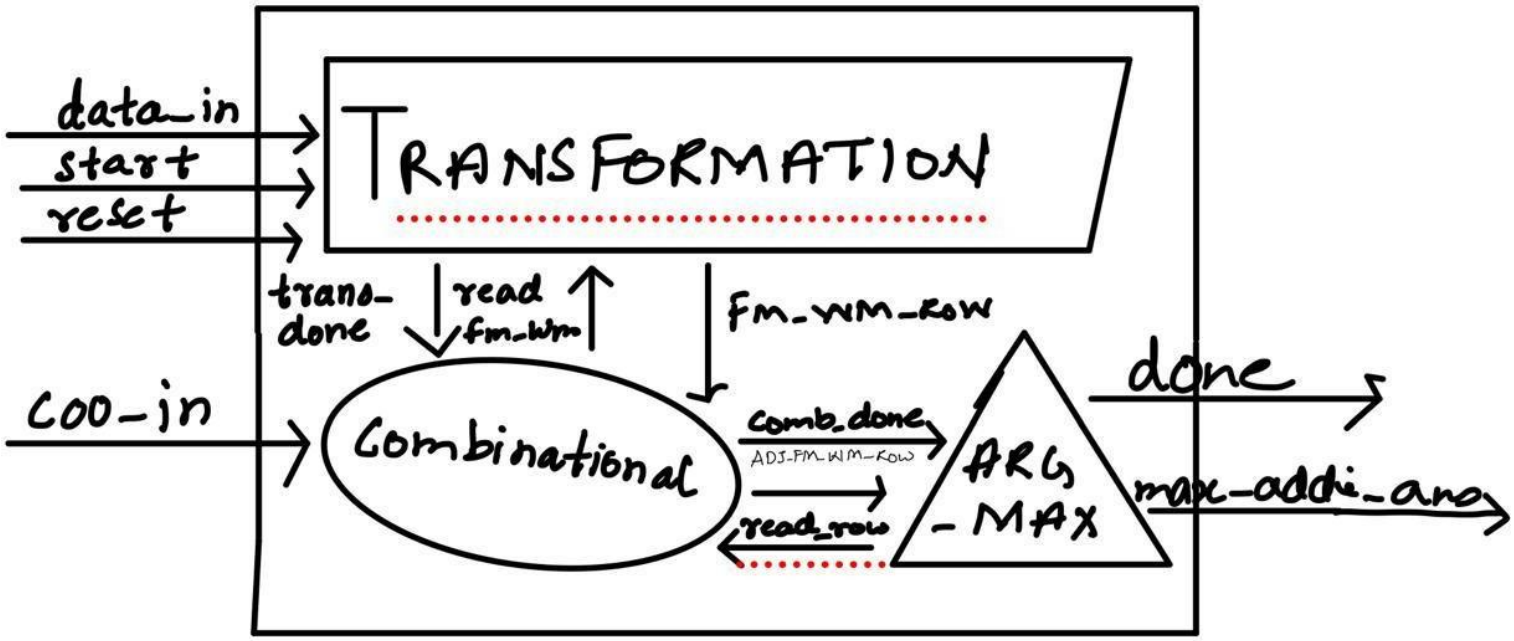
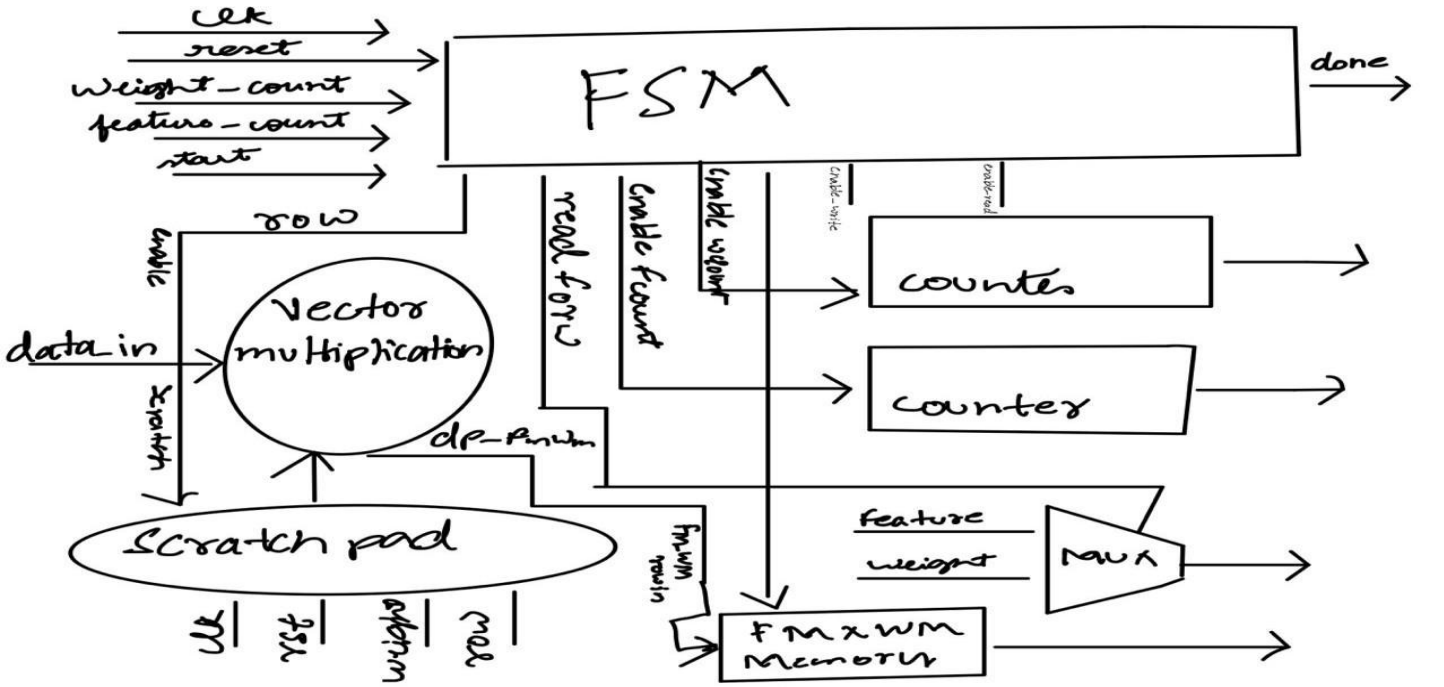
VLSI design lab4_milestone1

EEE 525 LAB 4
Milestone 1

Architecture of every block/High-level Block Diagram:



TRANSFORMATION BLOCK:



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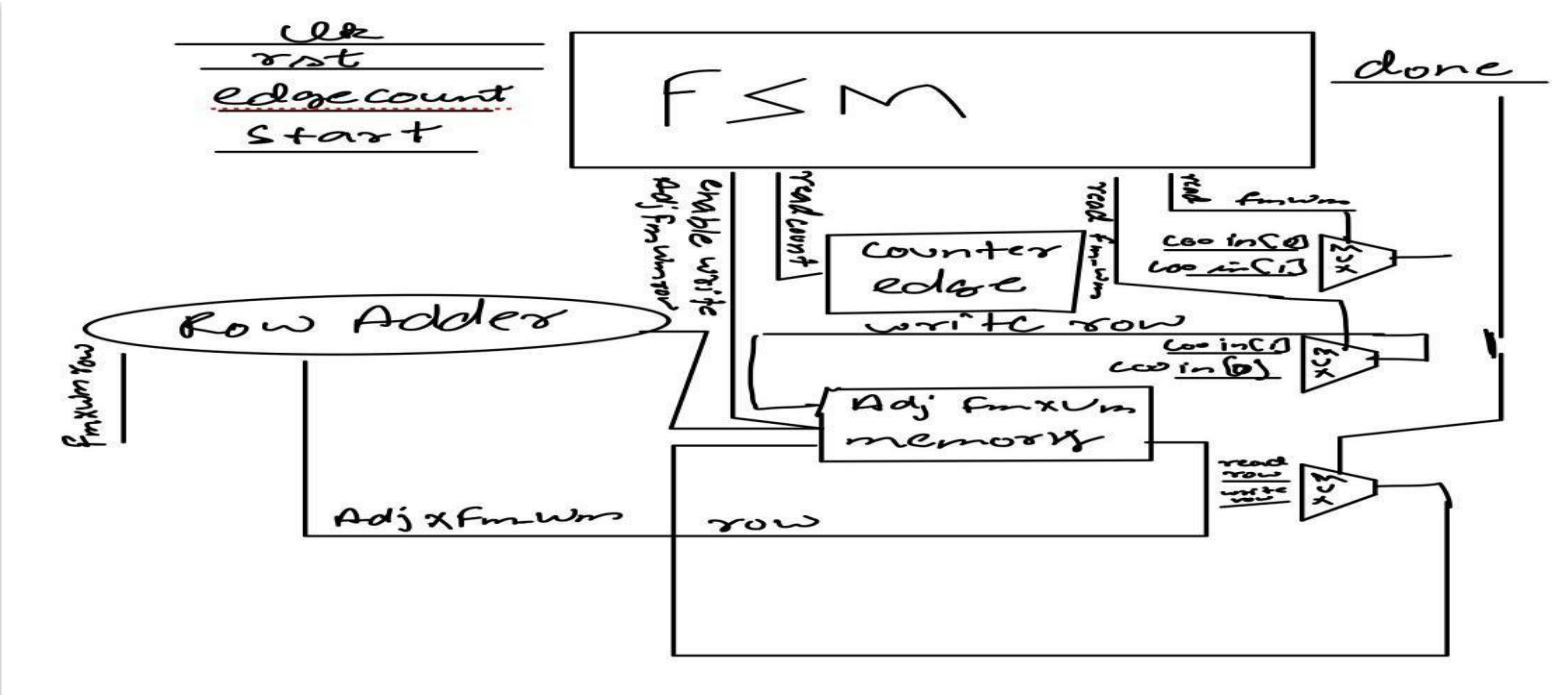
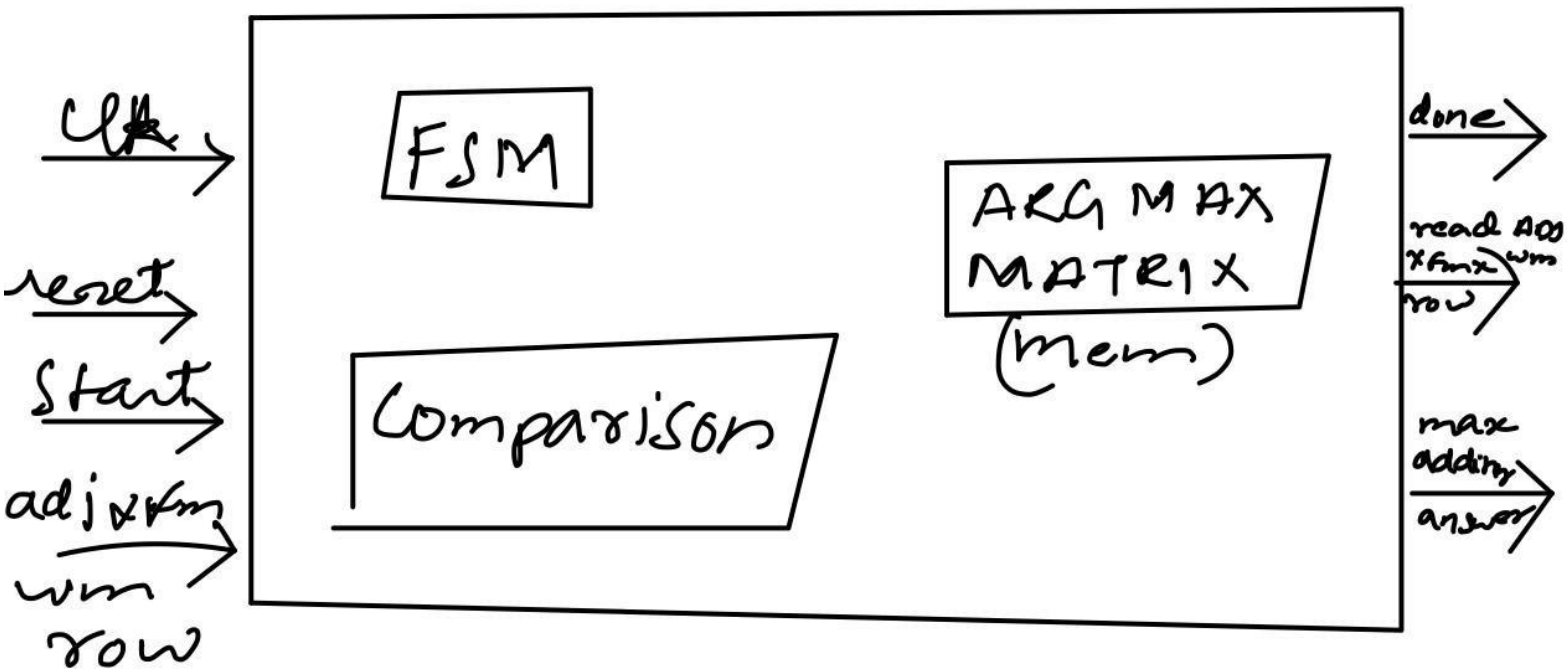
COMBINATION:



ARG_MAX:



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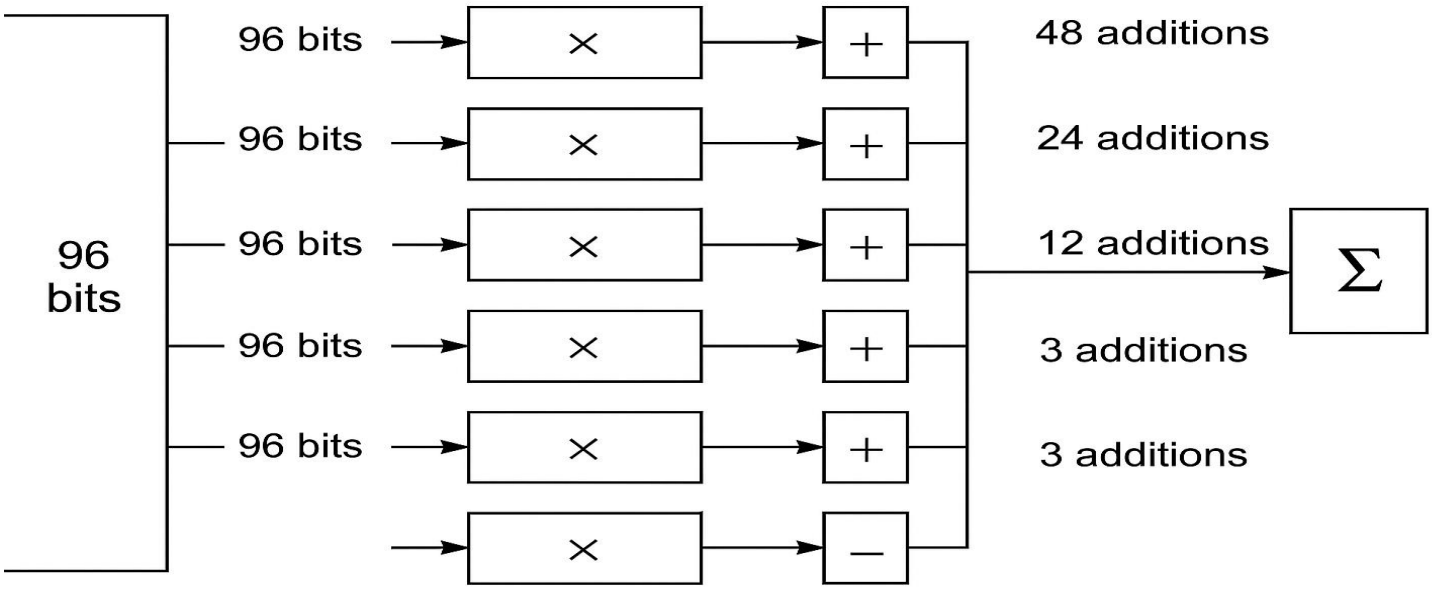
Design decisions: (with 1-2 appropriate figures)

Design choices: (with one or two suitable figurines)
In accordance with the GCN pipeline, we have developed the GCN module for a node classification task employing three primary functional blocks: Transformation, Combination, and Argmax. Below is a high-level architectural block diagram:
Block of Transformation

- For parallel addition calculation, we divided the 96-dimensional feature and weight vectors into 4 sections, each consisting of 48, 24, 12, 6, 3, and 1 components.
- This parallelism meets the <100ns criterion and improves latency.
- A 6x3 FM×WM matrix is produced by the transformation and is kept in memory. • Each 5-bit element is multiplied and accumulated into a 16-bit output.
  Product[96] → Add[48] → Add[24] → Add[12] → Add[6] → Add[3] → Final Add → Output



Combination Block

- An undirected graph's edges are stored in the COO (Coordinate List) input.
- At first, ADJ_FM_WM_Memory's memory addresses are all set to zero.
- The row vectors of the matching source and destination nodes are retrieved and appended for every edge from the FM×WM matrix.
- Efficient sparse aggregation is made possible by the simple vector addition used to accumulate the results into memory.

Argmax Block

- A straightforward max selection logic based on comparison is employed:

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- We begin by assuming that the first element in each row of the 6x3 ADJ_FM_WM_Memory is the maximum.
- After that, contrast it with the other two figures. Update the maximum in accordance with any larger ones.
- The projected class label is represented by the resultant index (2-bit) per row, which is saved in max_addi_answer.

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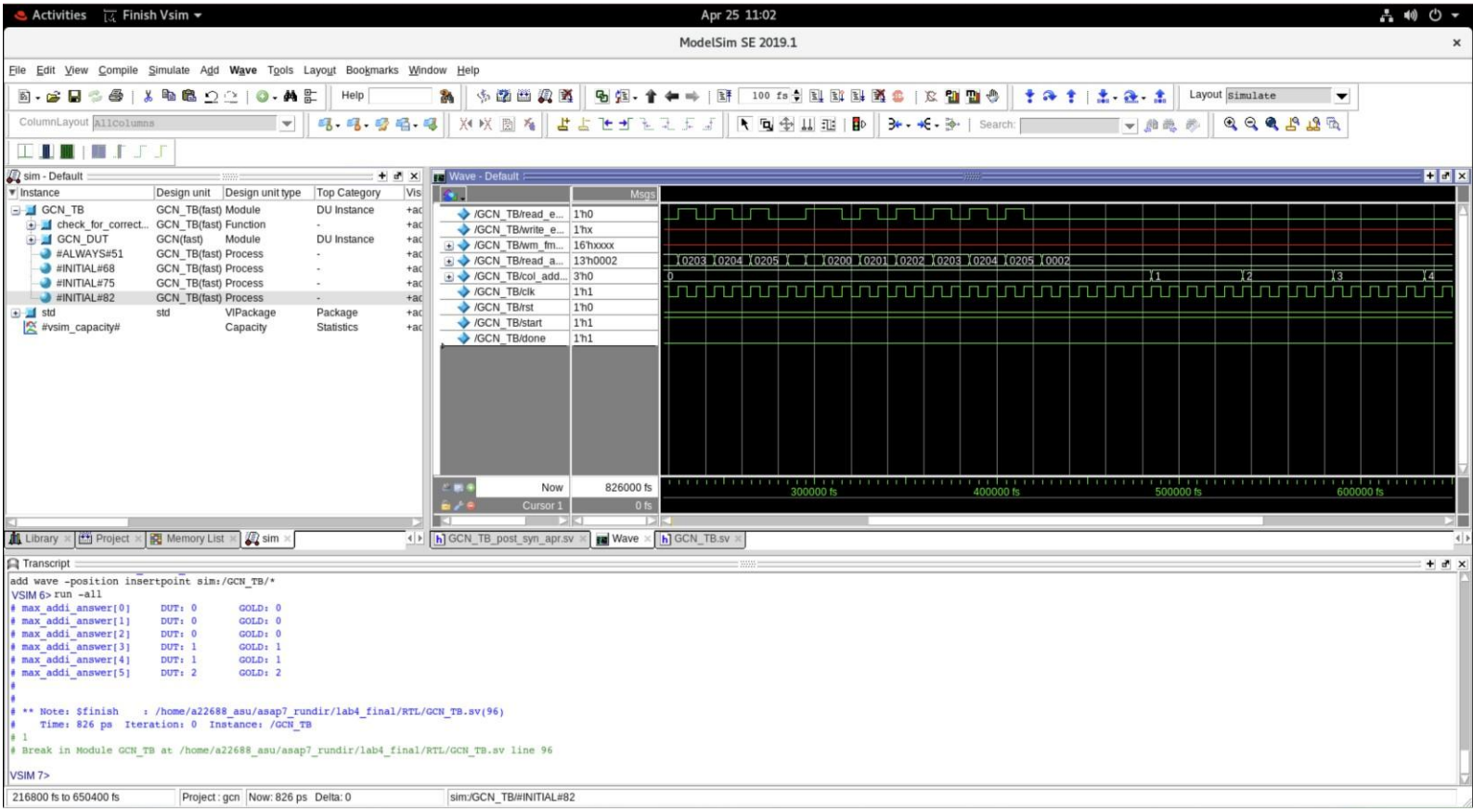
Behavioral Verilog – Simulation:



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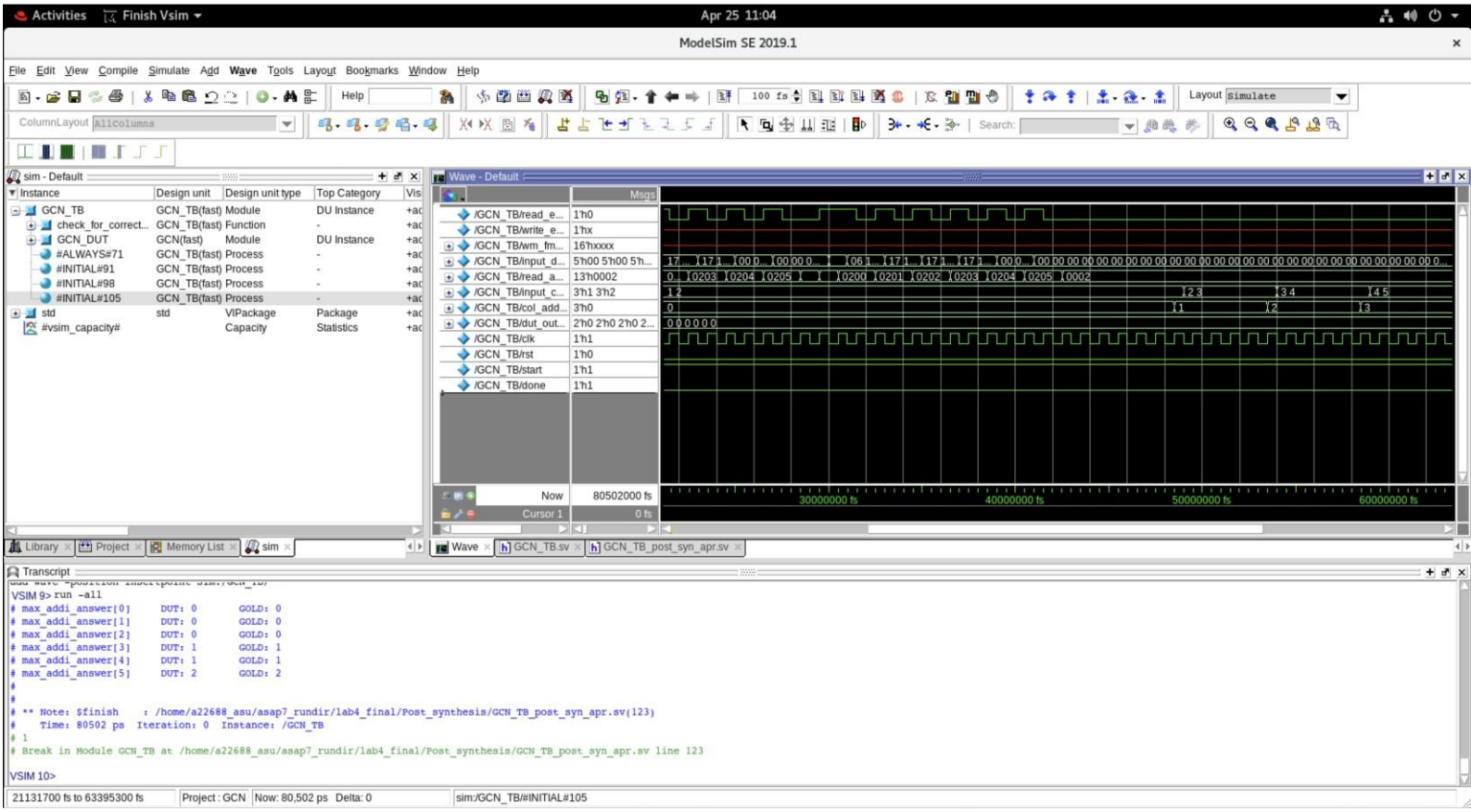
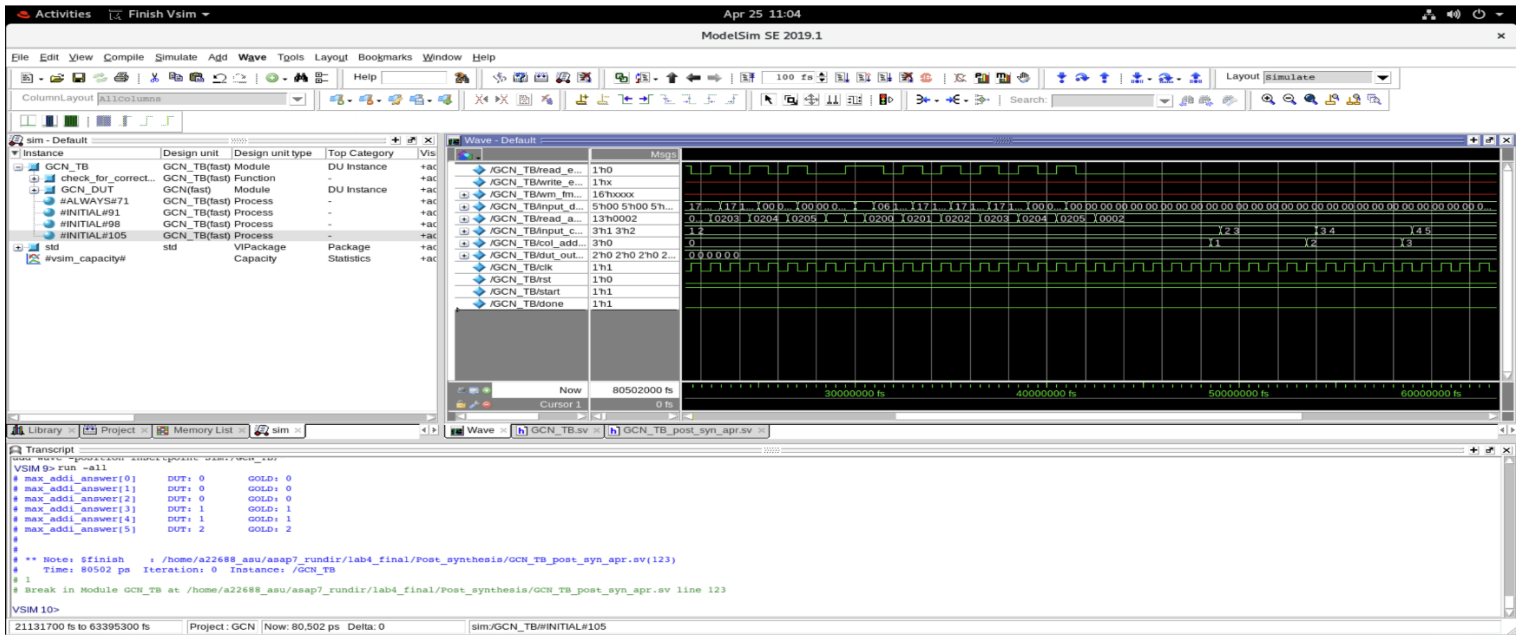
Post_Synthesis – Simulation:



Milestone 2

Total Latency:

- Total Latency: 80.502ns
- Screenshot of Modelsim:



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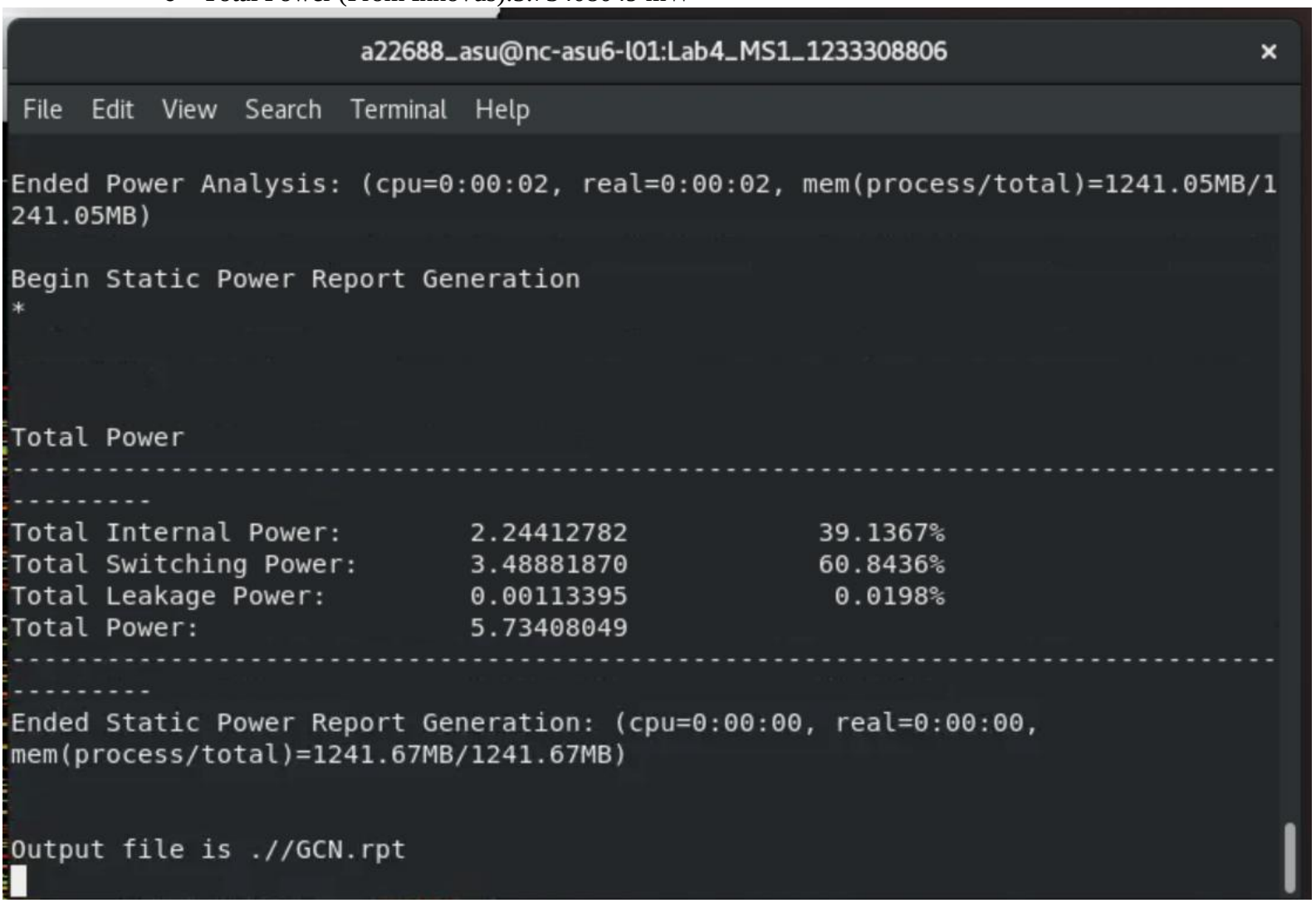
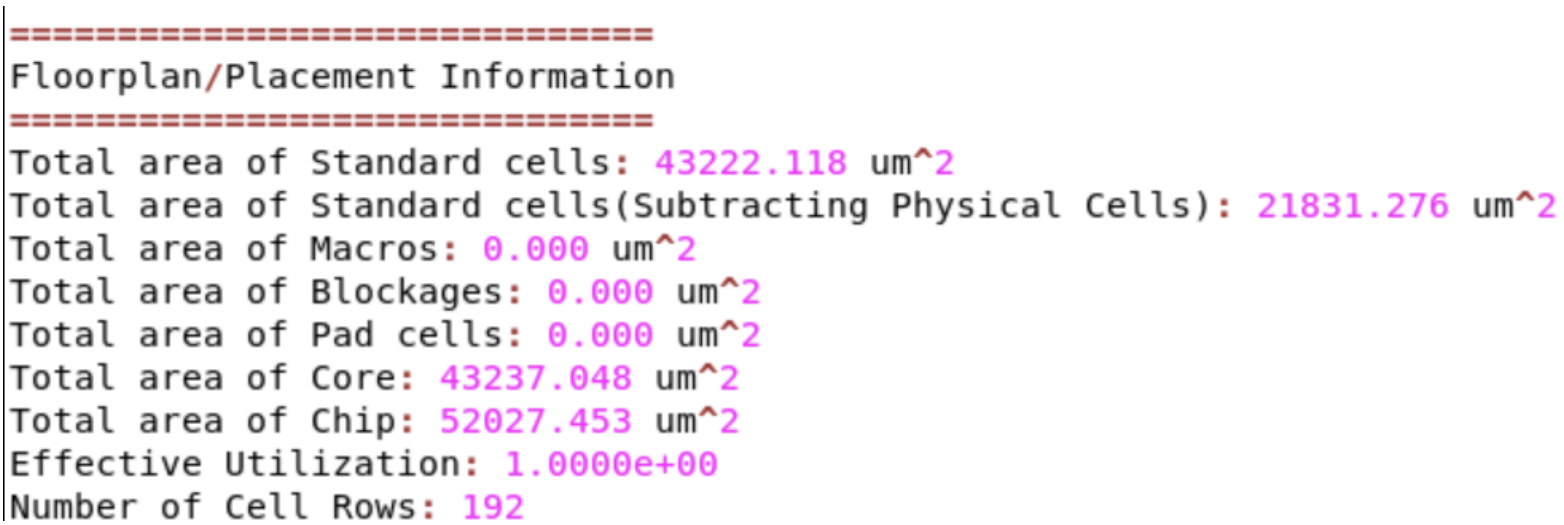
Power:

- Total Power (From Innovus):5.73408049 mW



Area:

- Standard cells + Filler cells: 0.043222118mm^2



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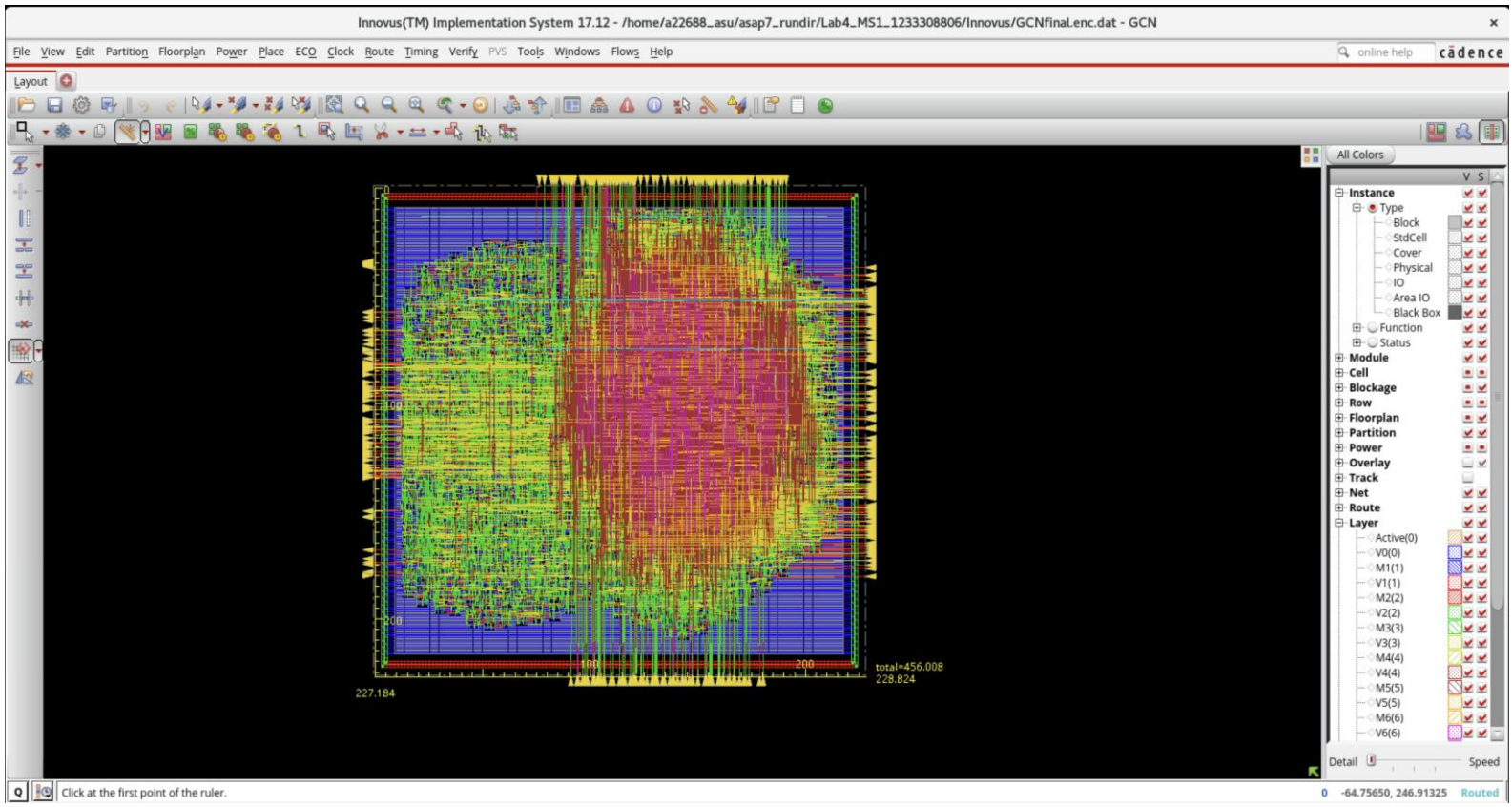

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Innovus density:

- Before filler cell insertion: **0.53621**

Open

GCN_postRoute.summary
~/asap7_rundir/Lab4_MS1_1233308806/Innovus/timingReports

```
#############################################################
#  Generated by:      Cadence Innovus 17.12-s095_1
#  OS:                Linux x86_64(Host ID nc-asu6-l10.apporto.com)
#  Generated on:      Wed Apr 30 03:50:03 2025
#  Design:            GCN
#  Command:           optDesign -postroute
#############################################################

-------------------------------------------------------
     optDesign Final SI Timing Summary
-------------------------------------------------------

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.057  |  0.057  |  0.063  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|  2187   |  1081   |  2182   |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+-------------------+
|                |              Real             |       Total       |
|    DRVs        +------------------+------------+-------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)   |
+----------------+------------------+------------+-------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)        |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)        |
|   max_fanout   |      0 (0)       |     0      |      0 (0)        |
|   max_length   |      0 (0)       |     0      |      0 (0)        |
+----------------+------------------+------------+-------------------+

Density: 53.621%
-------------------------------------------------------
```

Number of gates:

- Gates=31194
- Cells = **11198**

```
a22688_asu@nc-asu6-l09:Innovus

File  Edit  View  Search  Terminal  Help
innovus 4> reportGateCount
Gate area 0.6998 um^2
[0] GCN Gates=31194 Cells=11198 Area=21831.3 um^2
innovus 5>
```

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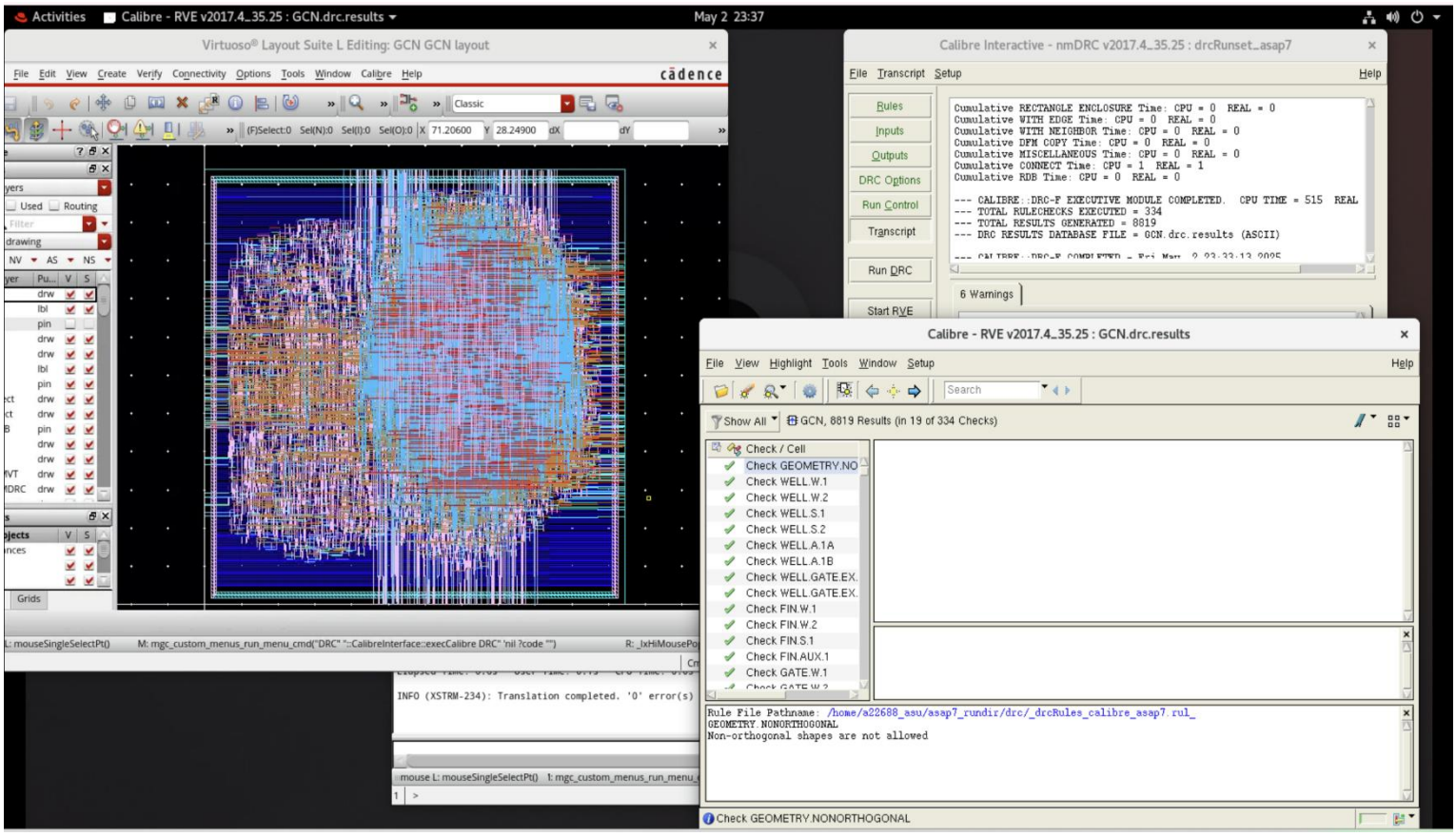
Post_APR – DRC Check:



Post_APR – LVS Check:

Name: Bharath Channaveerayya Hiremath
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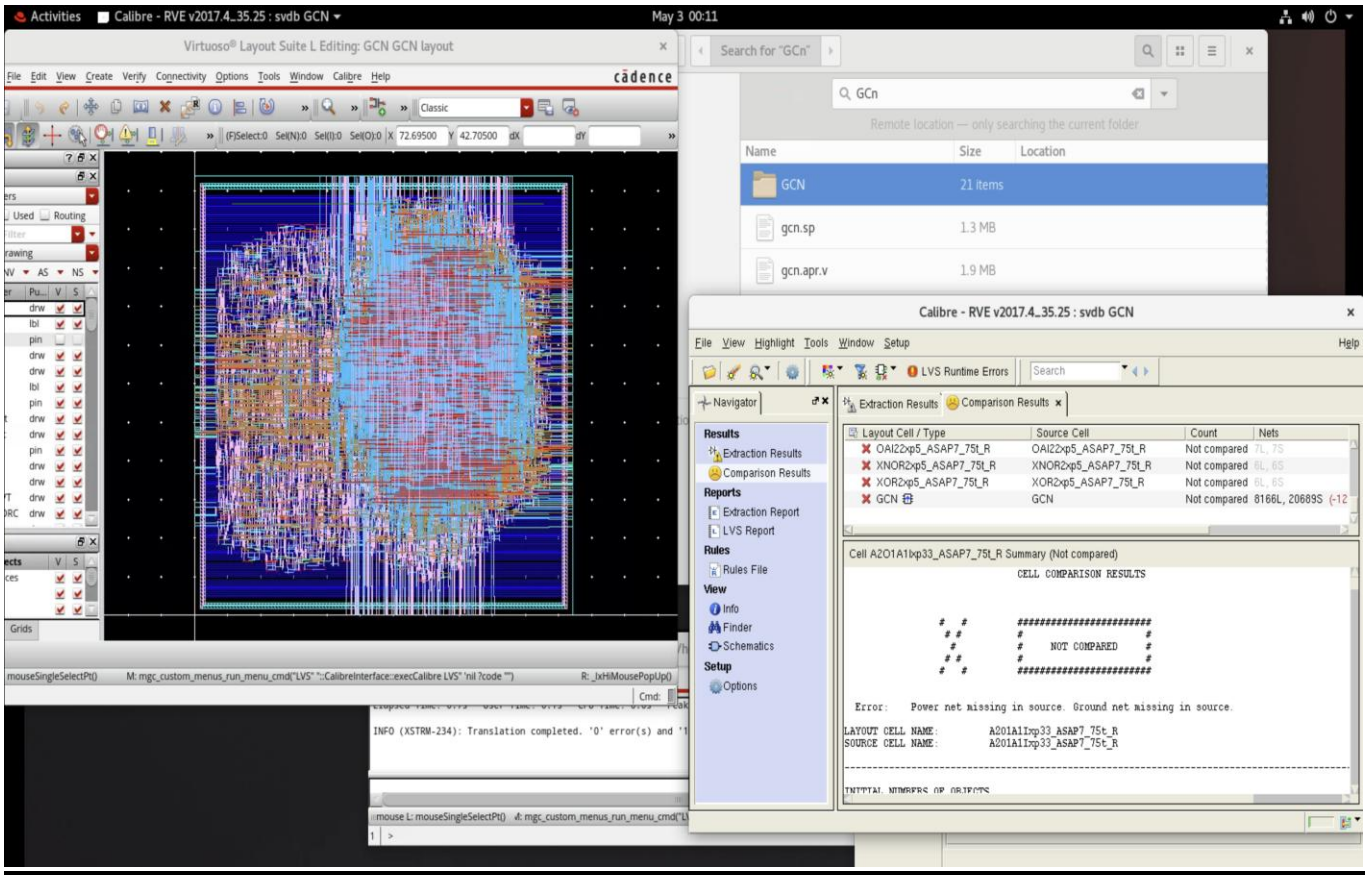

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Activities Text Editor May 2 23:40

Open GCN.conn.rpt
~/asap7_rundir/Lab4_MS1_1233308806/Innovus

```
############################################################
#  Generated by:      Cadence Innovus 17.12-s095_1
#  OS:                Linux x86_64(Host ID nc-asu6-l10.apporto.com)
#  Generated on:      Wed Apr 30 04:01:35 2025
#  Design:            GCN
#  Command:           verifyConnectivity
############################################################
Verify Connectivity Report is created on Wed Apr 30 04:01:35 2025



Multi-CPU acceleration using 16 CPU


Use pthread


Begin Summary
    Found no problems or warnings.
End Summary
```

Screenshot of your timing report for the worstcase hold and setup path

Worst setup timing

Activities Text Editor May 4 01:16

Open GCN_postRoute_all.tarpt
~/asap7_rundir/Lab4_MS1_1233308806/Innovus/timingReports

```
############################################################
#  Generated by:      Cadence Innovus 17.12-s095_1
#  OS:                Linux x86_64(Host ID nc-asu6-l01.apporto.com)
#  Generated on:      Sat May  3 23:55:30 2025
#  Design:            GCN
#  Command:           optDesign -postroute -hold
############################################################
Path 1: MET Setup Check with Pin t0/mem0_mem_reg_4__1__15_/CLK
Endpoint:   t0/mem0_mem_reg_4__1__15_/D (v) checked with  leading edge of 'clk'
Beginpoint: t0/sp0_memory_reg_95__2_/QN (v) triggered by  leading edge of 'clk'
Path Groups: {reg2reg}
Analysis View: default_setup_view
Other End Arrival Time          61.900
- Setup                          5.309
+ Phase Shift                 1000.000
= Required Time               1056.581
- Arrival Time                1000.140
= Slack Time                    56.440
     Clock Rise Edge                     0.000
     + Drive Adjustment                  4.600
     + Source Insertion Delay          -73.160
     = Beginpoint Arrival Time         -68.560
```

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Worst hold timing

Open

GCN_postRoute_all_hold.tarpt
~/asap7_rundir/Lab4_MS1_1233308806/Innovus/timingReports

```
#####################################################################
#  Generated by:      Cadence Innovus 17.12-s095_1
#  OS:                Linux x86_64(Host ID nc-asu6-l01.apporto.com)
#  Generated on:      Sat May  3 23:45:32 2025
#  Design:            GCN
#  Command:           optDesign -postroute -hold
#####################################################################
Path 1: MET Hold Check with Pin t0/sp0_memory_reg_71__0_/CLK
Endpoint:   t0/sp0_memory_reg_71__0_/D (v) checked with  leading edge of 'clk'
Beginpoint: data_in[120]               (v) triggered by  leading edge of 'clk'
Path Groups: {clk}
Analysis View: default_hold_view
Other End Arrival Time          5.590
+ Hold                         14.509
+ Phase Shift                   0.000
= Required Time                20.108
  Arrival Time                 20.100
  Slack Time                   -0.009
     Clock Rise Edge                        0.000
     + Input Delay                          0.100
     + Drive Adjustment                     3.100
     = Beginpoint Arrival Time              3.200
```