LOW POWER CMOS FULL ADDER DESIGN

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ABSTRACT

This Paper deals with low power Cmos full adder using 28nm Technology by taking merits of existing full-adders. In the present day scenario the world is moving forward to reduce the power consumption of the electronic devices we use. The proposed one-bit full adder has minimal power consumption when compared to a conventional Full adder. The proposed adder compared and then analyzed average power, Area and Max power with existing full adder.

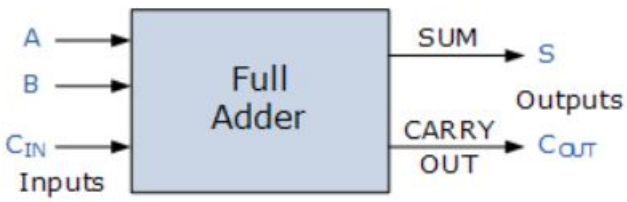
1. REFERENCE CIRCUIT DETAILS

With continuous increase in complexity and number of components on integrated circuits, power consumption of VLSI (very large scale integration) circuits is increasing at a rapid rate.. Large power consumption affects the circuit operation and reliability by increasing temperature of circuits which is not desirable.s. Full adders being core building blocks in different VLSI circuits like comparators, Performance of adder circuit highly affects the overall capability of the system.The block diagram of a conventional full adder circuit consists of three inputs and we obtain the outputs as sum and carry. The inputs can be denoted as A, B, Cin and the outputs can be represented by Sum and Cout.

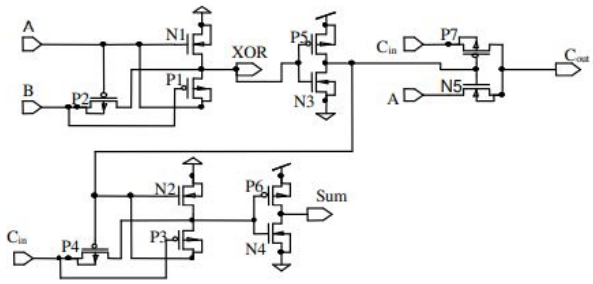
SUM=(A$\oplus B) \oplus Cin$
$Cout = A.B + Cin(A \oplus B)$

2. REFERENCE CIRCUIT

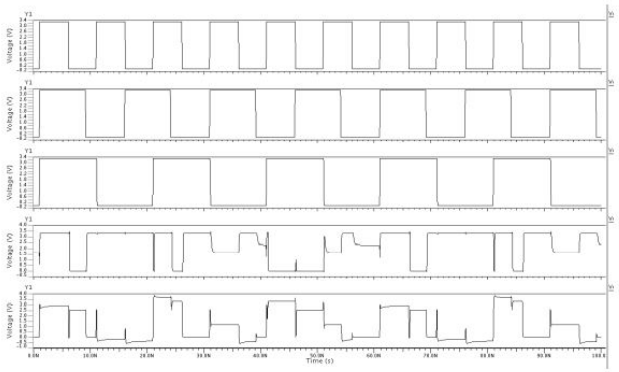
2.1. Block Diagram



2.2. Schematic



3. REFERENCE CIRCUIT WAVEFORMS



4. REFERENCES

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