



COL215 – DIGITAL LOGIC AND SYSTEM DESIGN

Department of Computer Science & Engineering,
IIT Delhi

Semester I, 2025 - 26

Lab Assignment 2 (Friday) : 7 Segment Display

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1. INTRODUCTION

- The purpose of this project is to design and implement a hardware circuit using Verilog on the Basys3 FPGA board that displays decimal digits 0-9 on a 7-segment display based on switch inputs. The project aims to demonstrate the process of reading binary inputs from physical switches (SW0-SW9) and driving an active-low 7-segment display to display the correct digit.
- The hardware platform used is the Basys 3 FPGA Board. The design process includes coding in Verilog, functional simulation, synthesis, implementation, and on-board testing.

2. DESIGN DECISIONS

Each digit corresponds to one dedicated input signal (`ze`, `on`, `tw`, `th`, `fo`, `fi`, `si`, `se`, `ei`, `ni`), representing the numbers 0 through 9, respectively.

Input Method

- Each digit is selected by setting its corresponding input signal to logic `1` while keeping the rest at `0`. We write the `if` statement for `ni`, then `if else` for `ei`, and so on. So that if two or more switches are set to `1`, the greatest number should be displayed on the screen.

Output Control

- The outputs `a` to `g` represent the seven segments of the display. The output `an0` controls the enable signal for the first

(rightmost) 7-segment display on the Basys3 board. Since the Basys3 uses common-anode 7-segment displays, a segment is turned ON by setting it to logic **0** (active-low).

Logic Implementation

- At the start of each evaluation (**always @(*)** block), all segments and the anode are set to logic **1** (OFF state). Depending on which digit input is active, specific segments are set to **0** to form the correct digit shape. Each digit's pattern is defined according to the standard 7-segment display segment evaluation table. Example:

Digit 1 (on == 1) → Segments **b** and **c** are ON (rest OFF).

Digit 2 (tw == 1) → Segments **a, b, d, e**, and **g** are ON.

Digit 8 (ei == 1) → All segments ON.

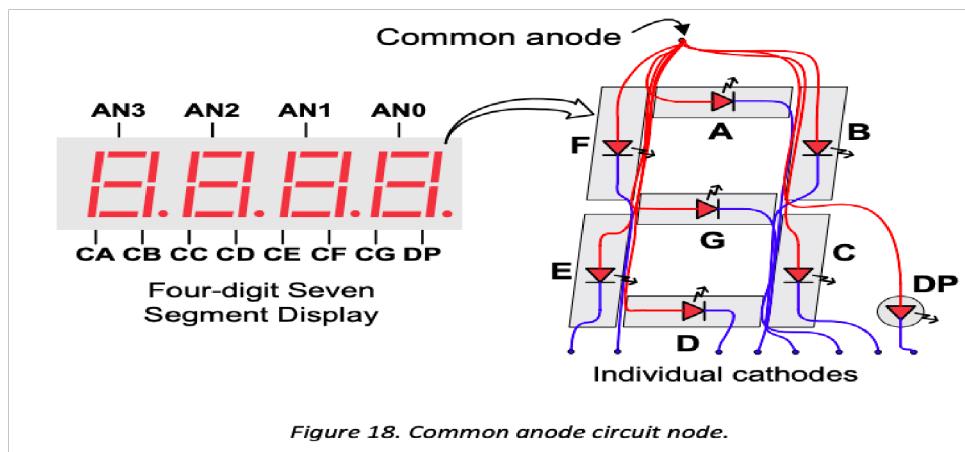
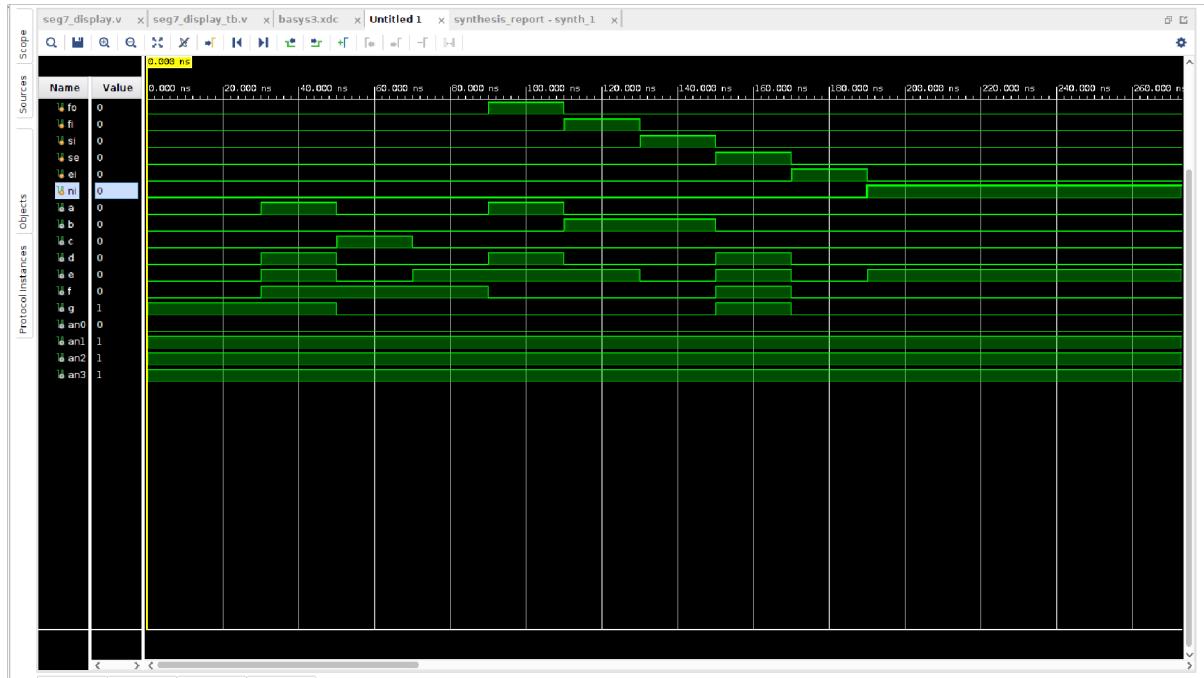
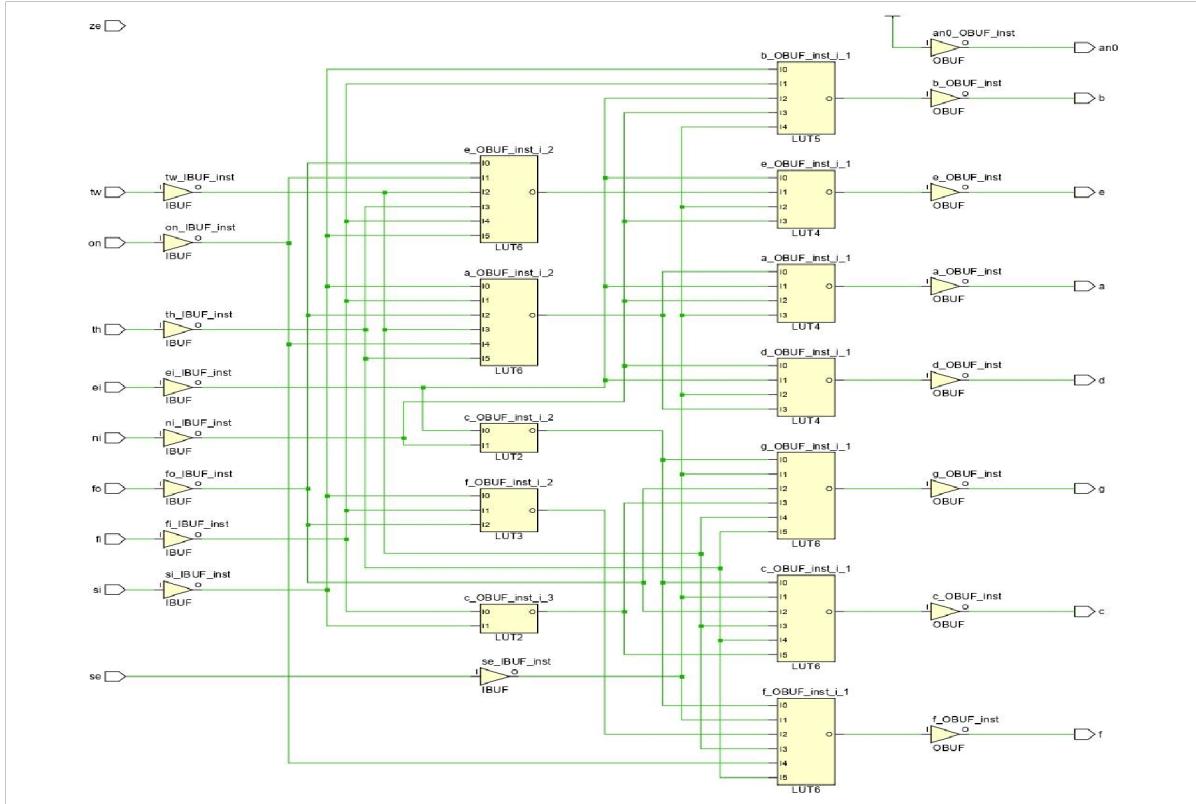


Figure 18. Common anode circuit node.

3. SIMULATION SNAPSHOTS



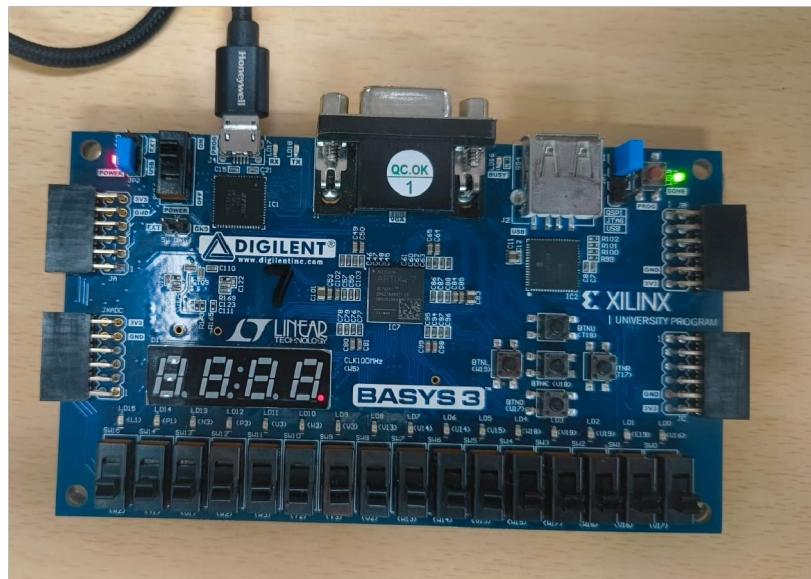
4. SCHEMATICS



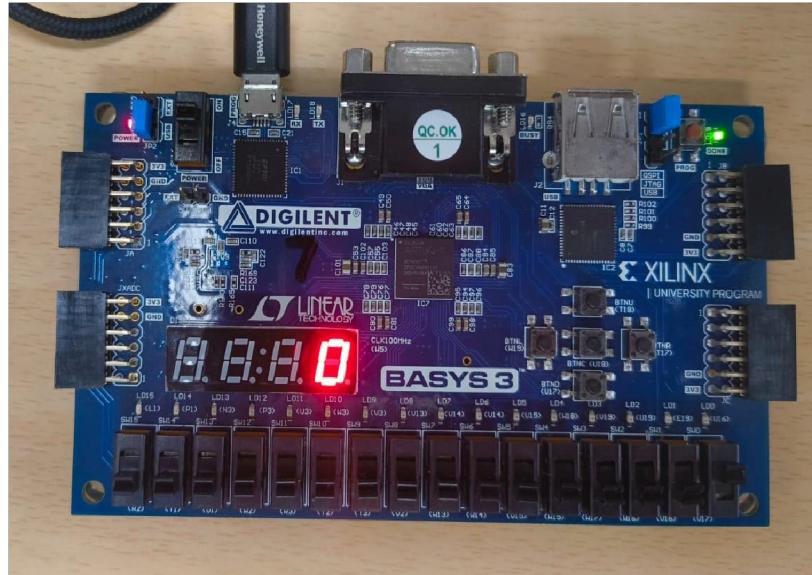
5. SYNTHESIS REPORT

Name	Constraints	Status	WNS	THS	WHS	WBS5	TPWS	Total Power	Failed Routes	Methodology	QoR Score	QoR Suggestions	LUT	FF	BRAM	URAM	DSP	Start	End
synth_1	constrs_1	synth_design Complete!											12	0	0	0	0	8/8/25, 2:41 PM	0
Impl_1	constrs_1	Running Design Initialization...																8/8/25, 2:41 PM	0

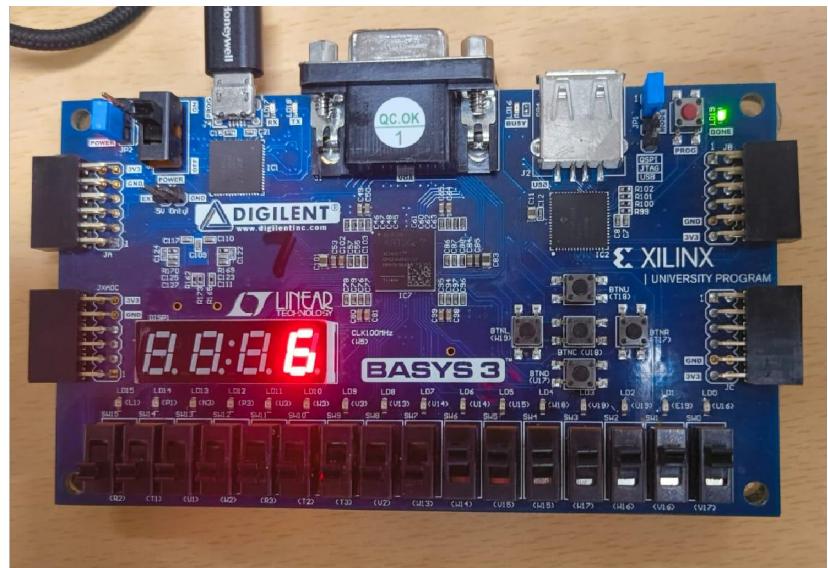
6. ON BOARD IMPLEMENTATION



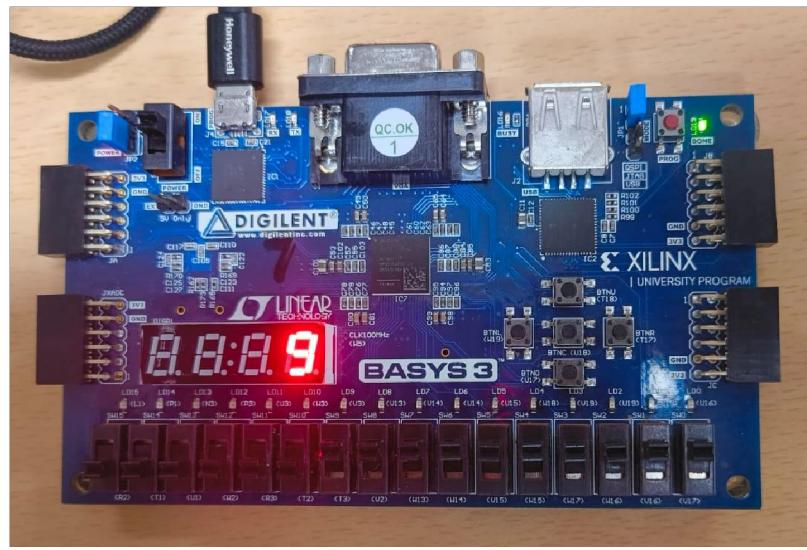
No output is given when all the switches are 0 .



Output is 0 when only **on** switch is set to 1.



Output is 6 when switches(**ze, on, tw, th, fo, fi, si**)
are set to 1.



Output is 9 when all the switches are set to **1**.