

## **COL – 215**

### **LAB ASSIGNMENT – 1(FRIDAY)**

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### **LAB DECISIONS**

Uses the code for AND\_gate and basys3.xdc file  
modifies the same code for OR\_gate and NOT\_gate and modifies the  
basys3.xdc file.

### **LAB WORK**

Set up the GCL for Vivado

Make a new project named “project\_1” in Vivado.

Create a new file named ‘AND\_gate’ and in it add the basys3.xdc file and then  
code the AND\_gate file.

Simulated the design for the AND\_gate and changed the value under force  
constants, and observe the changes

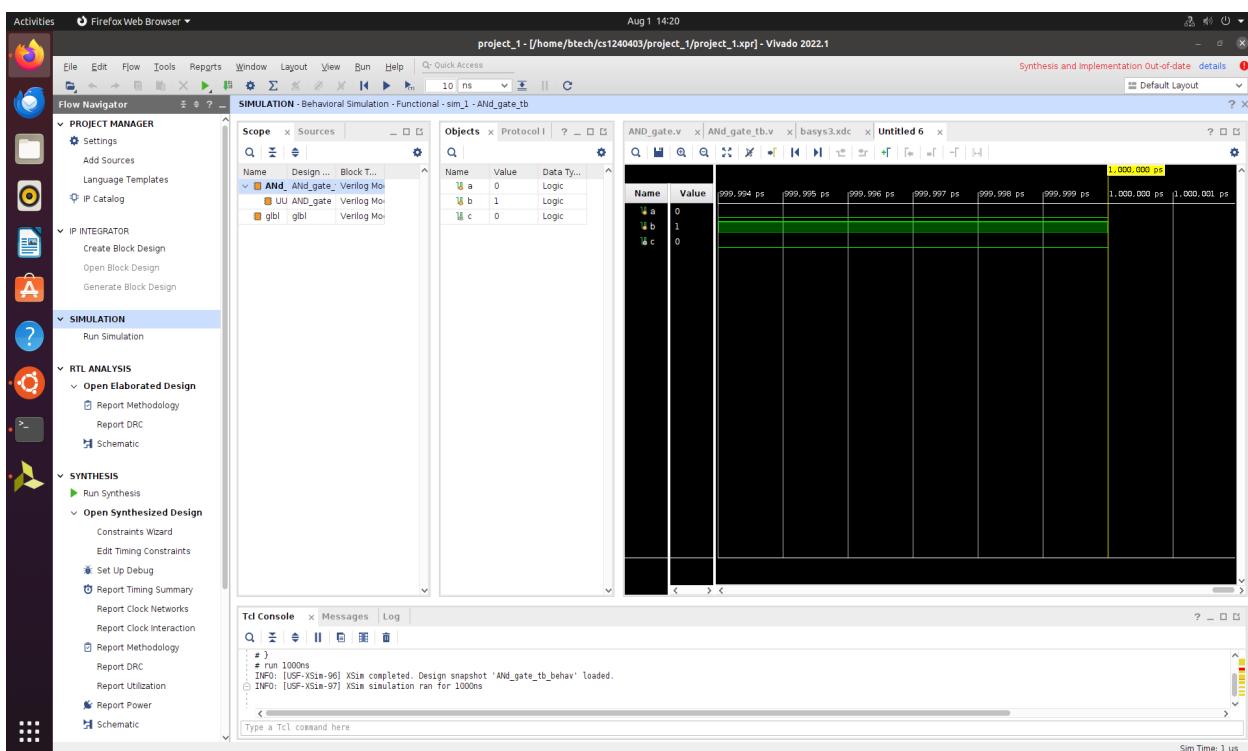
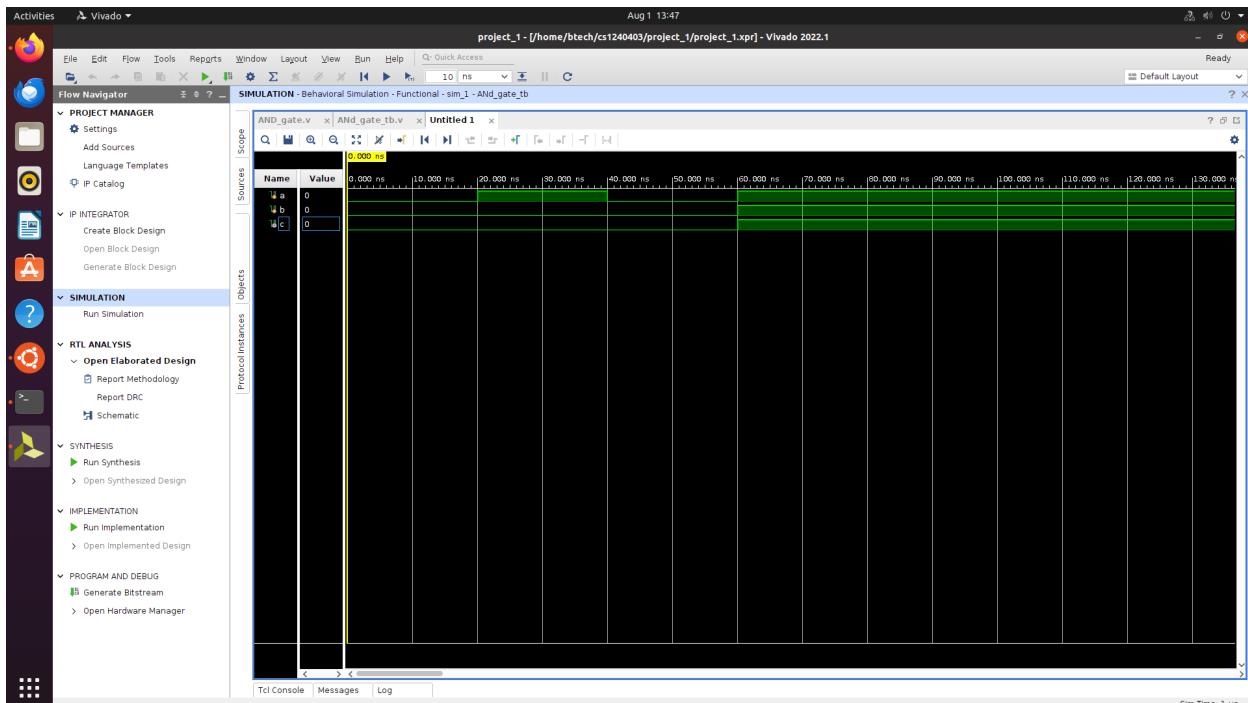
Edited the .xdc file and then ran synthesis, followed by run implementation.

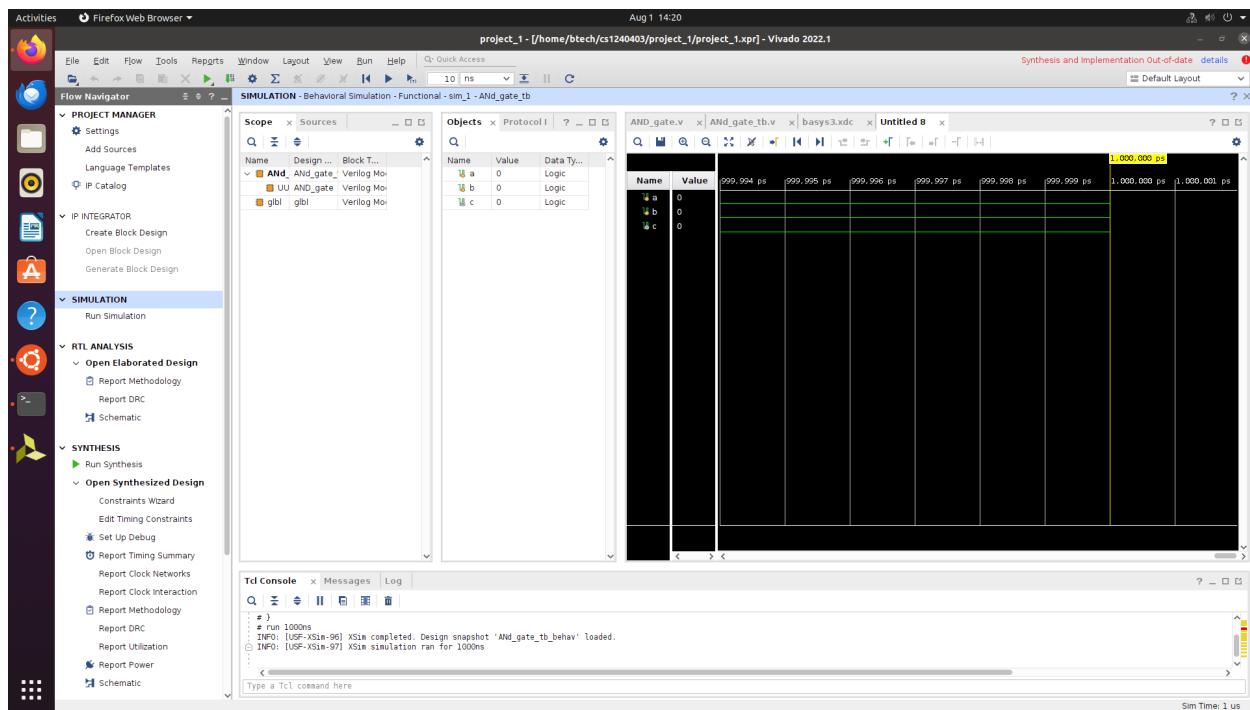
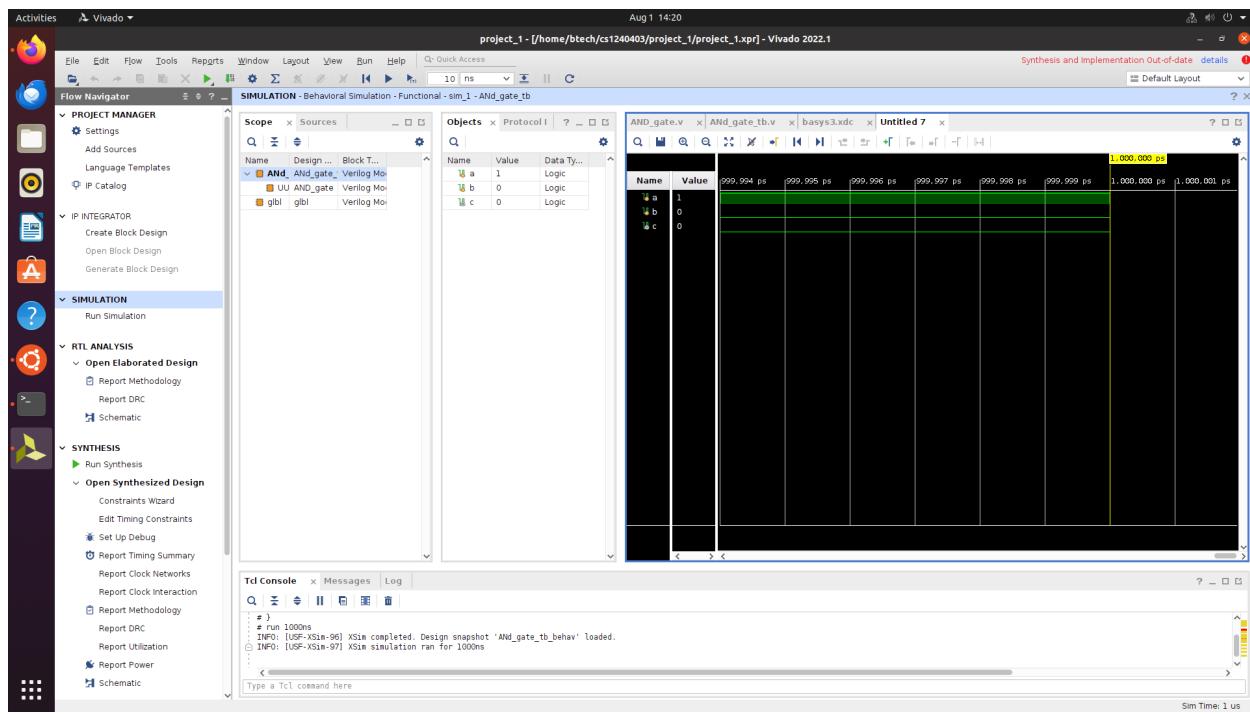
Generated the bitstream and then uploaded the code on the FPGA board.

And then repeated the same process for the OR\_gate and NOT\_gate.

### **SIMULATION SNAPSHOTS**

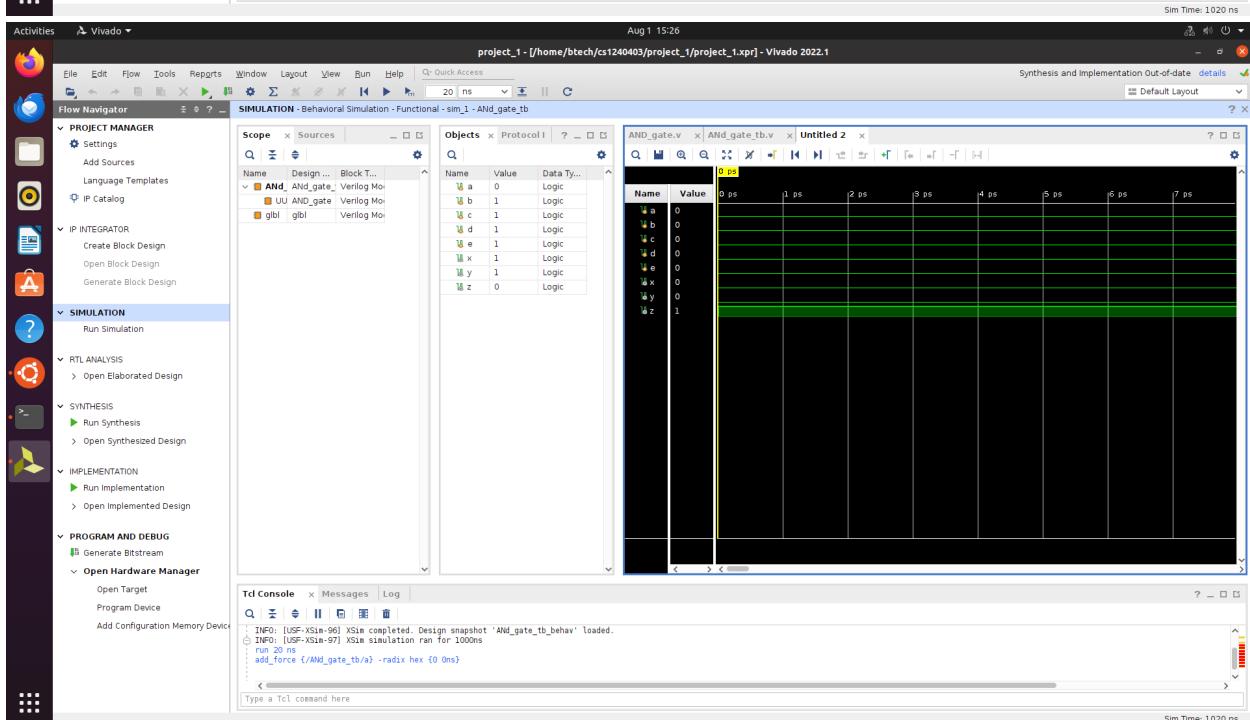
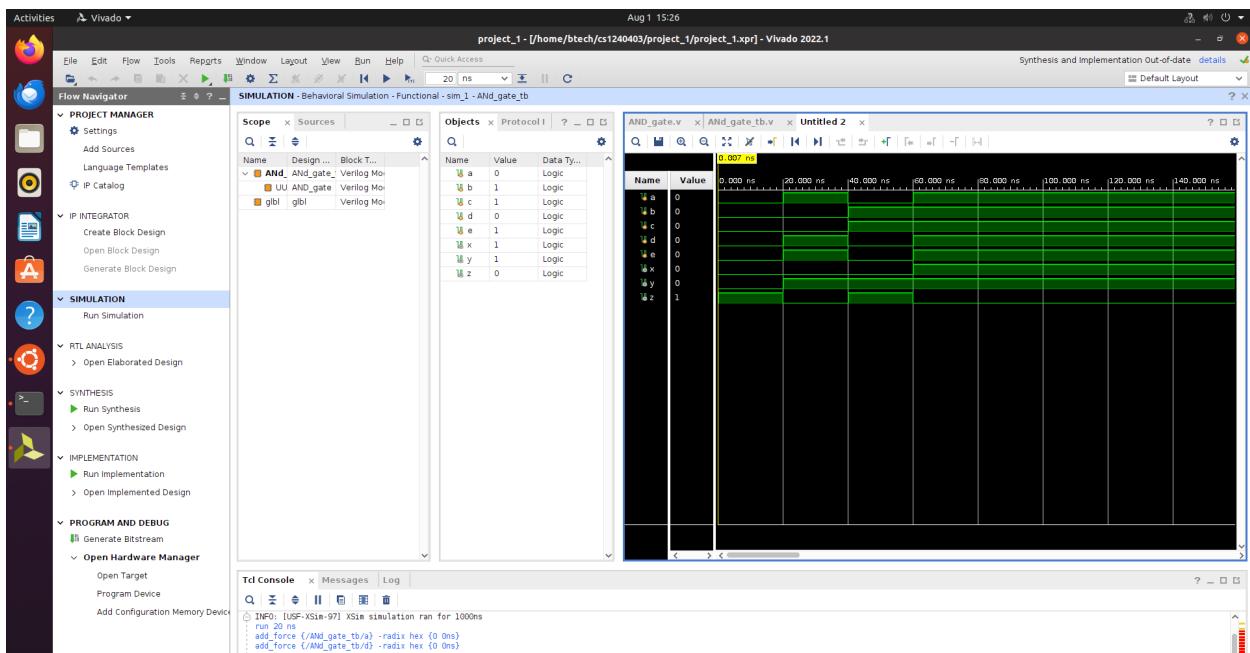
## AND\_gate

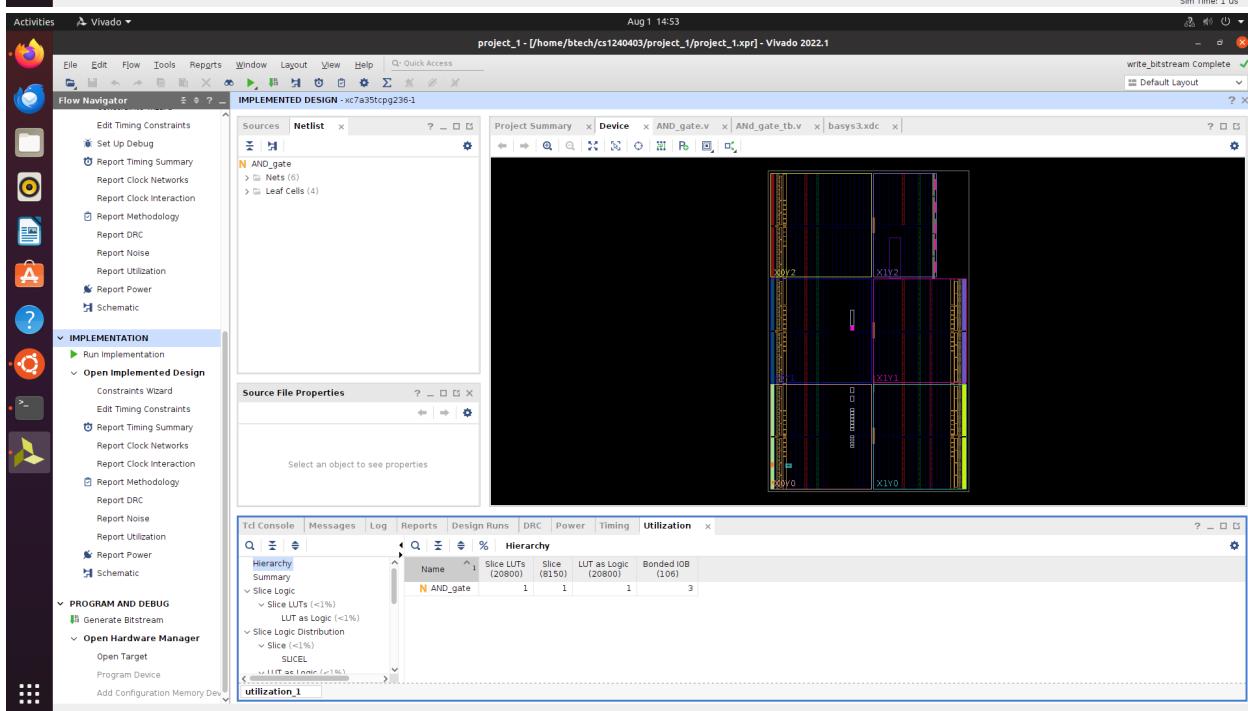
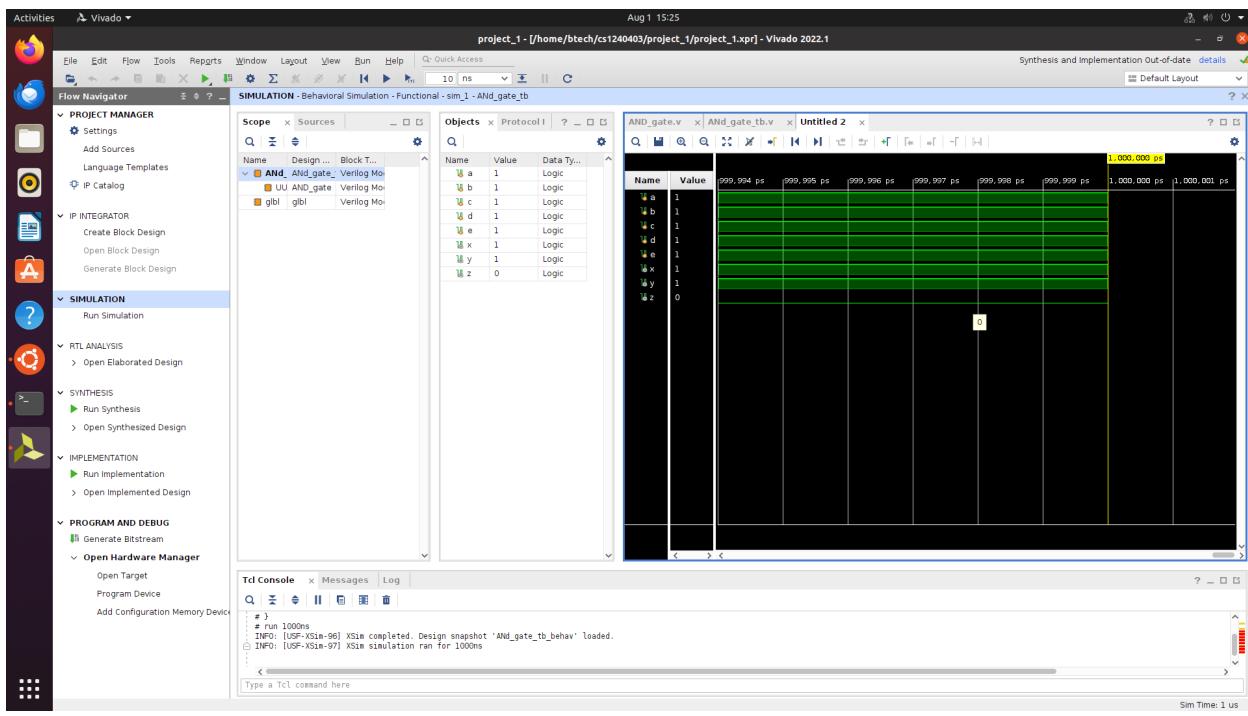




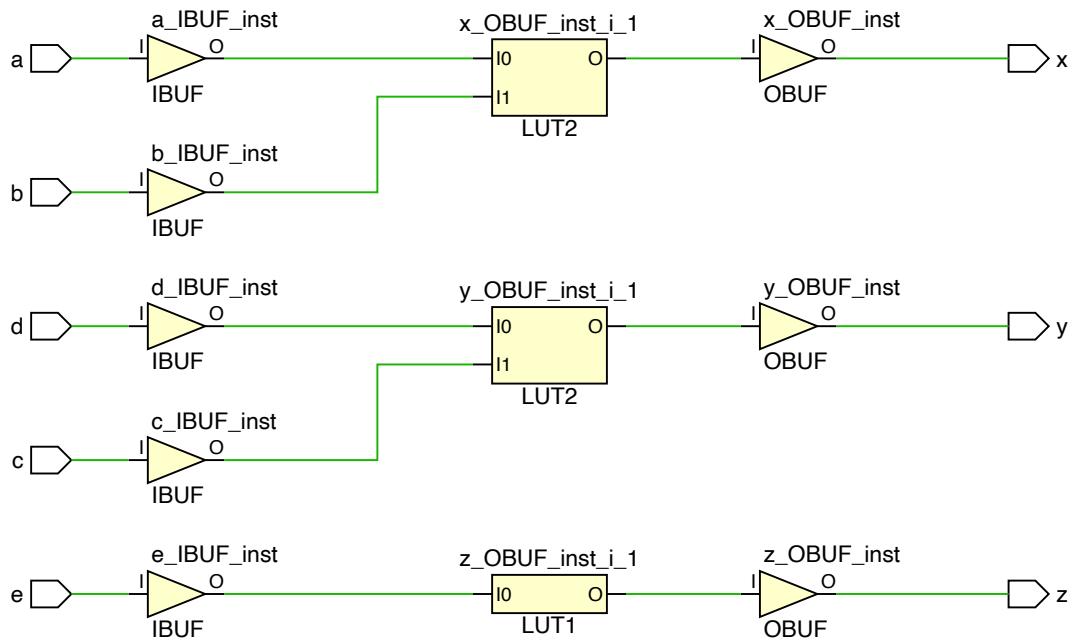
## ALL TOGETHER (AND\_GATE, OR\_GATE AND NOT\_GATE)

(AND\_GATE - input a, b – output x; OR\_GATE – input c,d – output y; NOT\_GATE – input e – output z)





## SCHEMATICS



## SYNTHESIS REPORT

Design Runs																				
Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	QoR Score	QoR Suggestions	LUT	FF	BRAM	URAM	DSP	Start	Elapsed
✓ synth_1	constrs_1	synth_design Complete!												3	0	0	0	0	8/1/25, 3:23 PM	00:00
✓ impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA		NA	2.217	0				3	0	0	0	0	8/1/25, 3:24 PM	00:01

## FPGA BOARD

