Function multiversioning in system image

All about vector registers

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Implement function multi versioning in sysimg #21849

Open yuyichao wants to merge 9 commits into `master` from `yyc/codegen/clone`

Conversation 99 | Commits 9 | Files changed 30

yuyichao commented on 13 May • edited — Member

Current TODO:

- [x] Implement more flexible cloning check
- [x] Handle "PLT" cloning
- [x] Generate dispatch data
- [x] Update sysimg loading
- [x] Fix `code_native`
- [x] ? Figure out what's wrong with AVX on x86.

Goal

Amount of implementation details

- Just enough to make Jeff happy
- Without losing the audience
- With a single version of the talk (**Important!**)

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How did it all begin

No performance scaling in threading #17395

Open ranjanan opened this issue on 13 Jul 2016 · 41 comments

ranjanan commented on 13 Jul 2016 Member

Consider the following code:

```
using Base.Threads
println("Number of threads = $(nthreads())")
x = rand(10^6)
y = zeros(10^6)
println("Warmup!")
for i = 1:10^6
    y[i] = sin(x[i])^2 + cos(x[i])^2
end
t1 = @elapsed for i = 1:10^6
    y[i] = sin(x[i])^2 + cos(x[i])^2
end
@assert sum(y) == 10^6
t2 = @elapsed @threads for i = 1:10^6
    y[i] = sin(x[i])^2 + cos(x[i])^2
end
@assert sum(y) == 10^6
println("Serial time = $t1")
println("Parallel time = $t2")
```

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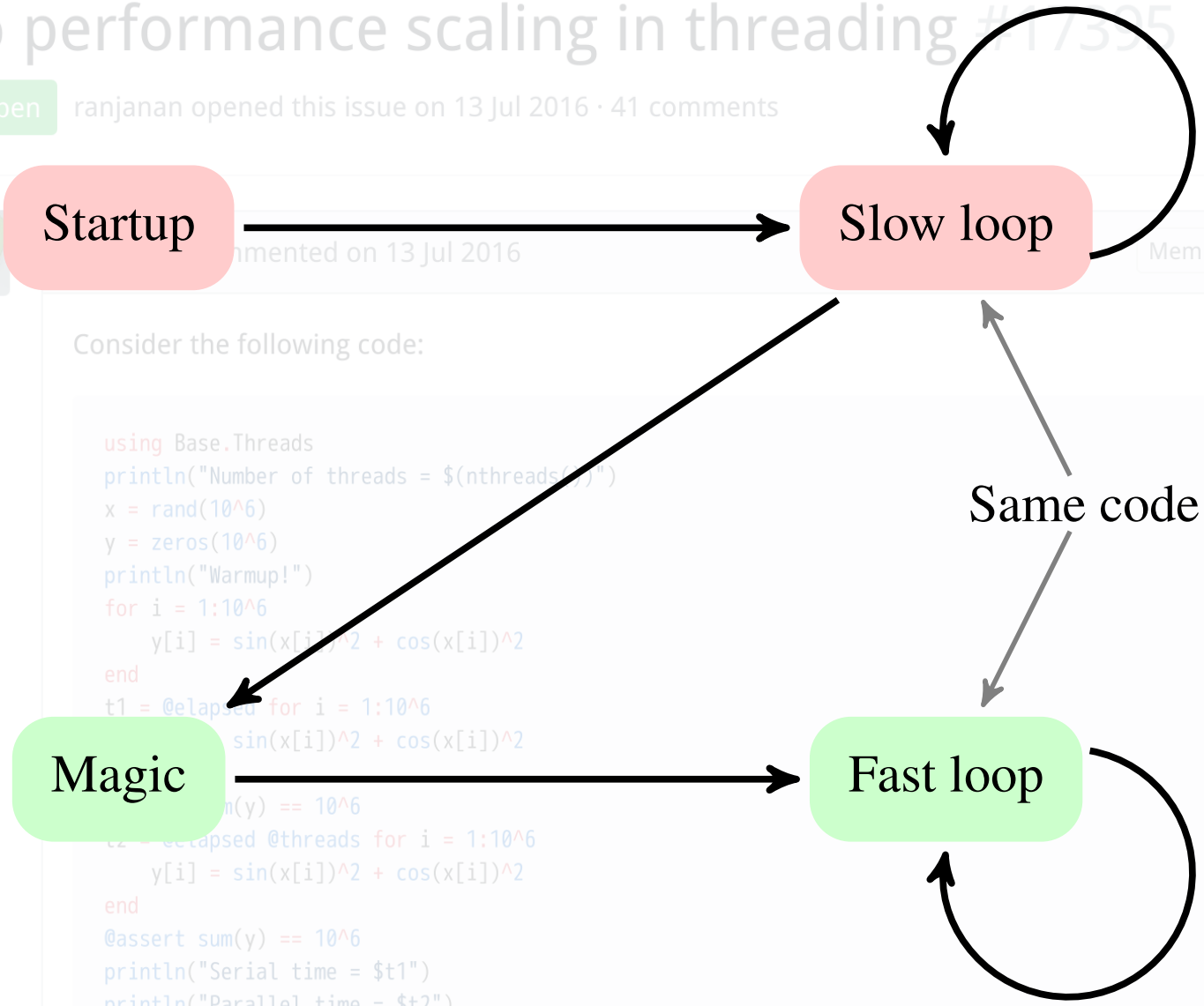
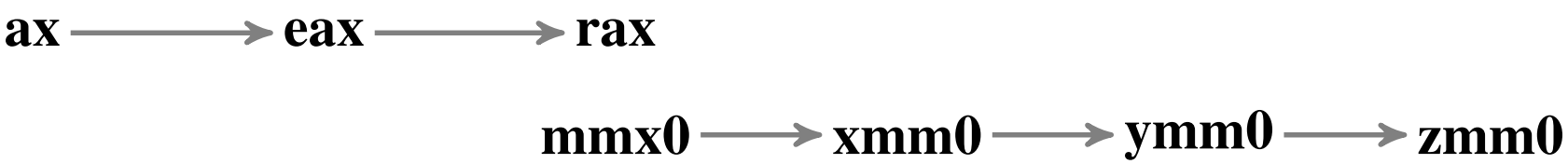


Register size



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ax → **eax** → **rax**

mmx0 → **xmm0** → **ymm0** → **zmm0**

More/larger registers → More states to manage

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(Intel got something wrong almost everytime)