EE517 LAB

Course Project

Design and Analysis of 2 stage OP-Amp in Cadence.

Submitted by,

GROUP 4

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Contents

1 OBJECTIVE

1) Design a 2-stage Op-amp with gm/Id methodology in 65 nm technology for given specifications.
2) Be familiar with the design steps of gm/Id methodology and mention the plots related to that in detail.
Specifications:
Slew Rate = 12 V/uS
$PhaseMargin \geq 60$
$DCGain \geq 75dB$
Unity Gain Bandwidth = 25MHz
ICMR = 0.6 - 0.9V
Load Capacitance = 10pF
Reference Current Source = 50uA

2 gm/ID design methodology

Mostly analog circuits traditionally work in strong inversion (saturation). Where as analog circuits which design in weak inversion has minimum power consumption but their speed is low. To make circuits which are high speed and low power we like to design circuits in Moderate inversion, but we don't have much insight for moderate inversion of mosfet. We don't have any design equations or model for moderate inversion like weak inversion or strong inversion.

So what we want is one single model that works in all operation regions.so using gm/ID methodology we can design our analog circuits in all regions without using any equation.

In gm/ID design methodology what we do is generate look up tables using simulation for different parameters and from that look up table we design our mosfet according to our need of application.

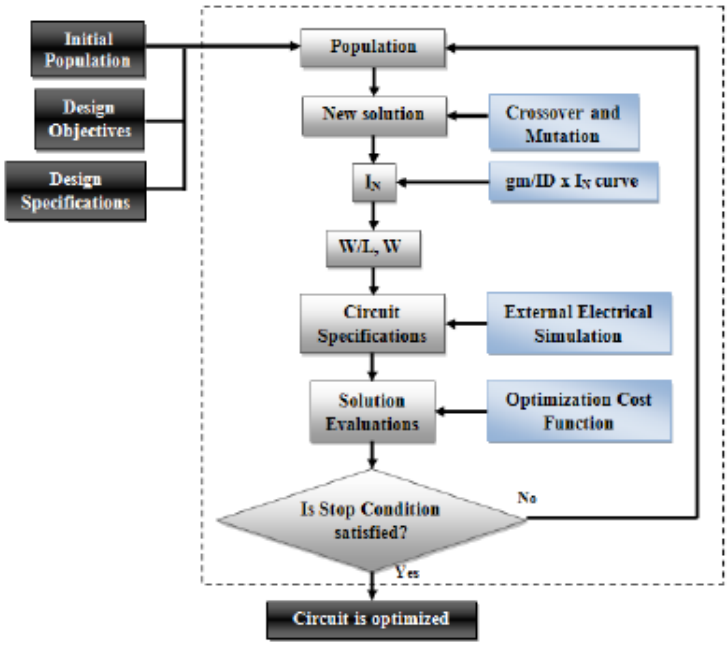

Figure 1: gm/gds over gm/ID

3 Graphs for PMOS

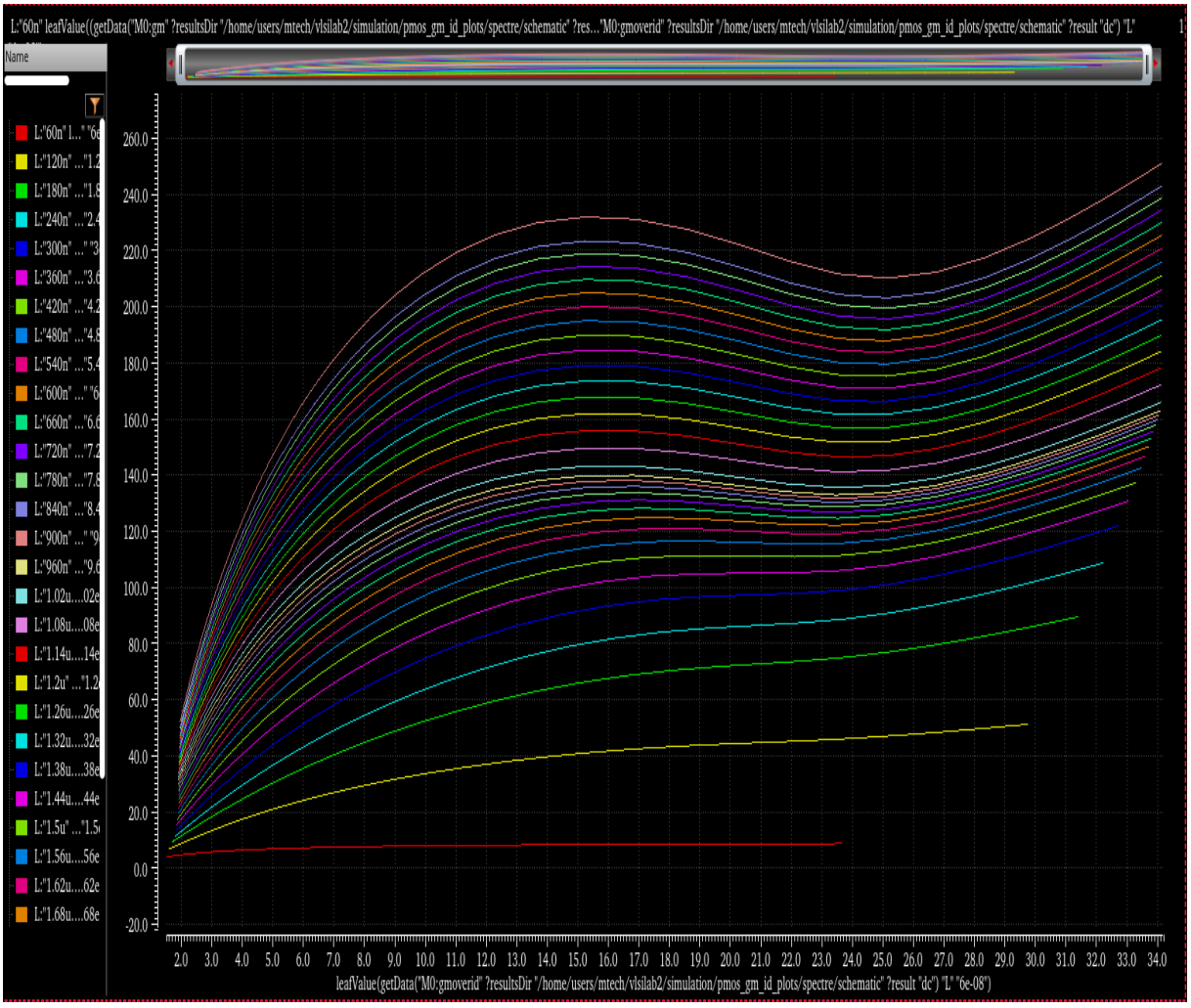

Figure 2: gm/gds over gm/ID

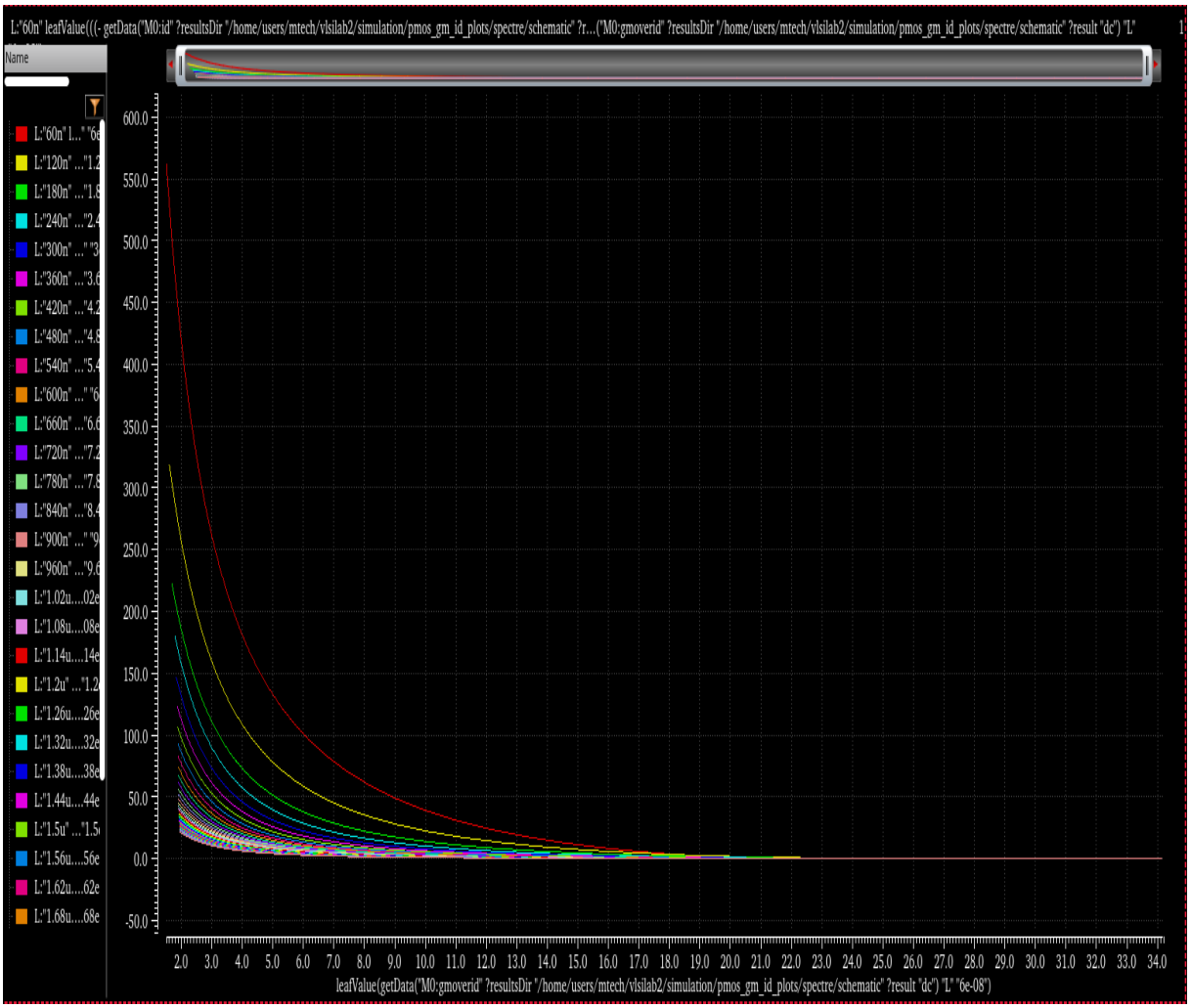

Figure 3: ID/W over gm/ID

4 Graphs for NMOS

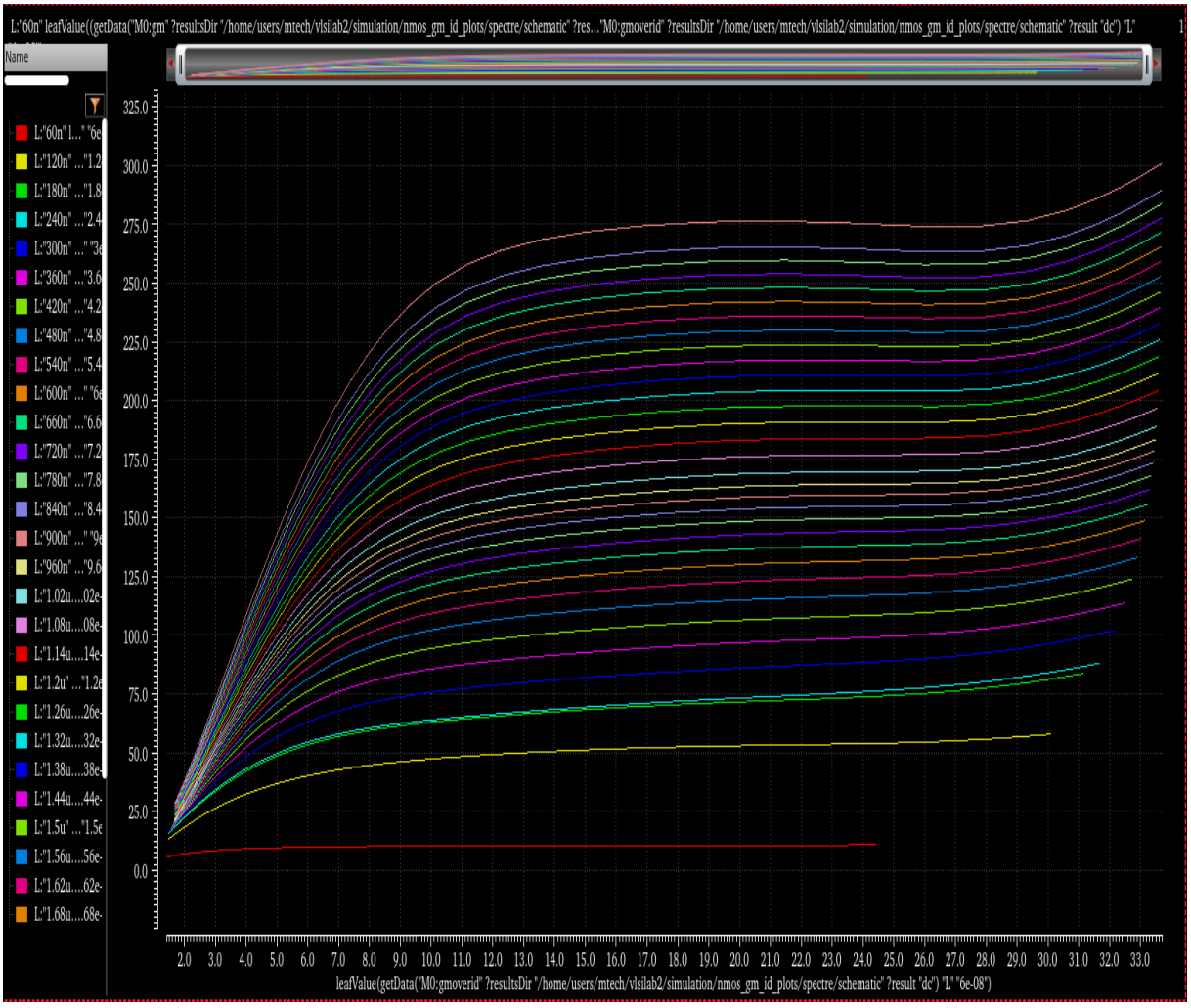

Figure 4: gm/gds over gm/ID

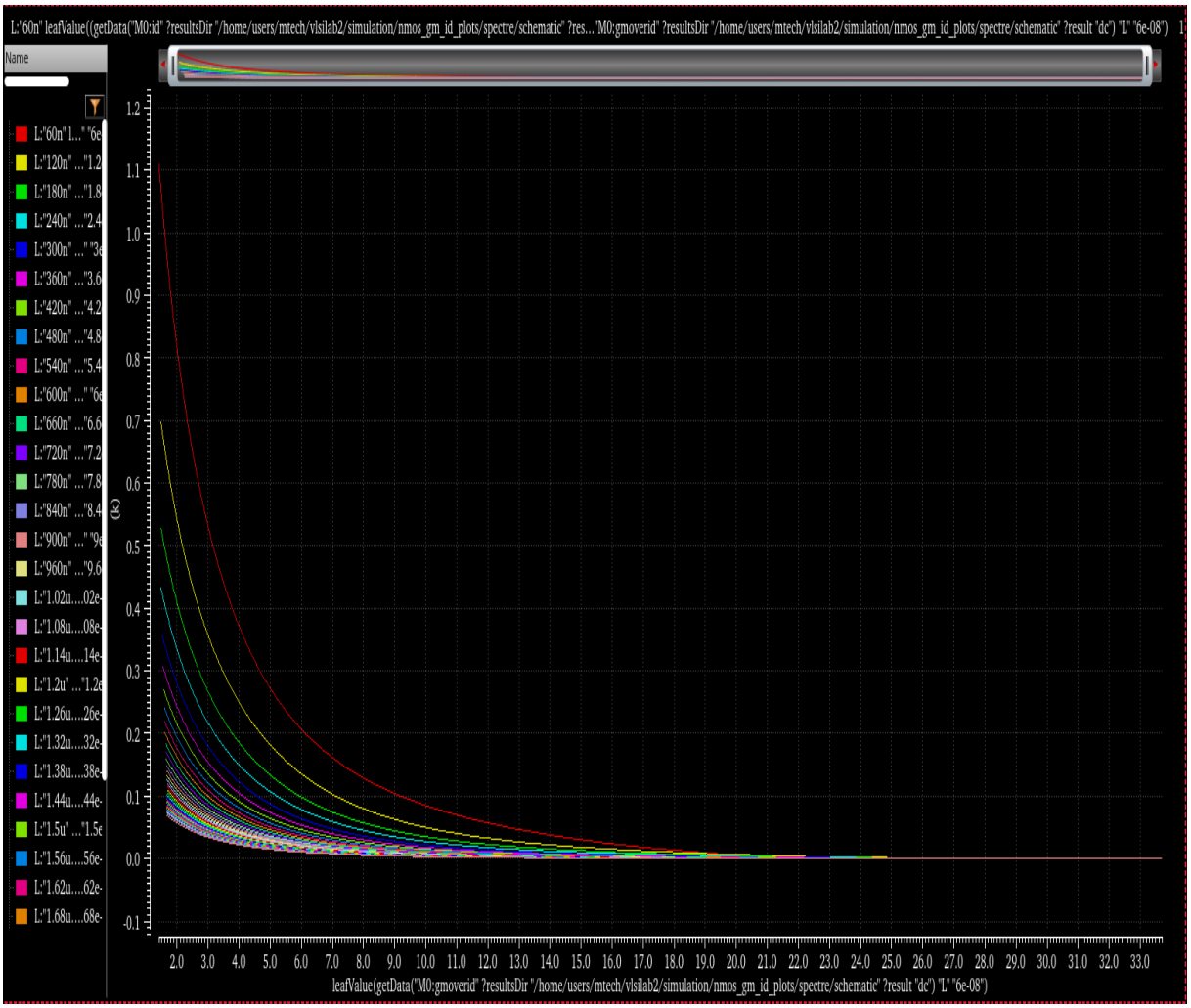

Figure 5: ID/W over gm/ID

5 Design Parameters

5.1 Design of M1 & M2

1) $C_C > 0.22 * C_L$ here, $C_L = 10pF$
$\Rightarrow C_C > 2.2pF choosing C_C = 2.4pF$
2)$I_{D1} = SlewRate * C_C = 14.4uA$
3) $GBW = \frac{g_{m1,2}}{2\pi C_C}$
$\Rightarrow g_{m1,2} = 0.377mS$
4)DC Gain = 75dB = 5623.41(linear)
Let, $A_v = 5700 = 76 * 75$
for first stage $A_{v1} = 76$
$A_{v1} = \frac{g_{m1,2}}{g_{ds1,2}+g_{ds3,4}}$
$g_{ds1,2} = g_{ds3,4}$ (assumed)
$g_{ds1,2} = 2.48uS$
5) $\frac{g_{m1,2}}{g_{ds1,2}} = 152.0161$ corresponding $\frac{g_{m1,2}}{I_{D1,2}} = 28.139$
from intersecting point of both from $\frac{g_m}{g_{ds}}$ over $\frac{g_m}{I_D}$ graph we will select the length for mosfet M1 and M2.$\Rightarrow L_{1,2} = 780nm$
and for that length we will select the $\frac{I_D}{W}$ from $\frac{I_D}{W}$ over $\frac{g_m}{I_D}$ graph since we know the I_D we got the width for M1 and M2 $\Rightarrow$W$_{1,2} = 134um$

5.2 Design of M3 & M4

since M3 and M4 need to operate in saturation regions we choose
$\frac{g_{m3,4}}{I_{D3,4}} = 7$ since we know $I_{D3,4} \Rightarrow g_{m3,4} = 100.8uS$
$\frac{g_{m3,4}}{g_{ds3,4}} = 40.6 \Rightarrow L_{3,4} = 240nm$
$W_{3,4} = 680nm$

5.3 Design of M6

$\frac{I_{D1}}{I_{D6}} \leq \frac{C_C}{2(C_L+C_C)} \Rightarrow I_{D6} \geq 148.8uA$
$g_{m6} = 2.84mS$
$\frac{g_{m6}}{I_{D6}} = 19.09$ Let L$_6 = 780nm(assumed)$ from $\frac{I_D}{W}$ over $\frac{g_m}{I_D} \Rightarrow W_6 = 460um$

5.4 Design of M7

Assume $g_{ds6} = g_{ds7}$ and $I_{D6} = I_{D7} \Rightarrow \frac{g_{m7}}{g_{ds7}} = 62.40$, $\frac{g_{m7}}{I_{D7}} = 9(assumed)$
$\Rightarrow$L$_7 = 240nm$ & $W_7 = 45um$

5.5 Design of M5 & M8

$L_{5,8} = 540nm$, $W_5 = 1.57umW_8 = 2.56um$ since they are currentmirrors.

6 Simulation Result

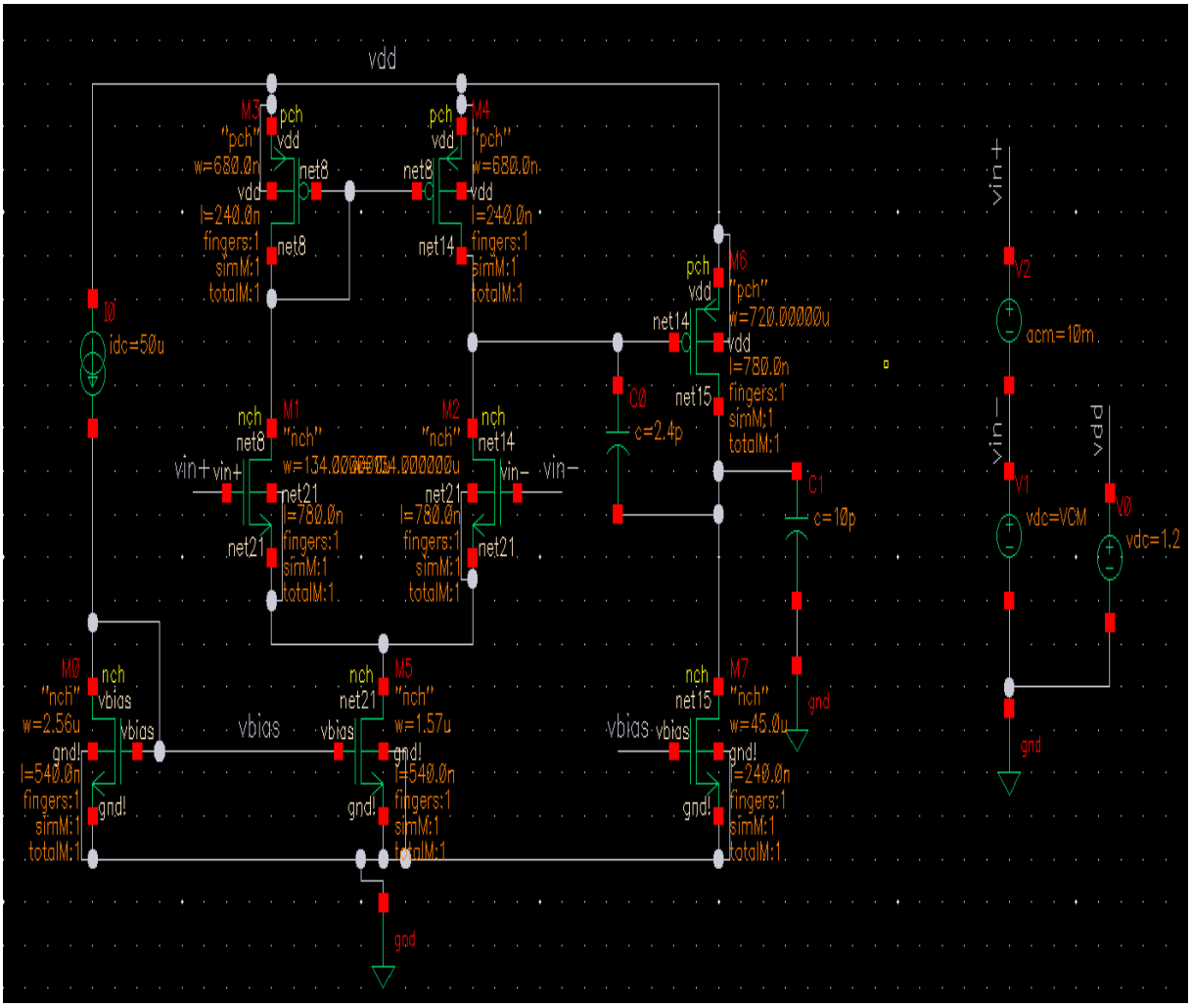

Figure 6: Circuit diagram Diagram

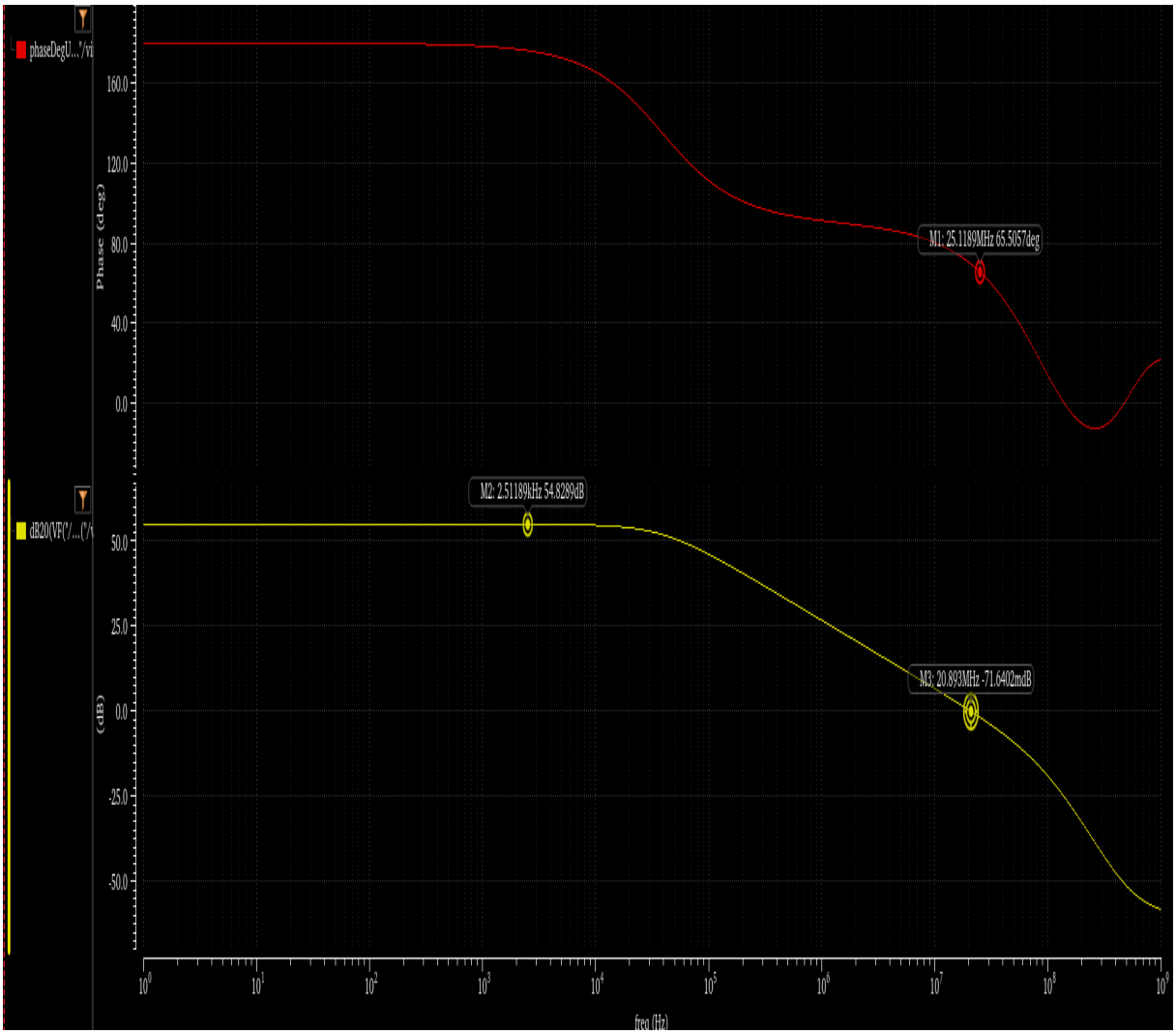

Figure 7: Voltage Gain, Phase Margin, Bandwidth

7 OBSERVATION

Voltage Gain	Phase	Bandwidth
54.62 dB	65.50°	20.89MHz

8 CONCLUSION

- To increase the gain we can increase the output resistance of second stage increasing transconductance or output resistance which will increase intrinsic gain of mosfet.
- Higher the Phase margin, the more stable the system.
- Conventional method have lot a approximations so design may not work as proper as we thought.
- Using gm/ID method short channel effect also cover in the graphs which is ignored in conventional method.
- So in this method we get proper parameters from look up tables or graphs.