SoC Tapeout: Environment Setup & Tool Installation

Section Key Points

Objective Set up environment, install EDA tools, enable collaboration, prepare

engineers for SoC tapeout.

Linux OS, RAM ≥32GB, multi-core CPU, SSD storage.

Environment Install Perl, Python, TCL, C/C++ libs.

Setup Set \$PATH, \$LM_LICENSE_FILE, \$TOOL_HOME.

Check file permissions and network access.

1. Obtain licenses.

Tool 2. Run installer (./install.sh).

Installation 3. Configure environment (\$PATH, source scripts).

4. Verify with demo projects and tool version.

RTL/Simulation: VCS, Xcelium, Questa. Synthesis: Design Compiler, Genus.

P&R: IC Compiler II, Innovus.

Common

Tools

Timing: PrimeTime, Tempus.

Verification: JasperGold, Formality.

Power: PrimePower, Voltus. DFT: Tessent, DFT Compiler.

Learning Linux & scripting \rightarrow RTL & digital design \rightarrow EDA tools \rightarrow Mini-projects

Path → Advanced: Power, DFT, tapeout readiness.

Shared scripts, version-controlled docs (Git), standardized folders, Collaboration

license/library access.

Industry Supports multi-team workflows, scalable designs, and prepares

Relevance engineers for industrial SoC tapeout projects.

Best Standardize setup, maintain logs, update tools/licenses, use version

Practices control.