your position is our focus

Application Note

Title	**ANTARIS®4 Design-In**		
Subtitle	Application Note		
Doc Type	!!! PRELIMINARY !!!		
Doc Id	GPS.G4-CS-05003-A1		
Revision Index	**Date**	**Name**	**Status / Comments**
Initial Version	30/09/2005	Thomas Christen	
A	12/12/2005	Thomas Christen	Add Leadfree information
A1	03/01/2006	Thomas Nigg	Correction to Figure 2 and 6

Content

1 Design-In/ Reference Schematics

The A4 signs marks changes between ANTARIS® and ANTARIS®4 family to allow existing ANTARIS® customers easier use of the new technology.

This application note is extracted from *the ANTARIS®4 System Integration Manual* (GPS.G4-MS4-05007), which will be published soon. Please check the u-blox website on http://www.u-blox.com about its availability.

1.1 Design-In Checklist for ANTARIS®4 A4

Designing-in a TIM-4x or LEA-4x GPS receiver is easy especially when a design is based on the reference design in *ANTARIS®4 System Integration Manual*. Nonetheless, it pays-off to do a quick sanity check of the design. This section lists the most important items for a simple design check. It helps to avoid an unnecessary respin of the PCB and helps to achieve the best possible performance.

☞ **Note** It's highly recommended to follow the Design-In Checklist when developing any ANTARIS® GPS applications. This may shorten the time to market and the development cost significantly.

Have you chosen the optimal module?

The ANTARIS®4 receiver family has been designed with the intention to have GPS receivers optimally tailored to different applications. Changing between the different variants is easy.

- ❑ Do you need SuperSense? – Then choose an xxx-x**H** or xxx-x**S** class receiver.
- ❑ If you want to be able to upgrade the firmware or to permanently save settings, you will have to use Programmable receiver module? – Then choose an xxx-x**H** or xxx-x**P** class receiver.

Check Power Supply Requirements and Schematic

- ❑ Is the power supply within the specified range?
- ❑ Are the voltages **VDDIO** and **VDDUSB** within the specified range?
- ❑ Place the LDO as near as possible to the **VCC** pin of the module; if this is not possible design a wide power track or even a power plane.
- ❑ Is the ripple on **VCC** below 50mVpp?

Backup Battery

- ❑ If you want to achieve a minimal TTFF after a power down, make sure to connect a backup battery to **V_BAT**.
- ❑ When you connect the backup battery for the first time, make sure **VCC** is on or – if not possible – power up the module for a short time (e.g. 1s) ASAP in order to avoid excessive battery drain (see sction 1.7).
- ❑ Make sure there are no pull-up or down resistors connected to the RxD1, RxD2, EXTINT0 and EXTINT1 as this could cause significant backup or sleep current (>25µA or more instead of 5µA). And check if you followed the recommendations in *section 1.7.1*.

Antenna (see Section 1.7)

- ❑ The total noise figure should be well below 3dB.
- ❑ Make sure the antenna is not placed close to noisy parts of the circuitry. (e.g. micro-controller, display, etc.)
- ❑ Add a 10R in front of **V_ANT** input for short circuit protection or use the antenna supervisor circuitry
- ❑ If you migrate from an ANTRARIS GPS receiver (TIM-Lx or LEA-LA) and have previously used the Antenna Short and Open Supervisor circuit, make sure to adapt the value of R5 (see section 1.9.4.2 for more details)

Serial Communication

- ❑ Choose UBX for an efficient (binary) data handling or if more data is required than supported by NMEA
- ❑ When using UBX protocol, check if the UBX quality flags are used properly.

- Choose NMEA for compatibility to other GPS modules, e.g. TIM-ST
- Customize the NMEA output if required (e.g. NMEA standard, #of digits, output filters etc.)

Schematic

- If required, does your schematic allow using different TIM-4x or LEA-4x variants? For TIM-4x modules see *Table 4* for a comparison, for LEA-4x refer to *Table 5*
- Leave the **RESET_N** pin open if not used. Don't drive it high!
- Leave **BOOT_INT** pin open if not used for firmware update.
- Check the **GPSMODE** pins connection for start-up configuration of Low Cost Receivers.
- Plan use of 2nd interface (USB or serial port) for firmware updates or as a service connector.

Layout optimizations (*Section 1.14*)

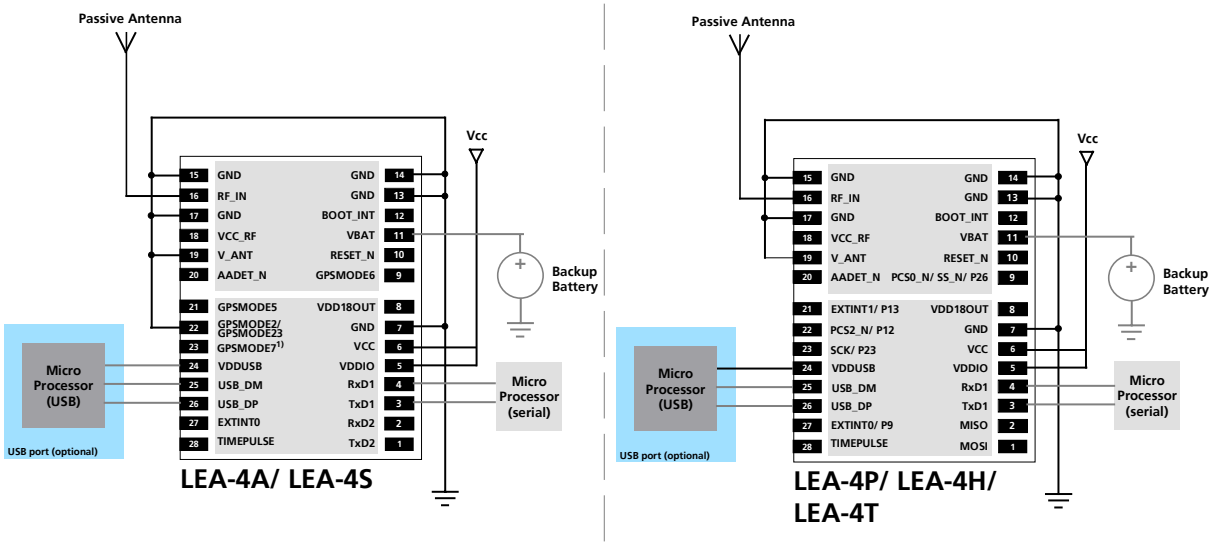
- Have you followed the Grounding concept?
- Is the GPS module placed according to the recommendation?
- Keep the micro strip as short as possible.
- Add a ground plane underneath the GPS module to reduce interference.
- For improved shielding, add as many vias as possible around the micro strip, around the serial communication lines, underneath the GPS module etc.

Calculation of the micro strip (*Section 1.14.2*)

- The micro strip must be 50 Ohms and it must be routed in a section of the PCB where minimal interference from noise sources can be expected.
- In case of a multi-layer PCB, use the thickness of the dielectric between the signal and the 1st **GND** layer (typically the 2nd layer) for the micro strip calculation.
- If the distance between the micro strip and the adjacent **GND** area (on the same layer) does not exceed 5 times the track width of the micro strip, use the "Coplanar Waveguide" model in AppCad to calculate the micro strip and not the "micro strip" model.

☞ **Note** Further details can be found in the *ANTARIS®4 System Integration Manual (GPS.G4-MS4-05007), which will soon be published on the u-blox website.*

1.2 LEA-4x Design



1) USB selfpowered setting

Figure 1: Passive Antenna Design for LEA-4x Receivers

Function	PIN (LEA)	I/O	Description	Remarks
Power				
VCC	6	I	Supply Voltage	Max allowed ripple on **VCC**=50mVpp
GND	7, 13-15, 17	I	Ground	Assure a good **GND** connection to all **GND** pins of the module, preferably with a large ground plane
VDD18OUT	8	O	1.8V supply output	1.8V output voltage reference. Leave open if not used.
VDDIO	5	I	Supply voltage for digital I/O pins	Power Supply for the digital I/O pins (e.g. serial ports, **TIMEPULSE**). Must be connected to **VDD18OUT**, **VCC** or other voltage source meeting datasheet specification. **Never leave open!** Otherwise outputs are not in operation.
VDD_USB	24	I	USB Power Supply	To use the USB interface connect this pin to 3.0 – 3.6V. See also *Section 1.2.2*. If no USB serial port used connect to GND
VBAT	11	I	Backup voltage supply	It's recommended to connect a backup battery to **V_BAT** in order to enable Warm and Hot Start features on the receivers (see section 1.7).
VBAT	11	I	Backup voltage supply	It's recommended to connect a backup battery to **V_BAT** in order to enable Warm and Hot Start features on the receivers (see also section 1.7). Otherwise connect to **GND**.
Antenna				
RF_IN	16	I	GPS signal input from antenna	The connection to the antenna has to be routed on the PCB. Use a controlled impedance of 50 Ohm to connect RF_IN to the antenna or the antenna connector. Don't supply DC through this pin. Use **V_ANT** pin to supply power.
V_ANT	19	I	Antenna Bias voltage	Connect to **GND** if Passive Antenna is used. If an active Antenna is used, add a 10R resistor in front of **V_ANT** input to the Antenna Bias Voltage or **VCC_RF** for short circuit protection or use the antenna supervisor circuitry.
VCC_RF	18	O	Output Voltage RF section	Can be used to power an external active antenna (**VCC_RF** connected to **V_ANT**). The max power consumption of the Antenna must not exceed the datasheet specification of the module (see section 1.9) Leave open if not used.
AADET_N	20	I	Active Antenna Detect	Signal pin for optional antenna supervisor circuitry (see section 1.9.4). Leave open if not used.

Function	PIN (LEA)	I/O	Description	Remarks
Serial Port /USB				The serial output voltage levels on Tx depend on the applied VDDIO voltage level.
TxD1	3	O	Serial Port 1	**VDDIO** serial port output. Leave open if not used.
RxD1	4	I	Serial Port 1	5V tolerant serial port input with internal pull-up resistor to **V_BAT**. Leave open if not used. ☞ **Note** Don't use an external pull up resistor.
TxD2[1]	1	O	Serial Port 2	**LEA-4A/LEA-4S** (only)**:** **VDDIO** serial port output. Leave open if not used.
RxD2[1]	2	I	Serial Port 2	**LEA-4A/LEA-4S** (only) **:** 5V tolerant serial port input with internal pull-up resistor to **V_BAT**. Leave open if not used. ☞ **Note** Don't use an external pull up resistor.
USB_DM	25	I/O	USB I/O line	USB1.1 bidirectional communication pin. To be fully compliant with USB standard follow the schematic recommendation in *Section 1.2.2*.
USB_DP	26			
System				
BOOT_INT	12	I	Boot mode	Do not connect on LEA-4A and LEA-4S receivers.
RESET_N	10	I	Hardware Reset (Active Low)	Leave open if not used. Do not drive high. See *section 1.8* for more information.
TIMEPULSE	28	O	Timepulse Signal	Configurable Timepulse signal (one pulse per second by default). Leave open if not used.
EXTINT0	27		External Interrupt	External interrupt pin to wake up receiver in FIXNow™ sleep mode. Internal pull-up resistor to **V_BAT**. Leave open if not used.
GPSMODE6/ PCS0_N/ SS_N/ P26	9	I/O	GPIO/ GPSMODE Pin	**LEA-4A/ LEA-4S:** GPSMODE Pin; leave open if default configuration is used. Refer to Section *1.10.2* for further information. **LEA-4P / LEA-4H/ LEA-4T:** GPIO Pin; leave open if not used. The General Purpose I/O (GPIO) can only be programmed with the ANTARIS® Software Customization Kit, please refer to the SCK Manual when intending to use of the GPIO's of the receiver.
GPSMODE5/ EXTINT1/ P13	21	I/O		
GPSMODE23[2]**/ GPSMODE2/ PCS2_N/P12**	22	I/O		
GPSMODE7/ SCK/ P23	23	I/O	USB Boot time configuration pin	**LEA-4A/ LEA-4S:** Defines the Power Supply mode of the GPS module. **GPSMODE7**=high (default) means that the module has it's own power supply. **GPSMODE7**=low means that the GPS module is powered by the USB bus. For details about configuration settings refer to *Section 1.10.2*. Connect to **GND**, when Bus Powered Mode is required. Otherwise leave open. **LEA-4P / LEA-4H/ LEA-4T:** GPIO Pin; leave open if not used The General Purpose I/O (GPIO) can only be programmed with the ANTARIS® Software Customization Kit, please refer to the SCK Manual when intending to use of the GPIO's of the receiver.
MOSI/ P24[3]	1	I/O	GPIO	**TIM-4H / TIM-4P** (only)**:** GPIO Pin; leave open if not used
MSIO/ P25[3]	2	I/O		

[1] Used as **MOSI** /**MISO**/ **GPIO** pins on LEA-4H, LEA-4P and LEA-4T.
[2] Connecting theGPSMODE23 pin (LEA-4S) to GND increased the FixNOW sleep mode current by about 50µA. Connecting theGPSMODE2 pin (LEA-4A to GND does however not have an impact on the FixNOW sleep mode current.
[3] Used as **RxD2**/ **TxD2** on LEA-4A and LEA-4S.

1.2.1 LEA Design with Active Antennas

Depending on the requirements one can choose between different active antenna configurations. For detachable active antennas an antenna supervisor circuitry (3) is recommended. For further details refer to *Section 1.7*.

1) External antenna power supply with short circuit detection
2) Internal antenna power supply with short circuit detection
3) External antenna power supply with full antenna supervisor[4].

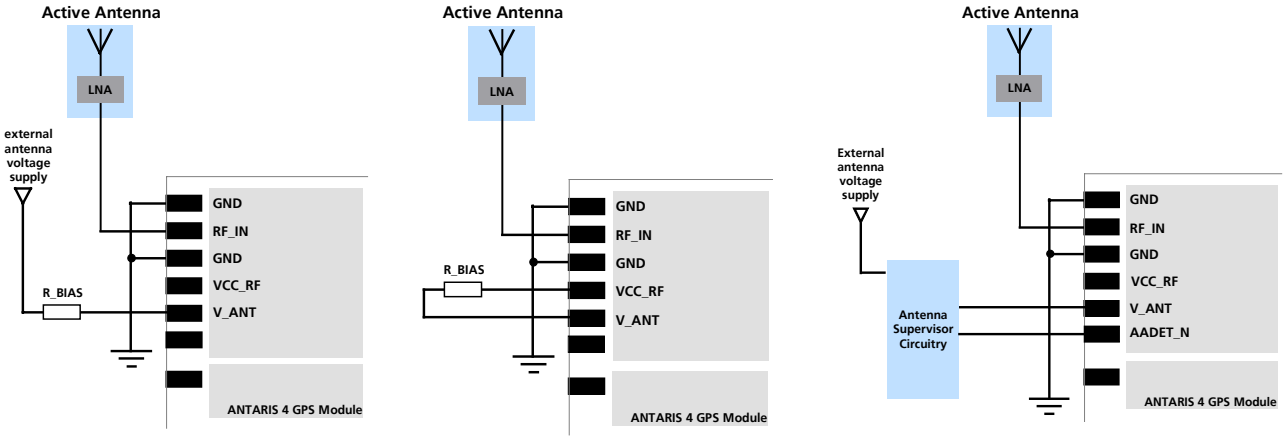


Figure 2: Different active antenna connections on LEA-4x receivers

1.2.2 USB serial port

The USB interface supports two different power modes. In the 'Self Powered Mode' the receiver is powered by its own power supply. **VDDUSB** is used to detect the availability of USB port.

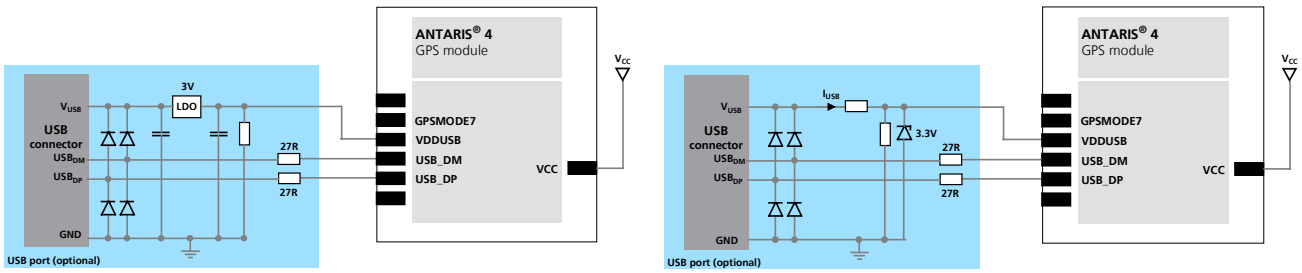


Figure 3: Self Powered USB Mode Schematic

In the 'Bus powered mode' no power supply for the GPS receivers is available. The USB bus is supplying power up to 100mA. To achieve a constant **VCC** a LDO is a requirement.

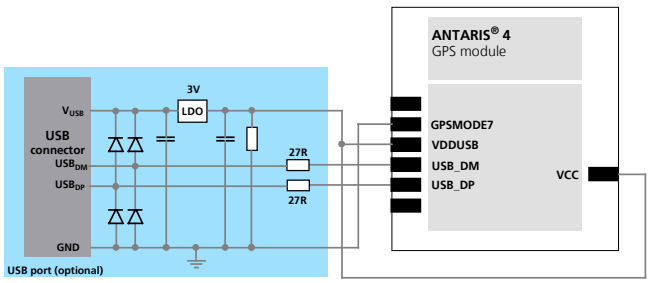


Figure 4: Bus Powered USB Mode Schematic

If USB serial port is not used connect **VDDUSB** to GND and leave **GPSMODE7**, **USB_DM** and **USB_DP** open.

[4] The antenna supervisor can also be combined with an internal (VCC_RF) voltage supply.

1.3 TIM-4x Design

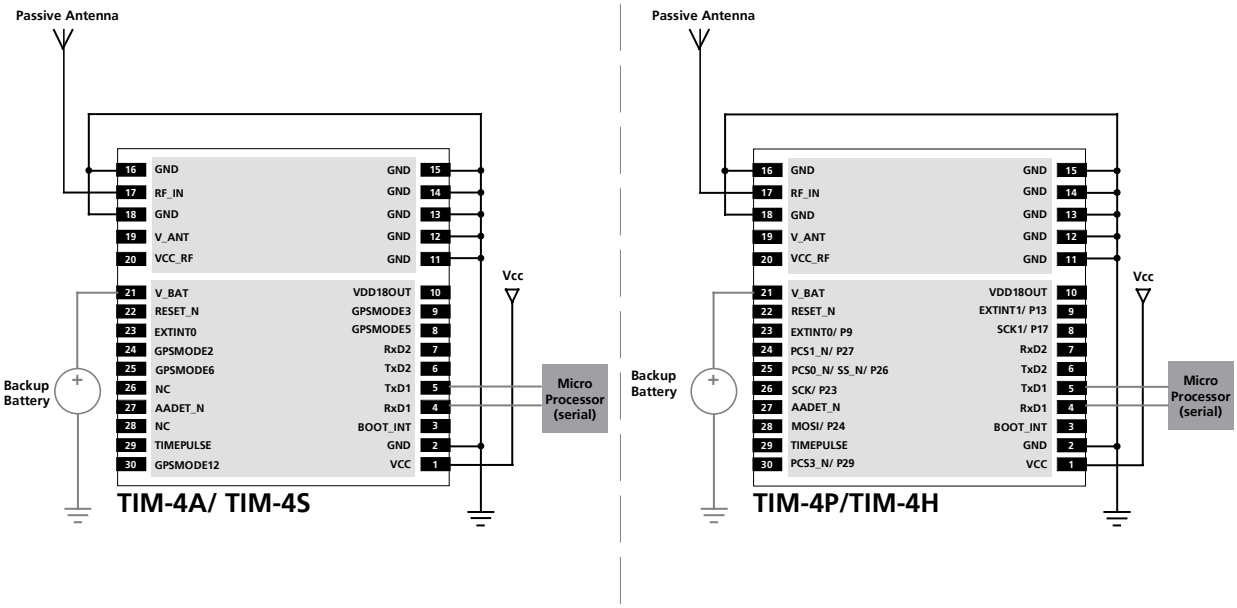


Figure 5: Passive Antenna Design for TIM-4x Receivers

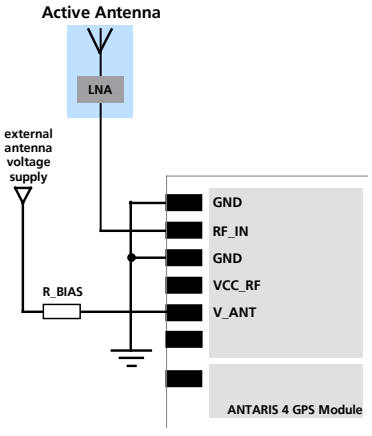
Function	PIN (TIM)	I/O	Description	Remarks
Power				
VCC	1	I	Supply Voltage	Max allowed ripple on **VCC**=50mVpp
GND	2,11-16,18	I	Ground	Assure a good **GND** connection to all **GND** pins of the module, preferably with a large ground plane.
VDD18OUT	10	O	1.8V supply output	1.8V output voltage reference. Leave open if not used.
VBAT	21	I	Backup voltage supply	It's recommended to connect a backup battery to **V_BAT** in order to enable Warm and Hot Start features on the receivers (see also section 1.7). Otherwise connect to **GND**.
Antenna				
RF_IN	17	I	GPS signal input from antenna	The connection to the antenna has to be routed on the PCB. Use a controlled impedance of 50 Ohm to connect RF_IN to the antenna or to the antenna connector. Don't supply DC through this pin. Use **V_ANT** pin to supply power.
V_ANT	19	I	Antenna Bias voltage	Connect to **GND** if Passive Antenna is used. If an active Antenna is used, add a 10R resistor in front of **V_ANT** input to the Antenna Bias Voltage or **VCC_RF** for short circuit protection or use the antenna supervisor circuitry.
VCC_RF	20	O	Output Voltage RF section	Can be used to power an external active antenna (**VCC_RF** connected to **V_ANT**). The max power consumption of the Antenna must not exceed the datasheet specification of the module. Leave open if not used.
AADET_N	27	I	Active Antenna Detect	Signal pin for optional antenna supervisor circuitry (see section 1.9.4). Leave open if not used.
Serial Port				The serial interface is 3V CMOS and 5V TTL compatible. For other voltage levels use the appropriate level shifters, e.g. MAX3232 in order to obtain RS232 compatible levels.
TxD1	5	O	Serial Port 1	3V
RxD1	4	I	Serial Port 1	5V tolerant serial port input. Internal pull-up resistor to **V_BAT**. Leave open if not used. ☞ **Note** Don't use an external pull up resistor.
TxD2	6	O	Serial Port 2	3V
RxD2	7	I	Serial Port 2	5V tolerant serial port input. Internal pull-up resistor to **V_BAT**. Leave open if not used. ☞ **Note** Don't use an external pull up resistor.

Function	PIN (TIM)	I/O	Description	Remarks
System				
BOOT_INT	3	I	Boot mode	Do not connect on TIM-4A and TIM-4S receivers.
RESET_N	22	I	Hardware Reset (Active Low)	Leave open if not used. Do not drive high. See *section 1.8* for more information.
TIMEPULSE	29	O	Timepulse Signal	Configurable Timepulse signal (one pulse per second by default). Leave open if not used.
EXTINT0	23	I	External Interrupt	External Interrupt Pin to wake up receiver in FIXNow™ sleep mode. Internal pull-up resistor to **V_BAT**[5]. Leave open if not used.
GPSMODE2[6]**/ PCS1_N/ P27**	24	I/O	GPIO/ GPSMODE Pin	**TIM-4A/ TIM-4S:** GPSMODE Pin; leave open if default configuration is used. Refer to Section *1.10.2* for further information. **TIM-4H / TIM-4P:** GPIO Pin; leave open if not used. The General Purpose I/O (GPIO) can only be programmed with the ANTARIS® 4 Software Customization Kit, please refer to the SCK Manual when intending to use of the GPIO's of the receiver.
GPSMODE5/ SCK1/ P17	8	I/O		
GPSMODE6/ PCS0_N/ SS_N/ P26	25	I/O		
GPSMODE12/ PCS3_N/ P29	30	I/O		
GPSMODE3/ EXTINT1/ P13/	9	I/O		
NU / SCK/ P23	26	I/O	GPIO / NC	**TIM-4A/ TIM-4S:** Not connected; leave open. **TIM-4H / TIM-4P:** GPIO Pin; leave open if not used
NU/ MOSI/ P24/	28	I/O		

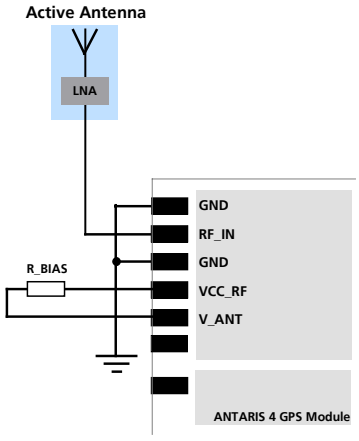
1.3.1 TIM Design with Active Antennas

Depending on the requirements one can choose between different active antenna configurations. For detachable active antennas an antenna supervisor circuitry (3) is recommended. For further details refer to *Section 1.9*.

1) External antenna power supply with short circuit detection



2) Internal antenna power supply with short circuit detection



3) External antenna power supply with full antenna supervisor[7].

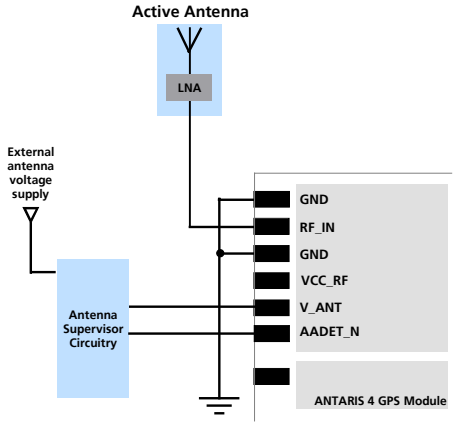


Figure 6: Different active antenna connections on TIM-4x receivers

[5] Do not pull up as it may increase your Battery Backup Current.
[6] Pull to **GND** to achieve Normal Sensitivity Mode setting at startup.
[7] The antenna supervisor can also be combined with an internal (VCC_RF) voltage supply.

1.4 Migration to ANTARIS®4 receivers

Migrating from an ANTARIS® to an ANTARIS®4 GPS receiver is a straightforward procedure. Nevertheless, the following points have to be considered during the migration.

1.4.1 Software Changes

ANTARIS®	ANTARIS®4	Remarks
UBX-CFG-NAV	UBX-CFG-NAV2	To ease the navigation configuration u-blox has introduced a new message. It has also additional features. UBX-CFG-NAV is not supported anymore on ANTARIS®4.
UBX-TIM-TM UBX-CFG-TM	*N/A*	Time mark feature Starting with firmware version 5.0, these messages are not longer supported!
N/A	UBX-TIM-TM2 UBX-CFG-TM2	Improved Time Mark feature. Only supported on LEA-4T.
UBX-RXM-RAW UBX-RXM-SFRB	UBX-RXM-RAW UBX-RXM-SFRB	Satellite RAW and subframe data. These messages have the same format than on ANTARIS® but on ANTARIS®4 receivers they are only supported on LEA-4T receivers.

1.4.2 Migration from LEA-LA to LEA-4A/LEA-4S

The pin-outs of LEA-LA and LEA-4A/LEA-4S modules do not differ significantly. *Table 1* compares the modules and highlights the differences to be considered.

Pin	LEA-LA		LEA-4A / LEA -4S		Remarks for Migration
	Pin Name	Typical Assignment	Pin Name	Typical Assignment	
1	**TXD2**	VDDIO level I/O	**TXD2**	VDDIO level I/O	No difference.
2	**RXD2**	VDDIO level I/O; pull up if not used	**RXD2**	VDDIO level I/O; not connected	Do not add an external pull up resistor; there is one built-in to **V_BAT**. Leave open if not used.
3	**TXD1**	VDDIO level I/O	**TXD1**	VDDIO level I/O	No difference
4	**RXD1**	VDDIO level I/O; pull up if not used	**RXD1**	VDDIO level I/O	Do not add an external pull up resistor; there is one built-in to **V_BAT**. Leave open if not used.
5	**VDDIO**	1.65 – 3.60V	**VDDIO**	1.65 – 3.60V	To be compatible to LEA-LA, **VDDIO** has to be set to Vcc to assure a 3.0V level at the serial ports. The GPSMODE pins do recognize 1.8V and 3.0V as "high" value at **VDDIO**.
6	**VCC**	2.70 – 3.30V	**VCC**	2.70 – 3.30V	No difference
7	**GND**	GND	**GND**	GND	No difference
8	**VDD18OUT**	Not connected	**VDD18OUT**	Not connected	No difference
9	**GPSMODE6**	Connected to GND or VDD_18OUT	**GPSMODE6**	Not connected	Backward compatible: This pin can be connected to GND, VDD18OUT or VCC. An external pull up resistor is not required as there is one built-in.
10	**RESET_N**	1.8V	**RESET_N**	1.8V	No difference
11	**V_BAT**	1.95 – 3.6V	**V_BAT**	1.50 – 3.6V	Wider voltage range. Uncritical for migration.
12	**BOOT_INT**	NC	**BOOT_INT**	NC	No difference
13	**GND**	GND	**GND**	GND	No difference
14	**GND**	GND	**GND**	GND	No difference
15	**GND**	GND	**GND**	GND	No difference
16	**RF_IN**	RF_IN	**RF_IN**	RF_IN	No difference
17	**GND**	GND	**GND**	GND	No difference
18	**VCC_RF**	VCC - 0.1V	**VCC_RF**	VCC - 0.1V	No difference
19	**V_ANT**	3.0V –5.0V	**V_ANT**	3.0V -5.0V	No difference
20	**AADET_N**	Connected to GND	**AADET_N**	Not connected	No external pull down resistor required, as there is already an internal pull down resistor. Please check resistor values *in section 1.9.4.*
21	**GPSMODE5**	Connected to GND or VDD_18OUT	**GPSMODE5**	Not connected	Backward compatible: This pin can be connected to GND, VDD18OUT or VCC. An external pull up resistor is not required as there is one built-in.

Pin	LEA-LA		LEA-4A / LEA -4S		Remarks for Migration
	Pin Name	Typical Assignment	Pin Name	Typical Assignment	
22	**GPSMODE2**	Connected to GND or VDD_18OUT	**GPSMODE2/ GPSMODE23**[8]	Not connected	Backward compatible: This pin can be connected to GND, VDD18OUT or VCC. An external pull up resistor is not required as there is one built-in.
23	**NC**	Not connected	**GPSMODE7**	Not connected	Placing a LEA-4x into an existing LEA-LA board design will disable USB port.
24	**NC**	Connected to GND	**VDDUSB**	Connected to GND	
25	**NC**	Not connected	**USB_DM**	Not connected	
26	**NC**	Not connected	**USB_DP**	Not connected	
27	**EXTINT0**	Connected to VDD18OUT	**EXTINT0**	Not connected	Do not add an external pull up resistor; there is one built-in to **V_BAT**. Leave open if not used.
28	**TIMEPULSE**	1.8V out	**TIMEPULSE**	VDDIO level I/O	Consider that **TIMPULSE** on LEA-4x is on **VDDIO** voltage level (1.8V on LEA-LA)

: Pins to be checked carefully

Table 1: Pin-out comparison LEA-LA vs. LEA-4A/4S

1.4.3 Migration from LEA-LA to LEA-4H/LEA-4P

The pin-outs of LEA-LA and LEA-4H/4P differ slightly. *Table 1* compares the modules and highlights the differences to be considered.

Pin	LEA-LA		LEA-4H / LEA-4P		Remarks for Migration
	Pin Name	Typical Assignment	Pin Name	Typical Assignment	
1	**TXD2**	VDDIO level I/O	**MISO**	VDDIO level I/O; not connected	Serial Port 2 not supported on LEA-4P/LEA-4H. Leave open if not used.
2	**RXD2**	VDDIO level I/O; pull up if not used	**MOSI**	VDDIO level I/O; not connected	
3	**TXD1**	VDDIO level I/O	**TXD1**	VDDIO level I/O	No difference
4	**RXD1**	VDDIO level I/O; pull up if not used	**RXD1**	VDDIO level I/O	Do not add an external pull up resistor; there is one built-in to **V_BAT**. Leave open if not used.
5	**VDDIO**	1.65 – 3.60V	**VDDIO**	1.65 – 3.60V	To be compatible to LEA-LA, **VDDIO** has to be set to Vcc to assure a 3.0V level at the serial ports. The GPSMODE pins do recognize 1.8V and 3.0V as "high" value at **VDDIO**.
6	**VCC**	2.70 – 3.30V	**VCC**	2.70 – 3.30V	No difference
7	**GND**	GND	**GND**	GND	No difference
8	**VDD18OUT**	Not connected	**VDD18OUT**	Not connected	No difference
9	**GPSMODE6**	Connected to GND or VDD_18OUT	**PCS0_N**	Not connected	Backward compatible: can be left open or connected to GND, VDDIO or VDD_18OUT.
10	**RESET_N**	1.8V	**RESET_N**	1.8V	No difference (see *section 1.8*).
11	**V_BAT**	1.95 – 3.6V	**V_BAT**	1.50 – 3.6V	Wider voltage range. Uncritical for migration.
12	**BOOT_INT**	NC	**BOOT_INT**	NC	No difference
13	**GND**	GND	**GND**	GND	No difference
14	**GND**	GND	**GND**	GND	No difference
15	**GND**	GND	**GND**	GND	No difference
16	**RF_IN**	RF_IN	**RF_IN**	RF_IN	No difference
17	**GND**	GND	**GND**	GND	No difference
18	**VCC_RF**	VCC - 0.1V	**VCC_RF**	VCC - 0.1V	No difference
19	**V_ANT**	3.0V –5.0V	**V_ANT**	3.0V -5.0V	No difference
20	**AADET_N**	Connected to GND	**AADET_N**	Not connected	No external pull down resistor required, as there is already an internal pull down resistor. Please check resistor values in *section 1.9.4*.
21	**GPSMODE5**	Connected to GND or VDD_18OUT	**EXTINT1**	Not connected	Do not add an external pull up resistor; there is one built-in. Leave open if not used. If permantently connected to GND, the FixNOW sleep mode is increased by up to 50µA

[8] Connecting the GPSMODE23 pin (LEA-4S) to GND increased the FixNOW sleep mode current by about 50µA. Connecting the GPSMODE2 pin (LEA-4A) to GND does however not have an impact on the FixNOW sleep mode current.

Pin	LEA-LA		LEA-4H / LEA-4P		Remarks for Migration
	Pin Name	Typical Assignment	Pin Name	Typical Assignment	
22	**GPSMODE2**	Connected to GND or VDD_18OUT	**PCS2_N**	Not connected	Backward compatible: can be left open or connected to GND, VDDIO or VDD_18OUT.
23	**NC**	Not connected	**SCK**	Not connected	Placing a LEA-4x into an existing LEA-LA board design will disable USB port.
24	**NC**	Connected to GND	**VDDUSB**	Connected to GND or VDD_USB	
25	**NC**	Not connected	**USB_DM**	Not connected	
26	**NC**	Not connected	**USB_DP**	Not connected	
27	**EXTINT0**	Connected to VDD18OUT	**EXTINT0**	Not connected	Do not add an external pull up resistor; there is one built-in to **V_BAT**. Leave open if not used.
28	**TIMEPULSE**	1.8V out	**TIMEPULSE**	VDDIO level I/O	Consider that **TIMPULSE** on LEA-4x is on **VDDIO** voltage level (1.8V on LEA-LA)

: Pins to be checked carefully

Table 2: Pin-out comparison LEA-LA vs. LEA-4x

1.4.4 Migration from TIM-Lx to TIM-4x pin out

The pin-outs of TIM-Lx and TIM-4x modules do not differ significantly. *Table 3* compares the modules and highlights the differences to be considered. Please note that this table does not consider any migration from TIM-LR.

Pin	TIM-Lx		TIM-4x		Remarks
	Pin Name	Typical Assignment	Pin Name	Typical Assignment	
1	**VCC**	2.70 – 3.30V	**VCC**	2.70 – 3.30V	No difference
2	**GND**	GND	**GND**	GND	No difference
3	**BOOT_INT**	NC	**BOOT_INT**	NC	No difference
4	**RXD1**	3.0V in; pull up to VCC if not used	**RXD1**	1.8 - 5.0V in	Do not add an external pull up resistor; there is one built-in to **V_BAT**. Leave open if not used.
5	**TXD1**	3.0V out	**TXD1**	3.0V out	No difference
6	**TXD2**	3.0V out	**TXD2**	3.0V out	No difference
7	**RXD2**	3.0V in; pull up to VCC if not used	**RXD2**	1.8 - 5.0V in	Do not add an external pull up resistor; there is one built-in to **V_BAT**. Leave open if not used.
8	**P17 / GPSMODE5**	1.8V I/O (LP: 3.0V), not connected	**P17/ GPSMODE5**	3.0V I/O, not connected	No difference[9]
9	**STATUS / GPSMODE3**	1.8V I/O (LP: 3.0V), not connected	**EXTINT1 / GPSMODE3**	3.0V I/O, not connected	Status Pin not available anymore; No difference[9] otherwise.
10	**VDD18_OUT** TIM-LP: **NC/GND**	Not connected	**VDD18OUT**	Not connected	No difference, except for **TIM-LP**.
11 to 16	**GND**	GND	**GND**	GND	No difference
17	**RF_IN**	RF_IN	**RF_IN**	RF_IN	No difference
18	**GND**	GND	**GND**	GND	No difference
19	**V_ANT**	3.0V -5.0V	**V_ANT**	3.0V -5.0V	No difference
20	**VCC_RF**	VCC - 0.1V	**VCC_RF**	VCC - 0.1V	No difference
21	**V_BAT**	1.95 – 3.6V	**V_BAT**	1.50 – 3.6V	Wider voltage range. Uncritical for migration.
22	**RESET_N**	1.8V	**RESET_N**	1.8V	No difference. Don't drive high. Refer to *section 1.8* for more information.
23	**EXTINT0**	Not connected	**EXTINT0**	Not connected	No difference
24	**PCS1_N/ GPSMODE2**	1.8V I/O (LP: 3.0V), not connected	**PCS1_N/ GPSMODE2**	3.0V I/O, not connected	No difference[9]
25	**PCS0_N/ GPSMODE6**		**PCS0_N/ GPSMODE6**		No difference[9]
26	**SCK/ GPSMODE7**		**SCK/ NC**		No difference on Programmable receivers[9]. But on TIM-4A: the Navigation rate cannot be changed anymore. It's always 1Hz.

[9] Higher output voltage is only significant when using GPIO pin functionality together with an SCKit application.

27	**AADET_N**	Not connected	**AADET_N**	Not connected	No external pull down resistor required as there is already an internal pull down register. Please check resistor values *in section 1.9.4.*
28	**MOSI/ GPSMODE8**	1.8V I/O (LP: 3.0V), not connected	**MOSI/ P24**	3.0V I/O, not connected	No difference on Programmable receivers[9]. But on TIM-4A/TIM-4S, the navigation rate cannot be changed anymore. It's always 1Hz.
29	**TIMEPULSE**	1.8V out (LP: 3.0V)	**TIMEPULSE**	3.0V out	Same functionality but different output voltage.
30	**PCS3_N/ GPSMODE12**	1.8V I/O (LP: 3.0V), not connected	**PCS3_N/ GPSMODE 12**	3.0V I/O, not connected	No difference[9]

: Pins to be checked carefully

Table 3: Pin-out comparison TIM-Lx vs. TIM-4x

1.5 Pin Comparison ANTARIS® to ANTARIS®4

Pin	ANTARIS®								ANTARIS®4				Pin
	TIM-LA /TIM-LC		TIM-LL/ TIM-LF/ TIM-LH		TIM-LP		TIM-LR		TIM-4A/ TIM-4S		TIM-4P/ TIM-4H		
	Pin Name	Typical Assignment	Pin Name	Typical Assignment	Pin Name	Typical Assignment	Pin Name	Typical Assignment	Pin Name	Typical Assignment	Pin Name	Typical Assignment	
1	**VCC**	2.70 – 3.30V	**VCC**	2.70 – 3.30V	**VCC**	2.70 – 3.30V	**VCC**	2.70 – 3.30V	**VCC**	2.70 – 3.30V	**VCC**	2.70 – 3.30V	1
2	**GND**	GND	**GND**	GND	**GND**	GND	**GND**	GND	**GND**	GND	**GND**	GND	2
3	**BOOT_INT**	NC	**BOOT_INT**	NC	**BOOT_INT**	NC	**BOOT_INT**	NC	**BOOT_INT**	NC	**BOOT_INT**	NC	3
4	**RXD1**	3.0V in	**RXD1**	3.0V in	**RXD1**	3.0V in	**RXD1**	3.0V in	**RXD1**	3.0V in	**RXD1**	3.0V in	4
5	**TXD1**	3.0V out	**TXD1**	3.0V out	**TXD1**	3.0V out	**TXD1**	3.0V out	**TXD1**	3.0V out	**TXD1**	3.0V out	5
6	**TXD2**	3.0V in	**TXD2**	3.0V out	**TXD2**	3.0V out	**TXD2**	3.0V out	**TXD2**	3.0V out	**TXD2**	3.0V out	6
7	**RXD2**	3.0V out	**RXD2**	3.0V in	**RXD2**	3.0V in	**RXD2**	3.0V in	**RXD2**	3.0V in	**RXD2**	3.0V in	7
8	**GPSMODE5**	NC (1.8V)	**SCK1/ P17**	NC (1.8V)	**SCK1/ P17**	NC (3.0V)	**FWD**	Direction (1.8V)	**GPSMODE5**	NC (3.0V)	**SCK1/ P17**	NC (3.0V)	8
9	**GPSMODE3**	NC (1.8V)	**STATUS**	NC (1.8V)	**STATUS**	NC (3.0V)	**STATUS**	NC (1.8V)	**GPSMODE3**	NC (3.0V)	**EXTINT1/P13**	NC (3.0V)	9
10	**VDD18OUT**	NC	**VDD18OUT**	NC	**RESERVED**	NC	**VDD18OUT**	NC	**VDD18OUT**	NC	**VDD18OUT**	NC	10
11 to 16	**GND**	GND	**GND**	GND	**GND**	GND	**GND**	GND	**GND**	GND	**GND**	GND	11 to 16
17	**RF_IN**	RF_IN	**RF_IN**	RF_IN	**RF_IN**	RF_IN	**RF_IN**	RF_IN	**RF_IN**	RF_IN	**RF_IN**	RF_IN	17
18	**GND**	GND	**GND**	GND	**GND**	GND	**GND**	GND	**GND**	GND	**GND**	GND	18
19	**V_ANT**	3.0V - 5.0V	**V_ANT**	3.0V - 5.0V	**V_ANT**	3.0V - 5.0V	**V_ANT**	3.0V - 5.0V	**V_ANT**	3.0V - 5.0V	**V_ANT**	3.0V - 5.0V	19
20	**VCC_RF**	VCC - 0.1V	**VCC_RF**	VCC - 0.1V	**VCC_RF**	VCC - 0.1V	**VCC_RF**	VCC - 0.1V	**VCC_RF**	VCC - 0.1V	**VCC_RF**	VCC - 0.1V	20
21	**V_BAT**	1.95 – 3.6V	**V_BAT**	1.95 – 3.6V	**V_BAT**	1.95 – 3.6V	**V_BAT**	1.95 – 3.6V	**V_BAT**	1.50 – 3.6V	**V_BAT**	1.50 – 3.6V	21
22	**RESET_N**	*ACTIVE LOW*	**RESET_N**	*ACTIVE LOW*	**RESET_N**	*ACTIVE LOW*	**RESET_N**	*ACTIVE LOW*	**RESET_N**	*ACTIVE LOW*	**RESET_N**	*ACTIVE LOW*	22
23	**EXTINT0**	NC (1.8V)	**EXTINT0/ P9**	NC (1.8V)	**EXTINT0/ P9**	NC (3.0V)	**SPEED**	Wheel Tick (1.8V)	**EXTINT0**	NC (3.0V)	**EXTINT0/ P9**	NC (3.0V)	23
24	**GPSMODE2**	NC (1.8V)	**PCS1_N/ P27**	NC (1.8V)	**PCS1_N/ P27**	NC (3.0V)	**PCS1_N**	SPI (1.8V)	**GPSMODE2**	NC (3.0V)	**PCS1_N/ P27**	NC (3.0V)	24
25	**GPSMODE6**	NC (1.8V)	**PCS0_N/ SS_N/ P26**	NC (1.8V)	**PCS0_N/ SS_N/ P26**	NC (3.0V)	**PCS0_N**	SPI (1.8V)	**GPSMODE6**	NC (3.0V)	**PCS0_N/ SS_N/ P26**	NC (3.0V)	25
26	**GPSMODE7**	NC (1.8V)	**SCK/ P23**	NC (1.8V)	**SCK/ P23**	NC (3.0V)	**SCK**	SPI (1.8V)	**NC**	NC	**SCK/ P23**	NC (3.0V)	26
27	**AADET_N**	NC (1.8V)	**AADET_N**	NC (1.8V)	**AADET_N**	NC (3.0V)	**MISO**	SPI (1.8V)	**AADET_N**	NC (3.0V)	**AADET_N**	NC (3.0V)	27
28	**GPSMODE8**	NC (1.8V)	**MOSI/ P24**	NC (1.8V)	**MOSI/ P24**	NC (3.0V)	**MOSI**	NC (1.8V)	**P24**	NC	**MOSI/ P24**	NC (3.0V)	28
29	**TIMEPULSE**	1.8V out	**TIMEPULSE**	1.8V out	**TIMEPULSE**	3.0V out	**TIMEPULSE**	1.8V out	**TIMEPULSE**	3.0V out	**TIMEPULSE**	3.0V out	29
30	**GPSMODE12**	NC (1.8V)	**PCS3_N/ P29**	NC (1.8V)	**PCS3_N/ P29**	NC (3.0V)	**AADET_N**	NC (1.8V)	**GPSMODE12**	NC (3.0V)	**PCS3_N/ P29**	NC (3.0V)	30

: Pins to be checked carefully; NC: Not connected

Table 4: Typical Pin Assignment TIM modules

Pin	ANTARIS®		ANTARIS®4				Pin
	LEA-LA		LEA-4A/ LEA-4S		LEA-4P/ LEA-4H/ LEA-4T		
	Pin Name	Typical Assignment	Pin Name	Typical Assignment	Pin Name	Typical Assignment	
1	**TxD2**	3.0V out	**TxD2**	3.0V out	**MOSI**	NC	1
2	**RxD2**	3.0V out	**RxD2**	1.8 to 5.0V in	**MISO**	NC	2
3	**TxD1**	3.0V out	**TxD1**	3.0V out	**TxD1**	3.0V out	3
4	**RxD1**	3.0V in	**RxD1**	1.8 to 5.0V in	**RxD1**	1.8 to 5.0V in	4
5	**VDDIO**	VCC	**VDDIO**	VCC	**VDDIO**	VCC	5
6	**VCC**	2.70 – 3.30V	**VCC**	2.70 – 3.30V	**VCC**	2.70 – 3.30V	6
7	**GND**	GND	**GND**	GND	**GND**	GND	7
8	**VDD18OUT**	1.8V out	**VDD18OUT**	1.8V out	**VDD18OUT**	1.8V out	8
9	**GPSMODE6**	NC (GND or VDD18OUT)	**GPSMODE6**	NC (GND or VDD18OUT)	**PCS0_N/ SS_N/ P26**	NC (3.0V)	9
10	**RESET_N**	*ACTIVE LOW*	**RESET_N**	*ACTIVE LOW*	**RESET_N**	*ACTIVE LOW*	10
11	**V_BAT**	1.95 – 3.6V	**V_BAT**	1.50 – 3.6V	**V_BAT**	1.50 – 3.6V	11
12	**BOOT_INT**	NC	**BOOT_INT**	NC	**BOOT_INT**	NC	12
13	**GND**	GND	**GND**	GND	**GND**	GND	13
14	**GND**	GND	**GND**	GND	**GND**	GND	14
15	**GND**	GND	**GND**	GND	**GND**	GND	15
16	**RF_IN**	RF_IN	**RF_IN**	RF_IN	**RF_IN**	RF_IN	16
17	**GND**	GND	**GND**	GND	**GND**	GND	17
18	**VCC_RF**	VCC - 0.1V	**VCC_RF**	VCC - 0.1V	**VCC_RF**	VCC - 0.1V	18
19	**V_ANT**	3.0V - 5.0V	**V_ANT**	3.0V - 5.0V	**V_ANT**	3.0V - 5.0V	19
20	**AADET_N**	NC (1.8V)	**AADET_N**	NC (1.8 to 5.0V)	**AADET_N**	NC (1.8 to 5.0V)	20
21	**GPSMODE5**	NC (GND or VDD18OUT)	**GPSMODE5**	NC (GND or VDD18OUT)	**EXTINT1/ P13**	NC (1.8 to 5.0V)	21
22	**GPSMODE2**	NC (GND or VDD18OUT)	**GPSMODE2**	NC (GND or VDD18OUT)	**PCS2_N/ P12**	NC (1.8 to 5.0V)	22
23	**N/C**	NC (1.8V)	**GPSMODE7**	NC (1.8 to 5.0V)	**SCK/ P23**	NC (1.8 to 5.0V)	23
24	**N/C**	GND	**VDDUSB**	3.0 –3.6V/ GND	**VDDUSB**	3.0 – 3.6V/ GND	24
25	**N/C**	NC (1.8V)	**USB_DM**	VDDUSB I/O	**USB_DM**	VDDUSB I/O	25
26	**N/C**	NC (1.8V)	**USB_DP**	VDDUSB I/O	**USB_DP**	VDDUSB I/O	26
27	**EXTINT0**	NC (1.8V)	**EXTINT0**	NC (1.8 to 5.0V)	**EXTINT0/ P9**	NC (1.8 to 5.0V)	27
28	**TIMEPULSE**	1.8V out	**TIMEPULSE**	VDDIO out	**TIMEPULSE**	VDDIO out	28

: Pins to be checked carefully; NC: Not connected

Table 5: Typical Pin Assignment LEA modules

1.6 Migration from TIM-ST to TIM-4x

A4

Migrating a TIM-ST design to one of the TIM-4x GPS receivers is usually an easy, straightforward procedure. This section summarizes most important differences.

NMEA Protocol

TIM-ST and TIM-Lx output NMEA data (GGA, GLL, GSA, GSV, RMC, VTG and ZDA messages) on port 1.

TIM-ST	TIM-4x (ANTARIS®4)	Remarks
NMEA V2.2	NMEA V2.3	Most NMEA parsers should be able to handle V2.2 and V2.3. Should your parser struggle with V2.3, configure TIM-4x to output NMEA V2.1 by sending an UBX-CFG-NMEA message.
12 channels	16 channels	ANTARIS®4 is able to track up to 16 satellites in parallel. Since one GSV message contains only up to 4 satellites, ANTARIS may send up to 4 GSV messages whereas TIM-ST only output 3. If this causes problem, reduce the NMEA output of ANTARIS to 12 satellites by sending a CFG-NMEA message
Lat and Long are output in case of invalid fixes	Lat and Long are only output for valid fixes	ANTARIS®4 can be reconfigured to output Lat and Long in case of invalid fixes by sending an UBX-CFG-NMEA message.
Accepts position up to a PDOP of 50	Accepts position up to a PDOP of 25	ANTARIS®4 receivers are more sensitive than TIM-ST. Hence the more conservative approach with a PDOP of 25 works usually fine. However, it's possible to configure TIIM-Lx to accept position with a higher PDOP by sending a UBX-CFG-NAV2 message
Lat and Long are output with 4, the time with 3 position after decimal point	Lat and Long are output with 5, the time with 2 position after decimal point	The NMEA specification is fairly open and allows minor variations in the implementation (e.g. number of position after decimal point, etc.) but it always requests commas between as a separator between NMEA data fields. One should therefore write a parser that searches for commas and extracts everything between two commas. This way, the parser is independent of the number of digits for the individual message fields. It will even be able to handle empty fields ",,". Beside the commas, a good parser should be able the handle the valid flags correctly. Data are only valid if the valid flag is set to valid. If it's set to invalid, the NMEA parser should reject data output by the receiver. By no means should it forward it to the application. Starting with Firmware 5.0, it's possible to configure ANTARIS®4 to output LAT & LON with 4 digits etc.
Supports proprietary NMEA messages (PSRF)	Supports proprietary NMEA messages (PUBX)	The NMEA specification does not include input messages. This is why GPS manufacturers introduce proprietary NMEA messages. If PSRF messages have been used with TIM-ST, migrate them to either PUBX or even better to UBX-CFG-xxx messages. The latter is preferred and it's easy since ANTARIS is able to handle 2 protocols on the same port.

Binary Protocol

TIM-ST supports SiRF binary protocol whereas TIM-4x supports UBX protocol. These two protocols are not compatible. It is necessary to migrate the host software to UBX protocol if SiRF binary was used before.

Antenna and Antenna Supervisor

TIM-ST does not have a built-in antenna supervisor whereas all TIM-4x modules have a built-in short-circuit detection. TIM-ST designs with external active antenna supervisor will not work without minor modifications to the circuitry.

Power Supply

TIM-4x receivers consume approximately 120mA less current, which is usually not a problem.

	TIM-ST	TIM-4x (ANTARIS®4)	Remarks
Vcc	2.75 – 3.45	2.7 – 3.3V	
Current Consumption	<160mA	Approx 36 – 40mA	TIM-4x current consumption depends on TIM-4x variant
Power Saving Mode	TPM, Push-2-fix	FixNOW	In most cases, it's not necessary to use FixNOW mode due to the much lower current consumption of TIM-4x

☞ **Note:** Make sure the ripple on Vcc is below 50mV.

Pin-out

The pin-outs of TIM-ST and TIM-4x modules do not differ significantly. *Table 6* compares the modules and highlights the differences to be considered.

Pin	TIM-ST		TIM-4x		Remarks
	Pin Name	Typical Assignment	Pin Name	Typical Assignment	
1	**VCC**	2.75 – 3.45V	**VCC**	2.70 – 3.30V	The nominal voltages are identical but the tolerances differ slightly. u-blox recommends using a 3.0V LDO for TIM-4x
2	**GND**	GND	**GND**	GND	No difference
3	**BOOT_INT**	NC	**BOOT_INT**	NC	No difference
4	**RXD1**	3.0V in	**RXD1**	1.8 to 5.0V in	No difference
5	**TXD1**	3.0V out	**TXD1**	3.0V out	No difference
6	**TXD2**	3.0V in	**TXD2**	3.0V out	No difference
7	**RXD2**	3.0V out	**RXD2**	1.8 to 5.0V in	No difference
8	**AA_SCD_N**	Not connected	**SCK1/ P17/ GPSMODE5**	Not connected	No difference, if Antenna Supervisor is not used.
9	**RF_ON**	Not connected	**EXTINT1/ GPSMODE3**	Not connected	No difference, if RF_ON has not been used.
10	**GND**	Not connected	**VDD18OUT**	Not connected	Different functionality on ANTARIS TIM modules. **Needs to be redesigned!**
11 to 16	**GND**	GND	**GND**	GND	No difference
17	**RF_IN**	RF_IN	**RF_IN**	RF_IN	No difference
18	**GND**	GND	**GND**	GND	No difference
19	**V_ANT**	3.0V –5.0V	**V_ANT**	3.0V -5.0V	No difference
20	**VCC_RF**	VCC - 0.1V	**VCC_RF**	VCC - 0.1V	No difference
21	**V_BAT**	1.85 – 3.6V	**V_BAT**	1.50 – 3.6V	Wider voltage range
22	**RESET_N**	3.0V	**RESET_N**	1.8V	Different voltage range. No problem as long as this pin is not driven high.
23	**NU**	Not connected	**EXTINT0**	3.0V I/O, not connected	This pin is an input on TIM-4x, hence no problem
24	**NU**	Not connected	**PCS1_N/ GPSMODE2**	3.0V I/O, not connected	No difference
25	**NU**	Not connected	**PCS0_N/ GPSMODE6**	3.0V I/O, not connected	No difference
26	**NU**	Not connected	**SCK/ NC**	3.0V I/O, not connected	No difference
27	**AA_OCD**	Not connected	**AADET_N**	3.0V I/O, not connected	No problem if this pin is not used on TIM-ST. If it was used to control the antenna voltage supply, a minor modification is required for TIM-4x designs.
28	**AA_CTRL**	Not connected	**MOSI/ NC**	3.0V I/O, not connected	No problem if this pin is not used on TIM-ST. If it was used to control the antenna voltage supply, a minor modification is required for TIM-4x designs.
29	**TIMEPULSE**	3.0V out	**TIMEPULSE**	3.0V out	No difference
30	**GND**	Not connected	**PCS3_N/ GPSMODE 12**	3.0V I/O, not connected	P29 is an input on TIM-4x, hence no problem

: Pins to be checked carefully

Table 6: Pin-out comparison TIM-ST vs. TIM-4x

1.7 Backup Battery

In case of a power failure on pin **VCC**, real-time clock and backup RAM are supplied through pin **V_bat**. This enables the ANTARIS®4 GPS Receiver to recover from power failure with either a hotstart or a warmstart (depending on the duration of **VCC** outage) and to maintain the configuration settings. If no Backup Battery is connected, the receiver performs a coldstart upon powered up.

☞ **Note** If no backup battery is available connect the V_bat pin to GND.

As long as Vcc is supplied to the ANTARIS®4 GPS Receiver, the backup battery is disconnected from the RTC and the backup RAM in order to avoid unnecessary battery drain (see *Figure 7*). Power to RTC and BBR is supplied from Vcc in this case.

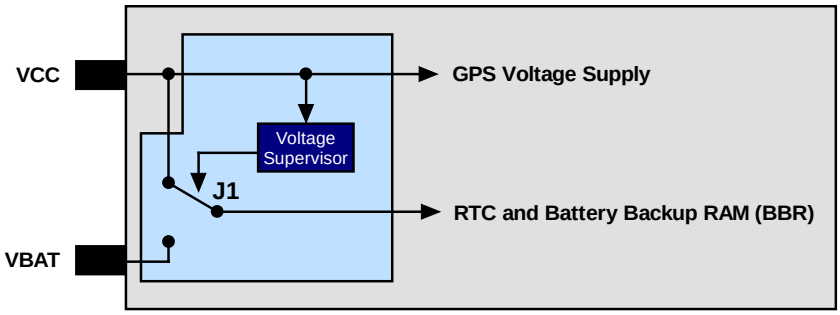


Figure 7: Backup Battery and Voltage

Before Vcc is supplied for the first time, switch J1 *Figure 7* is not initialized. In this case excessive battery drain might occur if the backup battery is connected to the **V_Bat** pin. The battery drain will drop to the specified level as soon as Vcc is applied the first time.

☞ **Note** It's advised to connect the backup battery while Vcc is on or – if not possible – power up the module for a short time (e.g. 1s) ASAP after connecting the backup battery in order to avoid excessive battery drain.

1.7.1 Avoiding excessive current in low power modes

Special attention has to be paid to the pins RxD1, RxD2, EXTINT0 and EXTINT1. These 4 pins can be used to wake up from FixNOW sleep modes. For that reason these pins are powered from backup supply, even if VCC is turned off. Since these pins have internal pull-up resistors, current (e.g. 15µA) flows through these internal resistors if the pin is driven low. To avoid this current, which increases the sleep or backup currents by an order of magnitude, there are different possibilities:

- Leave these pins open.
- Pull them to a "HIGH" while the receiver is in sleep or backup mode
- Make sure the outputs, which drive these pins, are high-impedance state while the receiver is in sleep or backup mode.

☞ **Note** Don't forget, that if you turn off your system, a current may flow from backup battery through the pull-up resistors of these 4 pins (RxD1, RxD2, EXTINT0 and EXTINT1) through ESD protection diodes of your circuit (i.e. micro-controller).

1.8 RESET_N

RESET_N is an open drain I/O pin, thus one can apply external logic to drive the **RESET_N** signal low to activate a hardware reset of the system. In most applications, the use of the **RESET_N** pin is not required since ANTARIS 4 GPS modules contain an internal reset chip. Leave RESET_N unconnected if not used.

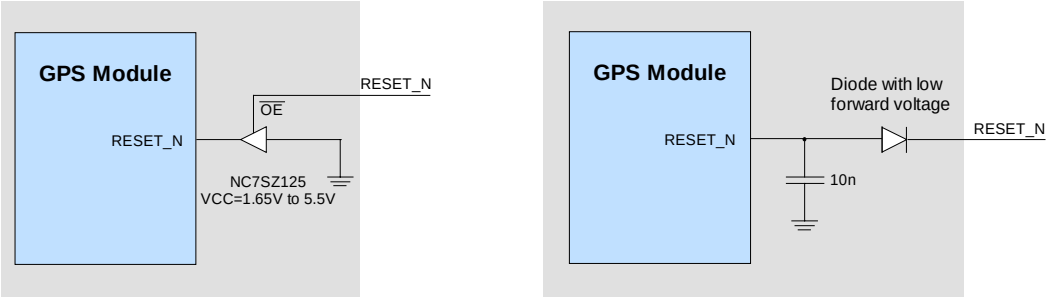


Figure 8: Examples for wiring RESET_N

☞ **Warning** Do not drive **RESET_N** high. The maximum output voltage at RESET_N is limited to 1.8 V. RESET_N is sensitive even to short voltage spikes. Keep this signal clean if routed outside the module.

1.9 Antenna and Antenna Supervisor

ANTARIS®4 GPS Receivers get the L1 band signals from GPS satellites at a nominal frequency of 1575.42 MHz. The RF signal is connected to the **RF_IN** pin.

ANTARIS®4 GPS modules can be connected to an on-board passive patch antenna or an active antenna.

☞ **Note** For ANTARIS®4 GPS receivers, the total preamplifier gain (minus cable and interconnect losses) must not exceed 50 dB. Total noise figure should be below 3 dB.

The ANTARIS®4 Technology supports either a short circuit protection of the active antenna or an active antenna supervisor circuit (open and short circuit detection). For further information refer to *Section 1.9.2ff).*

1.9.1 Passive Antenna

A design using a passive antenna requires more attention regarding the layout of the RF section. Typically a passive antenna is located near electronic components; therefore care should be taken to reduce electrical 'noise' that may interfere with the antenna performance. For further information about passive Antenna design refer to *Section 1.14*

Passive antennas do not require a DC bias voltage and can be directly connected to the RF input pin **RF_IN**. Sometimes, they may also need a passive matching network to match the impedance to 50 Ohms.

☞ **Note** Some passive antenna designs present a DC short to the RF input, when connected. If a system is designed with antenna bias supply AND there is a risk of a passive antenna being connected to the design, consider a short circuit protection.

☞ **Note** All ANTARIS®4 receivers have a built-in LNA required for passive antennas.

1.9.2 Active Antenna

Active antennas have an integrated low-noise amplifier. They can be directly connected to **RF_IN**. If an active antenna is connected to **RF_IN**, the integrated low-noise amplifier of the antenna needs to be supplied with the

correct voltage through pin **V_ANT**. Usually, the supply voltage is fed to the antenna through the coaxial RF cable. Active antennas require a power supply that will contribute to the total GPS system power consumption budget with additional 5 to 20 mA typically. Inside the antenna, the DC component on the inner conductor will be separated from the RF signal and routed to the supply pin of the LNA (see *Figure 9*).

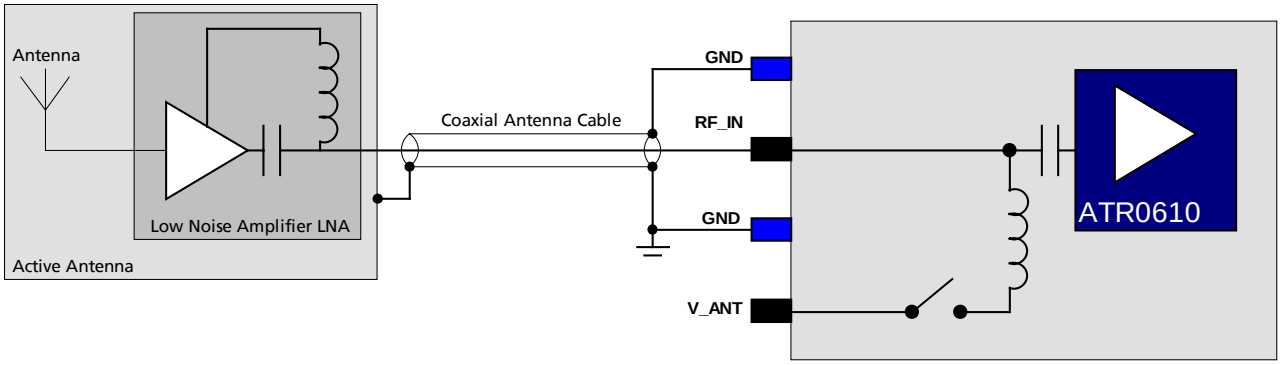


Figure 9: Active antenna biasing

Generally an active antenna is easier to integrate into a system design, as it is less sensitive to jamming compared to a passive Antenna. But an active Antenna must also be placed far from any noise sources to have a good performance.

! **Warning** Antennas should only be connected to the receiver when the receiver is not powered. Do not connect or disconnect the Antenna when the ANTARIS®4 GPS receiver is running. The receiver calibrates the noise floor on power-up, connecting the antenna after power-up can result in prolonged acquisition time.

! **Warning** Never feed supply voltage into RF_IN. Always feed via V_ANT into RF_IN.

☞ **Note** To test GPS signal reacquisition, we recommend physically blocking the signal to the antenna, rather than disconnecting and reconnecting the receiver.

1.9.3 Active Antenna Bias Power

There are two ways to supply the bias voltage to pin **V_ANT**. It can be supplied externally (please consider the datasheet specification) or internally. For Internal supply, the **VCC_RF** output must be connected to **V_ANT** to supply the antenna with a filtered supply voltage. However, the voltage specification of the antenna has to match the actual supply voltage of the ANTARIS®4 GPS Receiver (e.g. 3.0 V).

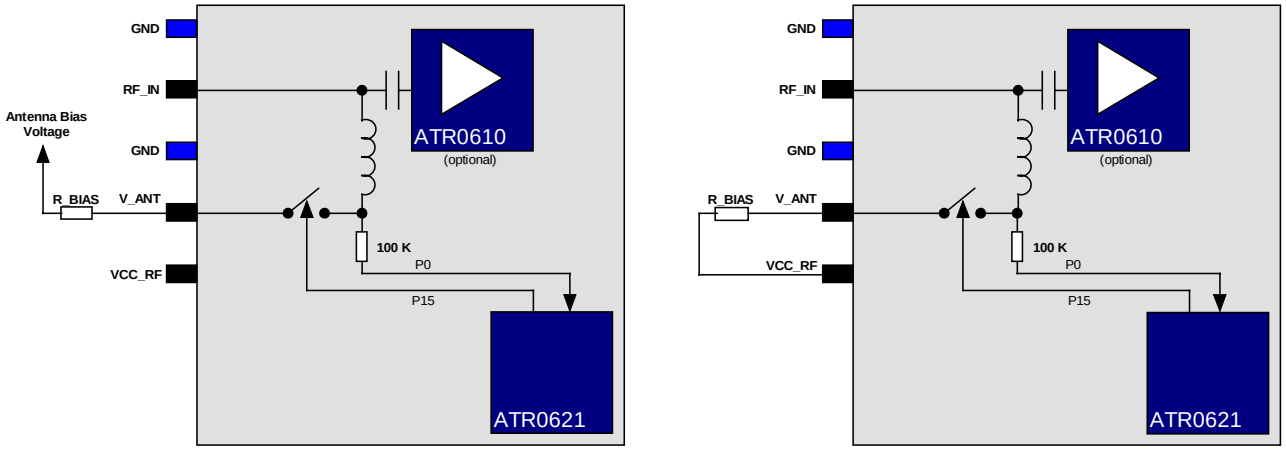


Figure 10: Supplying Antenna bias voltage

Since the bias voltage is fed into the most sensitive part of the receiver, i.e. the RF input, this supply should be virtually free of noise. Usually, low frequency noise is less critical than digital noise with spurious frequencies with harmonics up to the GPS band of 1.575 GHz. Therefore, it is not recommended to use digital supply nets to feed pin **V_ANT**.

An internal switch (under control of the ANTARIS®4 GPS software) can shutdown the supply to the external antenna whenever it is not needed. This feature helps to reduce power consumption when the GPS receiver is in Sleep Mode.

☞ **Note** The Antenna Supervisor will switch the antenna bias voltage off while **VCC** is off.

1.9.4 Active Antenna Supervisor

The ANTARIS® GPS Technology provides the means to implement an active antenna supervisor with a minimal number of parts. The antenna supervisor is highly configurable to suit various different applications.

1.9.4.1 Short Circuit Protection

If a reasonably dimensioned series resistor **R_BIAS** is placed in front of pin **V_ANT**, a short circuit situation can be detected by the baseband processor. If such a situation is detected, the baseband processor will shut down supply to the antenna. For firmware version earlier than 5.00, the voltage supply to the antenna will only be re-established after a hardware reset of the receiver, e.g. after power cycling. For firmware version 5 or later the receiver can be configured to try to reestablish antenna power supply periodically.

☞ **Note** To configure the antenna supervisor use the UBX-CFG-ANT message. For further information refer to the *ANTARIS®4 Protocol Specification.*

References	Value	Tolerance	Description	Manufacturer
R_BIAS	10 Ω	± 10%	Resistor, min 0.250 W	

Table 7: Short circuit protection, bill of material

! **Warning** Short circuits on the antenna input without current limitation will result in a permanent damage of the receiver! Therefore it's recommended to implement a R_BIAS in all applications, where the antenna can be disconnected by the end-user or with a long antenna cable.

☞ **Note** An additional R_BIAS is not required, when using a short and open active antenna supervisor circuitry as defined in *Section 1.9.4.2*, as the R_BIAS is equal to R2.

☞ **Note** Max voltage for the short circuit protection circuitry is V_ANT_MAX specified in the datasheet of the ANTARIS® GPS receiver.

1.9.4.2 Short and Open Circuit Active Antenna Supervisor

The Antenna Supervisor can be configured by a serial port message (using only UBX binary message).

When enabled the active antenna supervisor produces serial port messages (status reporting in NMEA and/or UBX binary protocol) which indicates all changes of the antenna circuitry (**disabled** antenna supervisor, antenna circuitry **ok**, **short** circuit, **open** circuit) and shuts the antenna supply down if required.

Following state diagram shall apply. Initial state after power-up is "Active Antenna OK".

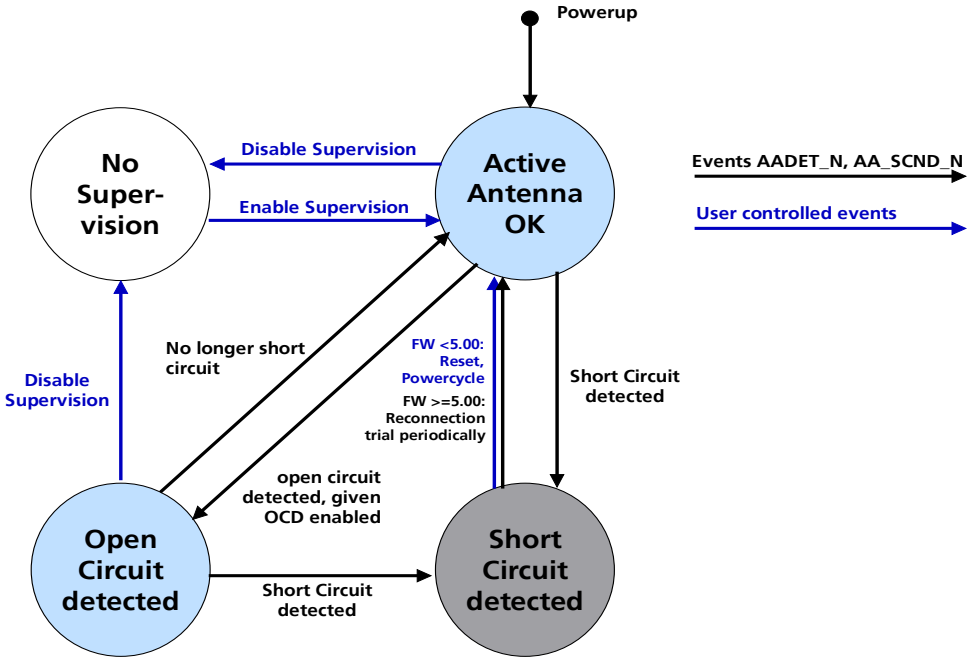


Figure 11: State Diagram of Active Antenna Supervisor

The active antenna supervisor provides the means to check the active antenna for open and short circuits and to shut the antenna supply off, if a short circuit is detected.

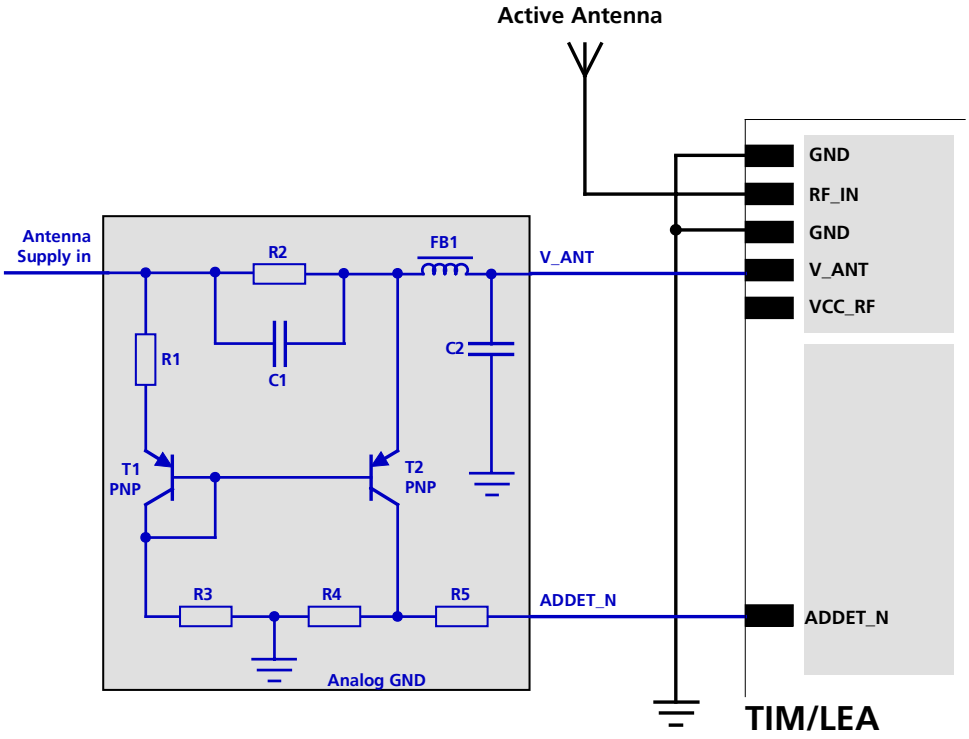


Figure 12: Schematic of open circuit detection

References	Value	Tolerance	Description	Remarks
C1	2.2 µF	± 10%	Capacitor, X7R, min 10 V	
C2	100 nF	± 10%	Capacitor, X7R, min 10 V	
FB1	600 Ω		Ferrite Bead	e.g. Murata BLM18HD601SN1
R1	56 Ω	± 10%	Resistor, min 0.063 W	
R2	10 Ω	± 10%	Resistor, min 0.250 W	
R3, R4	5.6 kΩ	± 10%	Resistor, min 0.063 W	
R5	OR or 47 kΩ	± 10%	Resistor, min 0.063 W	Use 0R if antenna voltage supply is <4.5V. Otherwise, use a 47k resistor.
T1, T2			PNP Transistor BC856B	e.g. Philips Semiconductors

Table 8: Active Antenna Supervisor, bill of material

☞ **Note** Maximum voltage for the short circuit protection circuitry is V_ANT_MAX as specified in the datasheet of the ANTARIS® GPS receivers.

Short Circuit Detection (SCD)

A short circuit in the active antenna pulls **V_ANT** to ground. This is detected inside the ANTARIS® GPS module and the antenna supply voltage will be shut down.

☞ **Note** Antenna short detection (SCD) and control is enabled by default.

Open Circuit Detection (OCD)

The open circuit detection circuit uses the current flow to detect an open circuit in the antenna. The threshold current is at 3-5mA. A current below 3mA will definitely indicate an open circuit. A current above 5mA will definitely indicate no open circuit (values apply for R2=10 Ω).

If the current through T2 is large, the voltage drop through R4 and therefore ADDET_N will be high, indicating an open connection. On the other hand, if the current is small, ADDET_N will be low.

☞ **Note** On Programmable GPS Modules the antenna open circuit detection (OCD) is disabled by default, on Low Cost modules it's enabled.

Message Reporting

At startup and on every change of the antenna supervisor configuration the ANTARIS® GPS module will output a NMEA ($GPTXT) or UBX (INF-NOTICE) message with the internal status of the antenna supervisor (disabled, short detection only, enabled).

None, one or several of the strings below are part of this message to inform about the status of the active antenna supervisor circuitry (e.g. "ANTSUPERV= AC SD OD PdoS").

Abbreviation	Description
AC	Antenna Control (e.g. the antenna will be switched on/ off controlled by the GPS receiver)
SD	Short Circuit Detection Enabled
OD	Open Circuit Detection Enabled
PDoS	Power Down on short

Table 9: Active Antenna Supervisor Message on startup (UBX binary protocol)

☞ **Note** To activate the antenna supervisor use the UBX-CFG-ANT message. For further information refer to the *ANTARIS®4 Protocol Specification.*

Similar to the antenna supervisor configuration the status of the antenna supervisor will be reported in a NMEA ($GPTXT) or UBX (INF-NOTICE) message at start-up and on every change.

Message	Description
ANTSTATUS=DONTKNOW	Active antenna supervisor is not configured and deactivated.
ANTSTATUS=OK	Active antenna connected and powered
ANTSTATUS=SHORT	Antenna short
ANTSTATUS=OPEN	Antenna not connected or antenna defective

Table 10: Active Antenna Supervisor Message on startup (NMEA protocol)

☞ **Note** The open circuit supervisor circuitry has a quiescent current of approximately 2mA. This current may be reduced with an advanced circuitry, which fulfils the same functionality as the u-blox suggested circuitry.

1.10 Receiver Configuration

1.10.1 Receivers with Flash

This section does not apply for ROM only receivers like TIM-4A/LEA-4A and TIM-4S/LEA-4S. For these receivers refer to section 1.10.2 for more information.

1.10.1.1 Configuration Concept

The ANTARIS®4 GPS Technology is fully configurable with UBX protocol configuration messages (message class UBX-CFG). The configuration of the receiver can be changed during normal operation mode. The configuration data is automatically stored to the current configuration section and becomes immediately active (see *Figure 13*). The ANTARIS®4 GPS core always uses the current configuration.

The settings from the current section will only become permanent settings if they are saved to the permanent configuration section with a 'SAVE' command. The permanent settings are copied to the current section after a start-up or whenever a 'LOAD' command is received. The 'CLEAR' command erases the settings in the permanent section but not the current section.

☞ **Note** The 'SAVE', 'LOAD' and 'CLEAR' commands can be sent to the receiver with an UBX-CFG-CFG message.

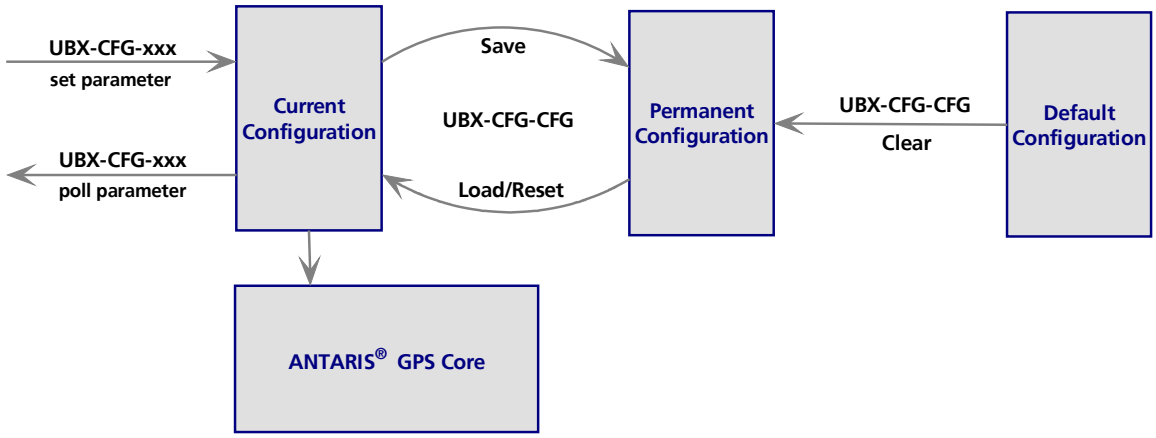


Figure 13: Configuration concept

An alternative approach is to hard-code user settings but this requires software customization. Low Cost receivers also offer the possibility to choose a configuration with pin settings (GPSMODE pins). For further information refer to *Section 1.10.2*.

1.10.1.2 Configuration Storage Media

The configuration may be stored in the on-chip battery backup RAM for Low Cost Receivers or the FLASH memory for Programmable Receivers. The stored configuration will be loaded on every restart. The firmware of the GPS receiver defines which media is used based on the available resources.

An overview of the memory/storage media

Memory/Storage Media	Specifics
SRAM (Static RAM)	Volatile RAM, stored data gets lost on a power down.
On-chip BBR (battery backup RAM) (Low Cost Receivers)	Volatile RAM, stored data remain only if a Backup Battery is applied. Also used to store receiver configuration and GPS data.
FLASH (Programmable GPS receivers)	Non Volatile RAM, used to store data, receiver configuration and user specific firmware code (only with SCKit).
ROM (Read Only Memory)	ROM holds the firmware of the GPS receiver

Table 11: Memory/ Storage Media on

1.10.1.3 Organization of the Configuration Sections

The configuration is divided into several sub-sections. Each of these sub-sections corresponds to one or several UBX-CFG messages.

Sub-Section		CFG - Messages	Description
0	PRT	UBX–CFG–PRT	Port settings
1	MSG	UBX–CFG–MSG UBX–CFG–NMEA	Message settings (enable/disable, update rate)
2	INF	UBX–CFG–INF	Information output settings (Errors, Warnings, Notice, Test etc.)
3	NAV DAT RATE TP TM	UBX–CFG–NAV2 UBX–CFG–DAT UBX–CFG–RATE UBX–CFG–TP UBX–CFG–TM2	Navigation Parameter Receiver Datum Measurement and Navigation Rate setting Timepulse Settings Timemark Settings
4	RXM SBAS	UBX–CFG–RXM UBX–CFG–SBAS	RXM SBAS
5	FXN	UBX–CFG–FXN	Parameters of FixNOW™ mode
6-9	EKF Configuration	UBX–CFG–EKF	EKF Configuration (TIM-LR only)
10	ANT	UBX–CFG–ANT	Antenna Configuration
11	Reserved	N/A	Reserved
12-15	User0 – User3	N/A	User settings, only available with the SCKit

Table 12: Configuration messages

☞ **Note** The sub-sections can be saved, loaded and cleared individually. If a sub-section is cleared, saved or loaded with one single UBX-CFG-CFG message, the ‚CLEAR' command will be executed first, then the ‚SAVE' and finally the ‚LOAD' command.

☞ **Note** The user sections (User0 – User3) are only usable in conjunction with the SCKit.

1.10.1.4 Change Configuration temporarily

To change the configuration temporarily, any of the UBX configuration messages can be sent over the Serial Communication Port. The receiver will change its configuration immediately after receiving the message. However it will not be stored in non-volatile memory.

1.10.1.5 Change Configuration permanently

To change a configuration permanently on the receiver, the configuration parameters must have been previously stored in order to be available at startup. Therefore any permanent change of configuration must be saved in the battery backup RAM for Low Cost receivers or FLASH for Programmable Receivers.

To store a configuration select the UBX – CFG (Config) – CFG (Configuration) save command in u-center AE and send the message to the receiver by pressing the send button (Send).

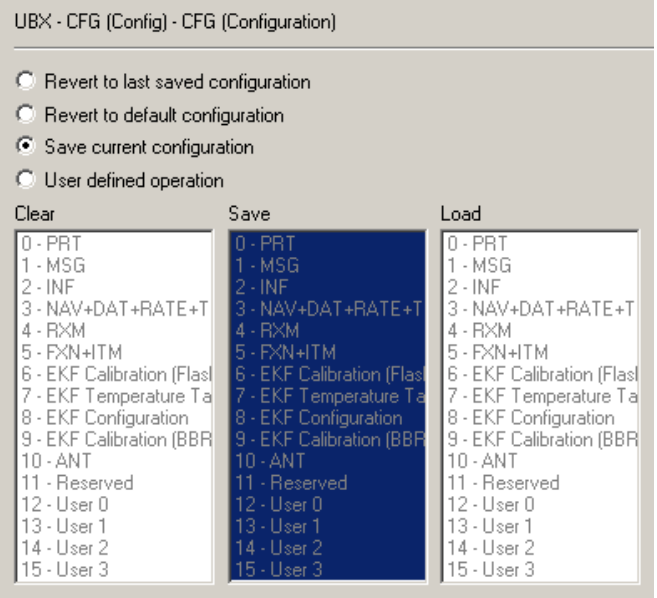


Figure 14: Saving a configuration section

☞ **Note** Use the <ctrl> + <left click> to deselect the last selection, if you choose "user defined".

1.10.1.6 Loading a Configuration

Generally there is no need to manually load configuration settings since they are automatically loaded at startup. The ability to force a load of the settings can be useful if you changed some settings (without saving them) and want to reset the configuration to the last saved configuration. To do this select the requested sections in the load box and send the message to the receiver.

1.10.1.7 Clear a Configuration permanently

Clearing a configuration can be useful if you want to reset to the factory default state. You have to load them afterwards to become effective.

☞ **Note** This operation only clears the configuration Memory. It doesn't reapply defaults. You need to do a „Load" or restart the system in order to load the defaults.

☞ **Note** When selecting sections in the Clear, Save and Load box Configuration is first cleared then saved and finally reloaded.

1.10.2 For ROM only receivers/ Low Cost Receivers (GPSMODE Pin configuration)

This section only applies for TIM-4A/LEA-4A and TIM-4S/LEA-4S. For all other receiver refer to Section 1.10.1 for more information.

1.10.2.1 Start-Up Pin Configuration (GPSMODE Pins)

A4

The start-up configuration of ROM based receivers like TIM-xA/TIM-xS or LEA-xA/LEA-4S is defined by the status of the GPSMODE pins after system reset. The default configuration can by altered by pulling up or down a number of so-called GPSMODE pins (see *Section 1.10.2.1* and *Table 13*) Alternatively, the system can be configured through message commands passed through the serial interface after start-up. *Figure 15* depicts the start-up procedure of ANTARIS®4 GPS receivers.

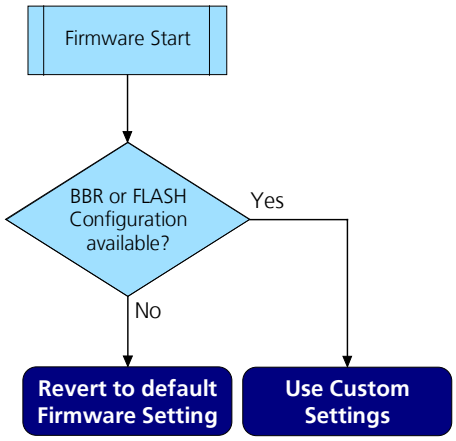


Figure 15: ANTARIS® GPS Technology Start-Up Procedure

☞ **Note** The start-up configuration can be changed at any time sending appropriate configuration commands over serial port.

TIM and LEA receivers support only a subset of all GPSMODE configurations of the ANTARIS®4 Chipset due to limited pin available on the receiver board.

Pin	Function	TIM-4A/ TIM-4S	LEA-4A	LEA-4S
GPSMODE2	GPS sensitivity settings	●	●	O
GPSMODE3		●	O	O
GPSMODE23		O	O	●
GPSMODE5	Serial I/O configuration	●	●	●
GPSMODE6		●	●	●
GPSMODE7	USB Power Mode[10]	O	●	●
GPSMODE12	Serial I/O configuration	●	O	O

●: Available/ O: Not Available

Table 13: Available GPSMODE's

[10] Redefined GPSMODE function for ANTARIS®4 – **caution** when implementing into ANTARIS® designs e.g. TIM-LC, TIM-LA

1.10.2.2 Sensitivity Settings

A4

For LEA-4A, TIM-4A and TIM-4S:

TIM-4x	LEA-A	GPSMODE3 [PU]	GPSMODE2 [PU]	Description
●	O	0	0	Auto
●	O	0	1	Fast Mode
●	●	1	0	Normal sensitivity mode
●	●	1	1	**High sensitivity mode**

●: Available/ O: Not Available/ : Default setting

Table 14: Sensitivity Settings with GPSMODE pins (for TIM-4x and LEA-4A)

For LEA-4S:

LEA-4S	GPSMODE23 [PD]	Description
●	0	**Auto**
●	1	High sensitivity mode

●: Available/ O: Not Available/ : Default setting

Table 15: Sensitivity Settings with GPSMODE pins (for TIM-4S and LEA-4S)

1.10.2.3 Serial I/O Configuration

A4

The ANTARIS® receiver features a two-stage I/O message and protocol selection procedure for the available serial ports.

1. The RTCM, NMEA or UBX protocol can be enabled or disabled for a given USART port.
2. Messages can be enabled or disabled for each enabled protocol on each port.

To handle the serial I/O configuration with GPSMODE pins, there are message sets defined and **all protocols are enabled on all ports** (for input and output).

TIM	LEA	GPSMODE			USART1/ USB	USART2	Message set	Information Messages (UBX INF)	Information Messages (NMEA TXT)
		12 PU	6 PU	5 PD	Output Protocol / Baudrate (kBaud)				
●	O	0	0	0	UBX / 57.6	NMEA / 19.2	High	User, Notice, Warning, Error	
●	O	0	0	1	UBX / 38.4	NMEA / 9.6	Medium	User, Notice, Warning, Error	
●	O	0	1	0	UBX / 19.2	NMEA / 4.8	Low	User, Notice, Warning, Error	
●	O	0	1	1	- / Auto	- / Auto	Off	None	None
●	●	1	0	0	NMEA / 19.2	UBX / 57.6	High		User, Notice, Warning, Error
●	●	1	0	1	NMEA / 4.8	UBX / 19.2	Low		User, Notice, Warning, Error
●	●	**1**	**1**	**0**	**NMEA / 9.6 (default)**	**UBX / 38.4 (default)**	**Medium**		**User, Notice, Warning, Error**
●	●	1	1	1	UBX / 115.2	NMEA / 19.2	Debug	All	

●: Available/ O: Not Available/ : Default setting

Table 16: Serial I/O configuration with GPSMODE pins

All available USART ports accept input messages in all three supported protocols (NMEA, RTCM, and UBX) at the configured baud rate. Input messages of all three protocols can be arbitrarily mixed. Response to a query input message will always use the same protocol as the query input message.

In Auto mode, no output message is sent out by default, but all input messages are accepted at any supported baud rate. Response to query input commands will be given using the same protocol and baud rate as it was used for the query command. Using the respective configuration commands, periodic output messages can be enabled.

The following message settings are used in the *Table 16* above:

Message Set	Protocol	Message Class	Messages
Low	**NMEA**	Standard	GGA, RMC
	UBX	NAV	SOL, SVINFO
Medium	**NMEA**	Standard	GGA, RMC, GSA, GSV, GLL, VTG, ZDA
	UBX	NAV	SOL, SVINFO, POSECEF, POSLLH, STATUS, DOP, VELECEF, VELNED, TIMEGPS, TIMEUTC, CLOCK
High	**NMEA**	Standard	GGA, RMC, GSA, GSV, GLL, VTG, ZDA, GRS, GST
		Proprietary	PUBX00, PUBX03, PUBX04
	UBX	NAV	SOL, SVINFO, POSECEF, POSLLH, STATUS, DOP,VELECEF, VELNED,TIMEGPS, TIMEUTC, CLOCK
		MON	SCHD, IO, IPC
Debug	**NMEA**	Standard	GGA, RMC, GSA, GSV, GLL, VTG, ZDA, GRS, GST
		Proprietary	PUBX00, PUBX03, PUBX04
	UBX	NAV	SOL, SVINFO, POSECEF, POSLLH, STATUS, DOP,VELECEF, VELNED,TIMEGPS, TIMEUTC, CLOCK
		MON	SCHD, IO, IPC
		RXM	RAW

: Default setting

Table 17: ROM message set

1.10.2.4 USB Power Mode

A4

GPSMODE7 defines the USB power mode of the module.

A "bus powered" device is supplied over the USB bus and is allowed to draw up to 100mA from the USB bus. The power mode is reported to the USB host, as i.e. the device classifies itself as a "Low-power bus-powered function" with no more than one USB power unit load.

To change USB settings use UBX-CFG-USB message.

A "self powered" device has it's own power source.

TIM	LEA	GPSMODE7 [PU]	Description
O	●	0	USB device is bus-powered (max. current limit 100 mA)
O	●	**1**	**USB device is self-powered (Default)**

●: Available/ O: Not Available/ : Default setting

Table 18: USB Power Modes

1.11 Footprint

A4

The GPS signal on earth surface is about 15dB below the thermal noise floor. Signal loss of the antenna or the RF connection should be minimized as much as possible. When defining a layout including a GPS receiver the placement of the antenna vs. the receiver, grounding, shielding and jamming of other digital devices are the most important topics to be considered very carefully.

This section provides important information enabling the design of a reliable and sensitive GPS system.

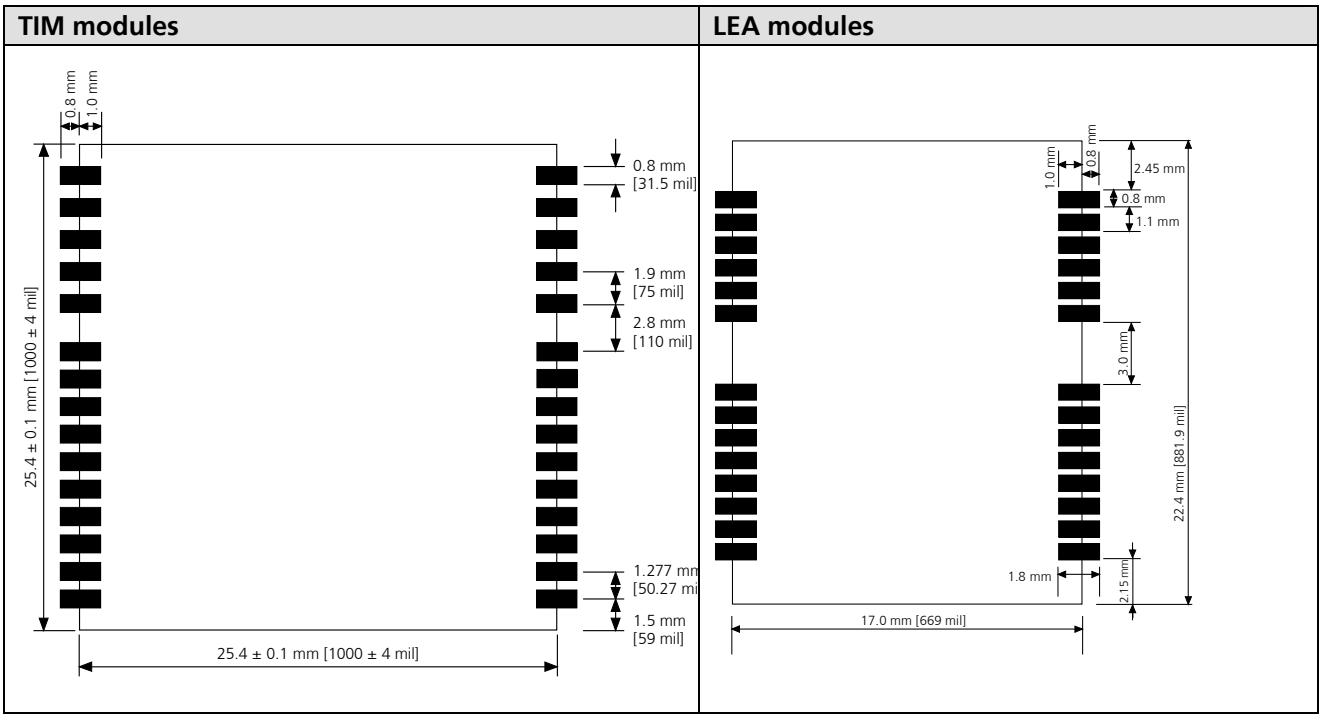


Figure 16: Recommended footprint

1.12 Paste Mask

To improve the quality of the soldering, define length of the paste-mask 0.4mm [16mil] longer than the pad length of the copper mask. The recommended thickness of the paste-mask should be 150µm [6mil]. The Solder mask has the same size as the Cu mask.

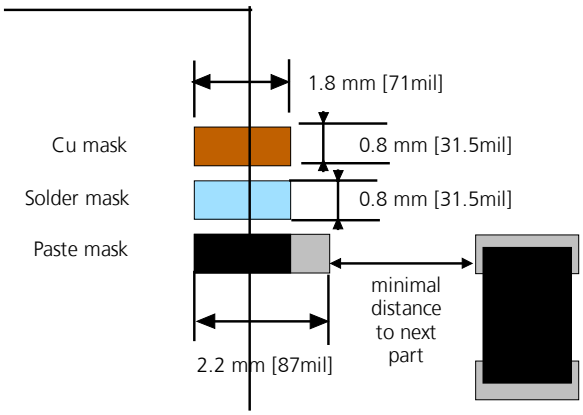


Figure 17: Recommendations for solder and paste mask

☞ **Note** Consider the paste mask outline when defining the minimal distance to the next part.

1.13 Placement

The placement of the ANTARIS®4 GPS Receiver on the PCB is very important to achieve maximum GPS performance. The connection to the antenna must be as short as possible to avoid jamming into the very sensitive RF section.

Make sure that RF critical circuits are clearly separated from any other digital circuits on the system board. To achieve this, position the receiver digital part towards your digital section of the system PCB.

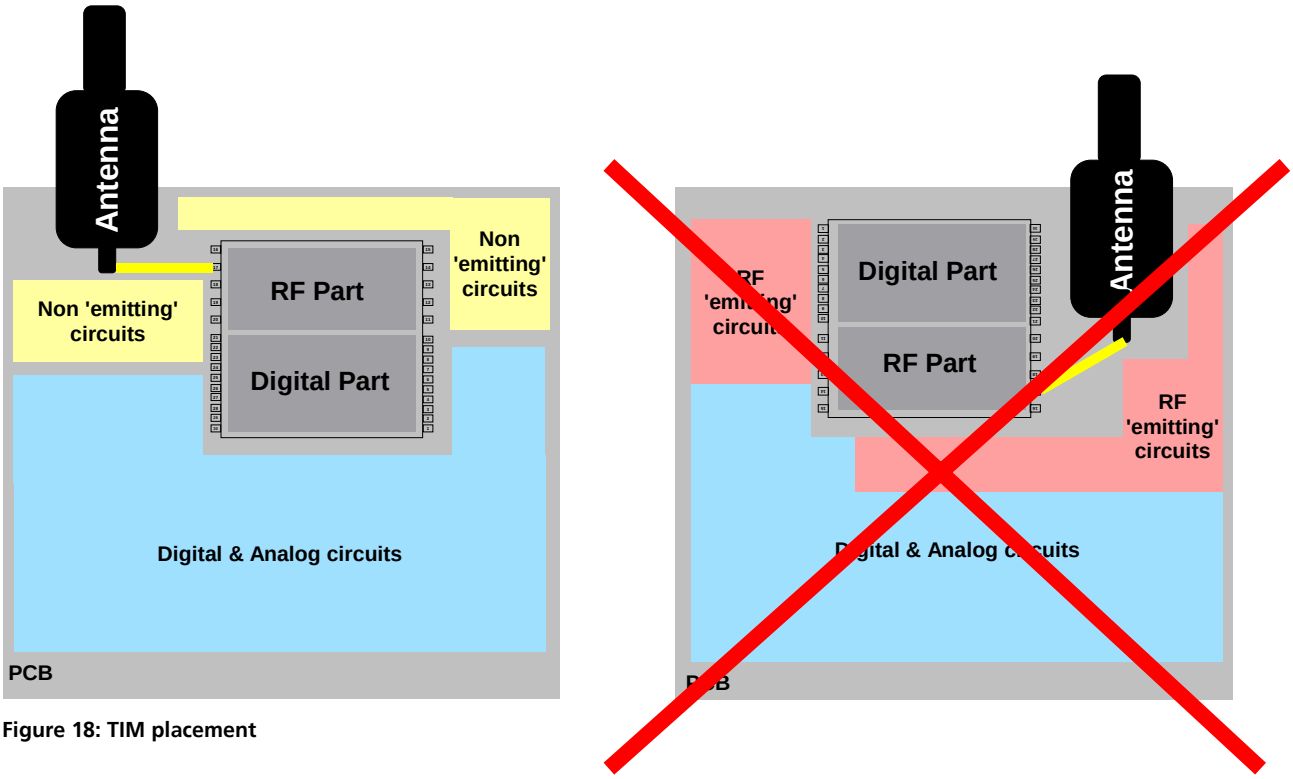


Figure 18: TIM placement

1.14 Layout

1.14.1 Antenna Connection and Grounding Plane Design

ANTARIS®4 can be connected to a passive patch antenna or an active antenna. The antenna RF connection is on the PCB and connects the **RF_IN** pin with the antenna feed point or the signal pin of the connector, respectively. *Figure 19* illustrates connection to a typical five-pin RF connector. One can also see the improved shielding for digital lines. Depending on the actual size of the ground area, additional vias should be placed in the outer region. In particular, the edges of the ground area should be terminated with a dense line of vias.

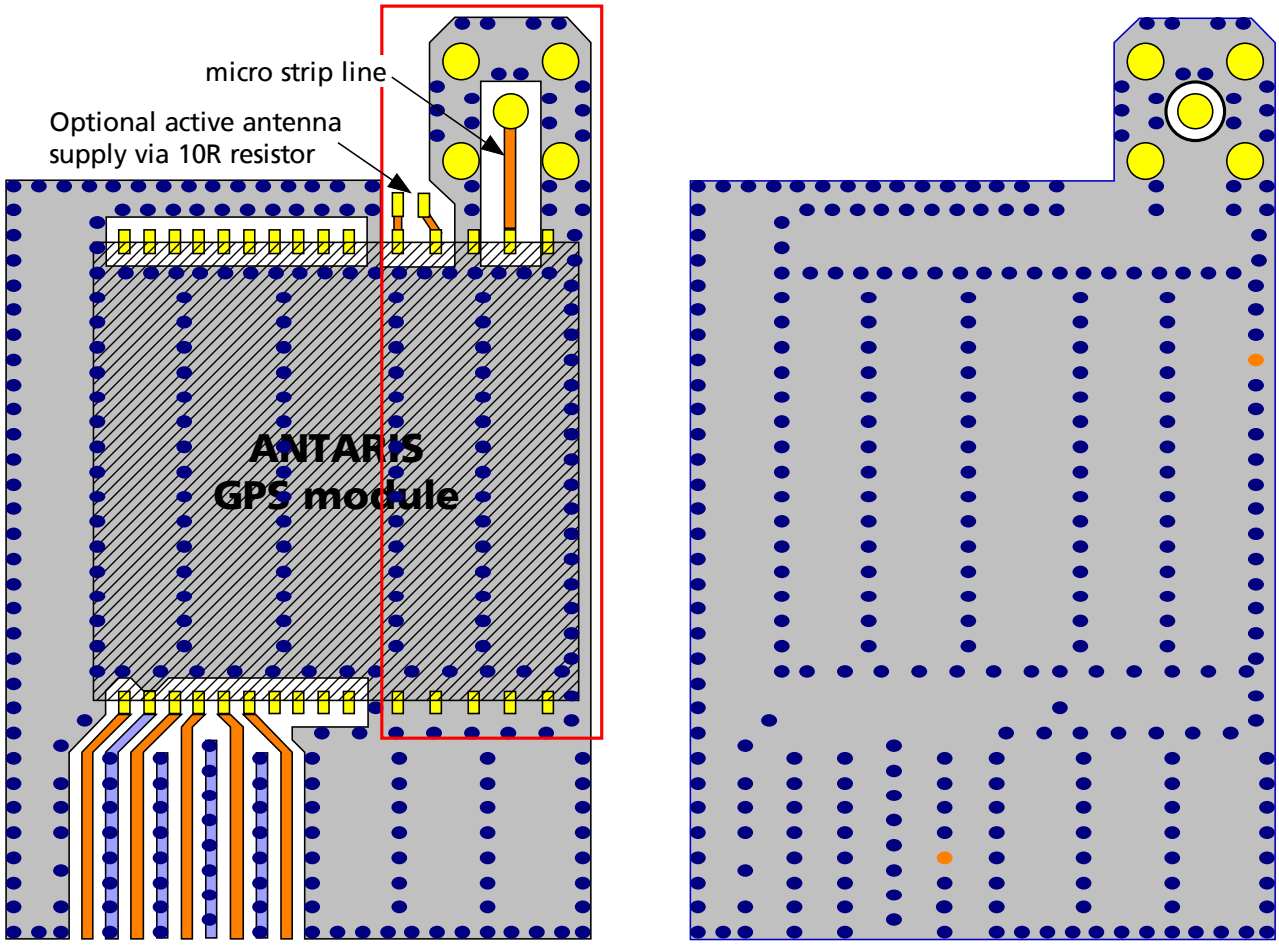


Figure 19: Recommended layout for TIM-xx

As visible in *Figure 19,* an isolated ground area is created around and below the RF connection. This part of the circuit has to be kept as far away from potential noise sources as possible. Make sure that no signal lines cross or vias of signal traces show up at the PCB surface underneath the area surrounded by the red rectangle. Also, the ground plane should be free from digital supply return currents in this area. On a multi layer board, the whole layer stack below the RF connection should be free of digital lines. This is because even a solid ground plane provides only limited isolation.

The impedance of the antenna connection has to match the 50 Ohm impedance of the receiver. To achieve an impedance of 50 Ohms, the width W of the micro strip has to be chosen depending on the dielectric thickness H, the dielectric constant ε_r of the dielectric material of the PCB and on the built-up of the PCB. *Figure 20* shows two different builds: A 2 Layer PCB and a 4 Layer PCB. The reference ground plane is in both designs on layer 2 (red). Therefore the effective thickness of the dielectric is different.

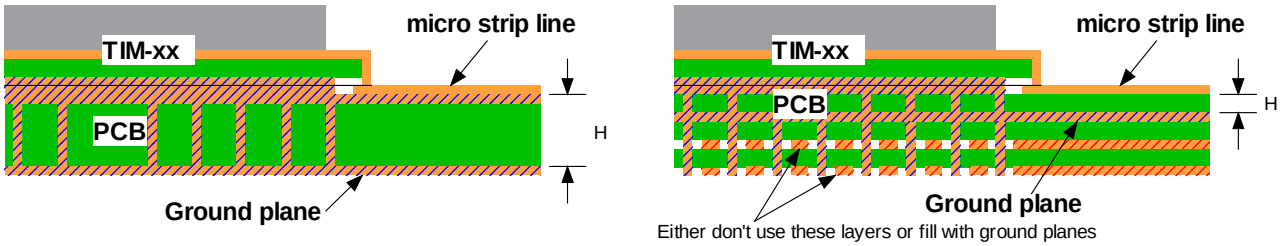
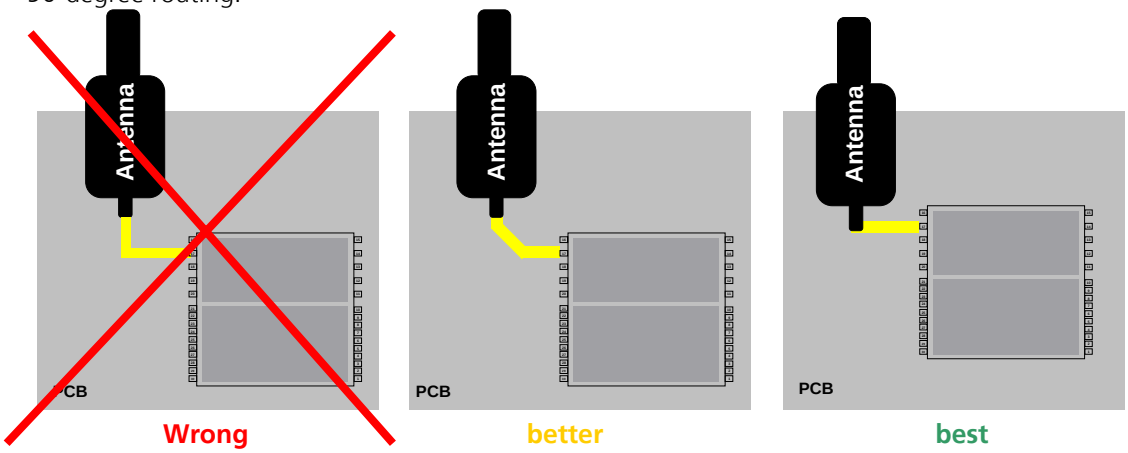


Figure 20: PCB build-up for Micro strip line. Left: 2-layer PCB, right: 4-layer PCB

General design recommendations:

- The length of the micro strip line should be kept as short as possible. Lengths over 2.5 cm (1 inch) should be avoided on standard PCB material and without additional shielding.
- Distance between micro strip line and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF connection close to digital sections of the design should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.



- Routing of the RF-connection underneath the receiver should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small (some 100 µm) and has huge tolerances (up to 100%). Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.
- In order to avoid reliability hazards, the area on the PCB under the receiver should be entirely covered with solder mask. Vias should not be open.

1.14.2 Antenna Micro Strip

There are many ways to design wave-guides on printed circuit boards. Common to all is that calculation of the electrical parameters is not straightforward. Freeware tools like AppCAD from Agilent or TXLine from Applied Wave Research, Inc. are of great help. They can be downloaded from *www.agilent.com* and *www.mwoffice.com*.

The micro strip is the most common configuration for printed circuit boards. The basic configuration is shown in *Figure 21* and *Figure 22*. As a rule of thumb, for a FR-4 material the width of the conductor is roughly double the thickness of the dielectric to achieve 50 Ohms line impedance.

For the correct calculation of the micro strip impedance, one does not only need to consider the distance between the top and the first inner layer but also the distance between the micro strip and the adjacent GND plane on the same layer

☞ **Note:** Use the Coplanar Waveguide model for the calculation of the micro strip.

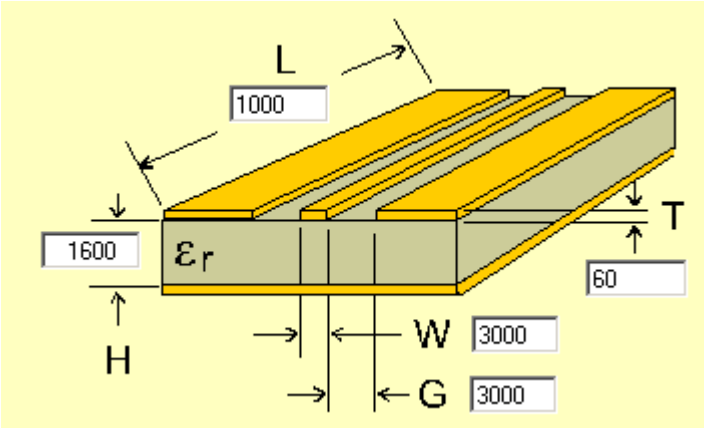


Figure 21: Micro strip on a 2-layer board (Agilent AppCAD Coplanar Waveguide)

Figure 21 shows an example of a 2-layer FR4 board of 1.6 mm thickness and a 35mm (1 once) copper cladding. The thickness of the micro strip is comprised of the cladding (35µm) plus the plated copper (typically 25µm). *Figure 22* depicts an example of a multi layer FR4 board with 18µm (½ once) cladding and 180µ dielectric between layer 1 and 2.

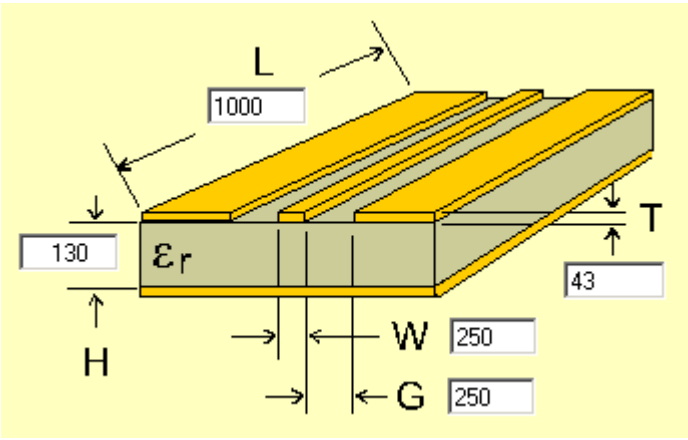


Figure 22: Micro strip on a multi layer board (Agilent AppCAD Coplanar Waveguide)

2 Product Handling

☞ **Note** As all ANTARIS®4 products are **LEAD FREE**, the product handling and soldering pocess has changed compared to ANTARIS® products.

2.1 Packaging

The ANTARIS®4 GPS Modules are delivered as hermetically sealed reeled tapes in order to enable efficient production, production lot set-up and tear-down.

Figure 23: Reeled ANTARIS® GPS Receiver modules

2.1.1 Reels

The ANTARIS®4 GPS Modules are available in two reel sizes. A 100pcs reel and a 500pcs reel. The dimensions of the two reels are shown in *Figure 24* and *Figure 25*.

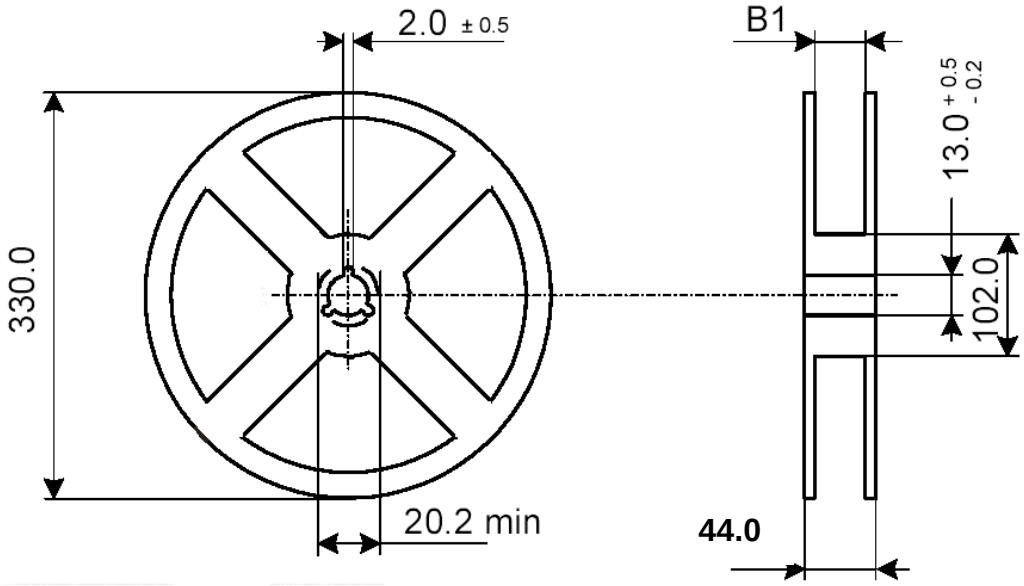


Figure 24: Dimensions of reel for 500 pieces

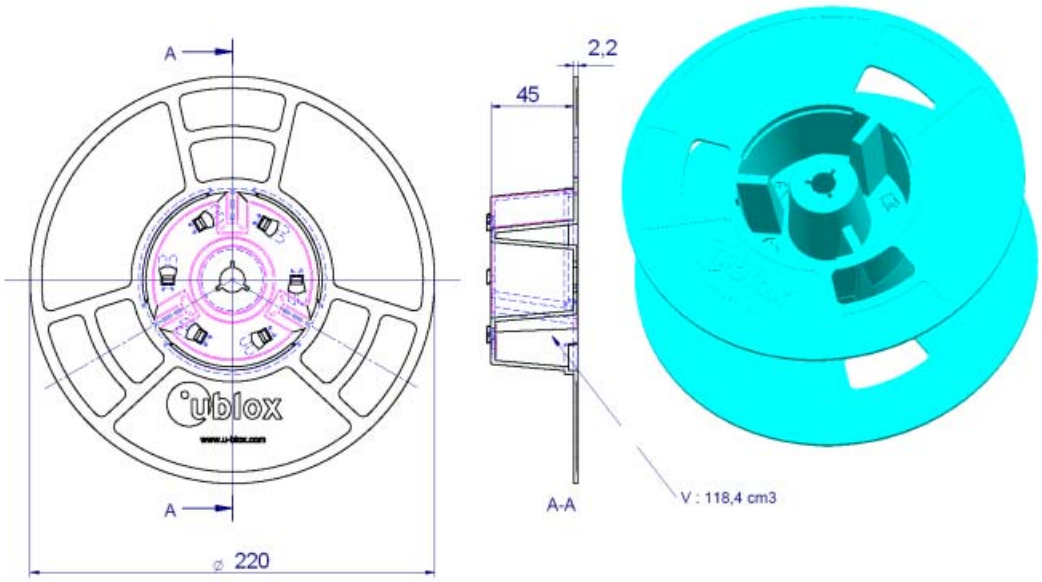


Figure 25: Dimension of reel for 100 pieces

2.1.2 Tapes

The tape of TIM GPS receivers is specified in *Figure 26*, the one for LEA GPS receivers in *Figure 27*. Units are in mm.

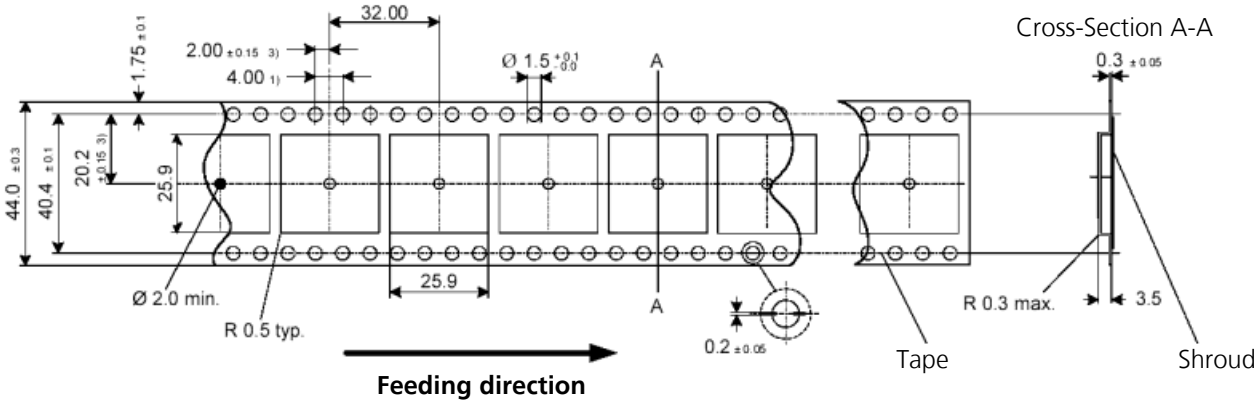


Figure 26: Dimensions of tape used for TIM GPS Receivers

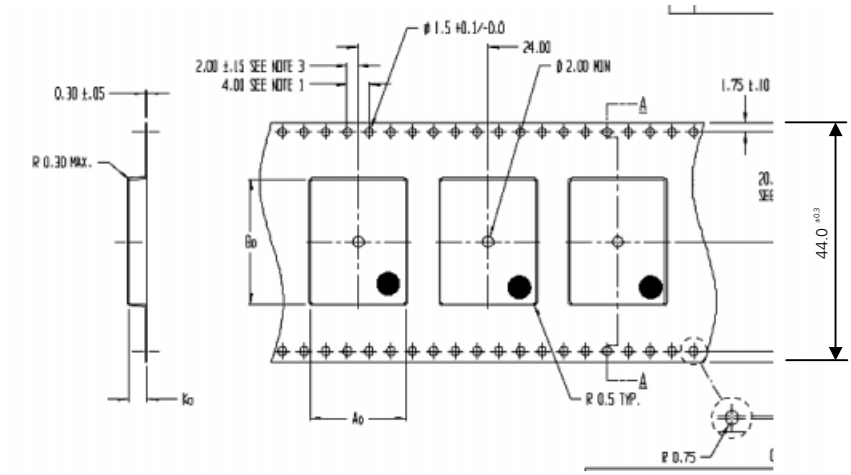


Figure 27: Dimensions of tape used for LEA GPS Receivers

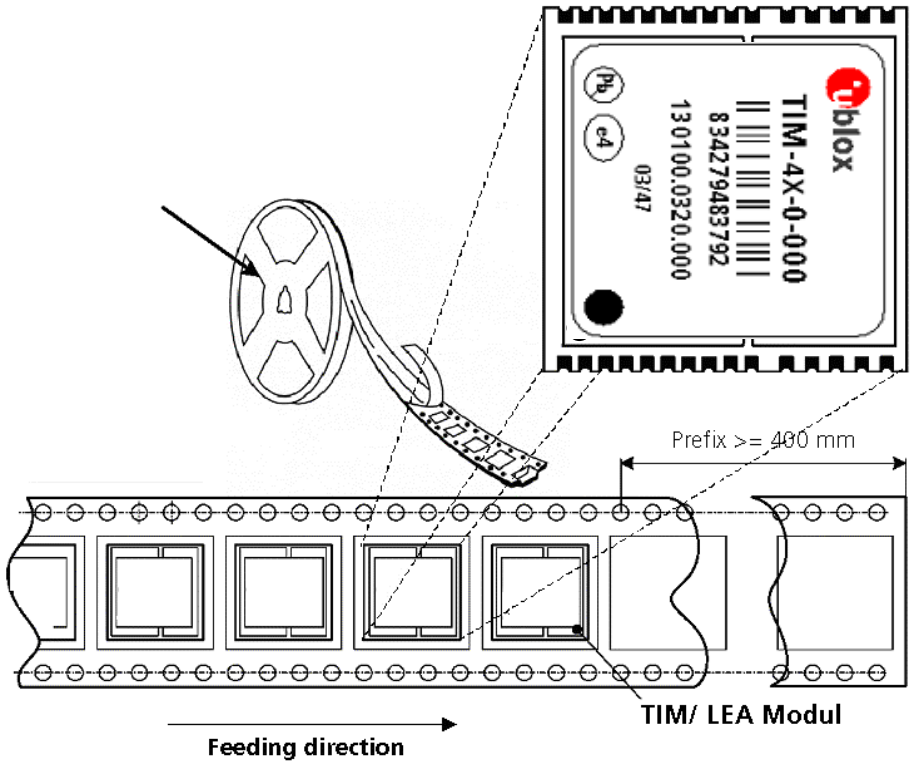


Figure 28: Reel - orientation of the ANTARIS® GPS Modules in relation to feed direction

2.2 Shipment, Storage and Handling

A4

2.2.1 Handling

The ANTARIS®4 GPS Module is designed and packaged to be processed in an automatic assembly line. The module is shipped in Tape-and-Reel.

! **Warning** The component contains highly sensitive electronic circuitry. Handling the ANTARIS®4 GPS Receiver without proper ESD protection may destroy or damage the GPS modules permanently.

! **Warning** According to JEDEC ISP, the ANTARIS®4 GPS Modules are moisture sensitive devices. Appropriate handling instructions and precautions are summarized in Sections *2.2.2* to *2.2.5*. Read them carefully to prevent permanent damages due to moisture intake.

2.2.2 Shipment

A4

The ANTARIS®4 GPS Modules are delivered on Tape-and-Reels in a hermetically sealed package ("dry bag") to prevent moisture intake and protection against electrostatic discharge. To prevent physical damages, the reels are individually packed in carton boxes.

The dry bag provides a JEDEC compliant MSD label (Moisture Sensitive Devices) describing the handling requirements to prevent humidity intake.

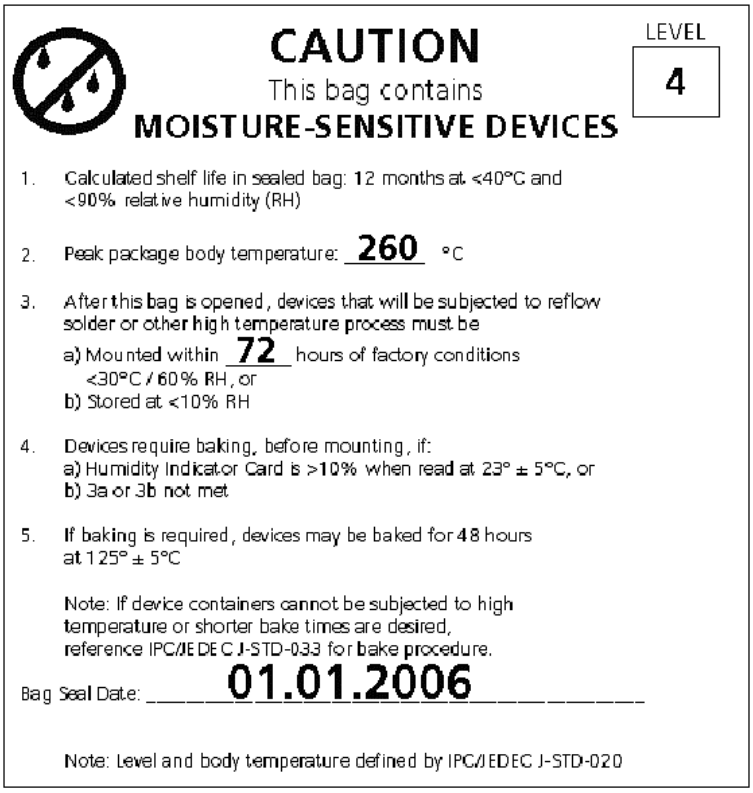


Figure 29: Applicable MSD Label (See *Section 3.1* for baking instructions)

2.2.3 Storage

Shelf life in sealed bag is 12 months at <40°C and <90% relative humidity.

2.2.4 Handling

A humidity indicator card and a desiccant bag to absorb humidity are enclosed in the sealed package. The parts are shipped on tape-and-reel in a hermetically sealed package. If no humidity has been drawn, the three fields in the humidity indicator card indicate blue color.

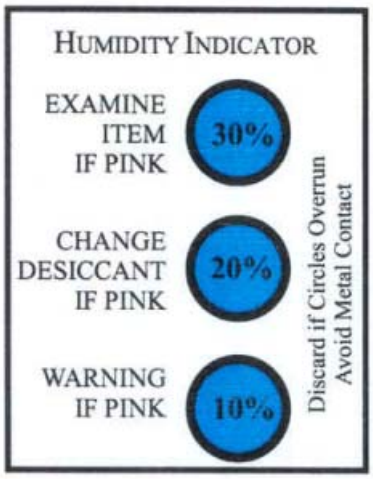


Figure 30: Humidity Indicator Card, good condition

2.2.5 Floor Life

For products with moisture sensitivity level 4, the floor life is 72 hours, or precisely three days. Under factory floor temperature and humidity conditions (<30°C, <60% relative humidity), the parts must be processed and soldered within this specified period of time.

Once the sealed package of the reel is opened and the parts exposed to humidity, they need to be processed within 72 hours (precisely three days) in a reflow soldering process. If this time is exceeded, or the sticker in the sealed package indicates that the goods have been exposed to moisture, the devices need to be pre-baked before used in the flow solder process. Please refer to *Section 2.3* for instructions on how to pre-bake the components.

2.3 Processing

A4

2.3.1 Moisture Preconditioning

Both encapsulant and substrate materials absorb moisture. JEDEC specification J-STD-020 must be observed to prevent cracking and delamination associated with the "popcorn" effect during solder reflow. The popcorn effect can be described as miniature explosions of evaporating moisture. Baking before processing is required in following cases:

- Humidity indicator card: At least one circular indicator is no longer blue
- Floor life or environmental requirements after opening the seal is opened has been exceeded, e.g. exposure to excessive seasonal humidity.

Recommended baking procedure:

Duration:	48 hours
Temperature:	125°C
Humidity:	Below 5%. Desiccant must be placed into the oven to keep humidity low.
Oven:	Convection flow oven. Also put desiccant pack into the oven for dehydration.
After work:	Put the baked components with desiccant and moisture indicator into a humidity proof bag and use a vacuum hot barrier sealing machine for sealing if not processed within specified floor time. Storage in a nitrogen cabinet or dry box is also a possible approach to prevent moisture intake.

! **Warning** Do not attempt to bake the ANTARIS®4 GPS Modules contained in tape and rolled up in reels. If you need to bake the ANTARIS®4 GPS Modules quickly at 125°C for 48 hours, remove them from the belt and place them individually onto the oven tray.

☞ **Note** A repeated baking process will reduce the wetting effectiveness of the pad contacts. This applies to all SMT devices.

2.3.2 Soldering Paste

A4

Use of "No Clean" soldering paste is strongly recommended, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering Paste:	LFSOLDER TLF-206-93F (Tamura Kaken (UK) Ltd.)
Alloy specification:	Sn 95.5/ Ag 3.9/ Cu 0.6 (95.5% Zinc/ 0.6 % Silver/ 0.6% Copper)
Melting Temperature:	216 - 221°C
Stencil Thickness:	150 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in *Figure 31*.

☞ **Note** The quality of the solder joints on the connectors ('half vias') should meet the appropriate IPC specification.

2.3.3 Reflow Soldering

A4

A convection type-soldering oven is strongly recommended over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Consider the "IPC-7530 Guidelines for temperature profiling for mass soldering (reflow and wave) processes, published 2001".

Preheat Phase

Initial heating of component leads and balls. Residual humidity will be dried out. Please note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: 1 - 4°C/s — If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.
- Time: 60 – 120 seconds — If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End Temperature: 150 - 200°C — If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ Reflow Phase

The temperature rises above the liquidus temperature of 216 - 221°C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above 220°C liquidus temperature: 20 - 40s
- Peak reflow temperature: 230 - 250°C

Cooling Phase

A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 3°C / s

☞ **Note** To avoid falling off, the ANTARIS®4 GPS Module shall be placed on the topside of the motherboard during soldering.

The final soldering temperature chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc. Exceeding the maximum soldering temperature in the recommended soldering profile may permanently damage the module.

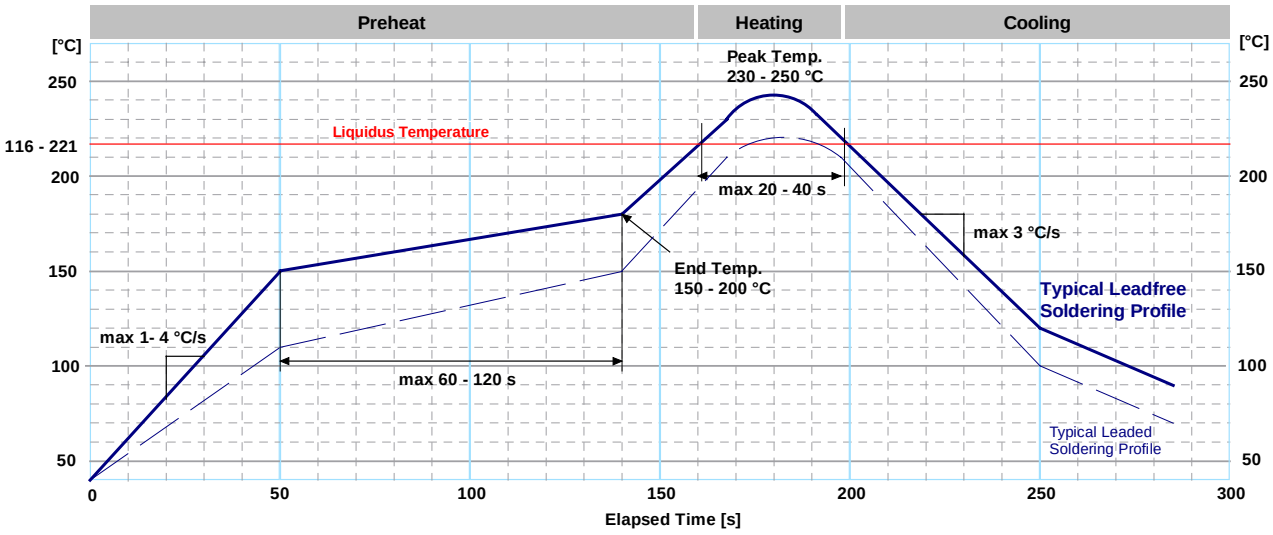


Figure 31: Recommended soldering profile

2.3.4 Optical Inspection

After soldering the ANTARIS®4 GPS Module, consider an optical inspection step to check whether:

- ANTARIS®4 GPS Module is properly aligned and centered over the pads
- All pads are properly soldered
- No excess solder has created contacts to neighboring pads, or possibly to pad stacks and vias nearby.

2.3.5 Cleaning

In general, cleaning the populated modules is strongly discouraged. Residuals, which are underneath the ANTARIS®4 GPS Modules, cannot be removed easily with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the ANTARIS®4 GPS Module. The combination of residuals of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or a similar organic solvent will likely flood soldering flux residuals into the two housings, which is a place not accessible for post-washing inspection. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will damage an ANTARIS® GPS Receiver permanently, in particular the quartz oscillators.

The best approach is to consider using a "no clean" soldering paste and eliminate the cleaning step past the soldering.

2.3.6 Repeated Reflow Soldering

Only a single reflow soldering process is encouraged for boards with an ANTARIS®4 GPS Module populated on it. Reason: Risk of falling off due to high weight in relation to the adhesive properties of the solder.

2.3.7 Wave Soldering

Base boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require a wave soldering to solder the THT components. Only a single wave soldering process is encouraged for boards with an ANTARIS®4 GPS Module populated on it.

2.3.8 Hand Soldering

Hand soldering is allowed. Use a Soldering iron temperature setting "7" which is equivalent to 350°C and carry out the hand soldering according to the IPC recommendations / reference documents IPC7711.

Place the ANTARIS®4 GPS Module precisely on the pads. Start with a cross-diagonal fixture soldering (e.g. pins 1 and 16), and then continue from left to right.

2.3.9 Rework

The ANTARIS®4 GPS Module can be unsoldered from the baseboard. Use desoldering braid made of copper. Avoid overheating the ANTARIS® GPS Modules.

A vacuum solder sucker is not recommended as solder residuals may remain in the gap below the module.

After all solder has been removed from all pads, lift the component carefully. Continue unsoldering carefully if the ANTARIS®4 GPS Module does still stick. After the module is removed, clean the pads before placing and hand-soldering a new module.

! **Warning** Never attempt a rework on the module itself, e.g. replacing individual components. Such actions will terminate warranty coverage immediately.

2.3.10 Conformal Coating

Conformal coating with Humiseal or a similar coating product may be necessary in dedicated applications. Please note that the metal covers and the sticker prevent optimum inflow of such liquids or aerosols.

☞ **Note** Conformal Coating will void the warranty.

2.3.11 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the ANTARIS®4 GPS Module before implementing this in the production.

☞ **Note** Casting will void the warranty.

2.3.12 Grounding Metal Covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done on customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interferences and noise.

☞ **Note** u-blox takes no warranty for damages on the ANTARIS®4 GPS Module caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

2.3.13 Use of any Ultrasonic Processes

Some components on the ANTARIS®4 GPS Module are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding etc.) may cause damage to the GPS Receiver.

☞ **Note** u-blox takes no warranty for damages on the ANTARIS®4 GPS Module caused of any Ultrasonic Processes.

3 Product Testing

3.1 u-blox In-Series Production Test

A4

u-blox focuses on a high quality of its products. To achieve a high standard it's our philosophy to supply fully tested units. Therefore at the end of the production process, every unit will be tested. Defective units will be analyzed in detail to improve the production quality.

This is achieved with automatic test equipment, which delivers a detailed test report for each unit. The following measurements are done:

- Digital self-test (Software Download, verification of FLASH firmware, etc.)
- Measurement of voltages and currents
- Measurement of RF characteristics (e.g. C/No)

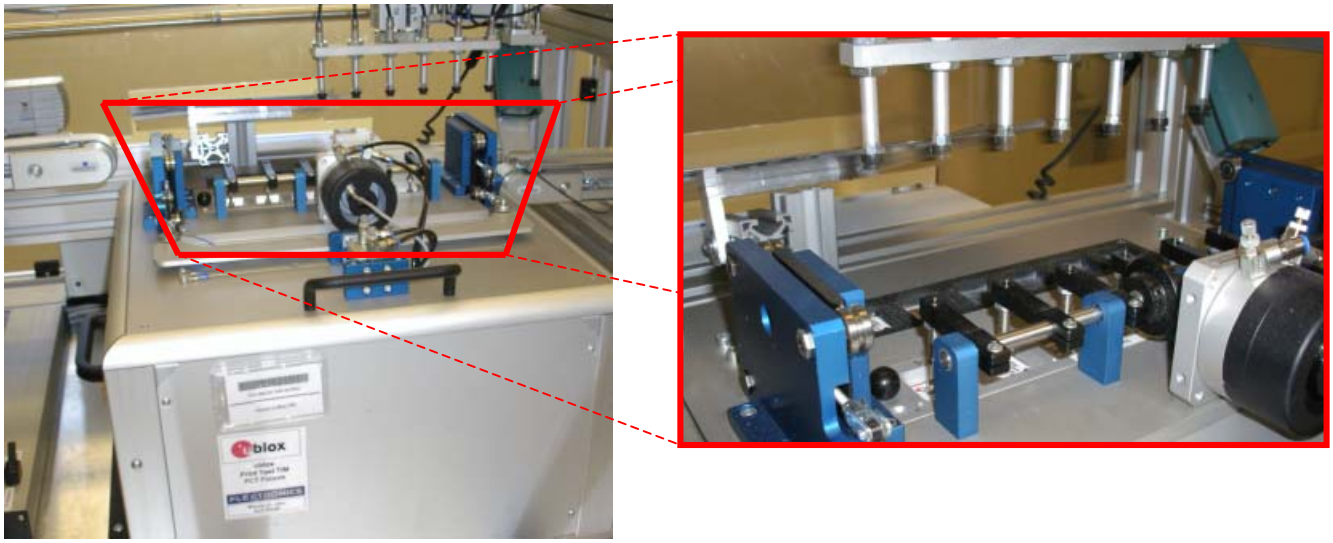


Figure 32: Automatic Test Equipment for Module Tests

3.2 Test Parameters for OEM Manufacturer

Based on the test done by u-blox (with 100% coverage), it is obvious that an OEM manufacturer doesn't need to repeat firmware tests or measurements of the GPS parameters/characteristics (e.g. TTFF) in his production test.

An OEM Manufacturer should focus on

- Overall sensitivity of the device (including antenna, if applicable)
- Communication to a host controller

3.3 System Sensitivity Test

The best approach to test the sensitivity of a GPS device is the use of a 1-channel GPS simulator. It assures reliable and constant signals at every measurement.

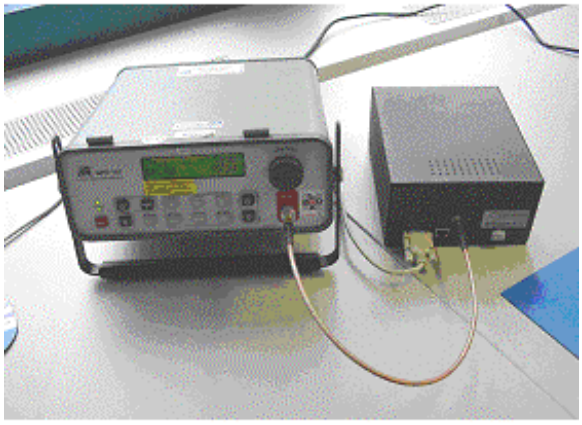


Figure 33: 1-channel GPS simulator

Here's a list of companies producing Single-Channel GPS Simulators:

- Spirent Communications Positioning Technology (previously GSS Global Simulation Systems) www.positioningtechnology.co.uk
- Welnavigate www.welnav.com
- JcAIR Test Systems www.jcair.com
- Aeroflex (previously IFR) www.aeroflex.com
- Rohde&Schwarz www.rohde-schwarz.com

3.3.1 Guidelines for Sensitivity Tests

1. Connect a 1-channel GPS simulator to the OEM product
2. Choose the power level in a way that the "Golden Device" would report a C/No ratio of 45 dBHz
3. Power up the DUT (Device Under Test) and allow enough time for the acquisition
4. Read the C/No value from the NMEA GSV or the UBX-NAV-SVINFO message (e.g. with u-center AE)
5. Reduce the power level by 10dB and read the C/No value again
6. Compare the results to a "Golden Device" or an ANTARIS® GPS EvalKit.

3.3.2 'Go/No go' tests for integrated devices

The best test is to bring the device to an outdoor position **with excellent visibility** (HDOP < 3.0). Let the receiver acquire satellites and compare the signal strength with a "Golden Device".

☞ **Note** As the electro-magnetic field of a redistribution antenna is not homogenous, indoor tests are in most cases not reliable. This kind of tests may be useful as a 'go/no go' test but not for sensitivity measurements.