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Design and Implementation of a DSP Based Digital Controller for a DC-DC Converter

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***Abstract*—The design and Digital Signal Processor (DSP) based implementation of a digital controller are presented for the dc-dc converter. Starting with a dc-dc buck converter and a given set of performance specifications, a digital PID controller is implemented in TMS320F2812 DSP. All the necessary DSP hardware or software techniques and algorithms required to implement the controller are discussed in detail. The steady state and dynamic response performance of the controller is presented in order to demonstrate the effectiveness of the design.**

Keywords-digital control, digital signal processor (DSP), DC-DC converter

I. INTRODUCTION

Digital signal processing (DSP) has been widely used in telecommunications, intelligent control, and motion control etc. Because of its high speed computation ability, high reliability, and cost reduction, digital control of dc-dc converter using DSP is becoming more and more common in industry today.

Modern 32-bit DSP controllers with processor speed up to 150MHz and enhanced peripherals such as, 12-bit A/D converter with conversion speed up to 80nSec, 32x32-bit MAC (multiplication and accumulation), 32-bit timers and real-time code debugging capability gives the power supply designers all the benefits of digital control and allows implementation of high bandwidth, high frequency power supplies without sacrificing performance [1-4]. Furthermore, these devices incorporate a high-precision ultra-fast ADC together with many control and communication peripherals for truly single-chip designs. Due to its architecture, which is specially optimized for C/C++, these devices offer good code efficiency, and give designers the ability to develop their sophisticated nonlinear control algorithms entirely in high-level languages.

This paper, therefore explains a step-by-step DSP based digital control design and implementation of a dc-dc converter. Starting with a dc-dc buck converter and a given set of performance specification, it discusses all the necessary DSP hardware or software techniques and algorithms required to implement the controller. These are first shown in MATLAB® and then verified by the experimental results.

II. DIGITAL CONTROL OF DC-DC CONVERTER

Fig. 1 shows a basic block diagram of a digitally controlled dc-dc converter with the use of TMS320F2812 DSP. As shown in Fig. 1, a single signal measurement is needed to implement the voltage mode control of the dc-dc converter. The output voltage v_o is measured, using a "sensor" with gain H and then input to the DSP via the ADC channel. The digitized sensed output voltage $Hv_o[k]$ is compared to the reference v_{ref}. The voltage loop controller $G_c(z)$ is designed to make the output voltage v_o follow the reference v_{ref} regardless of disturbances or component variations in the compensator, pulse-width modulator, gate driver, or converter power stage.

The digitized output $u[k]$of this controller provides the duty ratio command for the buck converter switch Q1. This command output is used to calculate the appropriate values for the timer compare registers in the on-chip PWM module. The PWM module uses this value to generate the PWM output and finally drives the buck converter switch Q1.

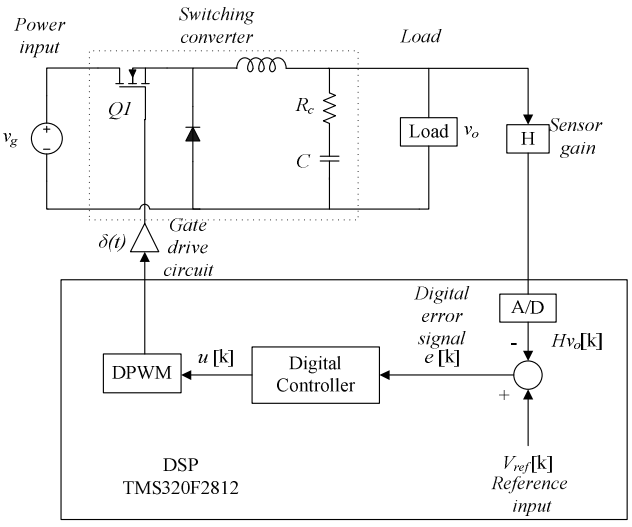

Figure 1. DSP based digital control of dc-dc converter.

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III. DIGITAL PID CONTROLLER DESIGN

A PID controller is designed for the buck converter shown in Fig. 1. The design began with the well-known small-signal model for this converter [5]:

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{v_g}{LC}\left[\frac{1 + sR_C C}{s^2 + \left(\frac{1}{RC} + \frac{R_C}{L}\right) + \frac{1}{LC}}\right] \quad (1)$$

The input voltage of the prototype buck converter is 24 V, and the output voltage v_o is 12 V. The load resistance R is $12\,\Omega$, L is $2.12mH$ and C is $220\mu F$. The parasitic elements, R_C is estimated to be $30m\Omega$. The switching frequency is 20 kHz. Fig. 2 is a Bode plot for the small signal model of (1) at the buck converter's nominal operating point. This plot was verified using MATLAB®.

Based on the Bode plot shown in Fig. 2, it indicates that this system has a very small phase margin. A compensator must be designed to ensure that the gain at low frequencies is high enough to minimize the steady-state error and that the crossover frequency should be as high as possible but about an order of magnitude below the switching frequency to allow the power supply to respond to transients quickly. The phase margin of the compensated system should be in the range of 45° to 70° to meet the transient response requirements [6].

The compensator in this study is a PID controller which is described by the following transfer function:

$$G_C(s) = K_p + \frac{K_i}{s} + K_d(s) \quad (2)$$

This controller has one pole at the origin and two zeros. The analog PID controller, $G_C(s)$ in Equation (2) is designed in MATLAB® using the available control design toolbox called "Siso tool". The corresponding controller $G_C(s)$ can be easily imported from the MATLAB® control design toolbox. This is found as:

$$G_C(s) = 0.0169 + \frac{2016.6}{s} + 1.0224 \times 10^{-3}s \quad (3)$$

The compensated loop gain is shown in Fig. 3. It can be seen that the phase of $T_c(s)$ is approximately equal to 69.7° at 1.16 kHz. Hence, the variation in component values, which causes the crossover frequency to deviate somewhat from 1 kHz, should have a little impact on the phase margin. In addition, it can be seen from Fig. 3 that the loop gain has a dc magnitude of 60dB.

The PID controller designed in the continuous time domain is then converted to the discrete time domain. The most straightforward technique uses a trapezoidal sum approximation for the integral term, and a backwards-difference approximation for the derivative term. The proportional term is directly used without approximation [7]. The PID algorithm can be expressed in the discrete-time domain as:

$$u(k) = K_p e(k) + K_i \frac{h}{2}\sum_{i=0}^{k}[e(i) + e(i-1)] + \frac{K_d}{h}[e(k) - e(k-1)] \quad (4)$$

where
K_p is the proportional mode control gain
K_i is the integral mode control gain
K_d is the derivative mode control gain
h is the sampling period
k is the discrete-time index: k = 0, 1,...

In this equation, $u(k)$ is the new duty cycle calculated from the K^{th}sample, and $e(k)$ is the error of the K^{th} sample. The error $e(k)$ is calculated as $e(k) = Ref - ADC(k)$, where $ADC(k)$ is the converted digital value of the K^{th} sample, and Ref is the digital value corresponding to the desired output voltage. The second term in the equation is the sum of the errors and $e(k) - e(k-1)$ is the difference between the error of the K^{th} sample and the error of the $(k-1)^{th}$ sample.

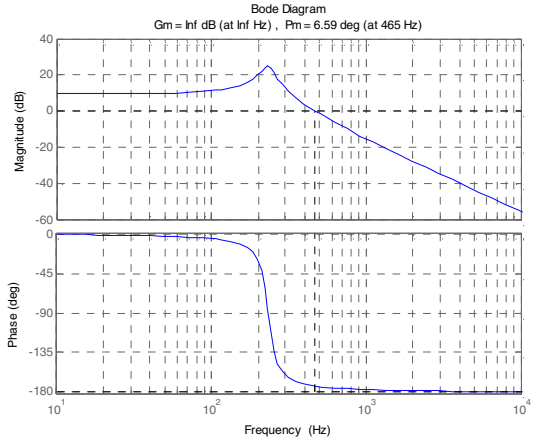

Figure 2. Bode plot of the buck converter small signal model.

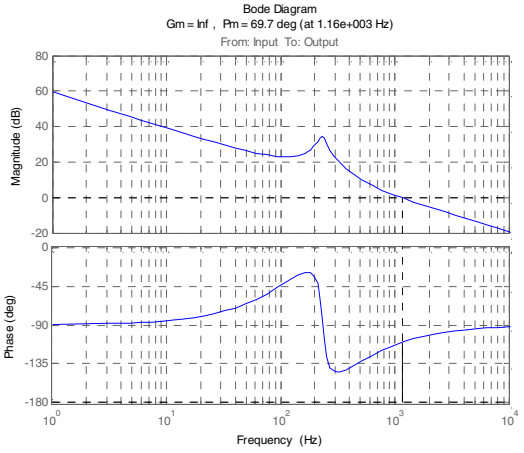

Figure 3. Bode diagram of compensated loop gain, $T_{c,PID}$.

IV. DIGITAL SAMPLING LOOP IMPLEMENTATION

The sampling scheme affects the digital controller design and, therefore, needs proper attention. The ADC of TMS320F2812 could be triggered by the EVA/B (period, compare, or underflow), the external pins, or software [5]. In the prototype work, the ADC is triggered by the T2CMPR (GP Timer 2 compare) of EVA. This enables the shifting of the ADC trigger point anywhere within the PWM period (as opposed to using the Timer 2 period to trigger the ADC, which would fix the ADC trigger at the end of the Timer 2 period and coincide with the instant when the PWM was switching off). Fig. 4 depicts this situation.

The SOC (start of conversion) is started by the T2CMPR (GP Timer 2 compare), and once the conversion completes, the EOC (end of conversion) interrupt is triggered. Then, the ADC interrupt routine is called in the program. Inside the interrupt service routine (ISR), the user software reads the converted value from the ADC result register, implements the designed controller of Equation (4) and then writes the new PWM duty ratio value to the appropriate PWM compare register. Finally, the PWM modulated value is calculated in terms of the new duty cycle, and then the registers are updated before the next trigger of the ADC conversion. Shown in Fig. 5 is the flowchart of the interrupt service routine to implement the control algorithm using a Texas Instruments TMS320F2812 digital signal processor (DSP) evaluation module.

The frequency of the PWM output is set up by configuring one of the on-chip Timers. GP Timer 1 (T1) is used to clock the PWM output at the desired switching frequency, which is 20 kHz in this work. These timers have associated compare registers which are used to write the calculated duty ratio values. These values then get compared with the timer counter value in order to generate the PWM output. The time at which a newly written compare value affects the actual PWM output duty ratio is controlled by associated PWM control registers. In this work, the PWM control registers are set up such that a new value written in the compare register, changes the actual PWM output duty ratio at the start of the subsequent timer (T1) period.

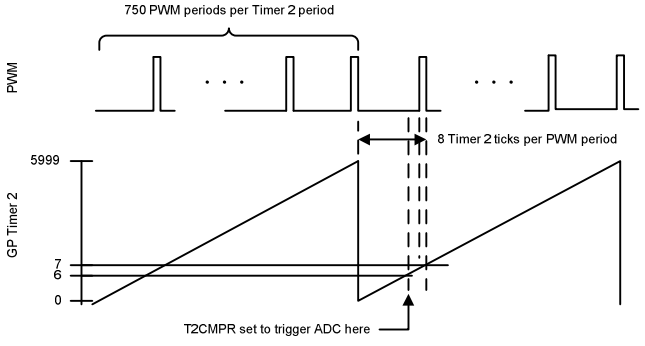

Figure 4. Time Relationship between PWM Period and ADC Triggering

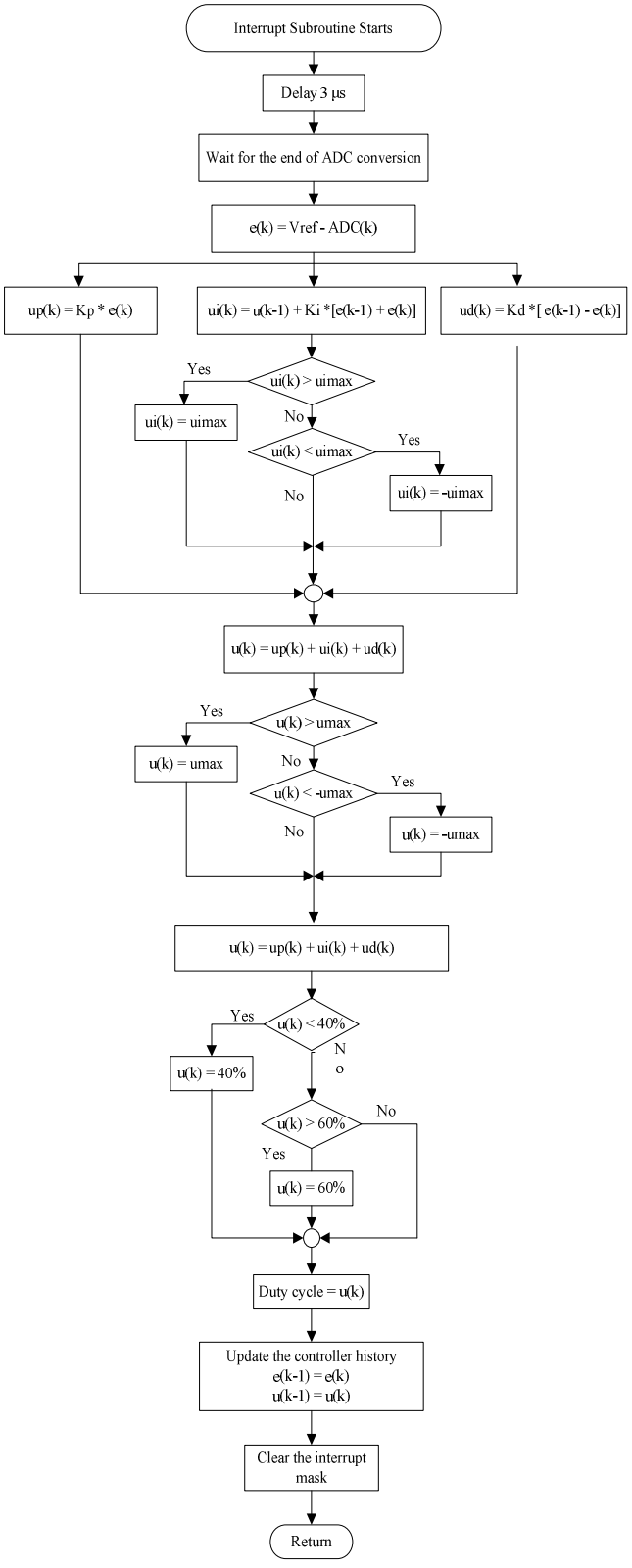

Figure 5. Interrupt service routine implementing PID control algorithm.

V. SIMULATION RESULTS

A MATLAB/SIMULINK® simulation diagram is shown in Fig. 7. The converter model includes parasitic elements and the parameters are measured values, which are listed in Table I. Simulated output voltage and duty cycle are plotted in Fig. 8.

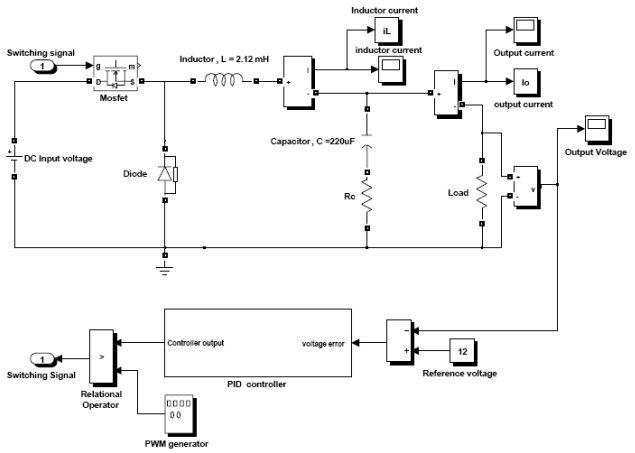

Figure 6. Simulation diagram in MATLAB/SIMULINK.

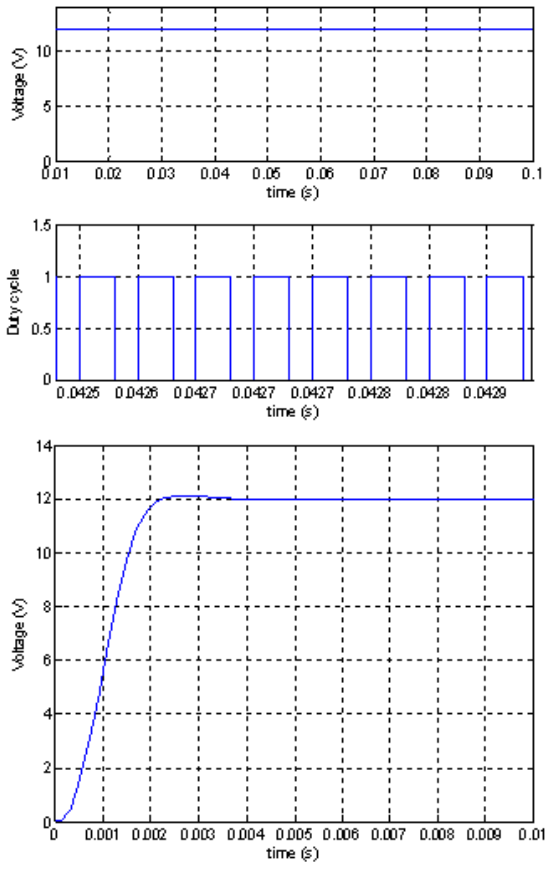

Figure 7. Simulated (top) steady state output voltage, (middle) duty cycle, and (bottom) output voltage during start up transient

VI. EXPERIMENTAL RESULTS

The digital PID controller has been tested experimentally. The parameters of the experimental buck converter and controller are listed in Table I. During experimental testing, several parameters were varied to analyse the controller performance. Measurements were recorded using a Tektronix TDS220 oscilloscope.

Table II lists the converter output voltage for various input voltages ranging from 20 to 30 V. The percentage of deviation of the output voltage from the reference voltage (V_{ref} = 12 V) is shown at the right hand column. The steady state response and PWM signal are shown in Fig. 8. Experiments confirm that changes on the input supply of the converter have very little effect on the steady-state response of the converter.

The behaviour of the model during the start up transient is analysed in order to evaluate the transient response of the converter. The start up transient response of the buck converter is shown in Fig. 9. The settling time is about 5 ms with very slight overshoot.

TABLE I. PARAMETERS OF THE EXPERIMENTAL SYSTEM

Parameter name	**Symbol**	**Nominal Value / Spec. no**
Input voltage	V_{g-H}	30V
	V_{g-L}	20V
Output voltage	V_o	12V
Output Capacitor	C	220µF
Inductor	L	2.12mH
Load resistance	R_L	18 Ω
Capacitor ESR	R_C	30 $m\Omega$
Switching frequency	f_s	20kHz
Power MOSFET	M	IRF 530
Power diode	D	MUR 820

TABLE II. OUTPUT VOLTAGE VARIATION USING DIGITAL PID CONTROLLER

Input Voltage, (V)	Output Voltage, (V)	Deviation (V)	Deviation (%)
20	11.997	-0.003	0.025
24	11.999	-0.001	0.008
30	12.002	+0.002	0.017

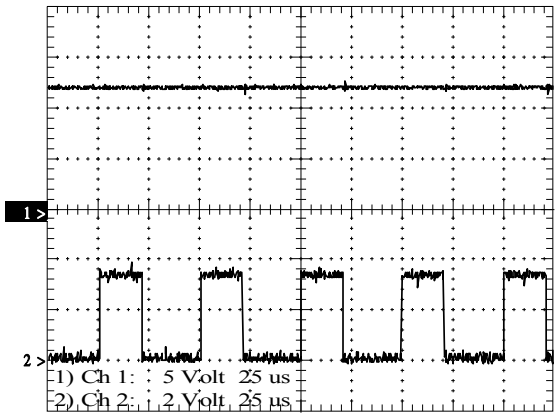

Figure 8. Steady state response of the buck converter

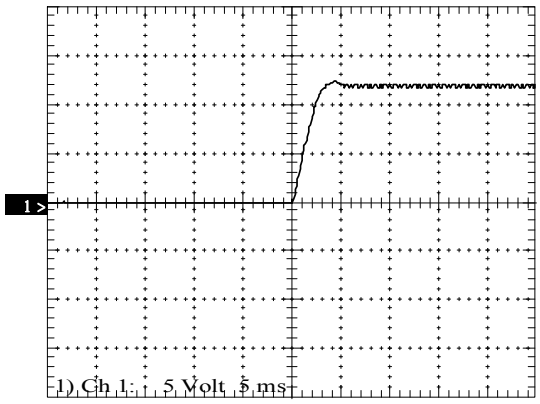

Figure 9. Start up transient response of the buck converter

VII. CONCLUSION

The authors have presented a digital based PID control approach for a buck-type dc–dc converter. The design approach of the controller design has been presented along with a detail description of the digital implementation of the controller using DSP. The experimental performance (steady-state accuracy and settling time) is consistent with that predicted by simulation results.

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