Design and Implementation of a Digital Controller For DC-to-DC Power Converters

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ABSTRACT

A digital signal processor (DSP) solution is proposed to control an H-bridge DC-DC isolated output power converter. The multiple mode digital controller is evaluated with an existing Westinghouse 1-kW power stage. The digital controller was developed using the dSPACE [1] rapid prototype development system and MATLAB/Simulink. It is evaluated using a real-time digital control development platform that included the actual Westinghouse converter power stage. Preliminary digital controller performance is presented that warrants continued investigation and development of this application of digital control and supports the use of the DSP as a viable component in Power Management and Distribution (PMAD) applications.

INTRODUCTION

The burgeoning interest in digitally controlled DC-DC power conversion is represented by the growing volume of literature on the subject [2-12]. The interest is strong in the aerospace industry, especially at NASA, for several reasons. First, efficient DC-DC power conversion is critically important in all space platforms, especially manned spacecraft. Second, all space borne systems require extensive telemetry data from all elements of the system. These requirements increase the cost and the complexity of all elements of the space system and further increase the expenditures of time and money required for sophisticated systems integration. Third, the high costs associated with the deployment of space systems constantly point research toward new technologies that promise to reduce the size and weight of system components while increasing overall system reliability and lowering integration costs. As outlined in the following work, digitally controlled DC-DC power conversion promises advantages in all of these areas.

OBJECTIVE

The principle goal of this effort is to demonstrate the following device-level improvements in an open-ended, digital configuration that will easily allow for the development and implementation of a number of system-level objectives.

DEVICE LEVEL IMPROVEMENTS -

1. Real-time optimization and adaptive compensation of the converter for varying load and/or line conditions.
2. Digital control to provide active compensation for mismatched FETs and/or aging components in the converter bridge.
3. Software implementation of under voltage protection, thereby eliminating inefficient hardware protection methods.
4. Greatly improved portability to other converters.
5. Possibility of implementing optimized active filter technology.

SYSTEM LEVEL IMPROVEMENTS - A digital control system architecture will include features to improve fault-tolerance and improve overall system performance. Such an architecture might involve a single DSP device controlling several DC-DC converters, with several such systems operating concurrently. Each DSP would be responsible for its assigned converters in addition to the monitoring of other devices. This architecture would allow for the following system capabilities or improvements:

1. Optimization of parallel converters under widely varying load conditions.
2. Controller redundancy to maintain converter operation in case of a DSP failure.
3. Independent verification of each converter's operation by secondary controllers.
4. Improved scalability.
5. Active load balancing.
6. Improved telemetric capabilities.

7. In situ frequency-domain analysis (FFT) of converter operations.
8. Early identification of potential device failures.
9. Improvement in overall system reliability and stability.
10. Active impedance control.

DIGITAL CONTROLLER DEVELOPMENT

The approach selected to develop this digital control architecture includes several key steps. First, a simple mathematical model of the system was developed as the initial basis of the controller design. Second, the digital control development platform was interfaced to the power converter. Third, the preliminary controller resulting from the simulation analysis was further developed using the digital control development platform and dSPACE's extensions to Simulink, the Real-Time Workshop (RTW). Finally, the control algorithm developed in this environment was programmed in native C code to avoid limitations of the Simulink/RTW environment and thereby improve overall controller performance.

MODELING AND SIMULATION

The modeling of DC-DC converters has resulted in several linearized [15-18] and quasi-linearized [19] solutions. These solutions generally consider only buck-boost class converters that require only a single Pulse Width Modulation (PWM) input. However, the converter system to be studied in this research is significantly more complicated. Its model will include a series of linear and non-linear blocks. The non-linear blocks can be quite complicated, especially the H-bridge block and the step-down isolation transformer block. However, since an objective of this investigation is a real-time digital control development platform that uses the actual converter, it is not necessary to precisely model the plant. Instead, a simple model was used to roughly test the proposed control system.

CONTROLLER DESIGN

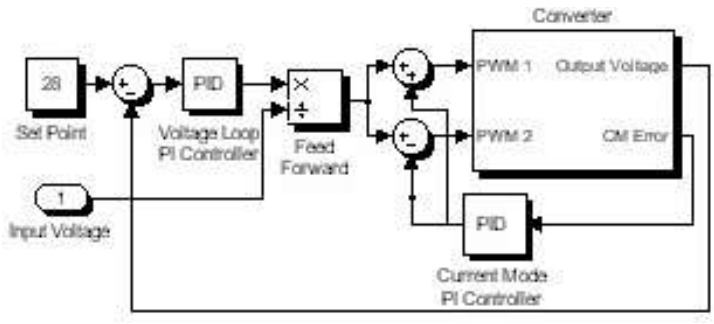

Figure 1 – Controller Block Diagram

A two-loop PI controller (Figure 1) was developed for the initial testing of the digital controller. Control of the converter is maintained through two phase-locked PWM signals.

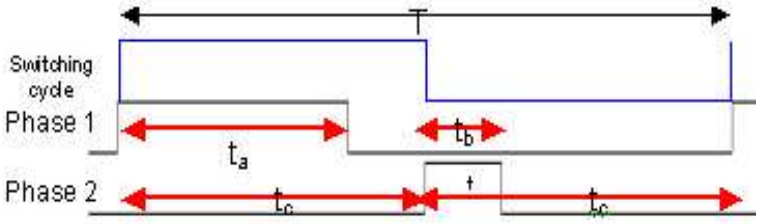

Figure 2 – Bi-Phase PWM Signal Definition, $2*t_c = T$, PWM Phase 1 duty cycle = t_a/t_c, PWM Phase 2 duty cycle = t_b/t_c. All units in seconds.

The converter requires alternating assertions of these PWM signals to drive an AC current through the transformer primary. Each PWM signal switches a high-side FET and the opposing low-side FET in the H-bridge. Asserting a particular PWM signal activates that set of FETs, allowing current to flow in one direction through the transformer. Asserting the opposite PWM signal allows current to flow in the opposite direction. The duty cycle of each PWM signal is directly proportional to the time current is flowing through the transformer during each half-cycle. Ideally, both PWM signals would be balanced. However, the transconductance of the FETs may vary by a factor of two nominally, and this imbalance may result in a DC current component through the transformer primary. Since this current may saturate the transformer core and limit it's ability to transmit power, the duty cycles of the driving PWM signals must be adjusted to compensate. Figure 2 illustrates an exaggerated case of current imbalance to completely define these two control signals. The top waveform of figure 2 is a uniform square wave of period T and 50% duty cycle. The middle waveform is one PWM channel and the lower waveform is the second channel. Time t_c exactly equals 0.5T. The duty cycle of channel one is define as t_a/t_c. The duty cycle of channel two is defined as t_b/t_c. Both of these quantities are strictly limited to the range $0 \le t \le 1$. However, the FETs exhibit a finite turn-off time, and it is possible that duty cycles near 1 may result in a shoot-through condition where FETs on one side of the H-bridge may momentarily be conducting simultaneously. These effects may damage or destroy converter components and must be avoided. Therefore, conventional designs implement a dead-band between the PWM phases. The dead-band used in this application is 5%. Therefore, the actual range of PWM duty cycles in this application is $0 \le t \le 0.95$.

Implementing the current mode control begins with calculating the current mode error. This is done by sensing the current through the transformer and integrating it to determine the average (DC) transformer primary current. A PI current loop controller is then used. The controller output is limited to restrict its control authority, and then differentially combined with the voltage loop controller output to determine the two PWM duty cycles.

The outer voltage loop is again a PI controller with feed forward of the converter input voltage. In this application,

the error signal drives a PI controller with a proportional gain near zero and an integral gain between 50 and 500. The output of the traditional PI control is then normalized by dividing it by the converter input voltage. This result is hard-limited to the range of +/- 1, then linearly scaled into the range between zero and one. This is the PWM duty cycle output of the voltage loop controller, and is then combined with the output of the current mode controller to form the two bi-phase PWM signals.

Additionally, all integration operations in the control implementation provide mechanisms that limit the integration and prevent integrator run-up. All limits in the controller are implemented by checking the limited variable against a programmed maximum (or minimum) value and assigning the maximum (or minimum, respectively) value if the variable exceeds the limit.

Finally, the controller implementation uses limited Boolean logic to shut down the converter under adverse input line conditions.

DIGITAL DC-DC CONVERTER ARCHITECTURE AND dSPACE SYSTEM TESTBED (FIGURES 3 &4)

The H-bridge DC-DC galvanically isolated power converter uses four FET switches to modulate filtered input power through a transformer.

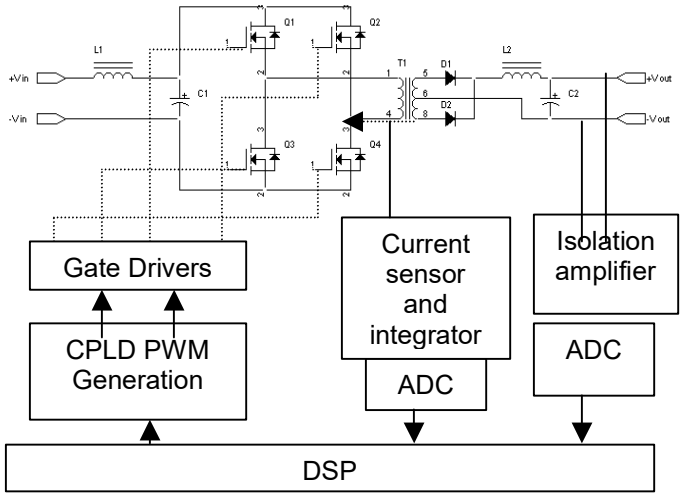

Figure 3 - Basic H-Bridge and Conceptual Diagram

To adapt this system to digital control, it is necessary to digitize both the output voltage and to sense and digitize the transformer current. These voltages are galvanically isolated from the digitization circuitry to avoid ground loops. Additionally, the transformer primary current must be sensed to allow current-mode control. As outlined in the previous section, it is actually the DC value of the primary current that is used in the control algorithm. In addition to the three aforementioned feed back variables, the input and output currents are also sensed. These currents will be used for further control development and for real-time input and output power measurements.

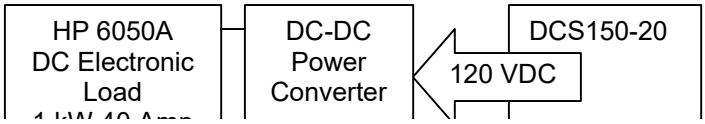

Figure 4 – Real-Time Digital Control Development Platform Block Diagram

This research utilizes a dSPACE DSP rapid-prototype development system based on the TMS320C40 DSP by Texas Instruments that provides 60 Mflops performance. The dSPACE system includes the DS1003 Modular DSP board, the DS2001 High Resolution ADC board, the DS2102 high-Resolution DAC board, and the DS4002 Timing and Digital I/O board. This configuration provides the following capabilities:

- Five ADC channels with 16-bit resolution and a sampling time of 6.2 microseconds.
- Six DAC channels with 16-bit resolution and a settling time of 2.0 microseconds.
- Single and/or three-phase PWM generation and measurement.
- Eight programmable digital I/O lines with 200ns resolution.
- Thirty-two additional digital I/O lines.

A Sorenson [13] Model DCS150-20 provides the nominal 120 VDC, 10 amps required by the Westinghouse converter. The testbed employs a Hewlett-Packard [14] Model 6050A DC Electronic load with the appropriate load modules. GPIB interfaced oscilloscopes with isolated probes and other GPIB instrumentation round out the testbed.

In interfacing the converter to the digital control development platform, a minimum of signal processing circuitry was used to scale and condition the measured variables for digitization and use in the controller. The circuitry was developed using Analog Devices AD210 Isolation Amplifiers. Two pole Butterworth filters are used on the voltage feedback channels to eliminate aliasing.

The Hall effect devices that measure the current signals provide the necessary electrical isolation. For the current loop feedback path, an F. W. Bell CLN-100 Hall effect current-mode sensor is employed, providing a bandwidth of 160 KHz. An analog integrator is used to determine the DC offset current in the transformer primary. For the input and output current measurements, F. W. Bell model BB-100 Hall-Effect current sensors are employed.

DIGITAL PWM GENERATION

In preparing the converter and the dSPACE system for the hardware-in-the-loop simulation, it was discovered that there was no direct way to maintain the phase lock between the two PWM channels that are required in the H-bridge. Using the dSPACE DSP hardware to

accomplish this would involve writing a low-level driver to guarantee that the two PWM signals were never simultaneously asserted.

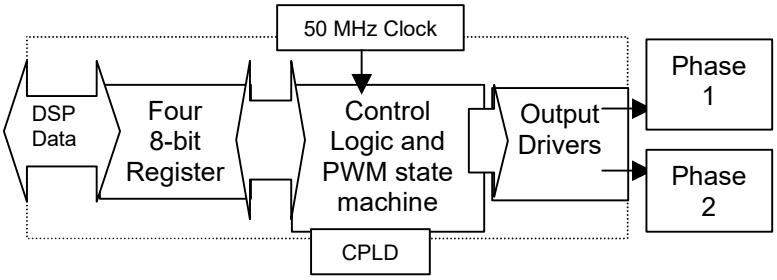

Figure 5 – PWM Generation

It was decided that a better solution would involve developing an Hardware Definition Language (HDL) program with which to program a complex programmable logic device (CPLD) that would interface to a digital output from dSPACE's DSP and generate the appropriate PWM signals. This novel CPLD architectural approach was designed to offer software-selectable switching frequencies and a PWM resolution of eight bits per PWM channel. Furthermore, the device was designed with the flexibility to allow for future improvements. Figure 5 shows the functional block diagram of the PWM generation circuitry. The PWM generation is controlled via four 8-bit registers as indicated in figure 5. Two registers hold the PWM duty cycle for each of the two phase-locked channels. The third register holds the divisor for the modulo-n clock generator circuit. The fourth register is reserved for future expansion and may be used in part to increase the PWM resolution. Using the 50 MHz clock in this implementation, the maximum attainable PWM frequency of the phase-locked PWM outputs is 100 kHz. Additionally, the phase is generated with quartz-crystal accuracy. The granularity of this implementation is better than 20 nanoseconds.

The additional expense of utilizing a CPLD in this application is easy to justify. Most importantly, the architecture of the CPLD-based PWM generator ensures that the PWM signals continue in the event of a DSP software failure. Under this condition, the PWM duty cycles will not change significantly and the converter will continue to provide a voltage output near the specified value. This allows the DSP time to restart and regain regulation of the converter without necessarily disrupting power conversion. Furthermore, the CPLD approach provides hardware-guaranteed phase lock between the two PWM signals; a software-based generation algorithm could be corrupted by an operating system failure in a multi-processing controller. Finally, the CPLD based PWM generator relieves the DSP of potentially significant processor bandwidth demands, freeing the DSP for advanced control computations, and other system-level distributed PMAD functions such as communication.

The digital PWM signal generation circuit was fabricated using an Altera 7000S family device and the CSU printed circuit board prototyping capabilities. The final device offers quartz-crystal accuracy in PWM signal generation with a resolution of less than 20 nanoseconds.

PRELIMINARY RESULTS

The Simulink/RTW–based control algorithm proved useful as a proof-of-concept study and was effective in controlling the system under low power (<100 watts) conditions. However, technical restrictions on the language of the environment resulted in an inefficient algorithm that was limited to a 2 kHz update frequency. This limitation required that the controller be implemented with smaller PI gains, effectively reducing the controller bandwidth. Subsequently, the control algorithm was manually coded into a native C program and downloaded directly into dSPACE's DSP processor. The native C controller executed easily at 25 kHz, utilizing only 33% of the CPU bandwidth, and ensured that the controller would provide an updated PWM duty ratio for each switching cycle. In addition to providing all the functionality of the Simulink/RTW–based controller, the C control also provided programmable running averaging on all feedback variables. After a cursory investigation of the effects of varying the number of samples, the researchers selected a three sample running average for this digital control application.

The resultant digital controller demonstrated an average output regulation better than 0.2% throughout the full power range of the converter. Controller performance in three fundamental measures of power regulation was measured and is documented in the following paragraphs. Each of these performance characterizations is presented for identical digital controllers using two distinct integral gains in the voltage PI controller. The values used are K_i =25 and K_i = 100. The current-mode control, switching frequency, sampling rate, and sampling average is identical in all cases as documented previously. The HP Infinium oscilloscope used for these characterizations is set to utilize its built-in bandwidth-limiting filter to clearly show controller response. The vertical scale of all graphs is 5 volts per division.

STEADY STATE CONTROLLER RESPONSE

The digital controller demonstrates good steady-state performance under the indicated conditions for both controller implementations. The results are shown graphically in figures 6(a) and 6(b). Both controllers indicate an average output value of 27.86 volts. Interestingly, the standard deviation in the output voltage for the lower-bandwidth controller (K_i = 25) is only 10 millivolts, compared to the 23.9 millivolts of the higher-bandwidth controller (K_i = 100).

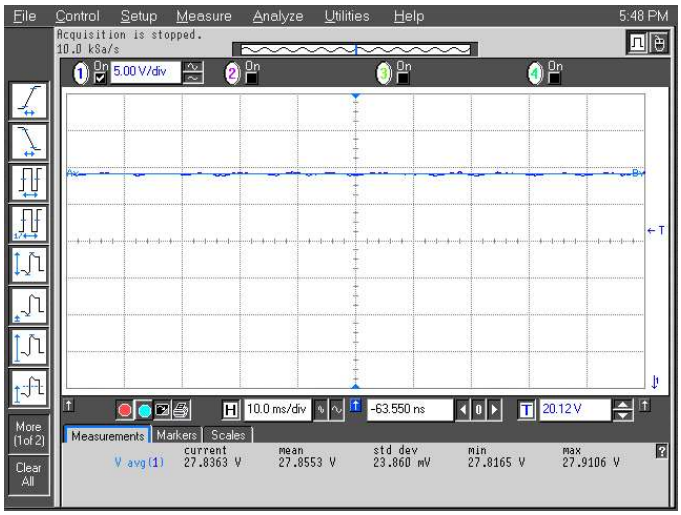

Figure 6a – Steady-state controller response, V_{set} = 28 volts I_{load} = 10 amps, K_i = 100.

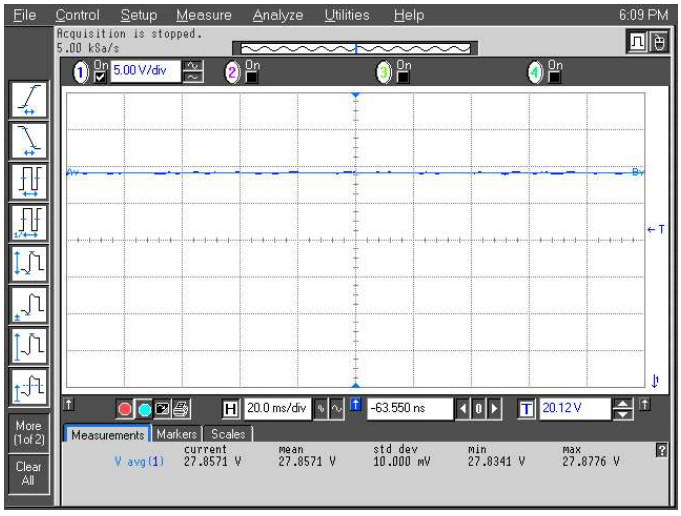

Figure 6b – Steady-state controller response, V_{set} = 28 volts I_{load} = 10 amps, K_i = 25.

LOAD TRANSIENT RESPONSE

Load transient response was determined using the HP6050A electronic load and its periodic transient generator. As shown in figures 7(a) and 7(b), the digital controller exhibits good response to load transients. Both controllers have similar output voltage fall-off on increasing load transients and similar voltage over-shoot on decreasing load transients. However, the faster time-constant of the higher bandwidth controller is clearly evident by comparing the recovery time of the two controllers. The faster controller requires only 25 milliseconds to recover from the decreasing load and 50

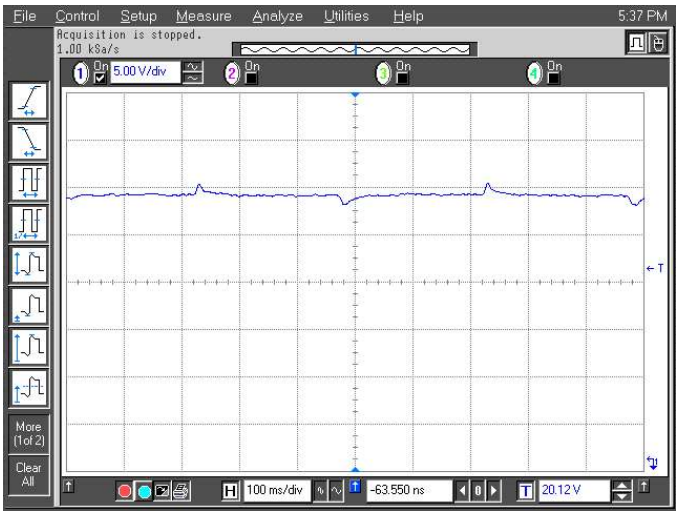

Figure 7a – Load Transient Response, V_{set} = 28 volts I_{load} = 2 to 10 amps, K_i = 100.

milliseconds for the increasing load. The slower controller requires approximately 125 milliseconds to recover from both transient cases. Again, the average output voltage of both controllers is the same.

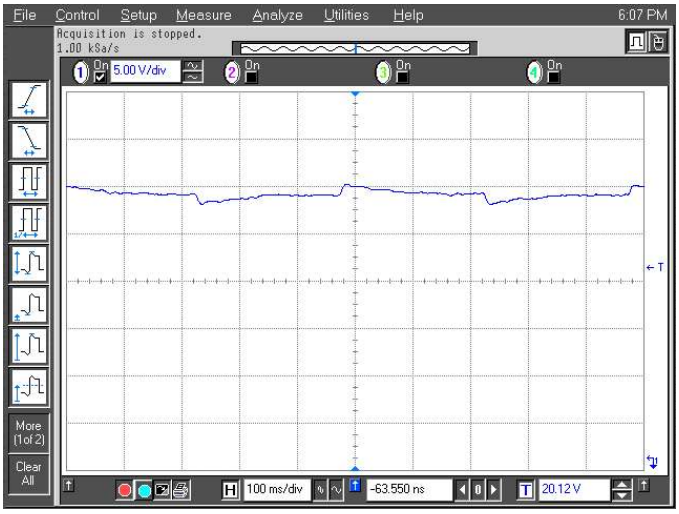

Figure 7b – Load Transient Response, V_{set} = 28 volts I_{load} = 2 to 10 amps, K_i = 25.

LINE TRANSIENT RESPONSE

Line transient response was determined using the Sorenson DC power supply's period transient generator. This produced line transients from 100 volts to 125 volts. The results are shown in figures 8(a) and (b). As in the load transient cases studied, the effect of the different controller bandwidth is clearly evident. However, the magnitudes of the output voltage transients are different for the two controllers. The higher bandwidth controller shows output transients of one volt in magnitude in response to the 25% input transients. The lower bandwidth controller exhibits output transients of approximately 3 volts in response to the same input transients.

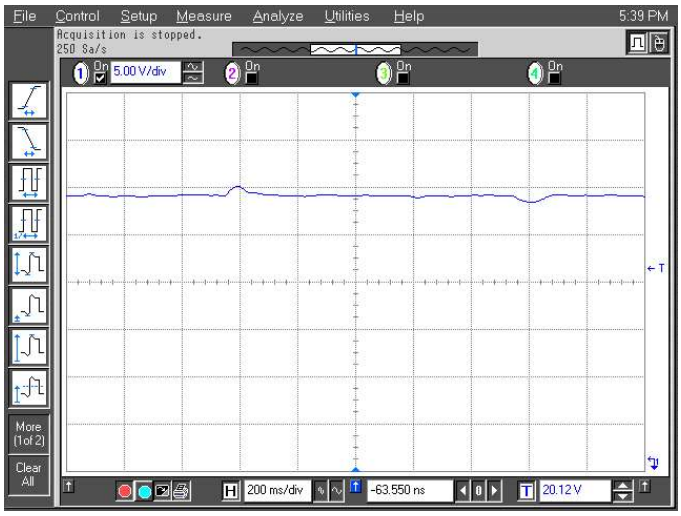

Figure 8a – Line Transient Response, V_{set} = 28 volts I_{load} = 10 amps, V_{in} = 100 volts to 125 volts, K_i = 100.

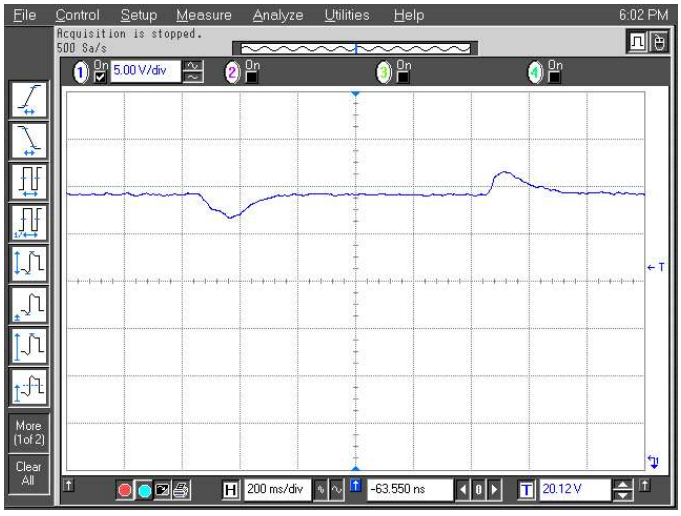

Figure 8b – Line Transient Response, V_{set} = 28 volts I_{load} = 10 amps, V_{in} = 100 volts to 125 volts, Ki = 25.

Recall that the digital controller developed for this application uses feed forward control on the input voltage to improve line transient response. To test the effectiveness of this control approach, the line transient test was repeated for the high bandwidth controller with the feed forward control removed.

Figure 9 illustrates the effectiveness of the feed forward control. The bottom trace indicates the identical result displayed in figure 8(a). The top trace is the performance of the controller without the feed forward control component using identical test parameters. Both traces are displayed using identical time and voltage scales. These data clearly indicate that the feed forward control implementation used in this controller improves the magnitude of the input line voltage induced output voltage transient by approximately 50% and reduces the duration of the disturbance by 25% to 50%.

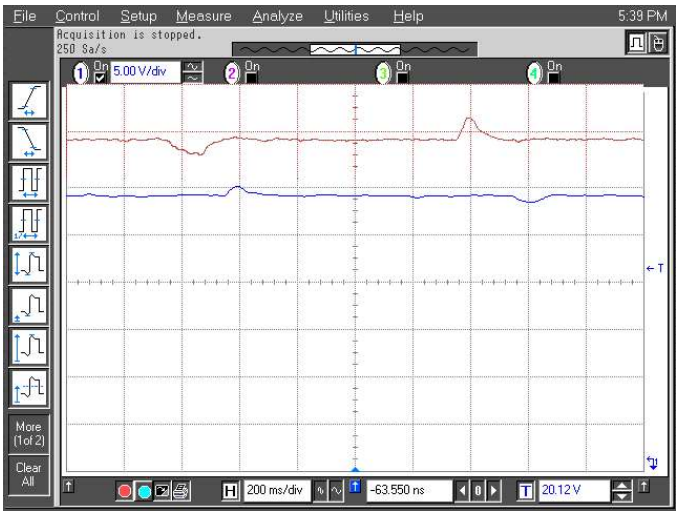

Figure 9 – Line Transient Response With and Without Feed Forward Control, V_{set} = 28 volts I_{load} = 10 amps, V_{in} = 100 volts to 125 volts, K_i = 100.

CONCLUDING REMARKS

This paper documents the elements of a research program to develop a DSP-based digital controller for a high power DC-to-DC converter. The controller developed features a novel architecture in which a CPLD device is used for PWM generation. Separating this converter function from the control DSP eases the DSP's computational load and provides a level of system fault tolerance. Evaluations of the initial selected control strategies show fast transient recovery for load and line disturbances and the potential for stable, tight steady-state output voltage regulation.

The results obtained thus far have identified several key issues that require further investigation. First, the current mode controller's structure and command authority must be thoroughly studied and refined. Second, the current controller's sensitivity to integral gain seems to indicate that either better noise filtering is needed in the data acquisition or a lead-lag compensator may be required to increase the system's phase margin. Third, there are indications that the 8-bit resolution per PWM channel may be near the minimum required in this application. Fourth, the effect of varying the switching frequency on converter input and output impedance should be analyzed to determine if the switching frequency might serve as a viable and useful control handle for the regulating system. Finally, nonlinear control techniques should be evaluated to determine the best controller for this application.

The digital controller and test bed developed in this research is ideally suited to resolve these issues and to help define the hardware and software requirements for the next generation of digital power conversion controllers. This next generation of digital control, employing powerful DSPs and fast network communication, may indeed form the basis of modular, distributed power management and distribution systems.

ACKNOWLEGMENTS

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DEFINITIONS, ACRONYMS, ABBREVIATIONS

ADC: Analog to Digital Converter
CPLD: Complex Programmable Logic Device
DAC: Digital to Analog Converter
DSP: Digital Signal Processor
FLOP: Floating Point Operation per Second
GPIB: General Purpose Instrumentation Bus
PMAD: Power Management and Distribution
PWM: Pulse Width Modulation
RTW: Real Time Workshop – dSPACE's extension to the Simulink Environment