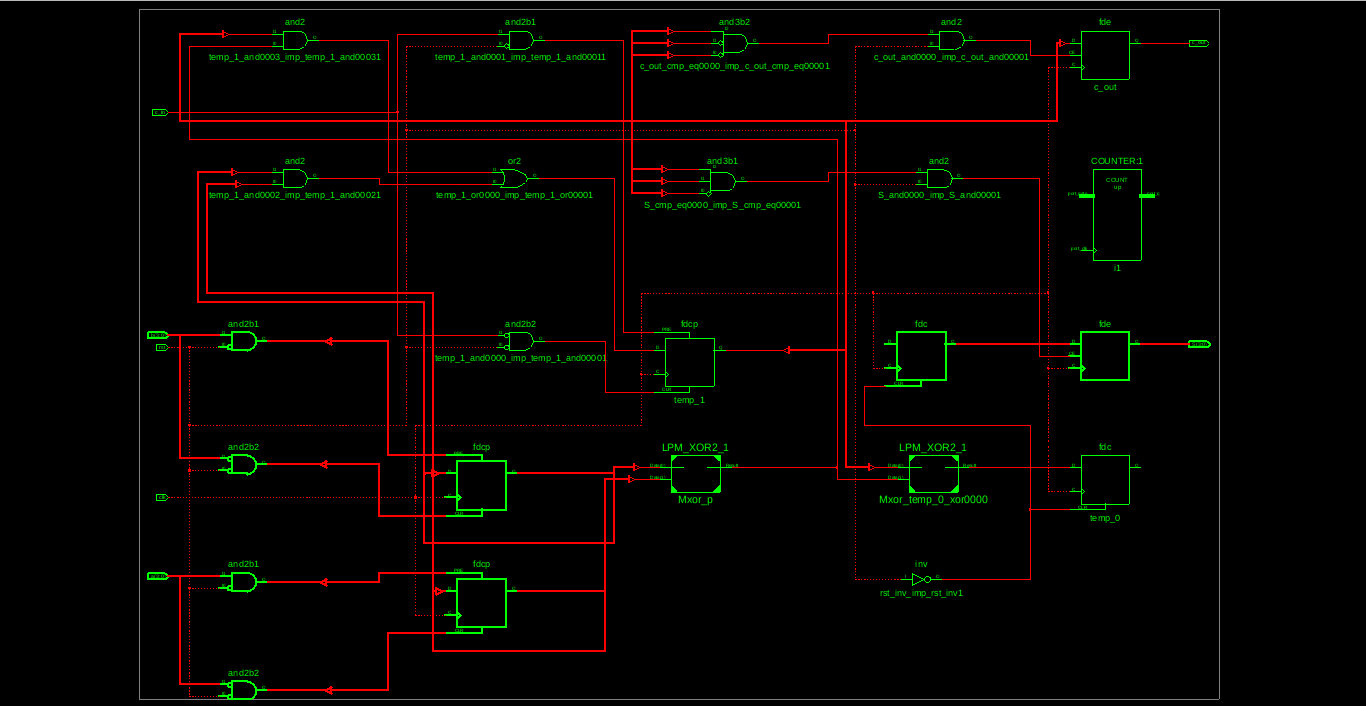
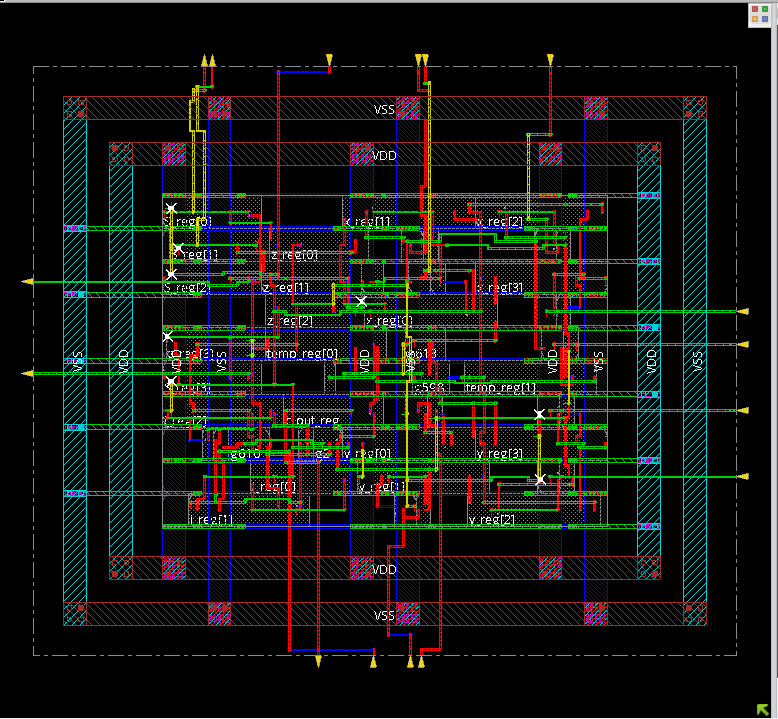
**DESIGN OF 4 BIT SERIAL ADDER:**

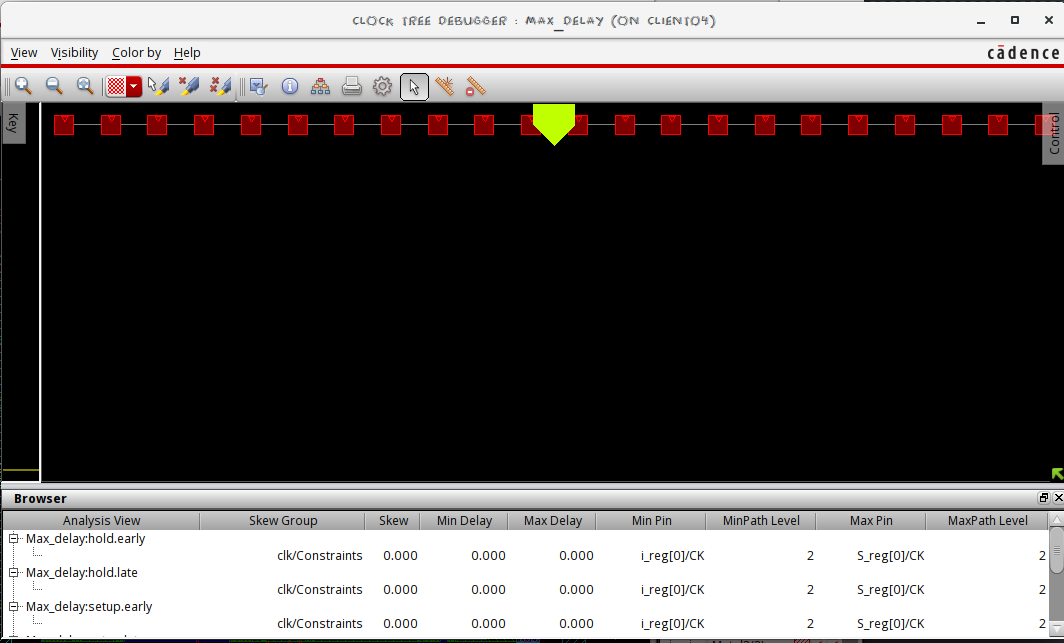
**RTL SCHEMATIC:**

****

**INNOVUS DESIGN:**

****

**CTS:**



**AREA REPORT:**

**(from Genus):**

Gate Instances Area Library

--------------------------------------

AO22X1 1 7.569 slow

CLKINVX1 2 4.541 slow

CLKXOR2X1 1 8.326 slow

DFFRHQX1 4 81.745 slow

DFFRX1 1 21.950 slow

DFFSRHQX1 9 245.236 slow

INVXL 1 2.271 slow

NAND2XL 10 30.276 slow

NAND3X2 1 8.326 slow

NOR2XL 1 3.028 slow

NOR3BX1 1 6.055 slow

OR2X1 9 40.873 slow

SDFFQXL 5 102.181 slow

SDFFRHQX1 3 74.933 slow

--------------------------------------

total 49 637.310

**(from Innovus)**

Depth Name #Inst Area (um^2)

---------------------------------------

0 serial\_add 49 639.5805

**POWER REPORT:**

**(from Genus):**

Leakage Dynamic Total

Instance Cells Power(nW) Power(nW) Power(nW)

-------------------------------------------------

serial\_add 49 3577.974 171615.089 175193.063

**(from Innovus):**

Total Power

-----------------------------------------------------------------------------------------

Total Internal Power: 0.11789337 92.6344%

Total Switching Power: 0.00577012 4.5339%

Total Leakage Power: 0.00360394 2.8318%

Total Power: 0.12726743

-----------------------------------------------------------------------------------------

**TIMING REPORTS:**

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 5 0.514 0.541 i\_0 (i\_0)

LUT4:I3->O 4 0.612 0.499 S\_and00001 (S\_and0000)

FDE:CE 0.483 S\_0

----------------------------------------

Total 2.649ns (1.609ns logic, 1.040ns route)

(60.7% logic, 39.3% route)

Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 5 / 5

-------------------------------------------------------------------------

Offset: 3.811ns (Levels of Logic = 2)

Source: rst (PAD)

Destination: S\_0 (FF)

Destination Clock: clk rising

Data Path: rst to S\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 21 1.106 1.111 rst\_IBUF (rst\_IBUF)

LUT4:I0->O 4 0.612 0.499 S\_and00001 (S\_and0000)

FDE:CE 0.483 S\_0

----------------------------------------

Total 3.811ns (2.201ns logic, 1.610ns route)

(57.8% logic, 42.2% route)

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 5 / 5

-------------------------------------------------------------------------

Offset: 4.040ns (Levels of Logic = 1)

Source: c\_out (FF)

Destination: c\_out (PAD)

Source Clock: clk rising

Data Path: c\_out to c\_out

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDE:C->Q 1 0.514 0.357 c\_out (c\_out\_OBUF)

OBUF:I->O 3.169 c\_out\_OBUF (c\_out)

----------------------------------------

Total 4.040ns (3.683ns logic, 0.357ns route)

(91.2% logic, 8.8% route)

**COMPARISON OF AREAs WITH OTHER DEVICES:**

|  |  |  |
| --- | --- | --- |
| DEVICE | AREA (GENUS) | AREA (INNOVUS) |
| D FLIPFLOP | 18.166 um^2 | 18.1656 um^2 |
| SERIAL ADDER | 637.310 um^2 | 637.3105 um^2 |
| SERIAL MULTIPLIER | 645.636 um^2 | 645.6357 um^2 |

**COMPARISON OF POWERs:**

|  |  |  |
| --- | --- | --- |
| DEVICE | POWER (GENUS) | POWER (INNOVUS) |
| D FLIPFLOP | 4230.914 nW | 0.00434972 mW |
| SERIAL ADDER | 175193.063 nW | 0.12726743 mW |
| SERIAL MULTIPLIER | 178773.456 nW | 0.13222011 mW |

**OBSERVATIONS:**

* The power in Innovus is lower than in Genus as Innovus optimises our design.