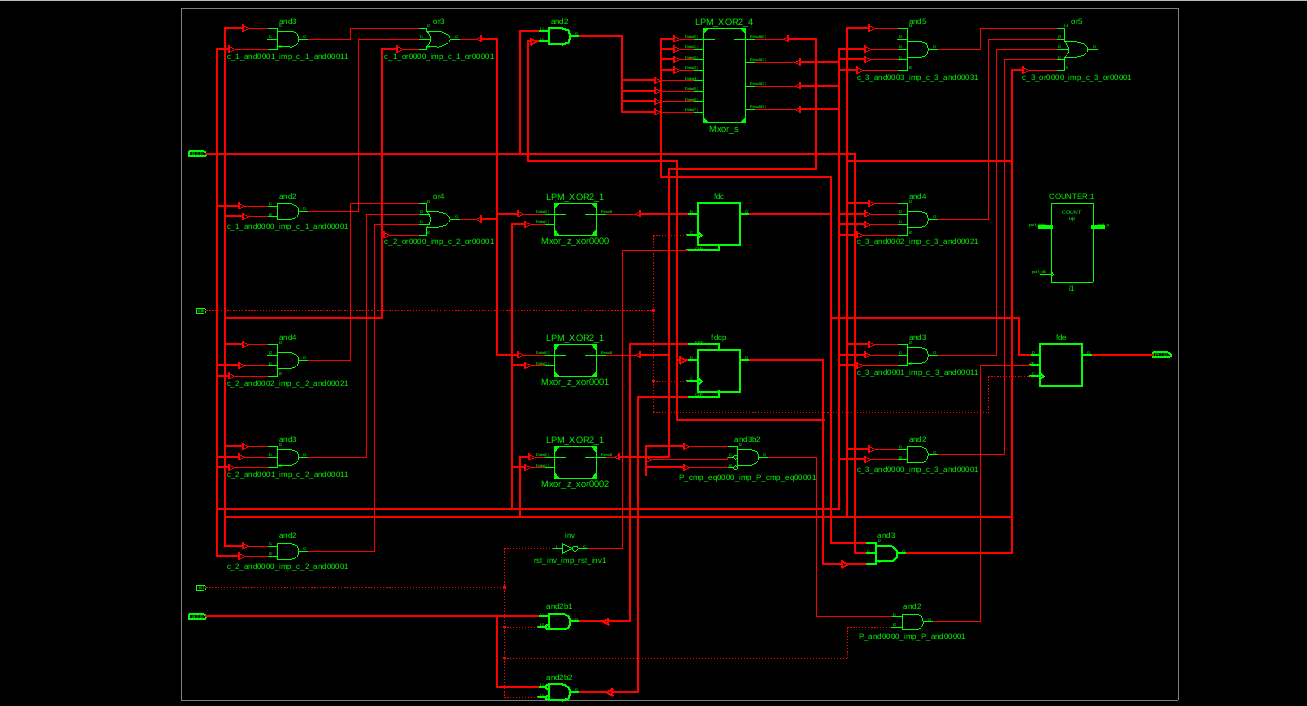
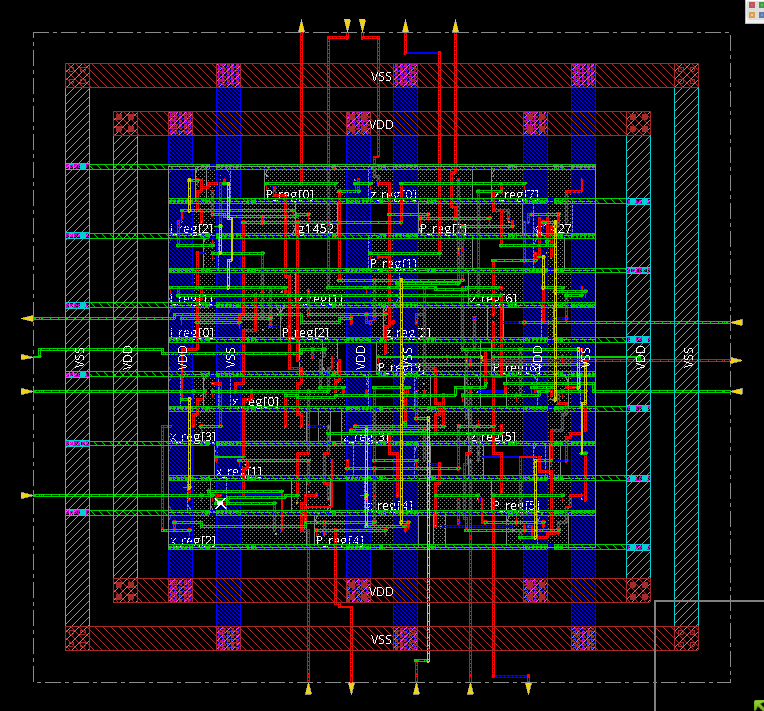
**DESIGN OF 4 BIT SERIAL MULTIPLIER:**

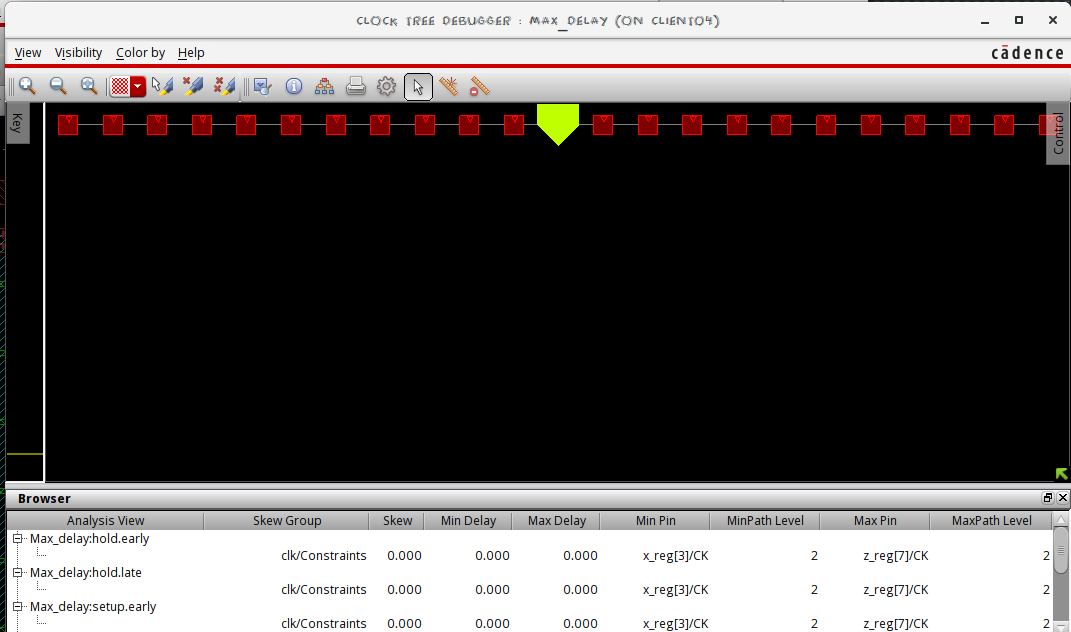
**RTL SCHEMATIC:**

****

**INNOVUS DESIGN:**

****

**CTS:**

****

**AREA REPORT:**

**(from Genus):**

Gate Instances Area Library

--------------------------------------

AND2X4 1 8.326 slow

AO22XL 1 7.569 slow

AOI22X1 1 6.055 slow

CLKINVX1 6 13.624 slow

DFFRHQX1 4 81.745 slow

DFFRX1 1 21.950 slow

DFFSRHQX1 4 108.994 slow

INVXL 3 6.812 slow

MXI2XL 3 18.166 slow

NAND2XL 10 30.276 slow

NOR3X1 1 4.541 slow

OAI22X1 1 6.055 slow

OR2X1 4 18.166 slow

SDFFQXL 8 163.490 slow

SDFFRHQX1 6 149.866 slow

--------------------------------------

total 54 545.636

**(from Innovus)**

Depth Name #Inst Area (um^2)

--------------------------------------

0 serialmul 54 545.6357

**POWER REPORT:**

**(from Genus):**

Leakage Dynamic Total

Instance Cells Power(nW) Power(nW) Power(nW)

------------------------------------------------

serialmul 54 3234.527 155121.930 176545.456

**(from Innovus):**

Total Power

-----------------------------------------------------------------------------------------

Total Internal Power: 0.10125463 91.7067%

Total Switching Power: 0.00731394 5.5316%

Total Leakage Power: 0.00365153 2.7617%

Total Power: 0.11256018

-----------------------------------------------------------------------------------------

**TIMING REPORTS:**

Timing constraint: Default period analysis for Clock 'clk'

Clock period: 2.568ns (frequency: 333.578MHz)

Total number of paths / destination ports: 68 / 31

-------------------------------------------------------------------------

Delay: 2.568ns (Levels of Logic = 2)

Source: x\_0 (FF)

Destination: z\_6 (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: x\_0 to z\_6

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDCP:C->Q 7 0.514 0.605 x\_0 (x\_0)

LUT4:I3->O 1 0.612 0.387 c<3>11\_SW0 (N2)

LUT4:I2->O 1 0.612 0.000 z\_xor00001 (z\_xor0000)

FDC:D 0.268 z\_6

----------------------------------------

Total 2.568ns (2.006ns logic, 0.992ns route)

(66.9% logic, 33.1% route)

Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 26 / 13

-------------------------------------------------------------------------

Offset: 3.746ns (Levels of Logic = 2)

Source: rst (PAD)

Destination: P\_0 (FF)

Destination Clock: clk rising

Data Path: rst to P\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 10 1.106 0.902 rst\_IBUF (rst\_IBUF)

LUT4:I0->O 8 0.612 0.643 P\_and00001 (P\_and0000)

FDE:CE 0.483 P\_0

----------------------------------------

Total 3.746ns (2.201ns logic, 1.545ns route)

(58.8% logic, 41.2% route)

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 8 / 8

-------------------------------------------------------------------------

Offset: 4.040ns (Levels of Logic = 1)

Source: P\_7 (FF)

Destination: P<7> (PAD)

Source Clock: clk rising

Data Path: P\_7 to P<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDE:C->Q 1 0.514 0.357 P\_7 (P\_7)

OBUF:I->O 3.169 P\_7\_OBUF (P<7>)

----------------------------------------

Total 4.040ns (3.683ns logic, 0.357ns route)

(91.2% logic, 8.8% route)

**COMPARISON OF AREAs WITH OTHER DEVICES:**

|  |  |  |
| --- | --- | --- |
| DEVICE | AREA (GENUS) | AREA (INNOVUS) |
| D FLIPFLOP | 18.166 um^2 | 18.1656 um^2 |
| SERIAL ADDER | 501.310 um^2 | 501.3109 um^2 |
| SERIAL MULTIPLIER | 588.436 um^2 | 588.4357 um^2 |

**COMPARISON OF POWERs:**

|  |  |  |
| --- | --- | --- |
| DEVICE | POWER (GENUS) | POWER (INNOVUS) |
| D FLIPFLOP | 4230.914 nW | 0.00434972 mW |
| SERIAL ADDER | 145783.063 nW | 0.12712743 mW |
| SERIAL MULTIPLIER | 166773.456 nW | 0.13222011 mW |

**OBSERVATIONS:**

* The power in Innovus is lower than in Genus as Innovus optimises our design.