**REPORT FOR ASSIGNMENT 1:**

**INTRODUCTION:**

The universal gates NAND & NOR, along with the basic gates AND, OR , XOR , XNOR and NOT are basic building blocks of bigger combinational circuits. These gates can be built from NMOS & PMOS transistors in complementary CMOS fashion.

**PROCEDURE:**

**First on Xilinx ISE:**

1. We write the codes and testbenches.

2. We run simulation using Isim to get timing diagrams.

3. We then run RTL synthesis to get the RTL diagrams.

**On CADENCE:**

**1. For timing diagrams:** First we do csh and source cshrc. Then we do NCLaunch and it opens SimVision with the timing diagram. We can change the scale as per our requirement to view the whole signal.

**2. For Genus:** We write the rc\_script.tcl file for each circuit and do genus -f rc\_script.tcl to load the file into genus. Inside genus we run Schematic to generate gate level diagrams. We also generate power, area and timing reports.

**3. For Innovus :** We generate .globals file for each circuit and launch innovus with it. We do: a. Floorplan b. Power rings & stripes c. Placing standard cells d. Routing

This gives a layout diagram of the circuit. We analyse the timing reports PreCTS, PostCTS, PostRoute, PrePlacement where CTS is **Clock Tree Synthesis.** We also analyse area and power reports from report\_area and report\_power.

**OBSERVATIONS AND REPORTS:**

**BASIC GATES:**

**For 2-input AND Gate: A.B = Y**

|  |  |  |
| --- | --- | --- |
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**GATE STATISTICS AND AREA:**

Gate Instances Area Library

---------------------------------

AND2XL 1 4.541 slow

---------------------------------

total 1 4.541

Type Instances Area Area %

--------------------------------------

logic 1 4.541 100.0

physical\_cells 0 0.000 0.0

--------------------------------------

total 1 4.541 100.0

**AREA from Innovus:**

Total area of Standard cells: 4.541 um^2

Total area of Standard cells(Subtracting Physical Cells): 4.541 um^2

Total area of Macros: 0.000 um^2

Total area of Blockages: 0.000 um^2

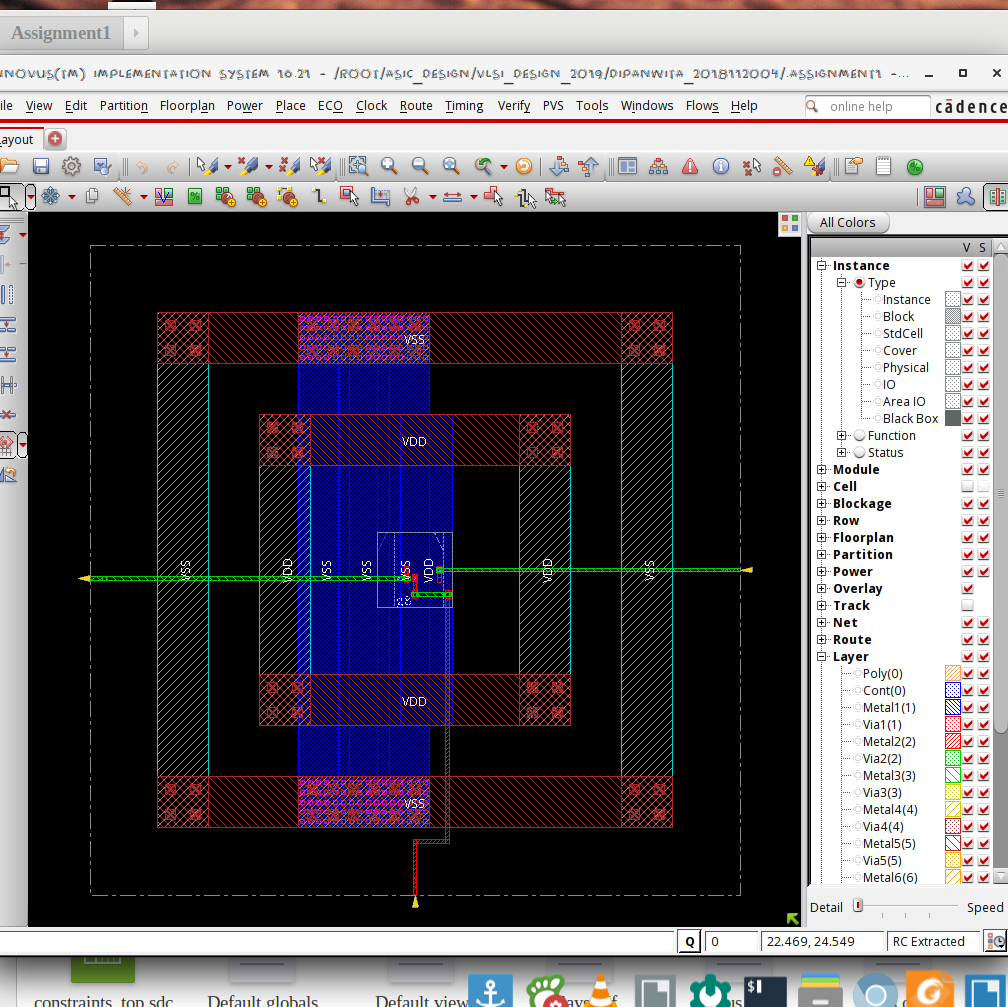
Total area of Pad cells: 0.000 um^2

Total area of Core: 6.812 um^2

Total area of Chip: 524.868 um^2

Effective Utilization: 6.6667e-01

**INNOVUS LAYOUT :**

****

**\*\*\* Innovus Statistics for net list andgate \*\*\***

Number of cells = 1

Number of nets = 3

Number of tri-nets = 0

Number of degen nets = 0

Number of pins = 6

Number of i/os = 3

Number of nets with 2 terms = 3 (100.0%)

Number of nets with >=10 terms = 0 (0.0%)

\*\*\* 1 Primitives used:

Primitive AND2XL (1 insts)

**POWER:**

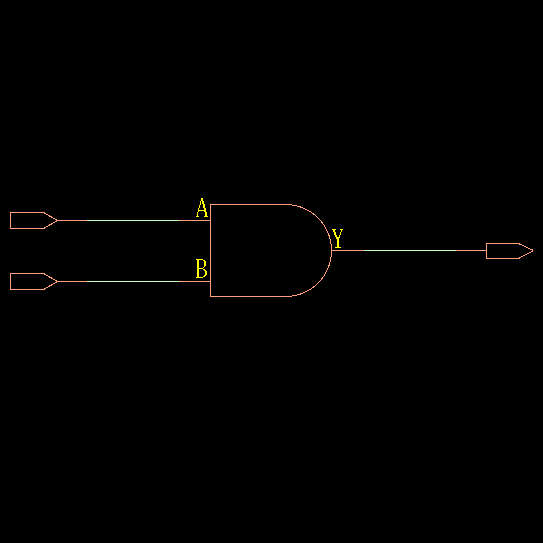
Leakage Dynamic Total

Instance Cells Power(nW) Power(nW) Power(nW)

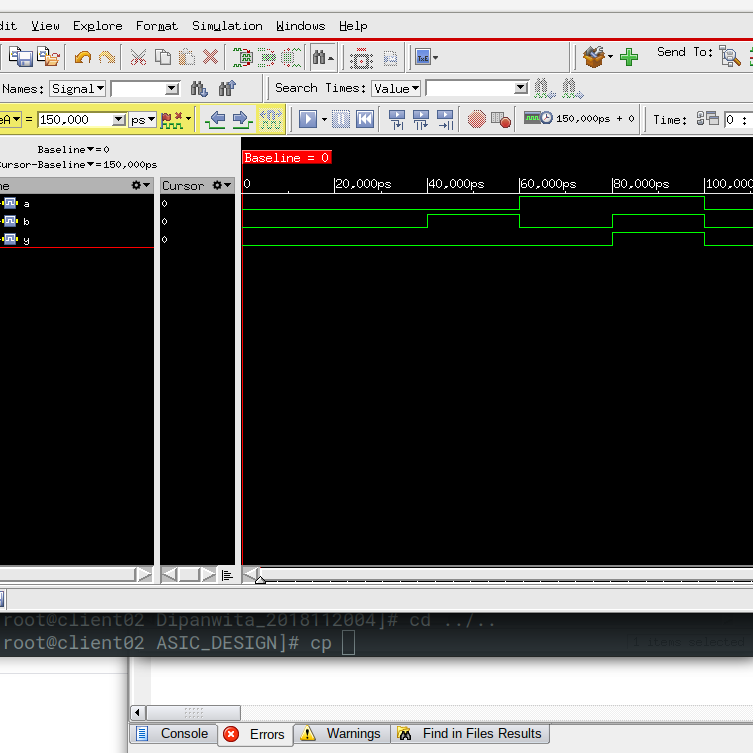
---------------------------------------------

andgate 1 24.663 88.320 112.983

**GATE LEVEL DIAGRAM:**



**TIMING DIAGRAM:**



**EXPLANATION OF TIMING DIAGRAM:**

1. Till 40,000 us A = 0, B =0, so Y = A.B = 0

2. From 40,000 us to 60,000 us , A = 0, B=1, Y = 0

3. From 60,000 us to 80,000 us, A = 1, B = 0, Y = 0

4. From 80,000 us to 100,000 us, A = 1, B=1, Y = 1

**For 2-input OR Gate: A + B = Y**

|  |  |  |
| --- | --- | --- |
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

**GATE STATISTICS & AREA:**

Gate Instances Area Library

--------------------------------

OR2X1 1 4.541 slow

--------------------------------

total 1 4.541

Type Instances Area Area %

--------------------------------------

logic 1 4.541 100.0

physical\_cells 0 0.000 0.0

--------------------------------------

total 1 4.541 100.0

**AREA from Innovus:**

Total area of Standard cells: 4.541 um^2

Total area of Standard cells(Subtracting Physical Cells): 4.541 um^2

Total area of Macros: 0.000 um^2

Total area of Blockages: 0.000 um^2

Total area of Pad cells: 0.000 um^2

Total area of Core: 6.812 um^2

Total area of Chip: 524.868 um^2

**\*\*\* Innovus Statistics for net list orgate \*\*\***

Number of cells = 1

Number of nets = 3

Number of tri-nets = 0

Number of degen nets = 0

Number of pins = 6

Number of i/os = 3

Number of nets with 2 terms = 3 (100.0%)

Number of nets with >=10 terms = 0 (0.0%)

\*\*\* 1 Primitives used:

Primitive OR2X1 (1 insts)

**POWER:**

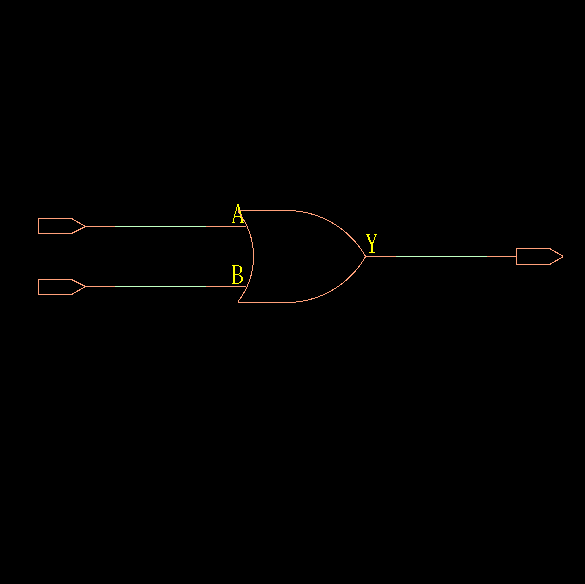
Leakage Dynamic Total

Instance Cells Power(nW) Power(nW) Power(nW)

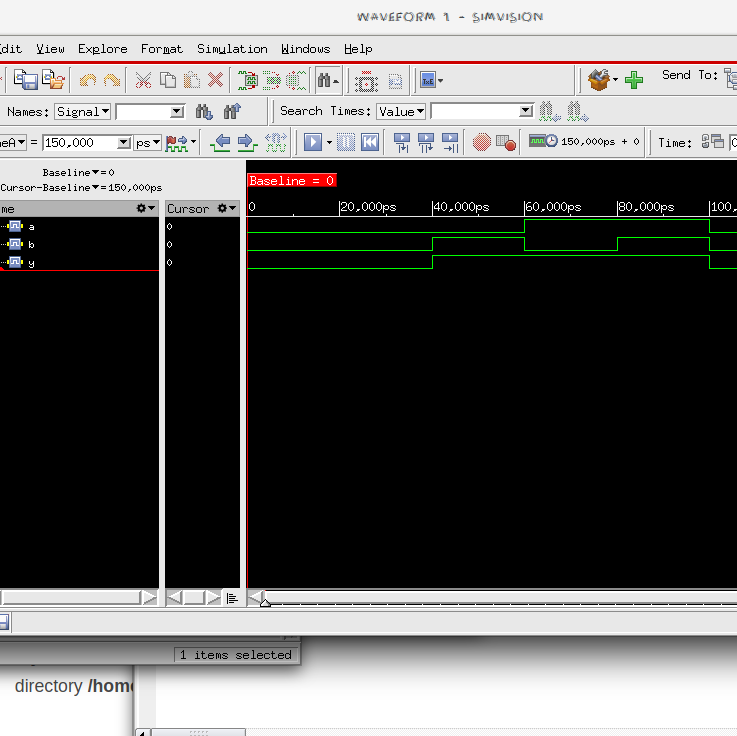
---------------------------------------------

orgate 1 42.556 93.213 135.769

**GATE LEVEL DESIGN:**



**TIMING DIAGRAM:**



**EXPLANATION OF TIMING DIAGRAM:**

1. Till 40,000 us A = 0, B =0, so Y = 0

2. From 40,000 us to 60,000 us , A = 0, B=1, Y = 1

3. From 60,000 us to 80,000 us, A = 1, B = 0, Y = 1

4. From 80,000 us to 100,000 us, A = 1, B=1, Y = 1

**For 2-input NOT Gate: Y = A’**

|  |  |
| --- | --- |
| A | Y |
| 0 | 1 |
| 1 | 0 |

**GATE STATISTICS & AREA:**

Gate Instances Area Library

--------------------------------

INVXL 1 2.271 slow

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total 1 2.271

Type Instances Area Area %

--------------------------------------

inverter 1 2.271 100.0

physical\_cells 0 0.000 0.0

--------------------------------------

total 1 2.271 100.0

**AREA from Innovus:**

Total area of Standard cells: 2.271 um^2

Total area of Standard cells(Subtracting Physical Cells): 2.271 um^2

Total area of Macros: 0.000 um^2

Total area of Blockages: 0.000 um^2

Total area of Pad cells: 0.000 um^2

Total area of Core: 3.784 um^2

Total area of Chip: 498.293 um^2

Effective Utilization: 6.0000e-01

**\*\*\* Innovus Statistics for net list notgate \*\*\***

Number of cells = 1

Number of nets = 2

Number of tri-nets = 0

Number of degen nets = 0

Number of pins = 4

Number of i/os = 2

Number of nets with 2 terms = 2 (100.0%)

Number of nets with >=10 terms = 0 (0.0%)

\*\*\* 1 Primitives used:

Primitive INVXL (1 insts)

**POWER:**

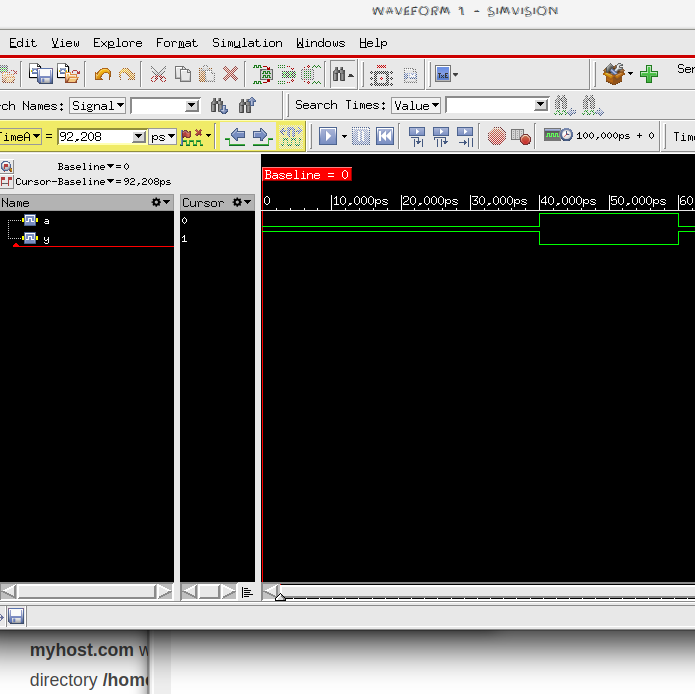
Leakage Dynamic Total

Instance Cells Power(nW) Power(nW) Power(nW)

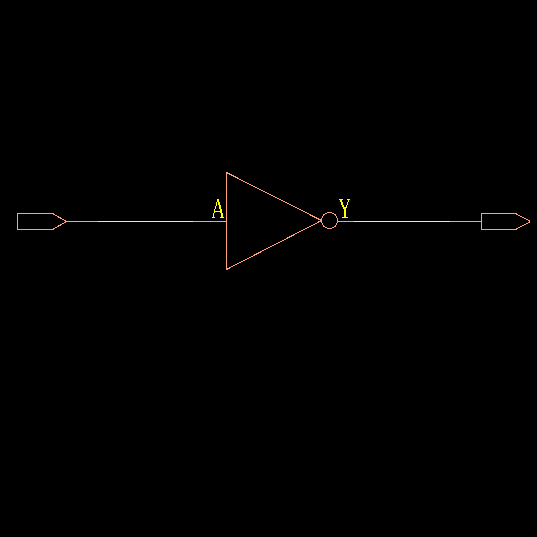
---------------------------------------------

notgate 1 8.757 44.417 53.174

**TIMING DIAGRAM:**



**GATE LEVEL DESIGN:**



**EXPLANATION OF TIMING DIAGRAM:**

1. Till 40,000 us A = 0, Y = 1

2. From 40,000 us to 60,000 us , A = 1,Y = 0

**For 2-input NOR Gate: Y = (A + B)’**

|  |  |  |
| --- | --- | --- |
| A | B | Y |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**GATE LEVEL DESIGN & AREA:**

Gate Instances Area Library

---------------------------------

NOR2XL 1 3.028 slow

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total 1 3.028

Type Instances Area Area %

--------------------------------------

logic 1 3.028 100.0

physical\_cells 0 0.000 0.0

--------------------------------------

total 1 3.028 100.0

**AREA FROM Innovus:**

Total area of Standard cells: 3.028 um^2

Total area of Standard cells(Subtracting Physical Cells): 3.028 um^2

Total area of Macros: 0.000 um^2

Total area of Blockages: 0.000 um^2

Total area of Pad cells: 0.000 um^2

Total area of Core: 4.541 um^2

Total area of Chip: 504.936 um^2

Effective Utilization: 6.6667e-01

**\*\*\* Innovus Statistics for net list norgate \*\*\***

Number of cells = 1

Number of nets = 3

Number of tri-nets = 0

Number of degen nets = 0

Number of pins = 6

Number of i/os = 3

Number of nets with 2 terms = 3 (100.0%)

Number of nets with >=10 terms = 0 (0.0%)

\*\*\* 1 Primitives used:

Primitive NOR2XL (1 insts)

**POWER:**

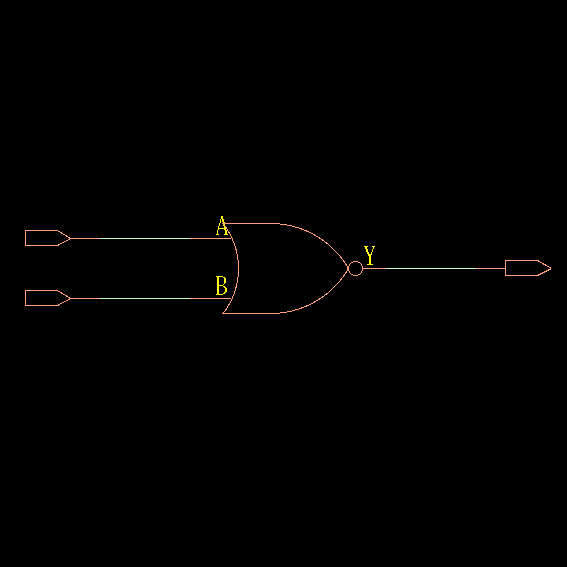
Leakage Dynamic Total

Instance Cells Power(nW) Power(nW) Power(nW)

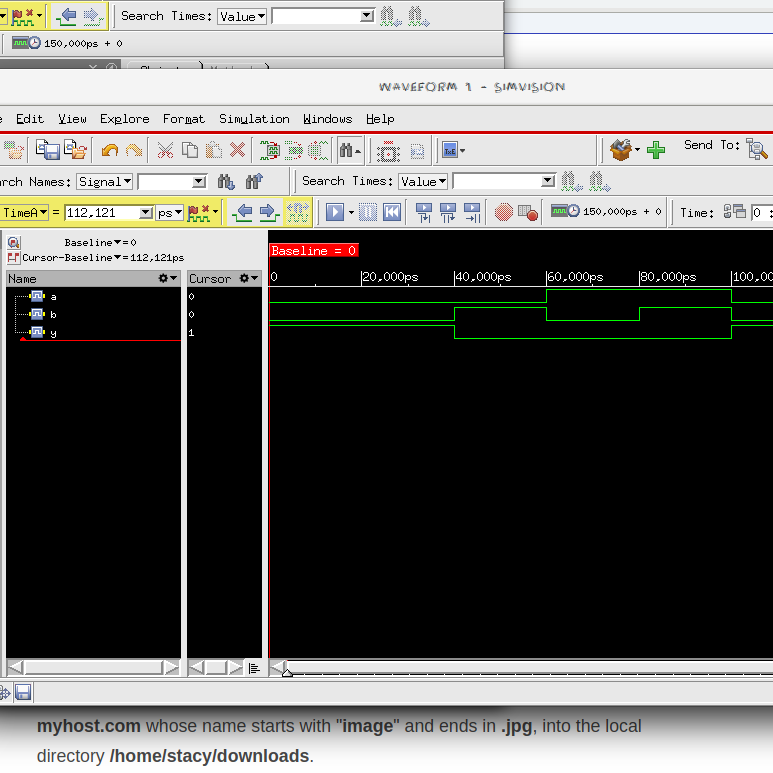
---------------------------------------------

norgate 1 12.358 80.475 92.834

**GATE LEVEL DIAGRAM:**

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**TIMING DIAGRAM:**

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**EXPLANATION OF TIMING DIAGRAM:**

1. Till 40,000 us A = 0, B =0, so Y = 1

2. From 40,000 us to 60,000 us , A = 0, B=1, Y = 0

3. From 60,000 us to 80,000 us, A = 1, B = 0, Y = 0

4. From 80,000 us to 100,000 us, A = 1, B=1, Y = 0

**For 2-input NAND Gate: Y = (A.B)’**

|  |  |  |
| --- | --- | --- |
| A | B | Y |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**GATE STATISTICS:**

Gate Instances Area Library

----------------------------------

NAND2XL 1 3.028 slow

----------------------------------

total 1 3.028

Type Instances Area Area %

--------------------------------------

logic 1 3.028 100.0

physical\_cells 0 0.000 0.0

--------------------------------------

total 1 3.028 100.0

**AREA From Innovus:**

Total area of Standard cells: 3.028 um^2

Total area of Standard cells(Subtracting Physical Cells): 3.028 um^2

Total area of Macros: 0.000 um^2

Total area of Blockages: 0.000 um^2

Total area of Pad cells: 0.000 um^2

Total area of Core: 4.541 um^2

Total area of Chip: 504.936 um^2

Effective Utilization: 6.6667e-01

**POWER:**

Leakage Dynamic Total

Instance Cells Power(nW) Power(nW) Power(nW)

---------------------------------------------

nandgate 1 9.289 59.793 69.083

**\*\*\* Innovus Statistics for net list nandgate \*\*\***

Number of cells = 1

Number of nets = 3

Number of tri-nets = 0

Number of degen nets = 0

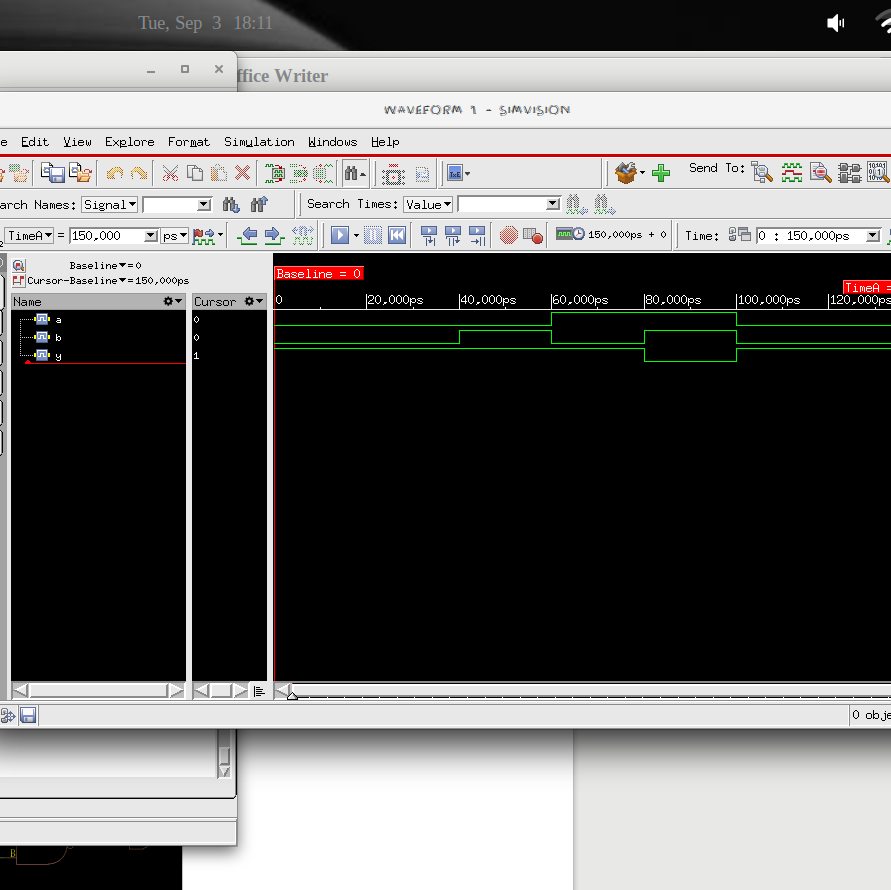
Number of pins = 6

Number of i/os = 3

Number of nets with 2 terms = 3 (100.0%)

Number of nets with >=10 terms = 0 (0.0%)

**TIMING DIAGRAM:**



**EXPLANATION OF TIMING DIAGRAM:**

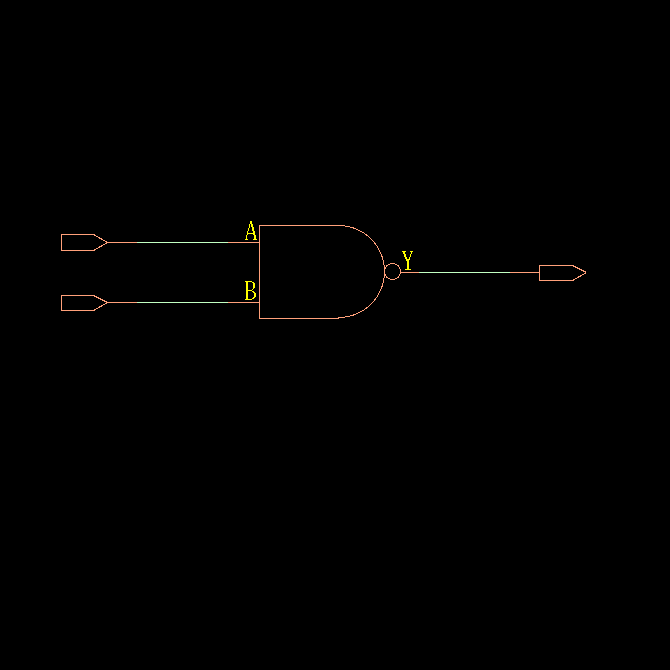
1. Till 40,000 us A = 0, B =0, so Y = (A.B)’ = 1

2. From 40,000 us to 60,000 us , A = 0, B=1, Y = 1

3. From 60,000 us to 80,000 us, A = 1, B = 0, Y = 1

4. From 80,000 us to 100,000 us, A = 1, B=1, Y = 0

**GATE LEVEL DIAGRAM:**

****

**For 2-input XOR Gate: Y = A.B’ + A’.B**

|  |  |  |
| --- | --- | --- |
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**GATE STATISTICS & AREA:**

Gate Instances Area Library

------------------------------------

CLKXOR2X1 1 8.326 slow

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total 1 8.326

Type Instances Area Area %

--------------------------------------

logic 1 8.326 100.0

physical\_cells 0 0.000 0.0

--------------------------------------

total 1 8.326 100.0

**AREA from Innovus:**

Total area of Standard cells: 8.326 um^2

Total area of Standard cells(Subtracting Physical Cells): 8.326 um^2

Total area of Macros: 0.000 um^2

Total area of Blockages: 0.000 um^2

Total area of Pad cells: 0.000 um^2

Total area of Core: 12.110 um^2

Total area of Chip: 571.375 um^2

Effective Utilization: 6.8750e-01

**\*\*\* Statistics for net list xorgate \*\*\***

Number of cells = 1

Number of nets = 3

Number of tri-nets = 0

Number of degen nets = 0

Number of pins = 6

Number of i/os = 3

Number of nets with 2 terms = 3 (100.0%)

Number of nets with >=10 terms = 0 (0.0%)

\*\*\* 1 Primitives used:

Primitive CLKXOR2X1 (1 insts)

**POWER:**

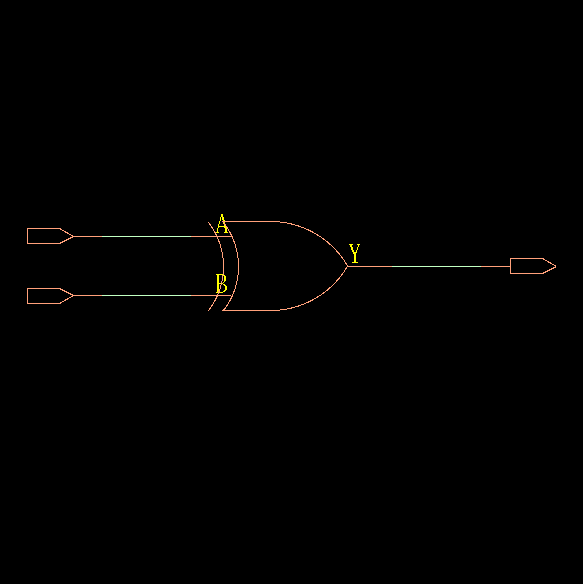
Leakage Dynamic Total

Instance Cells Power(nW) Power(nW) Power(nW)

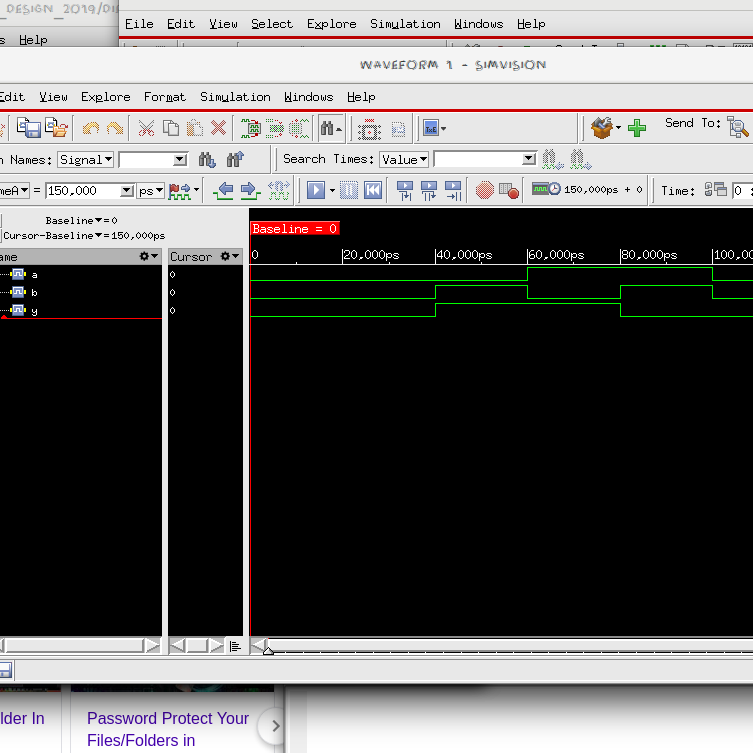
---------------------------------------------

xorgate 1 72.543 268.064 340.607

**GATE LEVEL DESIGN:**

****

**TIMING DIAGRAM:**

****

**EXPLANATION OF TIMING DIAGRAM:**

1. Till 40,000 us A = 0, B =0, so Y = 0

2. From 40,000 us to 60,000 us , A = 0, B=1, Y = 1

3. From 60,000 us to 80,000 us, A = 1, B = 0, Y = 1

4. From 80,000 us to 100,000 us, A = 1, B=1, Y = 0

**For 2-input XNOR Gate: Y = A.B + A’.B’**

|  |  |  |
| --- | --- | --- |
| A | B | Y |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**GATE STATISTICS & AREA:**

Gate Instances Area Library

----------------------------------

NAND2XL 1 3.028 slow

OAI21XL 1 4.541 slow

----------------------------------

total 2 7.569

Type Instances Area Area %

--------------------------------------

logic 2 7.569 100.0

physical\_cells 0 0.000 0.0

--------------------------------------

total 2 7.569 100.0

**AREA from Innovus:**

Total area of Standard cells: 7.569 um^2

Total area of Standard cells(Subtracting Physical Cells): 7.569 um^2

Total area of Macros: 0.000 um^2

Total area of Blockages: 0.000 um^2

Total area of Pad cells: 0.000 um^2

Total area of Core: 11.354 um^2

Total area of Chip: 564.732 um^2

Effective Utilization: 6.6667e-01

**POWER :**

Leakage Dynamic Total

Instance Cells Power(nW) Power(nW) Power(nW)

---------------------------------------------

xnorgate 2 18.018 186.241 204.259

**\*\*\* Innovus Statistics for net list xnorgate \*\*\***

Number of cells = 2

Number of nets = 4

Number of tri-nets = 0

Number of degen nets = 0

Number of pins = 10

Number of i/os = 3

Number of nets with 2 terms = 2 (50.0%)

Number of nets with 3 terms = 2 (50.0%)

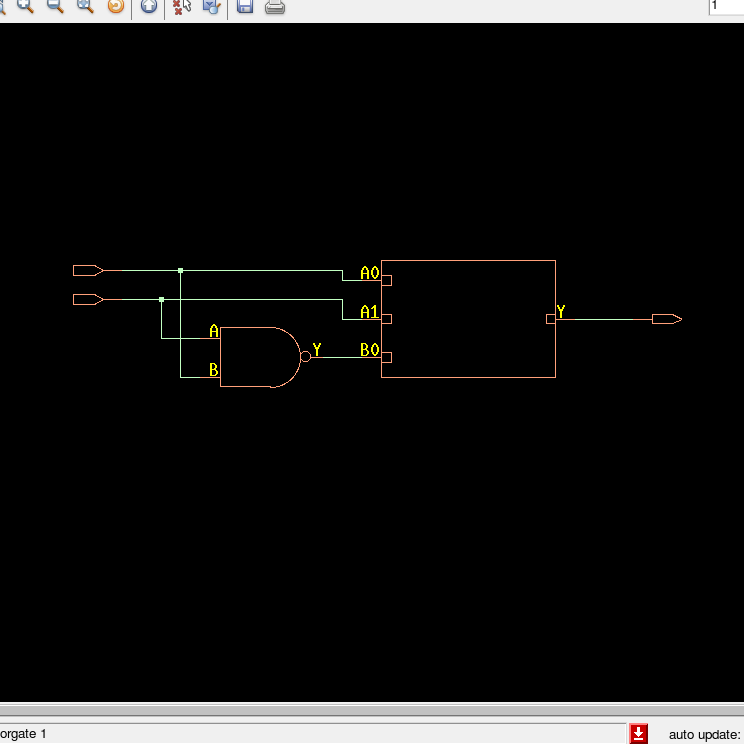
Number of nets with >=10 terms = 0 (0.0%)

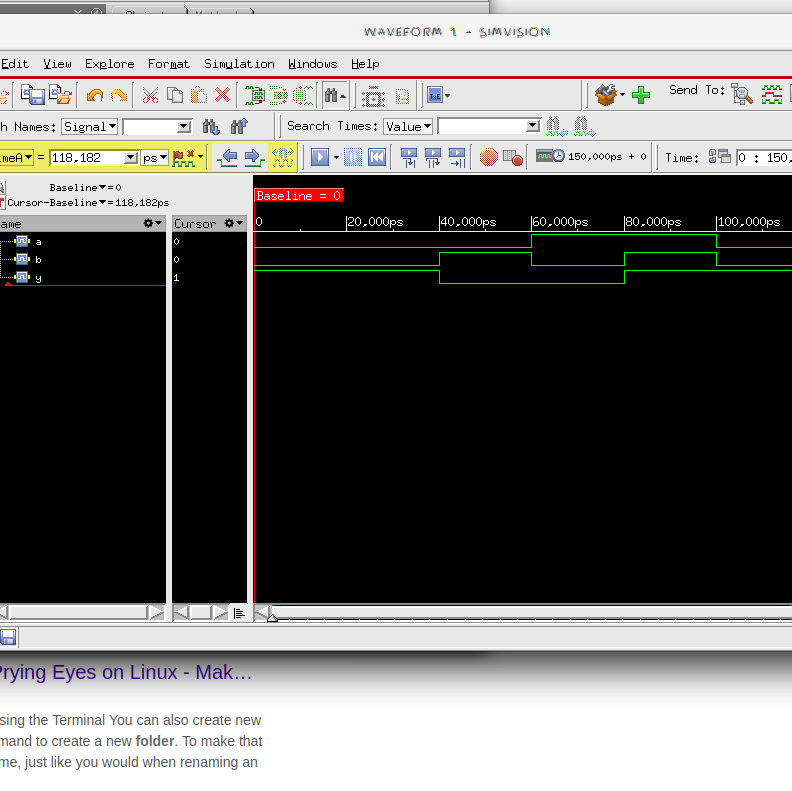
\*\*\* 2 Primitives used:

Primitive OAI21XL (1 insts)

Primitive NAND2XL (1 insts)

**GATE LEVEL DESIGN:**

****

****

**TIMING DIAGRAM:**

**EXPLANATION OF TIMING DIAGRAM:**

1. Till 40,000 us A = 0, B =0, so Y = 1

2. From 40,000 us to 60,000 us , A = 0, B=1, Y = 0

3. From 60,000 us to 80,000 us, A = 1, B = 0, Y = 0

4. From 80,000 us to 100,000 us, A = 1, B=1, Y = 1

COMBINATIONAL CIRCUITS:

QA.

GATE STATISTICS & AREA:

Gate Instances Area Library

---------------------------------

AO22X1 1 7.569 slow

---------------------------------

total 1 7.569

Type Instances Area Area %

--------------------------------------

logic 1 7.569 100.0

physical\_cells 0 0.000 0.0

--------------------------------------

total 1 7.569 100.0

**AREA from Innovus:**

Total area of Standard cells: 7.569 um^2

Total area of Standard cells(Subtracting Physical Cells): 7.569 um^2

Total area of Macros: 0.000 um^2

Total area of Blockages: 0.000 um^2

Total area of Pad cells: 0.000 um^2

Total area of Core: 11.354 um^2

Total area of Chip: 564.732 um^2

Effective Utilization: 6.6667e-01

POWER:

Leakage Dynamic Total

Instance Cells Power(nW) Power(nW) Power(nW)

----------------------------------------------

comb\_ckta 1 43.087 175.365 218.452

**\*\*\* Statistics for net list comb\_ckta \*\*\***

Number of cells = 1

Number of nets = 5

Number of tri-nets = 0

Number of degen nets = 0

Number of pins = 10

Number of i/os = 5

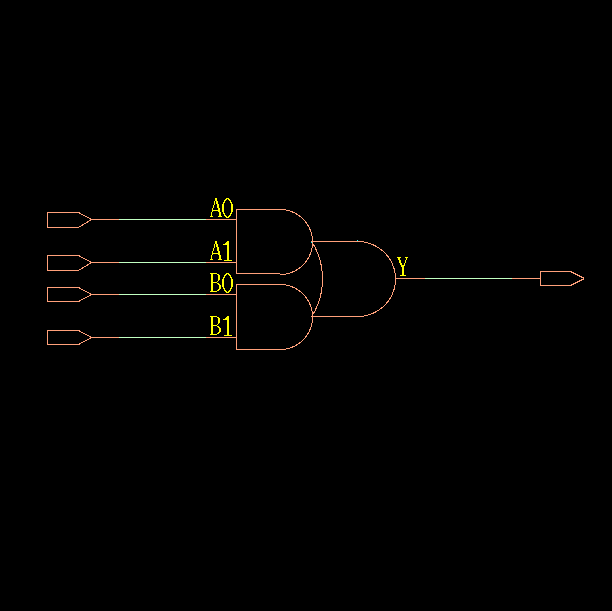
Number of nets with 2 terms = 5 (100.0%)

Number of nets with >=10 terms = 0 (0.0%)

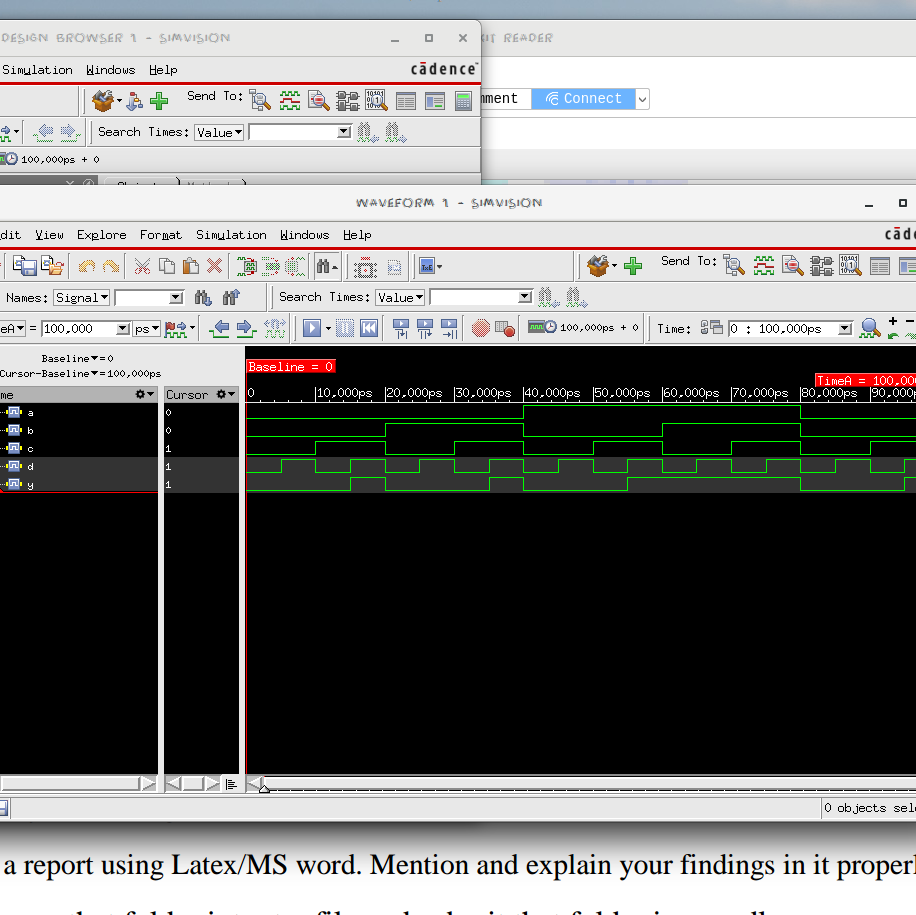
\*\*\* 1 Primitives used:

Primitive AO22X1 (1 insts)

GATE LEVEL DIAGRAM:



TIMING DIAGRAM:



EXPLANATION FOR TIMING DIAGRAM:

We generate all 16 possible combinations of A,B,C,D by toggling D every 5,000 us, B every 10,000 us, C every 20,000 us and D every 40,000 us. Y toggles every 20,000 us.

The output Y is given as per the truth table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | D | Y |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

QB.

GATE STATISTICS AND AREA:

Gate Instances Area Library

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AOI32XL 1 6.812 slow

NOR2BXL 1 4.541 slow

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total 2 11.354

Type Instances Area Area %

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logic 2 11.354 100.0

physical\_cells 0 0.000 0.0

---------------------------------------

total 2 11.354 100.0

**AREA from Innovus:**

Total area of Standard cells: 11.353 um^2

Total area of Standard cells(Subtracting Physical Cells): 11.353 um^2

Total area of Macros: 0.000 um^2

Total area of Blockages: 0.000 um^2

Total area of Pad cells: 0.000 um^2

Total area of Core: 16.652 um^2

Total area of Chip: 611.239 um^2

Effective Utilization: 6.8182e-01

**\*\*\* Statistics for net list comb\_cktb \*\*\***

Number of cells = 2

Number of nets = 8

Number of tri-nets = 0

Number of degen nets = 0

Number of pins = 16

Number of i/os = 7

Number of nets with 2 terms = 8 (100.0%)

Number of nets with >=10 terms = 0 (0.0%)

\*\*\* 2 Primitives used:

Primitive NOR2BXL (1 insts)

Primitive AOI32XL (1 insts)

POWER:

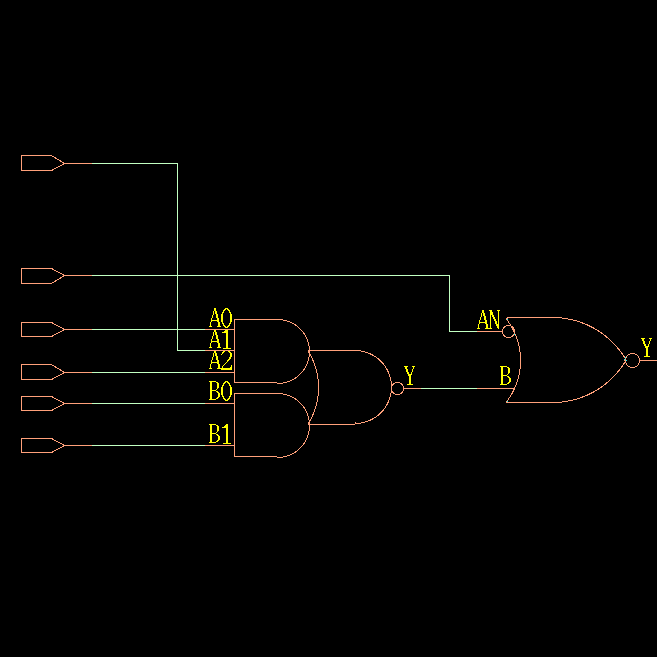
Leakage Dynamic Total

Instance Cells Power(nW) Power(nW) Power(nW)

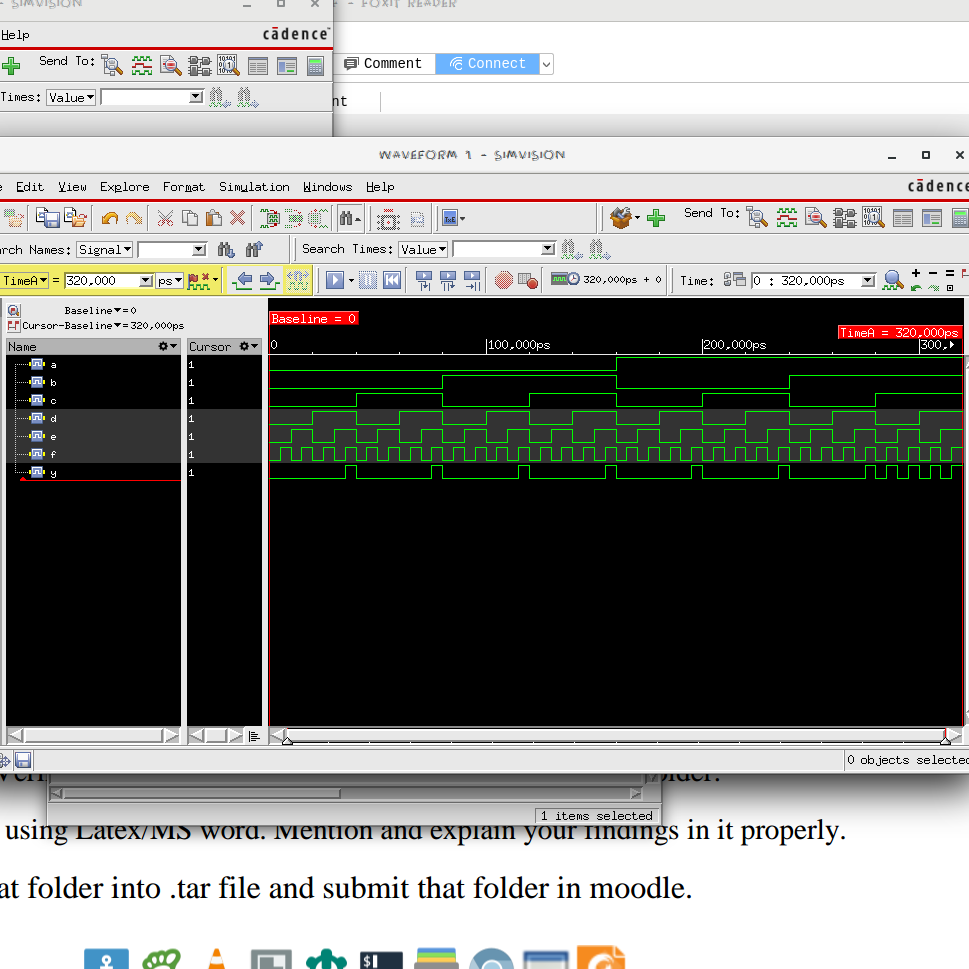
----------------------------------------------

comb\_cktb 2 28.902 296.661 325.562

GATE LEVEL DESIGN:



TIMING DIAGRAM:



EXPLANATION OF TIMING DIAGRAM:

We generate all 64 possible combinations of A,B,C,D,E and F by toggling F every 5,000 us, E every 10,000 us, D every 20,000 us, C every 40,000 us, B every 80,000 us and A every 160,000 us.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D | E | F | Y |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

QC.

GATE STATISTICS AND AREA:

Gate Instances Area Library

-----------------------------------

AND2X1 1 4.541 slow

INVXL 1 2.271 slow

OAI22XL 1 6.055 slow

-----------------------------------

total 3 12.867

Type Instances Area Area %

---------------------------------------

inverter 1 2.271 17.6

logic 2 10.597 82.4

physical\_cells 0 0.000 0.0

---------------------------------------

total 3 12.867 100.0

**AREA from Innovus:**

Total area of Standard cells: 12.867 um^2

Total area of Standard cells(Subtracting Physical Cells): 12.867 um^2

Total area of Macros: 0.000 um^2

Total area of Blockages: 0.000 um^2

Total area of Pad cells: 0.000 um^2

Total area of Core: 18.922 um^2

Total area of Chip: 631.171 um^2

Effective Utilization: 6.8000e-01

**\*\*\* Statistics for net list comb\_cktc \*\*\***

Number of cells = 3

Number of nets = 8

Number of tri-nets = 0

Number of degen nets = 0

Number of pins = 16

Number of i/os = 6

Number of nets with 2 terms = 8 (100.0%)

Number of nets with >=10 terms = 0 (0.0%)

\*\*\* 3 Primitives used:

Primitive OAI22XL (1 insts)

Primitive INVXL (1 insts)

Primitive AND2X1 (1 insts)

POWER:

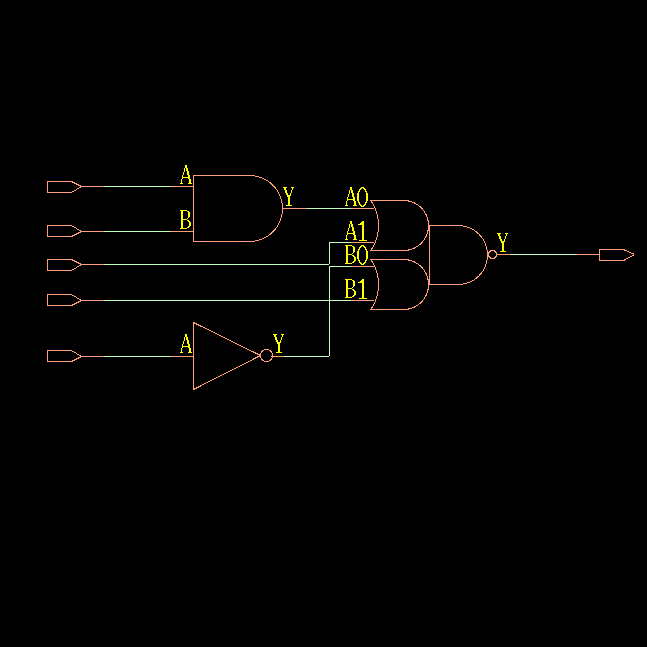
Leakage Dynamic Total

Instance Cells Power(nW) Power(nW) Power(nW)

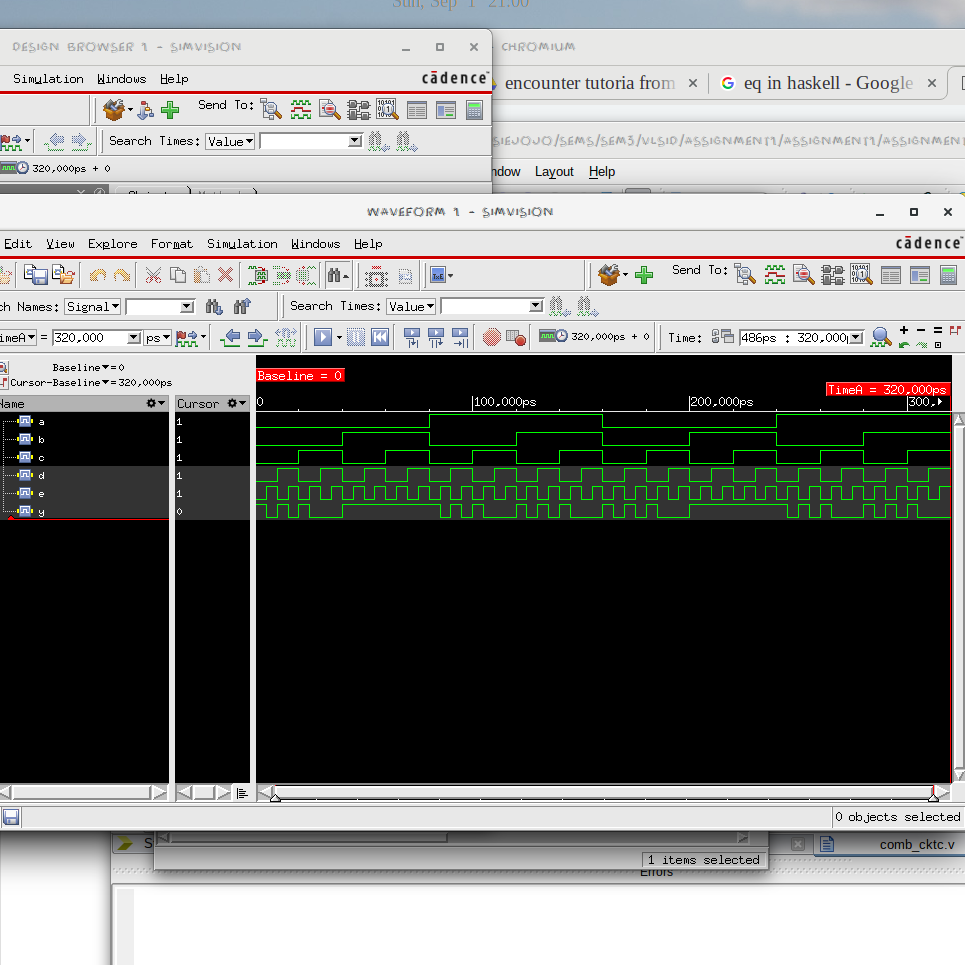
----------------------------------------------

comb\_cktc 3 47.977 319.757 367.735

GATE LEVEL DESIGN:



TIMING DIAGRAM:



EXPLANATION OF TIMING DIAGRAM:

We generate all 32 possible combinations of A,B,C,D and E by toggling E every 5,000 us, D every 10,000 us, C every 20,000 us, B every 40,000 us and A every 80,000 us.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A | B | C | D | E | Y |
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 |

**CONCLUSION:**

**Area Analysis:**

|  |  |
| --- | --- |
| **GATE** | **AREA (in um^2)** |
| ANDGATE | 4.5414 |
| ORGATE | 4.5414 |
| NOTGATE | 2.2707 |
| NORGATE | 3.0276 |
| NANDGATE | 3.0276 |
| XORGATE | 8.3259 |
| XNORGATE | 7.569 |
| COMBINATION CKT A | 7.569 |
| COMBINATION CKT B | 11.3535 |
| COMBINATION CKT C | 12.8673 |

* Clearly AND and OR gate have the same no of transistors (2 PMOS & 2 NMOS + Inverter ) so they have the same area.
* NOTGATE (1 PMOS & 1 NMOS) is clearly the smallest
* while NAND and NOR gate with 2 NMOS + 2 PMOS is smaller than AND and OR gate.
* XORGATE is bigger than XNORGATE as it has an extra inverter (4 NMOS+ 4 PMOS +inverter).
* CKTA has same area as XNORGATE, while CKTB and CKTC are clearly complexer and have higher area.
* CKTA is expected to be made of 4 NMOS & 4 PMOS, CKTB 6 NMOS + 6 PMOS and CKTC of 7 NMOS & 7 PMOS. ( if Complementary inputs available).
* CKTC has the highest area.

**Power Analysis:**

|  |  |
| --- | --- |
| **GATE** | **TOTAL POWER(in nW)** |
| ANDGATE | 112.983 |
| ORGATE | 135.769 |
| NOTGATE | 53.174 |
| NORGATE | 92.834 |
| NANDGATE | 69.083 |
| XORGATE | 340.607 |
| XNORGATE | 204.259 |
| COMBINATION CKT A | 218.452 |
| COMBINATION CKT B | 325.562 |
| COMBINATION CKT C | 367.735 |

* ANDGATE has the NMOS transistors in parallel while ORGATE has transistors in series. Clearly ORGATE has higher total power than ANDGATE.
* NOTGATE has the least total power.
* Similar to pt 1, NANDGATE has lower total power than NORGATE.
* The complexer the circuit, the more is the total power for them.
* Hence , CKTC has the highest power.

**Timing Analysis:**

The timing diagrams are as expected from the truth table.

The timing reports for PostCTS, PostRoute, PrePlace and PreCTS show 0 as all entries as there is no delay in the combinational circuits. WNS (Worst Negative Slack) and TNS (Total Negative Slack) for each circuit is 0.

**REFERENCES:**

1. Video uploaded on moodle by the TA.
2. <http://www.asic-world.com/>
3. <https://www.xilinx.com/products/design-tools/ise-design-suite.html>