Write the SystemC code and simulate for the following specification. Submit the codes as two '.h' files one '.cpp' file and one snapshot of the result.

- **Caution:** Do not copy from others, if found one who submit earliest will be evaluated and rest will not be evaluated and lab sessional marks would be 0.
- It will be evaluated on the basis of programming knowledge, proper indentation and appropriate comments, as well as result.
- Duration – 90 minutes

Specification:

Initially, the FSM shown below is in state ***S0***, waiting for the input request signal (***ri***)to be set. Once it is set, it will write the value in the input port into the register and transition to state ***S1***. In state ***S1***, the FSM sets the request signal (***r0***) for the output port, indicating that a value is written. From state ***S1***, three things can happen, depending on which handshake (input or output) completes first. If the input handshake completes (***ri*** falls low), the FSM goes to state ***S4***. If the output handshake responds (***a0*** raises high), the FSM goes to state ***S2***. If both handshakes complete at the same time, the FSM directly goes back to ***S0***.

Note: ***di*** and ***dout*** are 8-bit logic values, remaining all are 1-bit.