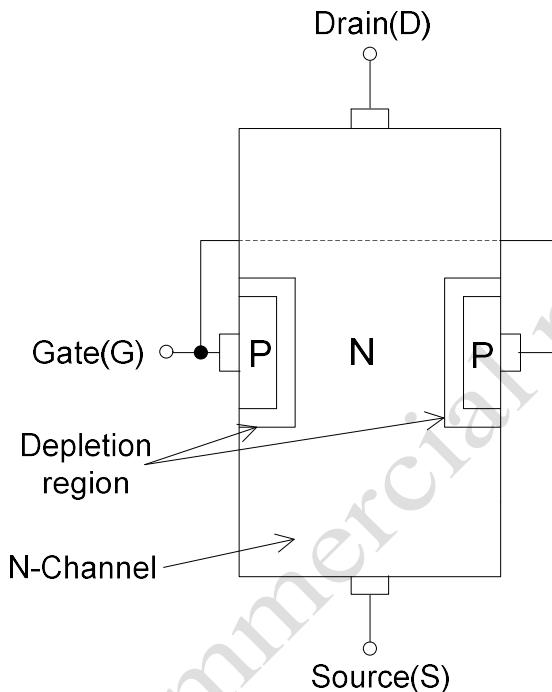


Module 1

Q1. Explain the construction and principle of operation of N-Channel and P-Channel Junction Field Effect Transistor (JFET).

Answer: N-Channel Junction Field Effect Transistor (JFET)

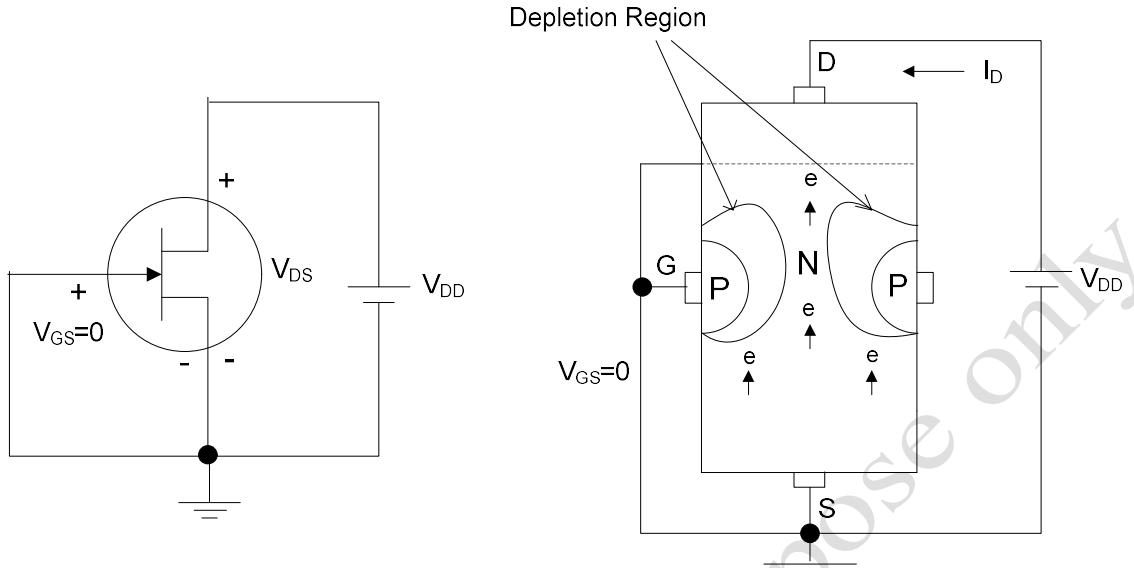
Construction:



The above figure shows the cross sectional view of the N-Channel JFET. P-type semiconductor material are embedded into the N-type semiconductor material as shown in the figure. N-type semiconductor material form a channel between embedded layers of P-type material. Two P-N junctions are formed. Contracts at the top and bottom are referred as Drain (D) and Source (S) respectively. Both the P-type are connected together to form Gate (G).

(Note: For P-Channel JFET, embedded material is N-type. Construction of P-Channel is left to you. In the remaining section, only N-Channel types are explained. P-channel types are left to you.)

Principle of Operation:



When a positive Drain (D)-Source (S) voltage (V_{DS}) is applied with Gate (G) shorted with the Source (S) terminal ($V_{GS}=0$), the electrons in the N-Channel are attracted to the Drain (D) terminal and due to the flow of electrons, Drain Current (I_D) is established. The value I_D depends on the applied V_{DS} and the resistance of the N-Channel. There is uniform voltage drop across the channel and the two P-N junctions are reverse biased. This results in increase of width of the depletion regions. The depletion regions are wider near the drain region.

I_D increases linearly with the increase of V_{DS} till saturation effect sets in. The value of V_{DS} where the saturation effect sets in is referred to as Pinch-Off (V_P) voltage. When V_{DS} reaches V_P , the value of I_D remains same with the further increase of V_{DS} .

The Gate-Source voltage (V_{GS}) is to control the value I_D . When a negative voltage is applied between Gate and Source terminals, there is an increase of width of the depletion layers and as a result the value of Drain Current (I_D) decreases. As the value V_{GS} is made further negative, at a certain value of negative V_{GS} , the Drain Current becomes zero. This voltage is referred as Gate-Source pinch-Off voltage.

The relation between the Drain Current, I_D for a given value of V_{GS} is given by

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

Where I_{DSS} is the Drain to Source Current when Gate is shorted with the Source.

V_P is the Pinch-Off voltage.

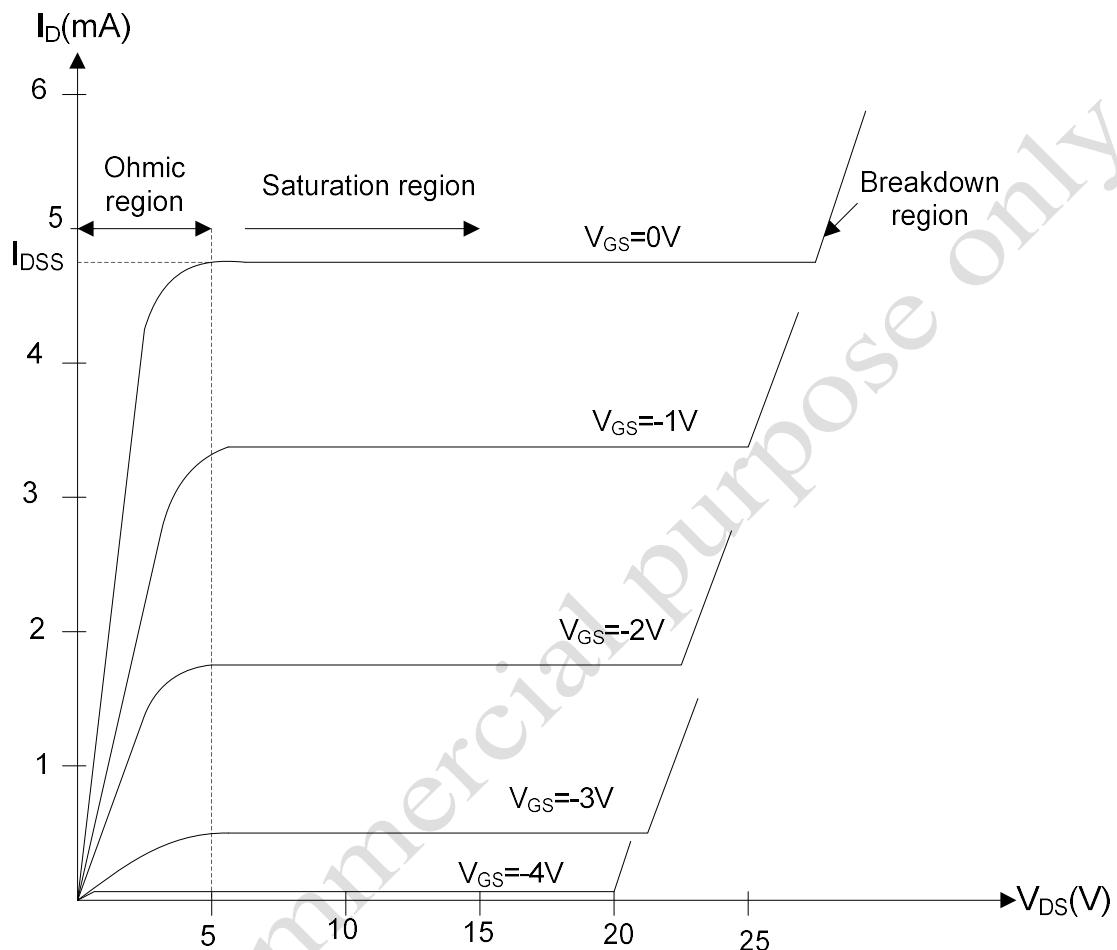
The drain resistance (r_d) in the saturation region is given by

$$r_d = \frac{r_0}{\left(1 - \frac{V_{GS}}{V_P} \right)^2} \quad \text{Where } r_0 \text{ is the resistance at } V_{GS}=0 \text{ and } V_P \text{ is the Pinch-Off voltage.}$$

Q2. Explain the Characteristics of N-Channel and P-Channel Junction Field Effect Transistor.

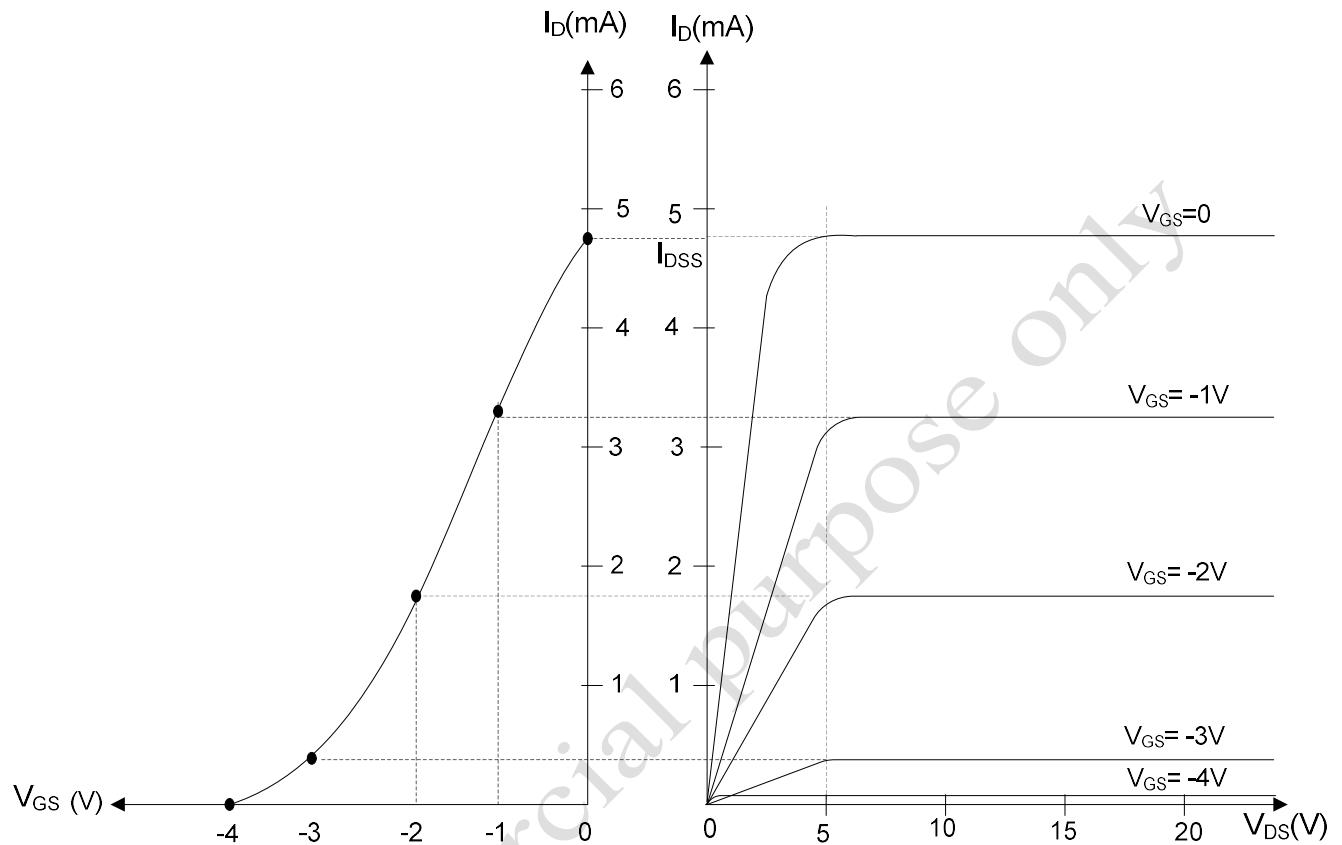
Answer: N-Channel Junction Field Effect Transistor (JFET)

Output Characteristic



The output characteristic of the N-Channel JFET is shown in the above diagram. Drain Current (I_D) is plotted against Drain-Source voltage (V_{DS}) keeping the Gate-Source voltage (V_{GS}) constant. As shown in the diagram, at lower value of Drain-Source voltage (V_{DS}), the Drain Current (I_D) is proportional Drain-Source voltage(V_{DS}) and it follows the Ohm's law. This region is referred as Ohmic region. As Drain-Source voltage (V_{DS}) increases further, at a certain value Drain Current (I_D) does not increase and this region as shown in the diagram is referred as Saturation region. If Drain-Source voltage(V_{DS}) is goes on increase, then after certain value of Drain-Source voltage(V_{DS}), the Drain Current (I_D) increases rapidly with small increase of Drain-Source voltage(V_{DS}) as shown in the diagram. This region is referred as breakdown region.

Transfer Characteristic



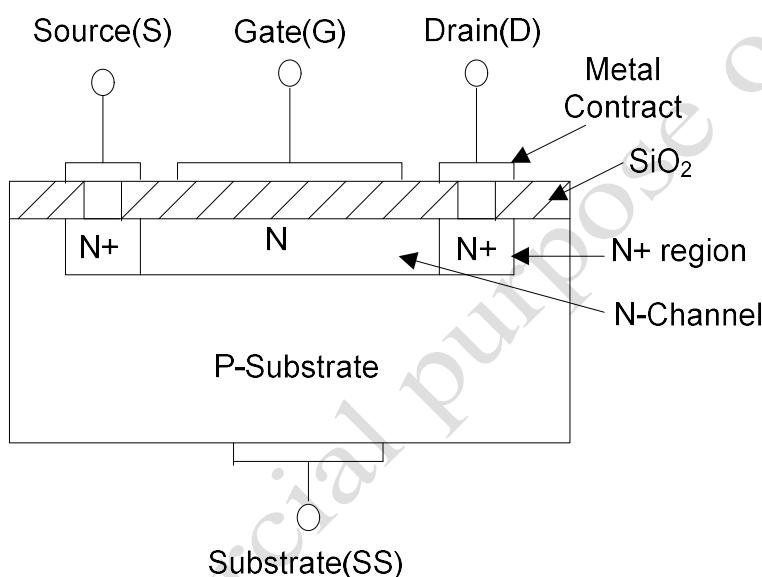
The transfer characteristic of the N-Channel JFET is shown in the above diagram. Drain Current (I_D) is plotted against Gate-Source voltage (V_{GS}) keeping the Drain-Source (V_{DS}) voltage constant.

Q3.Explain the construction and principle of operation of N-Channel and P-Channel Depletion Metal Oxide Semiconductor Field Effect Transistor (DE-MOSFET).

Answer: N-Channel Depletion Metal Oxide Semiconductor Field Effect Transistor (DE-MOSFET)

Construction:

Cross Section of an N-Channel DE-MOSFET



The above figure shows the construction of DE-MOSFET. It consists of a P-type substrate. Two N+ type regions linked by an N-channel are formed in the substrate. The source and the drain terminals are formed by connecting metal contacts to the two N+ regions. The gate terminal is connected to the insulating silicon dioxide (SiO₂) layer on the top of the N-channel. There is no direct connection between the gate terminal and the channel.

Principle of Operation:

When a positive voltage is applied between drain and source terminals (+V_{DS}), with gate shorted to the source (V_{GS}=0), then there is a flow of electrons towards drain terminal through N-channel as the electrons are attracted to the positive terminal at drain. This constitute Drain Current (I_D). The value of I_D increases with increase of V_{DS} up to a certain value of V_{DS}. After that value of V_{DS}, the I_D remain constant and this value is referred as I_{DSS} (Drain Current with Drain shorted with the source).

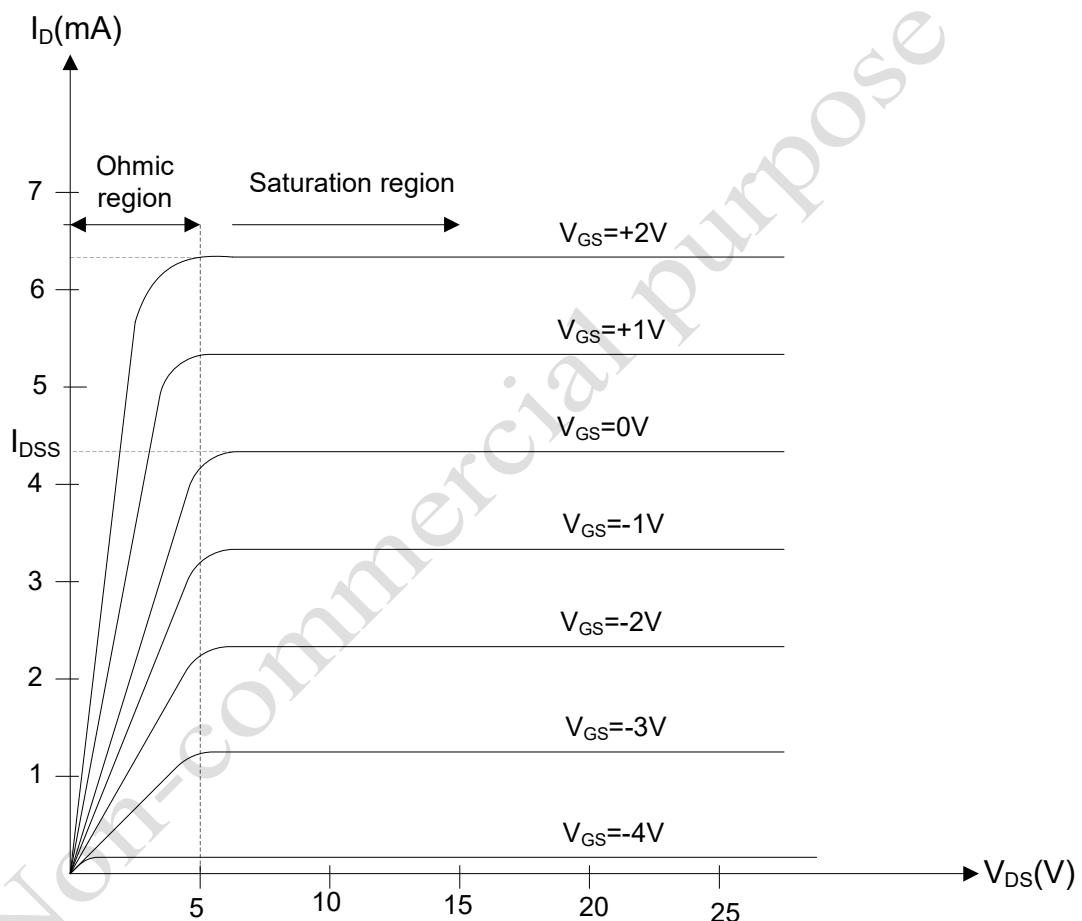
For positive gate to source voltage, the electrons (minority carrier) in the P-Substrate are attracted towards the gate terminal and concentration of electrons at the N-channel increases. As a result, the drain current increases. As the application of positive drain to source voltage

increases the drain current, the region of positive gate-source voltage is referred to as the enhancement region.

For negative gate to source voltage, the electrons in the N-channel are repelled towards the P-substrate and the concentration of electrons at the N-channel decreases. As a result, the drain current decreases. As the application of negative drain to source voltage decreases the drain current, the region of negative gate-source voltage is referred to as the depletion region. Therefore, gate to source voltage is used to control the gate current.

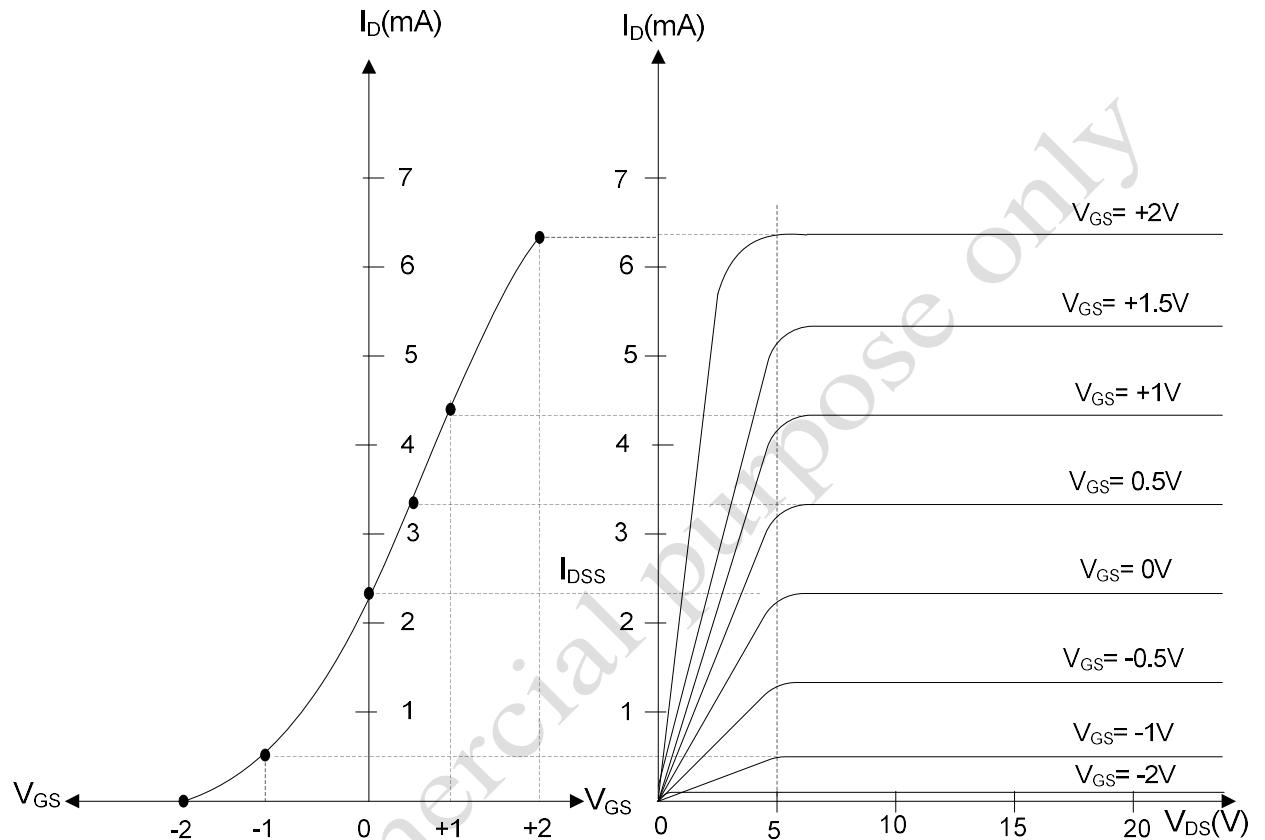
Q.4 Explain the characteristics of N-channel DE-MOSFET.

Answer: Output Characteristics of N-channel DE-MOSFET



The output characteristic of the N-Channel DE-MOSFET is shown in the above diagram. Drain Current (I_D) is plotted against Drain-Source voltage (V_{DS}) keeping the Gate-Source (V_{GS}) voltage constant. As shown in the diagram, at lower value of Drain-Source voltage (V_{DS}), the Drain Current (I_D) is proportional Drain-Source voltage(V_{DS}) and it follows the Ohm's law. This region is referred as Ohmic region. As Drain-Source voltage (V_{DS}) increases further, at a certain value Drain Current (I_D) does not increase and this region as shown in the diagram is referred as Saturation region.

Transfer Characteristics of N-channel DE-MOSFET



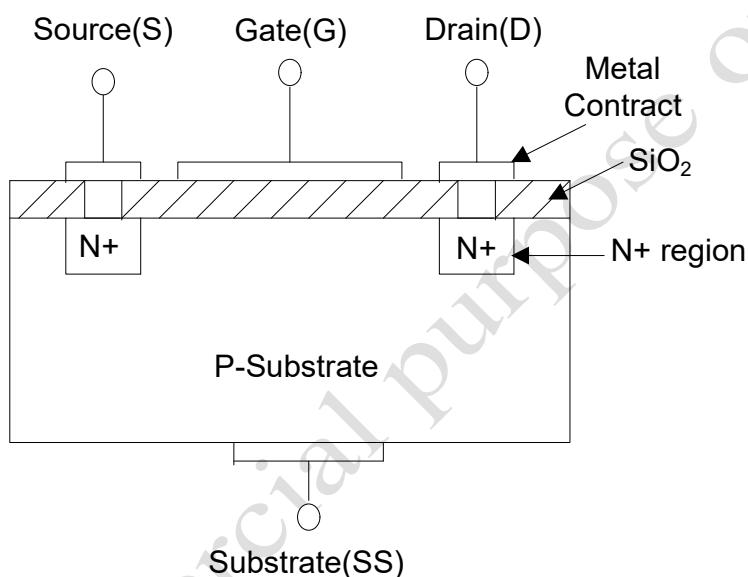
The transfer characteristic of the N-Channel DE-MOSFET is shown in the above diagram. Drain Current (I_D) is plotted against Gate-Source voltage (V_{GS}) keeping the Drain-Source (V_{DS}) voltage constant.

Q5.Explain the construction and principle of operation of N-Channel and P-Channel Enhancement Metal Oxide Semiconductor Field Effect Transistor (E-MOSFET).

Answer: N-Channel Enhancement Metal Oxide Semiconductor Field Effect Transistor (E-MOSFET)

Construction:

Cross Section of an N-Channel E-MOSFET



The above figure shows the construction of E-MOSFET. It consists of a P-type substrate. The source and the drain terminals are formed by connecting metal contacts to the two N^+ regions. The gate terminal is connected to the insulating silicon dioxide (SiO_2) layer . There is no direct connection between the gate terminal and the semiconductor.

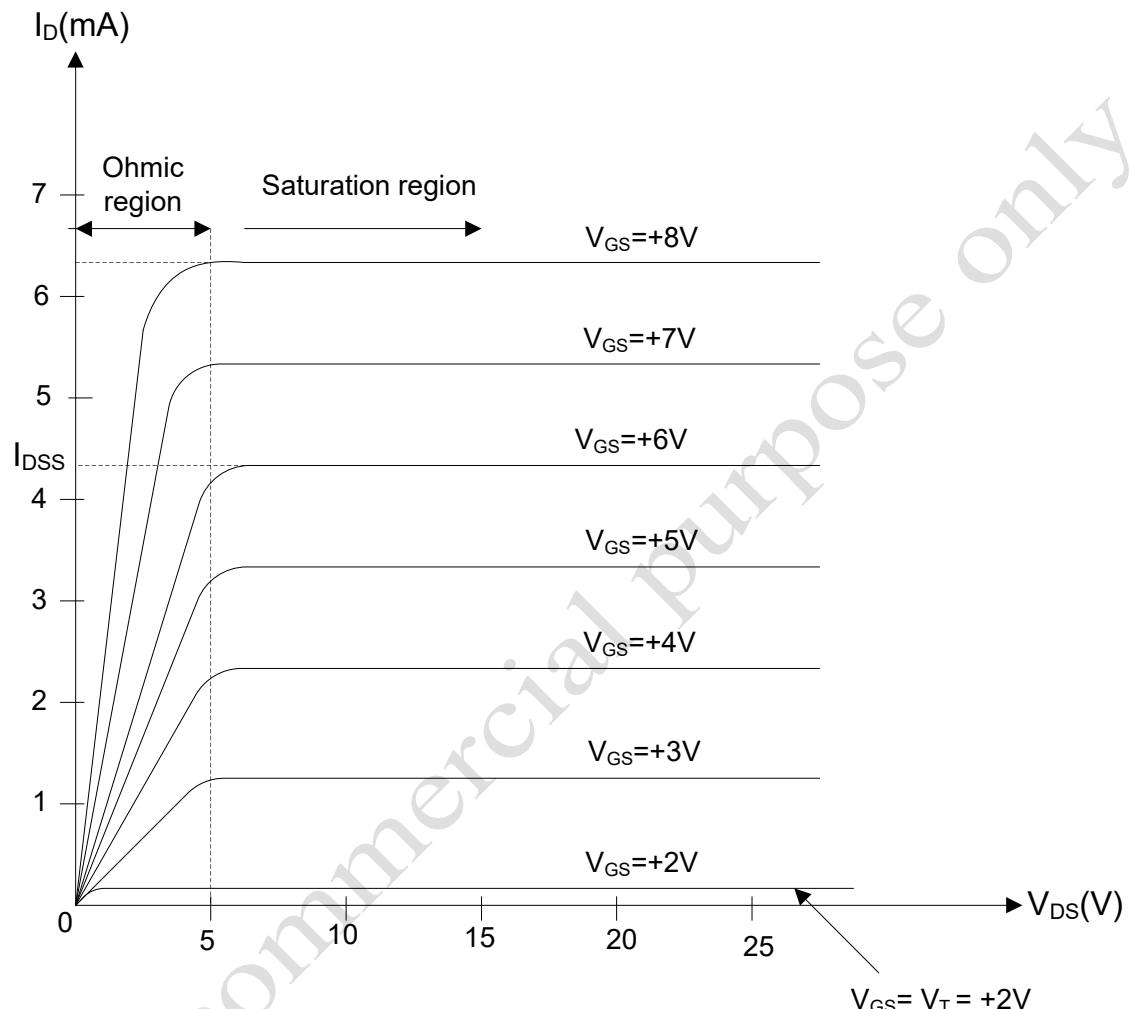
Principle of Operation:

When a positive voltage is applied between drain and source terminals ($+V_{DS}$), with gate shorted to the source ($V_{GS}=0$), then there is no flow of electrons towards drain terminal as N-channel is absent.

For positive gate to source voltage, the electrons (minority carrier) in the P-Substrate are attracted towards the gate terminal and concentration of electrons between the two N^+ region increases. As a result, the drain current starts only when sufficient gate to source is applied. The minimum gate to source voltage required for the significant starting drain current is referred as threshold voltage (V_T).

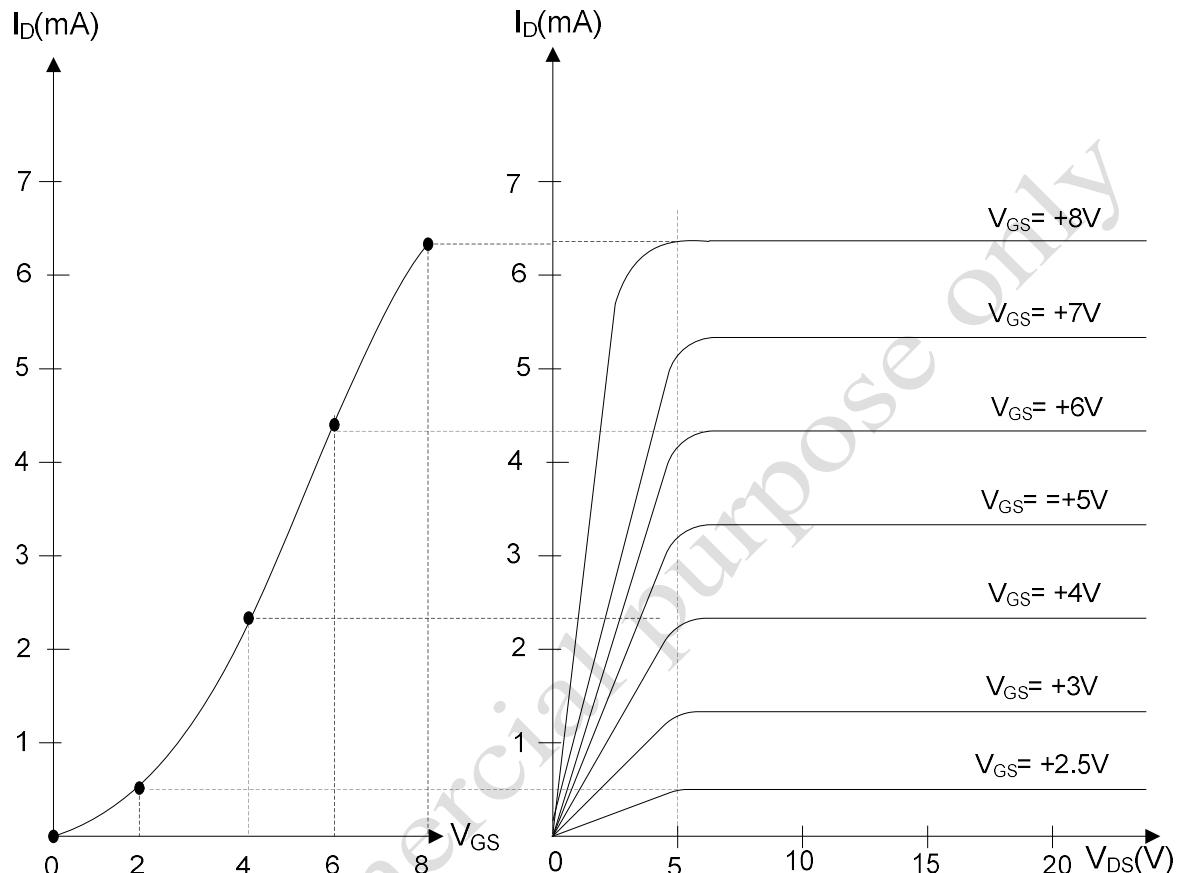
Q.6 Explain the characteristics of N-channel E-MOSFET.

Answer: Output Characteristics of N-channel E-MOSFET



The output characteristic of the N-Channel E-MOSFET is shown in the above diagram. Drain Current (I_D) is plotted against Drain-Source voltage (V_{DS}) keeping the Gate-Source (V_{GS}) voltage constant. As shown in the diagram, at lower value of Drain-Source voltage (V_{DS}), the Drain Current (I_D) is proportional Drain-Source voltage(V_{DS}) and it follows the Ohm's law. This region is referred as Ohmic region. As Drain-Source voltage (V_{DS}) increases further, at a certain value Drain Current (I_D) does not increase and this region as shown in the diagram is referred as Saturation region.

Transfer Characteristics of N-channel E-MOSFET



The transfer characteristic of the N-Channel E-MOSFET is shown in the above diagram. Drain Current (I_D) is plotted against Gate-Source voltage (V_{GS}) keeping the Drain-Source (V_{DS}) voltage constant.

Q7. Mention the difference between JFET and MOSFET,

Answer:

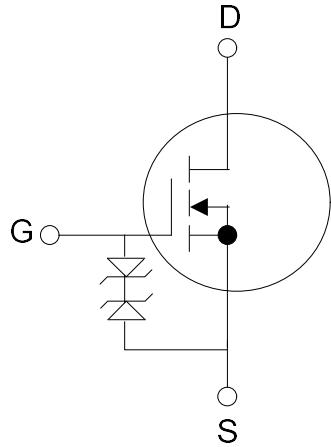
JFET	MOSFET
1. JFETs are operated in depletion mode only.	1. DE-MOSFET can be operated in both depletion and enhancement mode and E-MOSFET are operated in enhancement mode only.
2. Input resistance of JFET is around $10^9\Omega$.	2. Input resistance of MOSFET is much higher than JFET. Input resistance of MOSFET is around $10^{13}\Omega$.
3. Drain resistance of JFET is much higher than MOSFET. Drain resistance of JFET is in the range of $100\text{ K}\Omega$ to $1\text{ M}\Omega$.	3. Drain resistance of MOSFET is in the range of $1\text{ K}\Omega$ to $50\text{ K}\Omega$
4. Leakage gate current for JFET is much higher than MOSFET. Leakage gate current for JFET is in the range of $100\text{ }\mu\text{A}$ to 100nA .	4. Leakage gate current for MOSFET is smaller than JFET. Leakage gate current for MOSFET is in the range of 100nA to 10 pA .
5. Construction of JFETs are more difficult than MOSFET and JFET are less widely used than MOSFET.	Construction of MOSFET are easier than JFET and MOSFET are widely used than JFET.

Q8. Discuss about the handling of MOSFET.

Answer: Due to the presence of thin Silicon dioxide (SiO_2) layer in MOSFET, they are easily get damaged if not properly handled.

A person accumulates static charge from surrounding. When that person handles a MOSFET, that charge may create a potential difference across the SiO_2 layer and that potential difference may breakdown the insulation of SiO_2 layer.

An effective method to prevent MOSFET from damage is to connect Zener diodes back to back between the gate and the source terminal as shown in the figure below. Connecting Zener diodes back to back between the gate and the source terminal prevent the rise potential difference across Silicon dioxide(SiO_2) layer to a specified maximum limit.



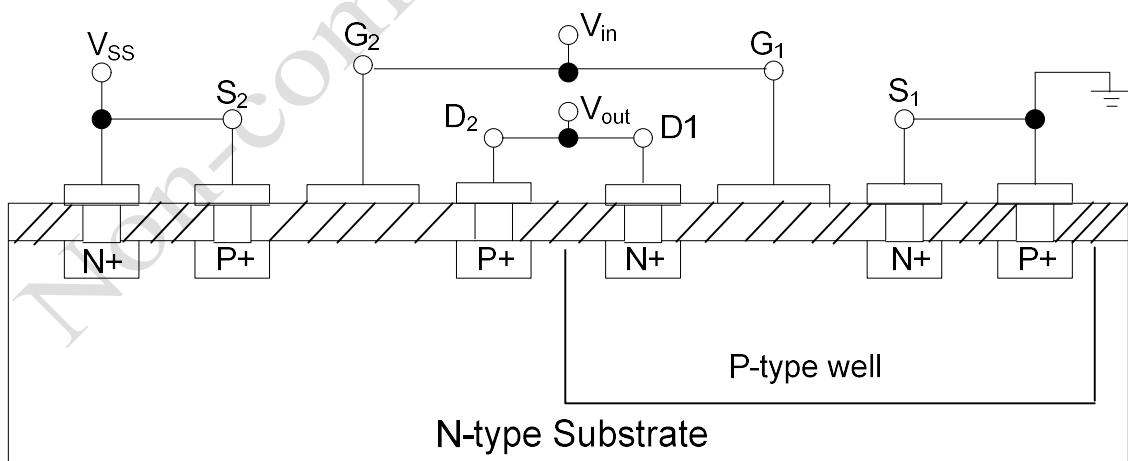
Q9. Discuss the application of Field Effect Transistors (FET).

Answer: Applications Field Effect Transistors (FET) are mentioned below:

- (i) Amplifiers: FET devices are commonly used as low-noise amplifiers and as buffer amplifiers.
- (ii) Analog Switch: FETs are used as analog switches.
- (iii) Multiplexer: FET devices are used in multiplexer circuits where each FET device acts as a single-pole single-throw switch.
- (iv) Current Limiters: FETs can be used as current limiter in an electronic circuit.
- (v) Voltage-variable resistors: FETs when operated in the ohmic region, acts as voltage-variable resistor.
- (vi) Oscillators: FETs are used in phase shift oscillators.

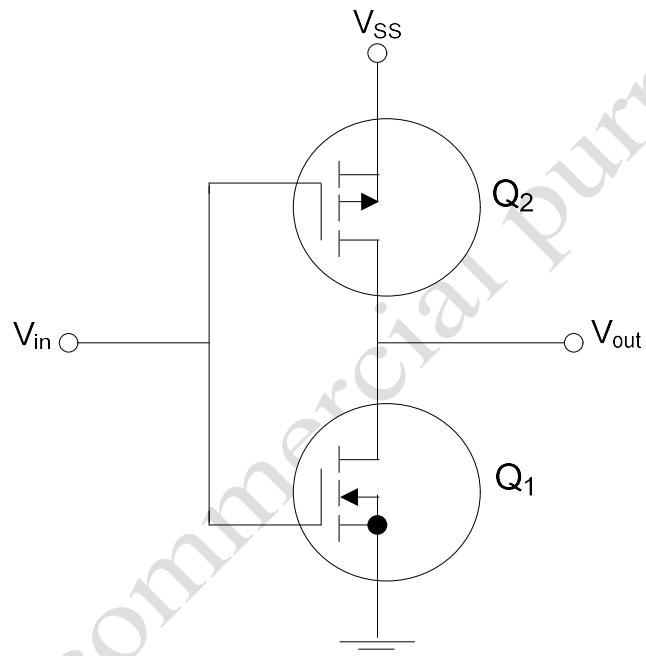
Q.10 Explain the working of CMOS inverter device.

Answer: Construction of CMOS Inverter



Complementary metal oxide semiconductor (CMOS) is those in which both P-type and N-type E-MOSFETs are diffused onto the same chip. The above figure shows the basic CMOS Inverter.

CMOS Inverter Circuit Diagram



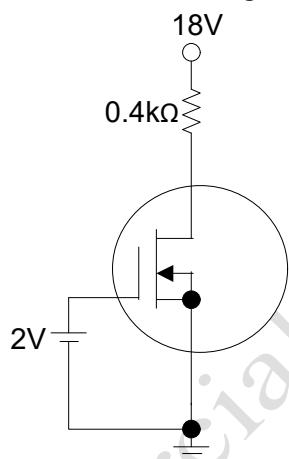
The basic inverter circuit using CMOS is shown above. Inverter is a logic circuit that inverts the applied input signal. The complementary N-type and P-type E-MOSFETs are connected in series with their gate terminals tied together to form input terminal. The drain terminals are connected together to form output terminal.

When the input voltage V_{in} is at logic LOW, the gate-source voltage of Q_2 (P-channel E-MOSFET) is $-V_{ss}$ which makes Q_2 in ON state resulting low resistance path between V_{ss} and V_{out} . The gate-source voltage for Q_1 (N-channel E-MOSFET) is zero which makes Q_1 is in OFF state resulting very high resistance between output terminal and ground. As a result the output voltage is equal to V_{ss} , that is, V_{out} is HIGH.

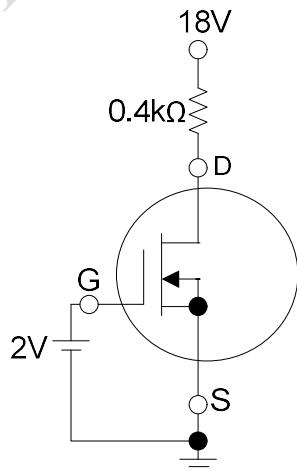
When the input voltage V_{in} is at logic HIGH, the gate-source voltage of Q_2 (P-channel E-MOSFET) is zero which makes Q_2 in OFF state resulting high resistance path between V_{ss} and V_{out} . The gate-source voltage for Q_1 (N-channel E-MOSFET) is HIGH which makes Q_1 is in

ON state resulting low resistance between output terminal and ground. As a result the output voltage , V_{out} is HIGH.

Q11. Figure below shows a biasing configuration using DE-MOSFET. Given that the saturation drain current is 8mA and the pinch-off voltage is -2V, determine the value of gate-source voltage, drain current and the drain-source voltage.



Answer: The figure below shows the circuit along with terminals.



From the above figure, Gate-source voltage (V_{GS}) is 2V.

$$\text{We know, in a DE-MOSFET, } I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

Here, given that $I_{DSS}=8\text{mA}$ and $V_P=-2\text{V}$

$$\text{Hence, } I_D = 8 \times 10^{-3} \times \left(1 - \frac{2}{-2}\right)^2 = 32 \times 10^{-3} = 32\text{mA}$$

Now, applying Kirchhoff's voltage law to output section, we have

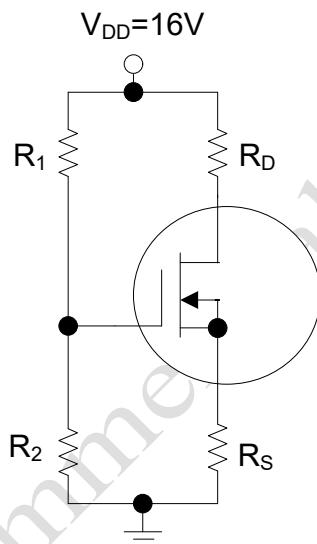
$$18 - 0.4 \times 10^3 \times 32 \times 10^{-3} - V_{DS} = 0$$

$$\Rightarrow V_{DS} = 5.2\text{V}$$

Therefore, Gate-source voltage=2V, Drain current=32mA and Drain-source voltage=5.2V

Q12. Design a voltage-divider-bias network using a DE-MOSFET with the supply voltage $V_{DD}=16\text{V}$, $I_{DSS}=10\text{mA}$ and $V_P = -5\text{V}$ to have a quiescent drain current of 5mA and gate voltage of 4V . (Assume the drain resistor R_D to be four times the source resistor R_S).

Answer: The following is a voltage divider bias network using DE-MOSFET.



Given $V_{DD}=16\text{V}$, Gate Voltage (V_G)=4V, Drain current (I_D)= 5mA , $I_{DSS}=10\text{mA}$ and $V_P = -5\text{V}$

As the quiescent drain current (I_D) is less than the saturation drain current (I_{DSS}), the MOSFET is operated in the depletion mode.

We know, in a DE-MOSFET,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \Rightarrow 5 \times 10^{-3} = 10 \times 10^{-3} \times \left[1 + \frac{V_{GS}}{5}\right]^2 \Rightarrow \left[1 + \frac{V_{GS}}{5}\right]^2 = 0.5$$

$$\Rightarrow 1 + \frac{V_{GS}}{5} = \pm \sqrt{0.5} \Rightarrow 1 + \frac{V_{GS}}{5} = 0.7 \text{ (Only +ve is considered, otherwise } V_{GS} \text{ will be large negative, less than } -V_P)$$

$$\Rightarrow V_{GS} = -1.5\text{V}$$

The gate-source voltage,

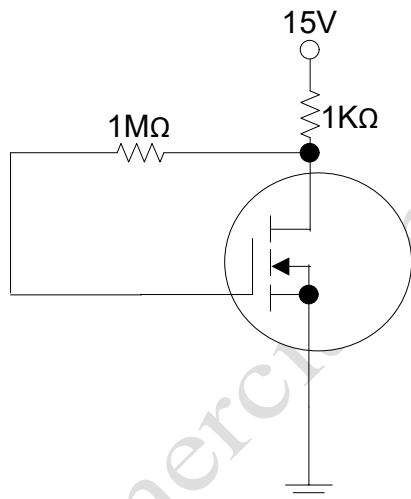
$$V_{GS} = V_G - V_S \Rightarrow V_{GS} = V_G - I_D R_S \Rightarrow -1.5 = 4 - 5 \times 10^{-3} \times R_S \Rightarrow R_S = 1.1 K\Omega$$

$$R_D = 4 \times R_S \text{ (Given)} \Rightarrow R_D = 4.4 K\Omega$$

Assume $R_2 = 1 K\Omega$

$$\text{Again, } V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} \Rightarrow 4 = \frac{1000}{R_1 + 1000} \times 16 \Rightarrow R_1 = 3000 \Omega = 3 K\Omega$$

Q13. Figure below shows a circuit using E-MOSFET. Given that the threshold voltage for the MOSFET is 2V and $I_{D(on)} = 6mA$ for $V_{GS(on)} = 5V$, determine the value of the operating point.



Answer: Drain current(I_D) in an E-MOSFET is given by

$$I_D = K(V_{GS} - V_T)^2 \Rightarrow 6 \times 10^{-3} = K(5-2)^2 \Rightarrow K = \frac{2}{3} \times 10^{-3} \text{ A/V}^2$$

$$V_{GS} = V_{DD} - I_D R_D \Rightarrow V_{GS} = 15 - I_D \times 1 \times 10^3 \Rightarrow V_{GS} = 15 - 1000I_D$$

$$\text{Now, } I_D = K(V_{GS} - V_T)^2 \Rightarrow I_D = \frac{2}{3} \times 10^{-3} (15 - 1000I_D - 2)^2 \Rightarrow 1500I_D = (13 - 1000I_D)^2$$

$$\Rightarrow 1500I_D = 169 - 26000I_D + 10^6 I_D$$

$$\Rightarrow 10^6 I_D - 27500I_D + 169 = 0$$

$$\Rightarrow I_D = \frac{27500 \pm \sqrt{(27500)^2 - 4 \times 10^6 \times 169}}{2 \times 10^6}$$

$$\Rightarrow I_D = \frac{27500 \pm \sqrt{80250000}}{2 \times 10^6} = \frac{27500 \pm 8958.24}{2 \times 10^6} = 9.27 \text{ mA or } 18.23 \text{ mA}$$

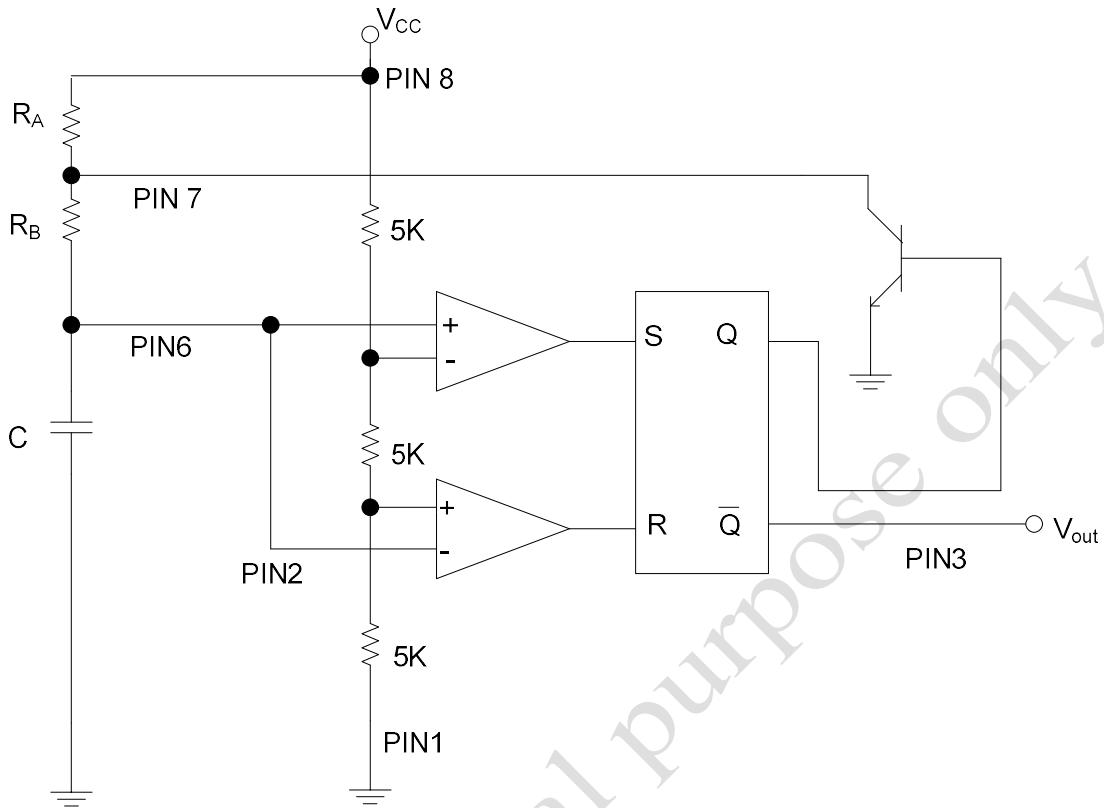
For $I_D = 9.27 \text{ mA}$, $V_{GS} = 15 - 1000I_D = 15 - 1000 \times 9.27 \times 10^{-3} = 5.73 \text{ V}$ which is selected

For $I_D = 18.23 \text{ mA}$, $V_{GS} = 15 - 1000I_D = 15 - 1000 \times 18.23 \times 10^{-3} = -3.23 \text{ V}$ which is rejected since V_{GS} should be positive and more than threshold voltage for E-MOSFET

Therefore, the operating point is (9.27mA, 5.73V)

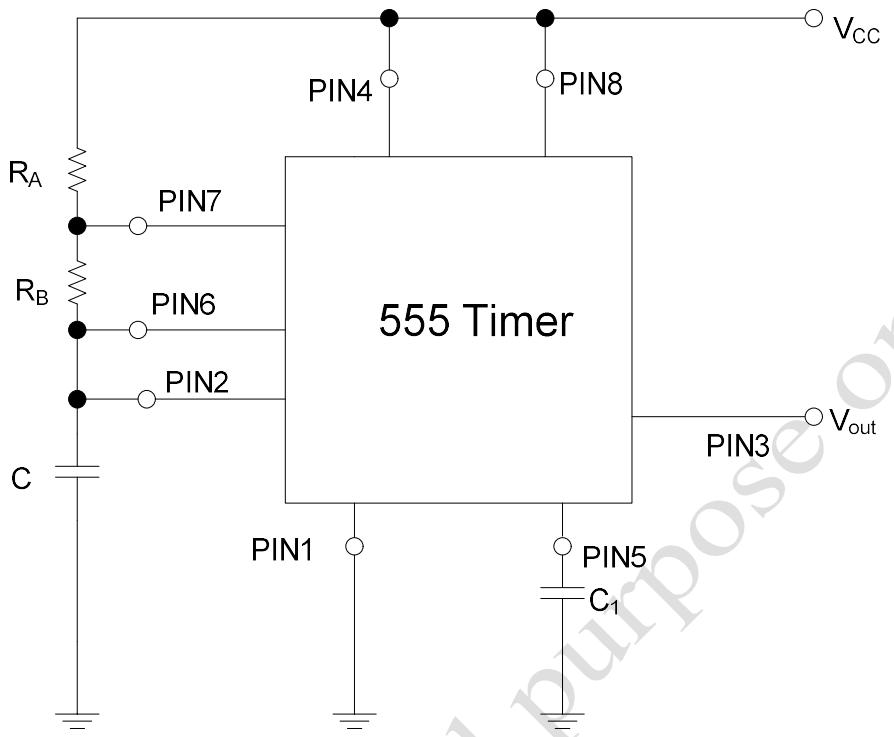
Q14. Explain the Astable Operation of multivibrator using 555 Timer IC.

Answer: The following figure shows the 555 Timer connected for astable operation.

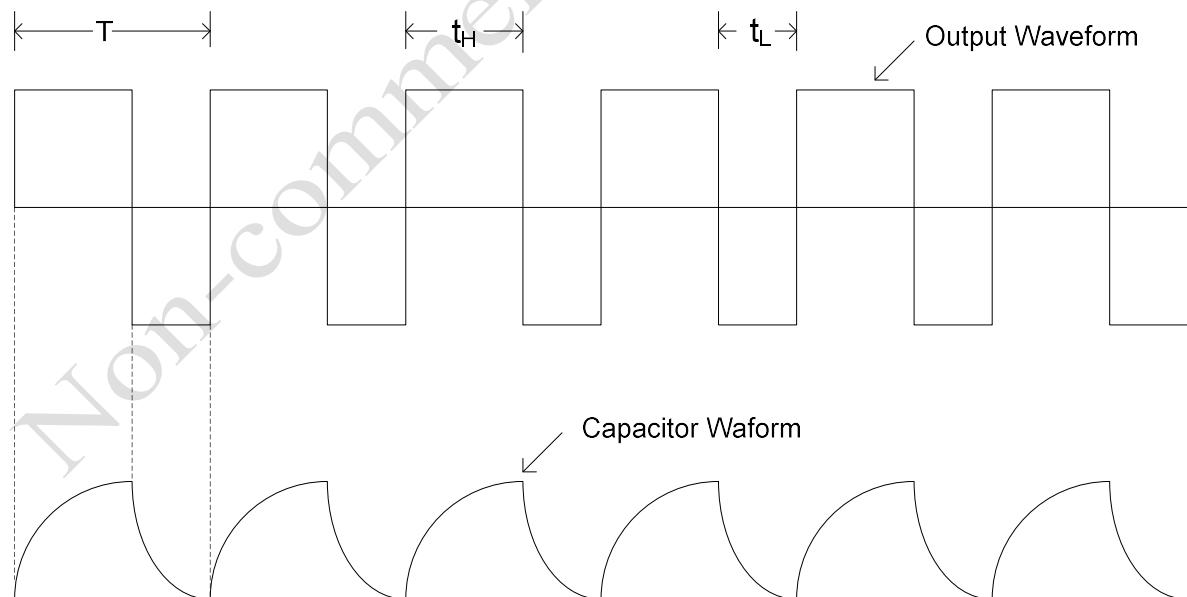


As shown in the figure, the 555 Timer contains a voltage divider, two comparators, an RS flip flop, and an npn transistor. Since the voltage divider has equal resistors, the top comparator has a trip point of $UTP = \frac{2V_{CC}}{3}$ and the lower comparator has a trip point of $LTP = \frac{V_{CC}}{3}$. The Pin 6 is connected to the upper comparator. The voltage on the pin 6 is called threshold voltage. Initially, the Q output of the RS flip-flop is LOW and V_{out} is HIGH. The transistor is in CUT OFF and there is no collector current through R_A . This makes the capacitor to start charging from V_{CC} . As the capacitor plate voltage starts rising and reaches $UTP = \frac{2V_{CC}}{3}$, trip occurs and the output of the upper comparator SET the RS flip-flop. At this point, Q the output of RS flip is HIGH and V_{out} is LOW. This forces the transistor in saturation and saturated current flows through the collector resistor R_A and the capacitor stop charging. The capacitor start discharge through R_B and the transistor. When the capacitor voltage falls and reaches $LTP = \frac{V_{CC}}{3}$, trip occurs and the output of the lower comparator RESET the RS flip-flop. At this point, Q the output of RS flip is LOW and V_{out} is HIGH. This process repeats. V_{out} remains HIGH while capacitor charges and remains LOW while capacitor discharges.

The following figure shows the block diagram of 555 Timer connected for astable operation.

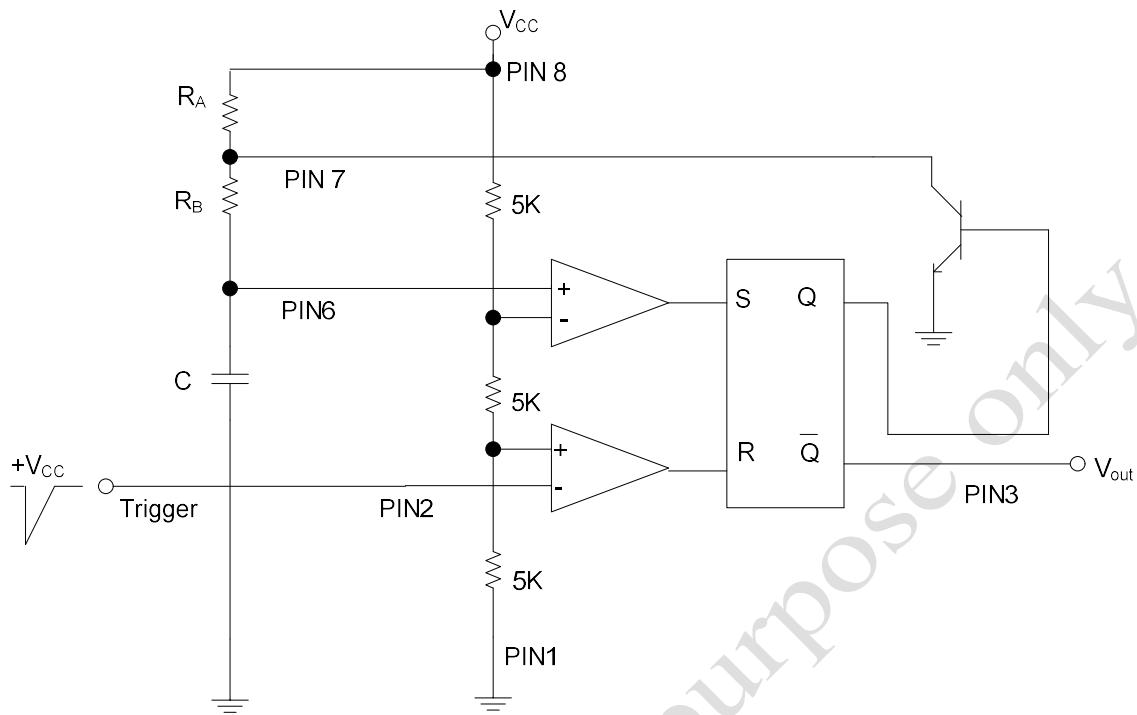


The following figure shows output waveform and the capacitor waveform.



Q15. Explain the Monostable Operation of multivibrator using 555 Timer IC.

Answer: The following figure shows the 555 Timer connected for monostable operation.

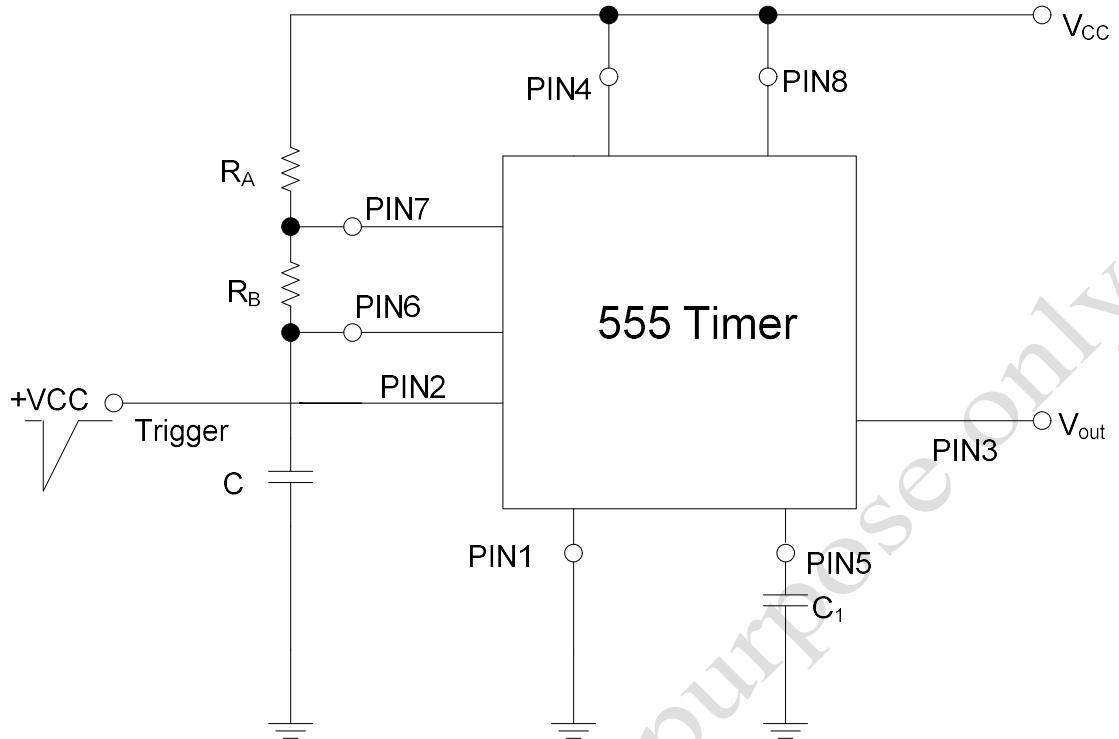


As shown in the figure, the 555 Timer contains a voltage divider, two comparators, an RS flip flop, and an npn transistor. Since the voltage divider has equal resistors, the top comparator has a trip point of $UTP = \frac{2V_{CC}}{3}$ and the lower comparator has a trip point of $LTP = \frac{V_{CC}}{3}$.

Initially, the Q output of the RS flip-flop is HIGH and V_{out} is LOW. This saturates the transistor and capacitor is at ground. This circuit remains in this stage until a trigger arrives.

When the trigger input falls less than $V_{CC}/3$, the lower comparator reset the flip-flop and the Q output of the flip-flop changes to LOW, the transistor goes to cut off, allowing the capacitor to charge. At this point, V_{out} is HIGH. The capacitor charges and when the capacitor voltage reaches $2V_{CC}/3$, the upper comparator sets the flip-flop. The Q output of the flip-flop changes to HIGH and turns on the transistor. The capacitor starts discharging through the transistor. At this point, V_{out} is LOW. Therefore, the V_{out} remains HIGH only for the period while capacitor charges after a trigger is made. V_{out} again comes back to LOW until another trigger is made.

The following figure shows the block diagram of 555 Timer connected for monostable operation.



Q16. Discuss the Ideal Opamp versus practical Opamp.

Answer: The following is the comparison between Ideal Opamp and Practical Opamp

Ideal Opamp	Practical Opamp
Internal Impedance is infinite	Input Impedance range 100KΩ to 1000MΩ
Output Impedance is zero	Output impedance range from 10Ω to 100Ω
Open loop differential voltage gain is infinite	Open loop gain is in the range of 10,000 to 100,000
Bandwidth is infinite	Bandwidth is limited.
DC input and output offset voltage is zero	Finite DC input and output offset voltage
Input differential voltage is zero	Finite differential voltage is finite

Q17. Discuss the performance parameters of operational amplifier.

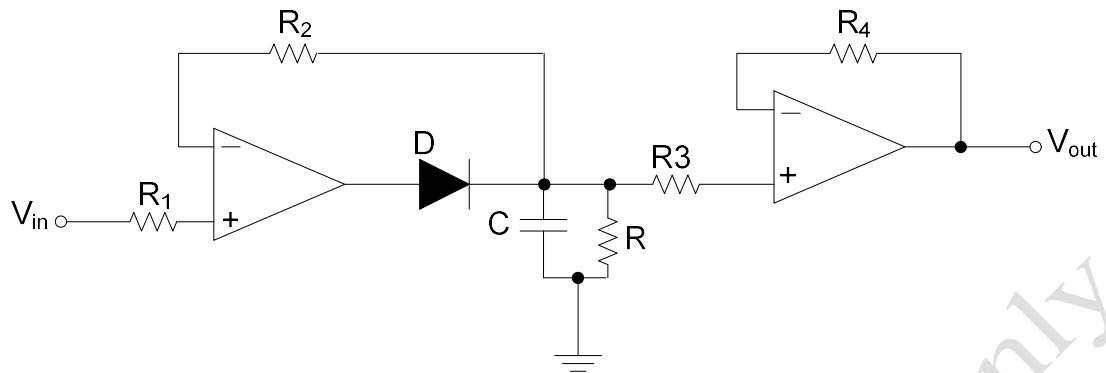
Answer: The following are the performance parameters of operational amplifier:

- (i) Bandwidth: Bandwidth of operational amplifier is the range frequencies it can amplify for a given amplifier gain.

- (ii) Slew rate: It is defined as the rate of change of output voltage time. It gives the idea as to how well the opamp output follows a rapidly changing waveform at the input.
- (iii) Open-Loop Gain: Open-loop gain is the ratio of single-ended output to the differential input.
- (iv) Common Mode Rejection Ratio (CMRR): It is the ratio of the desired differential gain (A_d) to the undesired common mode gain(A_c). CMRR is a measure of the ability of the opamp to suppress common mode signal. The ratio of CMRR is usually expressed $20\log(A_d/A_c)$ dB.
- (v) Power Supply rejection Ratio (PSRR): PSRR is defined as the ratio of change in the power supply voltage to corresponding change output voltage. PSRR is also defined as the ratio of change in one of the power supply voltage to the change in the input offset voltage with the other power supply voltage held constant.
- (vi) Input Impedance: Input Impedance is the impedance looking into the input terminals of the opamp and mostly expressed in terms of resistance only.
- (vii) Output Impedance: Output Impedance is defined as the impedance between the output terminal of the opamp and the ground.
- (viii) Settling Time: Settling Time is expressed as the time taken by the opamp output to settle within a specified percentage of the final value in response to a step input. It gives the response of the opamp to large step input.
- (ix) Offset and Offset Drifts: An ideal opamp should produce a zero output for a zero differential input. But it is not so in the case of practical opamps. It is observed that a DC differential voltage is to be applied externally to get a zero output. This externally applied input is referred to as the input offset voltage. Output offset voltage is the voltage at the output with the both input terminals grounded. Input offset current is the difference between the two bias current flowing towards the inputs of the opamp. Input bias current defined as the average of the two bias currents flowing into the two input terminals of the opamp.

Q18. Explain the Peak Detector Circuit.

Answer: The following is the circuit diagram for a Peak Detector Circuit:



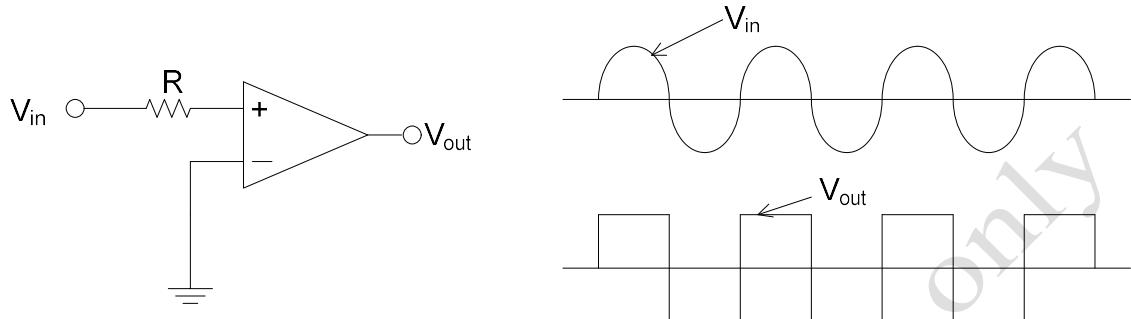
Peak detector circuit produces a voltage at the output equal to peak amplitude of the input signal. During the positive half cycle, the diode D is forward biased. The capacitor charges rapidly to the peak from the output of the opamp. As the input starts decreasing beyond the peak, the diode gets reversed biased, thus isolating the capacitor from the output of the opamp. The capacitor can now discharge only through resistor (R) connected across it. The value of R is much large. The purpose of the resistor is to allow a discharge path so that output can respond to changing amplitudes of the signal peak. The buffer circuit connected ahead of the capacitor prevents any discharge of the capacitor. The capacitor voltage, that is, the peak of the input is the output voltage.

Q19. Explain the following comparators:

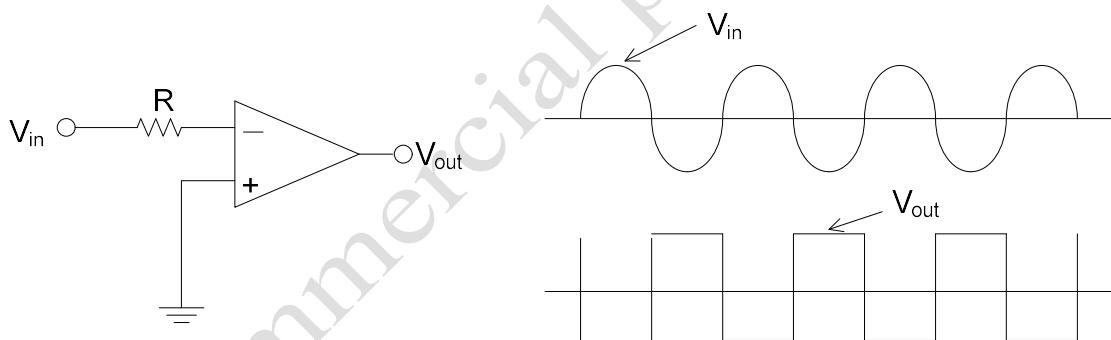
- (a) Zero crossing detector
- (b) Comparator with reference
- (c) Comparator with hysteresis
- (d) Window comparator

Answer: (a) The following is the circuit diagram and waveform of the Zero crossing detector.

Non-Inverting zero crossing detector



Inverting zero crossing detector

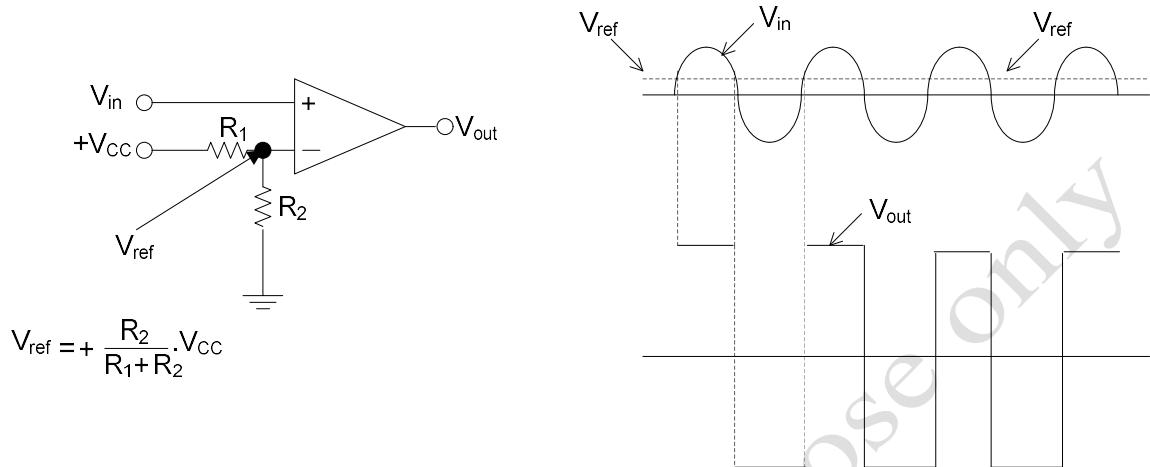


Non-Inverting Zero Crossing Detector: As shown in waveform, output (V_{out}) of the operational amplifier is $+V_{sat}$ during the positive half cycle. As the input wave crosses zero voltage, the output (V_{out}) changes from $+V_{sat}$ to $-V_{sat}$. That is, output (V_{out}) of the operational amplifier is $-V_{sat}$ during the negative half cycle.

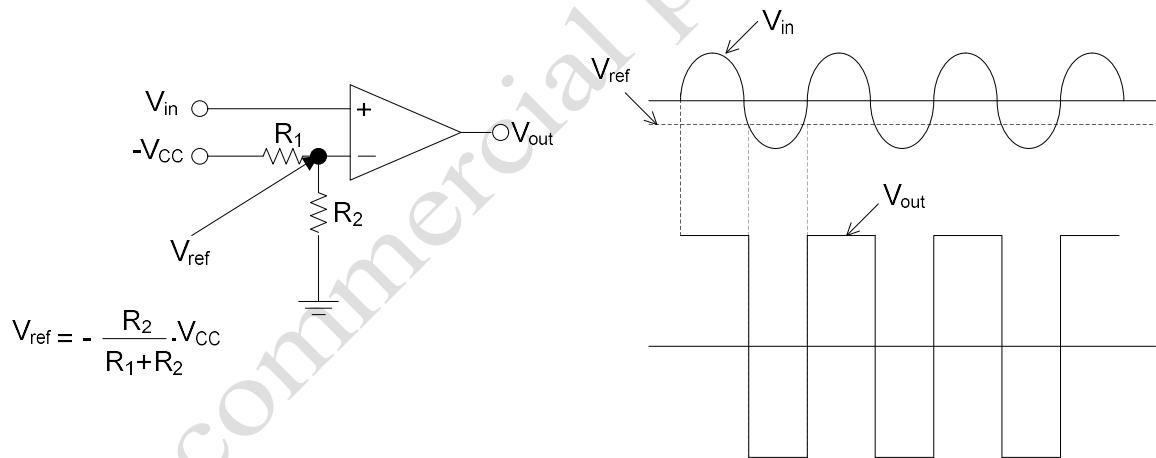
Inverting Zero Crossing Detector: As shown in waveform, output (V_{out}) of the operational amplifier is $-V_{sat}$ during the positive half cycle. As the input wave crosses zero voltage, the output (V_{out}) changes from $-V_{sat}$ to $+V_{sat}$. That is, output (V_{out}) of the operational amplifier is $+V_{sat}$ during the negative half cycle.

(b) The following is the circuit diagram and waveform of the comparator with reference.

Non-Inverting comparator with positive reference



Non-Inverting comparator with negative reference



Non-inverting comparator with positive reference:

The potential at non-inverting terminal is $V_{ref} = + \frac{R_2}{R_1 + R_2} \cdot V_{CC}$

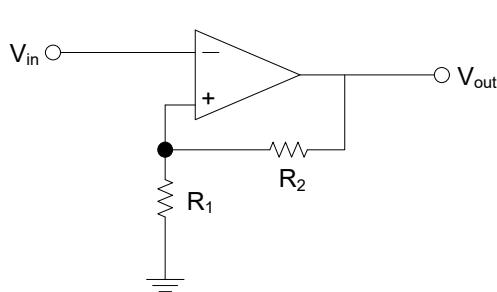
If $V_{in} > V_{ref}$, the output $V_{out} = +V_{sat}$ and If $V_{in} < V_{ref}$, the output $V_{out} = -V_{sat}$

Non-inverting comparator with negative reference:

The potential at non-inverting terminal is $V_{ref} = - \frac{R_2}{R_1 + R_2} \cdot V_{CC}$

If $V_{in} > V_{ref}$, the output $V_{out} = +V_{sat}$ and If $V_{in} < V_{ref}$, the output $V_{out} = -V_{sat}$

(c) Following is the circuit diagram and waveform of comparator with hysteresis:

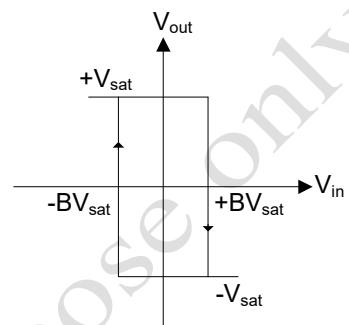


$$B = \frac{R_1}{R_1 + R_2}$$

$$UTP = +BV_{sat}$$

$$LTP = -BV_{sat}$$

$$H = 2BV_{sat}$$

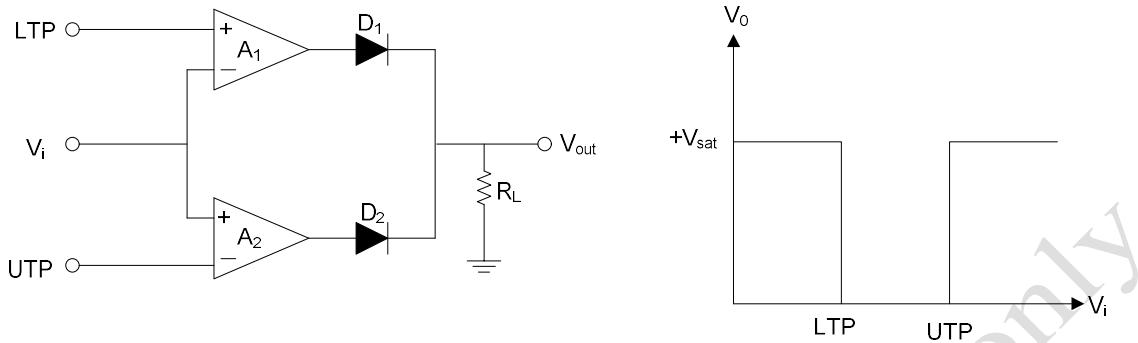


Let us assume $V_{out} = +V_{sat}$, then voltage at non-inverting terminal is $UTP = \frac{R_1}{R_1 + R_2} \cdot V_{CC}$

When the input signal (V_{in}) exceeds this voltage, the output $V_{out} = -V_{sat}$. Then then voltage at non-inverting terminal is $LTP = -\frac{R_1}{R_1 + R_2} \cdot V_{CC}$

When the input signal (V_{in}) goes below this voltage, the output $V_{out} = +V_{sat}$. Then then voltage at non-inverting terminal is $UTP = +\frac{R_1}{R_1 + R_2} \cdot V_{CC}$ again

(d) Following is the circuit diagram and waveform for window comparator:



In a window comparator, there are two reference voltages called lower trip point (LTP) and upper trip point (UTP).

When the input voltage is less than the lower trip point (LTP), the output of the upper operational amplifier (A₁) is $+V_{sat}$ and the output of the lower operational amplifier (A₂) is $-V_{sat}$. Therefore, diode D₁ is forward biased and the diode D₂ is reversed biased. As a result, the output across R_L is $V_{out}=+V_{sat}$.

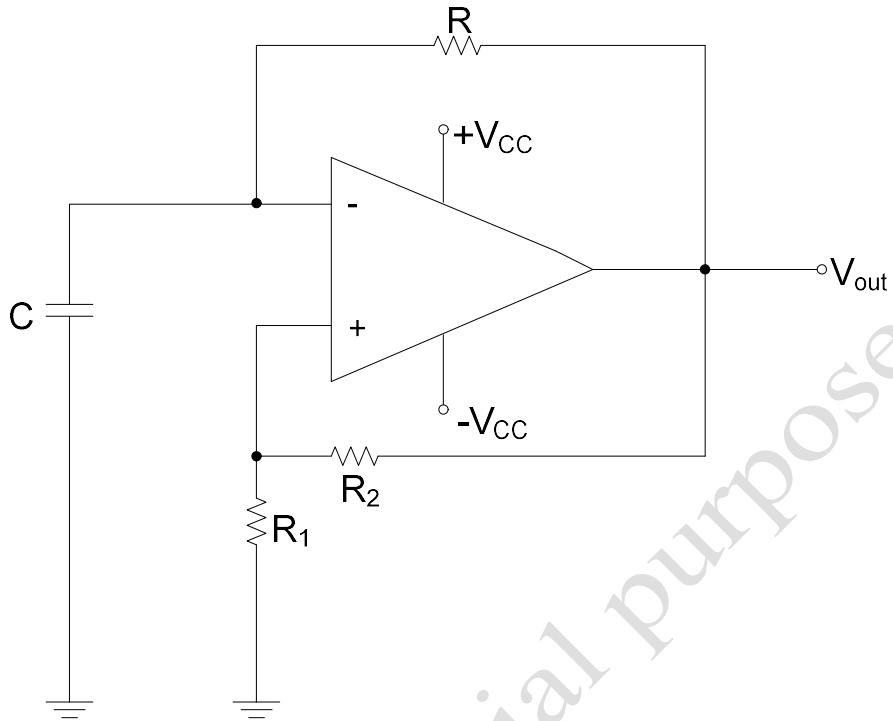
When the input voltage is greater than upper trip point (UTP), the output of the upper operational amplifier (A₁) is $-V_{sat}$ and the output of the lower operational amplifier (A₂) is $+V_{sat}$. Therefore, diode D₁ is reversed biased and the diode D₂ is forward biased. As a result, the output across R_L is $V_{out}=+V_{sat}$.

When the input voltage is greater than the lower trip point (LTP) and lower than upper trip point (UTP), output of both operational amplifiers (A₁ and A₂) is $-V_{sat}$. Therefore, both diode D₁ and the diode D₂ are reversed biased. As a result, the output across R_L is $V_{out}=0$.

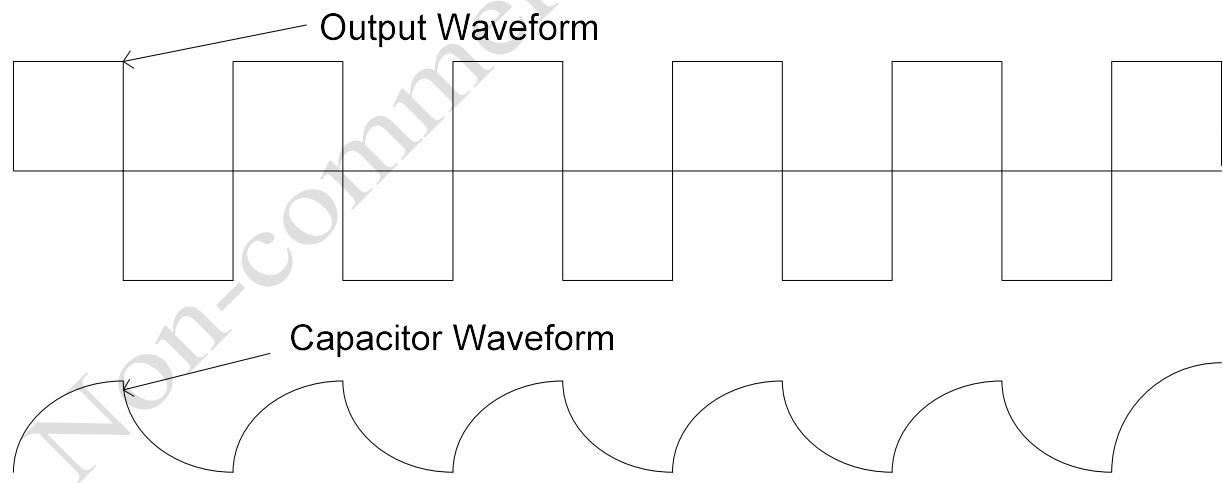
Q20. Explain the Relaxation Oscillator using operational amplifier.

Answer: Following is the circuit diagram and wave form of the relaxation oscillator using operational amplifier.

Circuit diagram:



Waveform:



Relaxation oscillator is an oscillator circuit that produces a non-sinusoidal output. Time period of the oscillator is dependent on the charging time of a capacitor connected in the oscillator circuit.

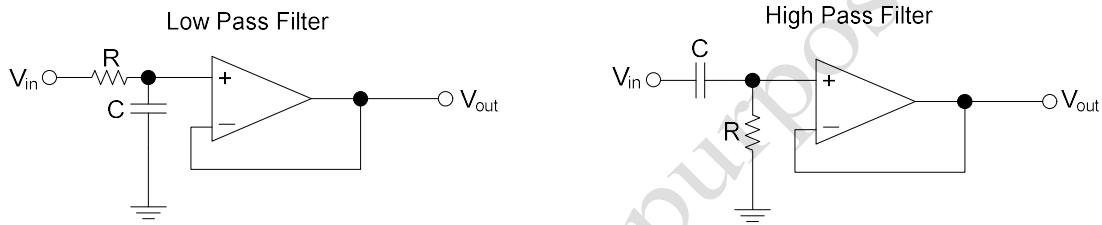
Let us assume $V_{out} = +V_{sat}$, then voltage at non-inverting terminal is $\frac{R_1}{R_1 + R_2} \cdot V_{cc}$

At this point, the capacitor starts charging towards $+V_{sat}$ through R and as the capacitor voltage reaches the voltage at non-inverting terminal, the output $V_{out} = -V_{sat}$. At the same time, the voltage at the non-inverting terminal changes to $-(R_1/(R_1+R_2))V_{sat}$. The capacitor starts discharging towards $-V_{sat}$. As voltage reaches $-(R_1/(R_1+R_2))V_{sat}$, the output is $V_{out} = +V_{sat}$ and the cycle repeats.

The time period of the output wave form is $T = 2RC\ln(\frac{1+B}{1-B})$ where $B = \frac{R_1}{R_1 + R_2}$

Q21. Explain the Active Filters.

Answer: Following are circuits diagram for Low Pass filter and High Pass filter;

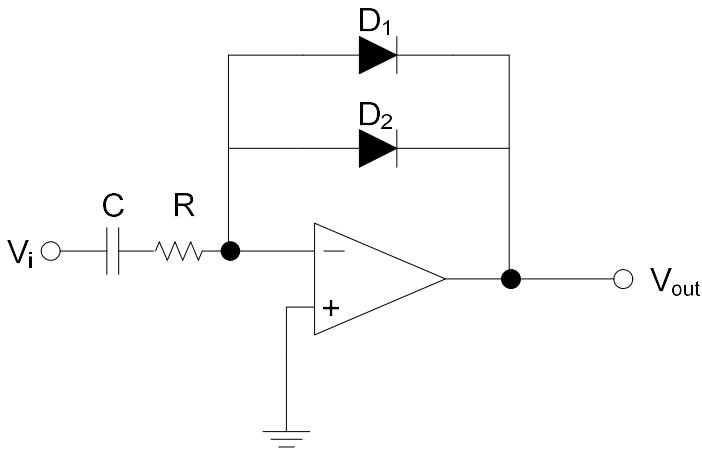


Low Pass filter: At low frequencies, the reactance of the capacitor is much higher than the resistance of the R-C circuit and hence, the output voltage is nearly equal to the applied input voltage. The operational amplifier is acting as voltage follower.

High Pass filter: At high frequencies, the reactance of the capacitor is much lower than the resistance of the R-C circuit and hence, the output voltage is nearly equal to the applied input voltage. The operational amplifier is acting as voltage follower.

Q22. Explain the non-linear amplifier.

Answer: The following is the circuit diagram for non linear amplifier.



In a non-linear amplifier, the gain value is a non-linear function of the amplitude of the input signal. A simple method to achieve non-linear amplification is by connecting a non-linear device such as PN junction diode in the feedback path.

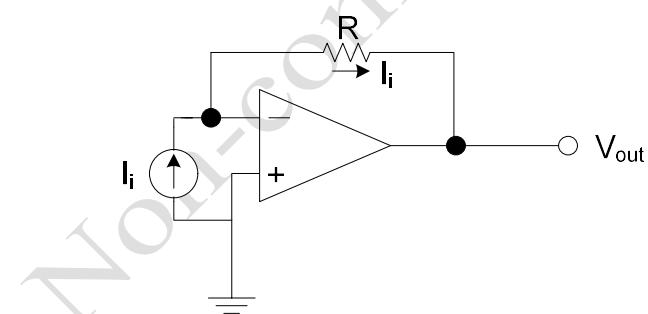
In the above circuit, the diodes act as open circuit and the gain is high due to minimum feedback when the value of the input signal is small. The diodes offer very small resistance and the gain is low when the value of the input signal is large. Such a circuit typically may cause the output voltage to change in the ratio of 2:1 for an input change of 1000:1. Resistance R_1 decides the compression ratio. Higher the value of R_1 , lesser the compression ratio.

A common application of such a non-linear amplifier is in AC bridge balance detectors.

Q23. Explain the current to voltage converter and the voltage to current converter.

Answer: Current to voltage converter:

Following is circuit diagram for current to voltage converter.



Current to voltage converter is transimpedance amplifier. An ideal transimpedance amplifier has zero input impedance and zero output impedance.

The circuit shown above is transimpedance amplifier having voltage shunt feedback with a feedback factor of unity.

$$V_o = I_i \times R \times \left(\frac{A_{OL}}{1 + A_{OL}} \right)$$

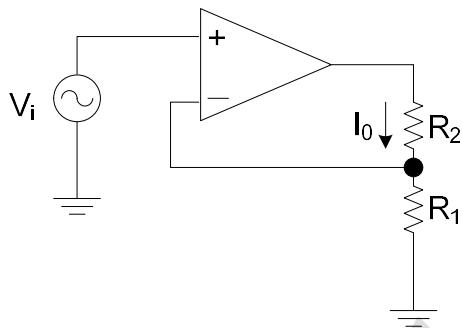
For, $A_{OL} \gg 1$, $V_o = I_i \times R$

The output voltage, $Z_{in} = \frac{R}{1 + A_{OL}}$

$$Z_o = \frac{R_o}{1 + A_{OL}} \text{ where } R_o \text{ is the output resistance of the opamp}$$

Voltage to current converter:

Following is circuit diagram for voltage to current converter.



Voltage to current converter is transconductance amplifier. An ideal transconductance amplifier has infinite input impedance and infinite output impedance.

The circuit shown above is transconductance amplifier.

$$I_0 = \frac{V_i}{R_1 + \frac{R_1 + R_2}{A_{OL}}}, \text{ If } A_{OL} \gg 1 \text{ then } I_0 = \frac{V_i}{R_1}$$

$$\text{Closed loop input impedance is given by } Z_{in} = R_i \times \left(1 + A_{OL} \times \frac{R_1}{R_1 + R_2} \right)$$

$$\text{Closed loop output impedance is given by } Z_o = R_1 \times \left(1 + A_{OL} \times \frac{R_1}{R_1 + R_2} \right)$$

Module 2

Q1. What is Gate? State and prove De Morgan's theorems.

Answer: A digital circuit having one or more input signals but only one output signal is called a gate.

De Morgan's first theorem: The complement of a sum is equal to the product of the complements.

$$\overline{A+B} = \overline{A}\cdot\overline{B}$$

Proof: We know from Boolean Algebra

$$X + \overline{X} = 1, X \cdot \overline{X} = 0, X + YZ = (X + Y)(X + Z)$$

$$Let P = A + B \text{ and } Q = \overline{A}\cdot\overline{B}$$

$$\begin{aligned} P+Q &= (A+B) + (\overline{A}\cdot\overline{B}) \\ &= (A+B+\overline{A})(A+B+\overline{B}) [X + YZ = (X + Y)(X + Z)] \\ &= (B+1)(A+1) \\ &= 1 \cdot 1 = 1 \end{aligned}$$

$$Therefore, Q = \overline{P} \Rightarrow \overline{A}\cdot\overline{B} = \overline{A+B} \Rightarrow \overline{A+B} = \overline{A}\cdot\overline{B}$$

OR

$$P \cdot Q = (A+B)\cdot\overline{A}\cdot\overline{B} = A\cdot\overline{A}\cdot\overline{B} + B\cdot\overline{A}\cdot\overline{B} = 0 + 0 = 0$$

$$Therefore, Q = \overline{P} \Rightarrow \overline{A}\cdot\overline{B} = \overline{A+B} \Rightarrow \overline{A+B} = \overline{A}\cdot\overline{B}$$

De Morgan's second theorem: The complement of a product is equal to the sum of the complements.

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

Proof: We know from Boolean Algebra

$$X + \overline{X} = 1, X \cdot \overline{X} = 0, X + YZ = (X + Y)(X + Z)$$

$$Let P = AB \text{ and } Q = \overline{A} + \overline{B}$$

$$P + Q = Q + P = (\overline{A} + \overline{B}) + AB = (\overline{A} + \overline{B} + A)(\overline{A} + \overline{B} + B) = (1 + \overline{B})(1 + \overline{A}) = 1 \cdot 1 = 1$$

$$Therefore, Q = \overline{P} \Rightarrow \overline{A} + \overline{B} = \overline{AB} \Rightarrow \overline{AB} = \overline{A} + \overline{B}$$

OR

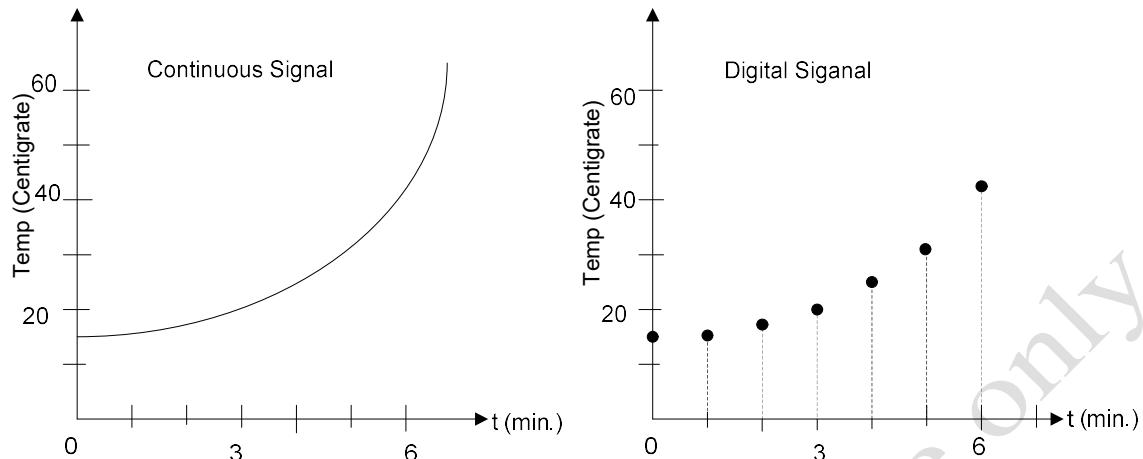
$$P \cdot Q = AB \cdot (\overline{A} + \overline{B}) = AB \cdot \overline{A} + AB \cdot \overline{B} = 0 + 0 = 0$$

$$Therefore, Q = \overline{P} \Rightarrow \overline{A} + \overline{B} = \overline{AB} \Rightarrow \overline{AB} = \overline{A} + \overline{B}$$

Q2. Differentiate analog and digital signals.

Answer: Analog signals are continuous and all possible values are considered. In the figure below, temperature is measured for water in a container which is heated for particular duration at all possible instant of time as a continuous signal.

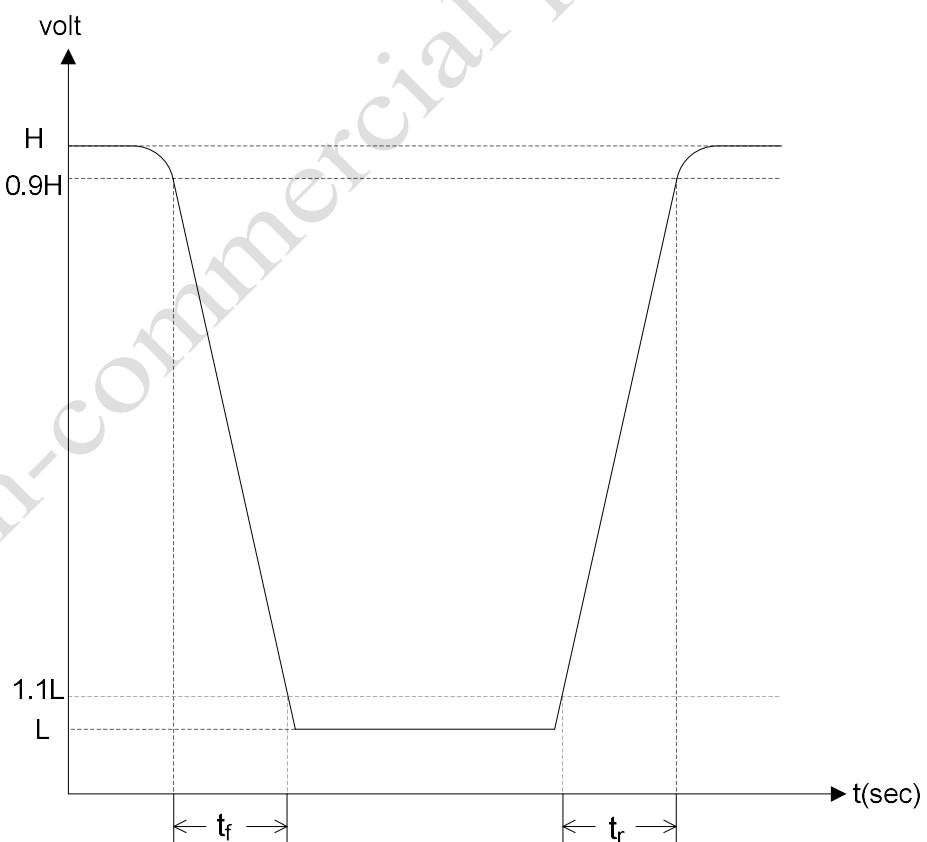
Digital signal are only finite values at particular interval. In the figure below, temperature is measured for water in a container which is heated for particular duration at discrete interval of time as a digital signal.



Q3. Define (i) rise time (ii) fall time (iii) period (iv) frequency (v) duty cycle of a digital signal.

Answer: (i) Rise Time: It is defined as the time required for a signal to rise from its low level to its high level. Rise Time is measured as the time required between $1.1L$ and $0.9H$ as shown in the figure. For example, suppose $H=4V$ and $L=2V$, then $1.1L=2.2V$ and $0.9H=3.6V$.

(ii) Fall Time: It is defined as the time required for a signal to fall from its high level to its low level. Fall Time measured is as the time required between $0.9H$ and $1.1L$ as shown in the figure. .

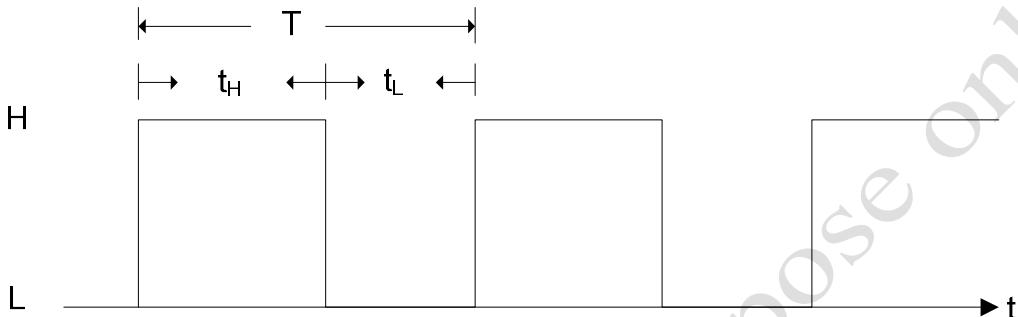


(iii) Period (T): Time required to complete one high and one low. As shown in the figure, t_H is the time required to complete one high and t_L is the time required to complete one low. $T=t_H+t_L$

(iv) Frequency (f): Frequency is the reciprocal of the time period. $f=1/T$

(v) Duty Cycle: Duty cycle $H=\frac{t_H}{T}$ and Duty cycle $L=\frac{t_L}{T}$

Duty cycle H is the ratio of time the signal is high to the time period. Duty cycle L is the ratio of time the signal is low to the time period.



Q4. (i) Prove that duty cycle of a symmetrical waveform is 50%. (ii) What is the value of high duty cycle (duty cycle H) if the frequency of a digital waveform is 5 MHz and the width of the positive pulse is 0.05 μ s? (iii) An asymmetrical signal waveform is high for 2ms and low for 3ms. Find Frequency, Period , Duty cycle low, Duty cycle high

Answer: For a symmetrical waveform, High period is $T/2$ and the Low period is $T/2$ where T is the time period.

$$(i) \text{Therefore, Duty Cycle } H = \frac{T/2}{T} \times 100\% = 50\% \text{ and Duty Cycle } L = \frac{T/2}{T} \times 100\% = 50\%$$

$$(ii) f = 5 \text{MHz}$$

$$\text{Period, } T = \frac{1}{f} = \frac{1}{5 \times 10^6} = 0.2 \mu\text{s}$$

$$\text{Width of the high pulse} = 0.05 \mu\text{s}$$

$$\text{Duty cycle } H = \frac{0.05}{0.2} \times 100\% = 25\%$$

$$(iii) t_H = \text{Width of high signal} = 2 \text{ms and } t_L = \text{Width of low signal} = 3 \text{ms}$$

$$\text{Period, } T = t_H + t_L = 2 + 3 = 5 \text{ms}$$

$$\text{Frequency, } f = \frac{1}{T} = \frac{1}{5 \times 10^{-3}} = 200 \text{Hz}$$

$$\text{Duty cycle low} = \frac{t_L}{T} = \frac{3 \text{ms}}{5 \text{ms}} \times 100\% = 60\%$$

$$\text{Duty cycle high} = \frac{t_H}{T} = \frac{2 \text{ms}}{5 \text{ms}} \times 100\% = 40\%$$

Q5. Describe positive logic and negative logic. List the equivalences in positive and negative logic.

Answer: If a binary 0 stands for low voltage and a binary 1 stands for high voltage, then this is called positive logic.

If a binary 1 stands for low voltage and a binary 0 stands for high voltage, then this is called negative logic.

Let us consider the table below as an example:

A	B	Y
LOW	LOW	LOW
LOW	HIGH	HIGH
HIGH	LOW	HIGH
HIGH	HIGH	HIGH

If we use positive logic, the above table is converter to:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

This is the truth table for OR Gate

If we negative logic, the same table is converted to:

A	B	Y
1	1	1
1	0	0
0	1	0
0	0	0

This is the truth table for AND Gate

Therefore, positive OR \leftrightarrow negative AND

Following are the equivalences in positive and negative logic:

Positive OR \leftrightarrow Negative AND

Positive AND \leftrightarrow Negative OR

Positive NOR \leftrightarrow Negative NAND

Positive NAND \leftrightarrow Negative NOR

Q6. Prove that (a) “Positive OR” logic is equal to “Negative AND” logic (b) “Positive AND” logic is equal to “Negative OR” logic (c) “Positive NOR” logic is equal to “Negative NAND” logic (d) “Positive NAND” logic is equal to “Negative NOR” logic

Answer: (a) Let us consider the table below:

A	B	Y
LOW	LOW	LOW
LOW	HIGH	HIGH
HIGH	LOW	HIGH
HIGH	HIGH	HIGH

If we use positive logic, the above table is converter to:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

This is the truth table for OR Gate

If we negative logic, the same table is converted to:

A	B	Y
1	1	1
1	0	0
0	1	0
0	0	0

This is the truth table for AND Gate

Therefore, “Positive OR” logic is equal to “Negative AND” logic:

(b) : (a) Let us consider the table below:

A	B	Y
LOW	LOW	LOW
LOW	HIGH	LOW
HIGH	LOW	LOW
HIGH	HIGH	HIGH

If we use positive logic, the above table is converter to:

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

This is the truth table for AND Gate

If we negative logic, the same table is converted to:

A	B	Y
1	1	1
1	0	1
0	1	1
0	0	0

This is the truth table for OR Gate

Therefore, “Positive AND” logic is equal to “Negative OR” logic

(c) (a) Let us consider the table below:

A	B	Y
LOW	LOW	HIGH
LOW	HIGH	LOW
HIGH	LOW	LOW
HIGH	HIGH	LOW

If we use positive logic, the above table is converted to:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

This is the truth table for NOR Gate

If we use negative logic, the same table is converted to:

A	B	Y
1	1	0
1	0	1
0	1	1
0	0	1

This is the truth table for NAND Gate

Therefore, “Positive NOR” logic is equal to “Negative NAND”

(d) Let us consider the table below:

A	B	Y
LOW	LOW	HIGH
LOW	HIGH	HIGH
HIGH	LOW	HIGH
HIGH	HIGH	LOW

If we use positive logic, the above table is converted to:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

This is the truth table for NAND Gate

If we use negative logic, the same table is converted to:

A	B	Y
1	1	0
1	0	0
0	1	0
0	0	1

This is the truth table for NOR Gate

Therefore, “Positive NAND” logic is equal to “Negative NOR” logic

Q7. What is a universal gate? List the universal gates and prove their universalities.

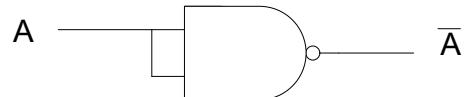
Answer: A universal gate is a gate that can be used to realize any other gate and therefore, a universal gate can be used to realize any Boolean function without using any other gate.

Universal gates are NOR gate and NAND gate.

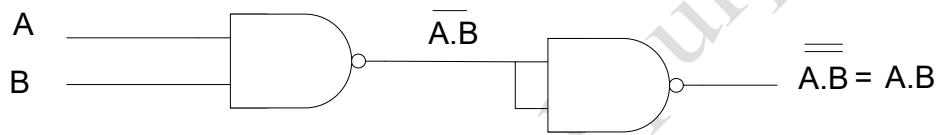
Proof of NAND gate as universal gate:

Any Boolean function can be implemented using NOT gate, AND gate and OR gate. Therefore, if NOT gate, AND gate and OR gate are implemented using NAND gate only, then it will be proved that NAND gate is a universal gate.

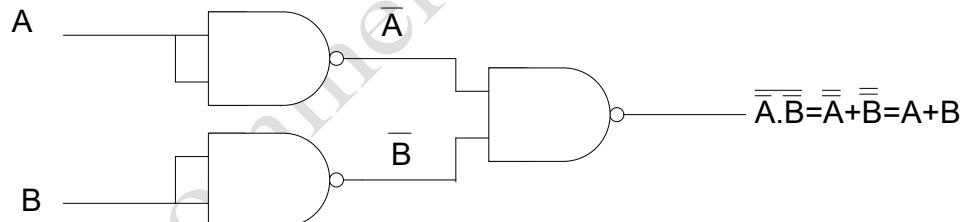
Implementing NOT using NAND gate



Implementing of AND gate using NAND gates



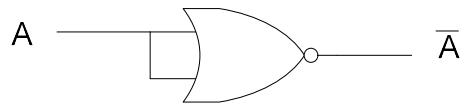
Implementing OR using NAND gate



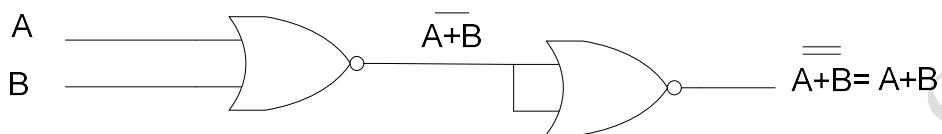
Proof of NOR gate as universal gate:

Any Boolean function can be implemented using NOT gate, AND gate and OR gate. Therefore, if NOT gate, AND gate and OR gate are implemented using NOR gate only, then it will be proved that NOR gate is a universal gate.

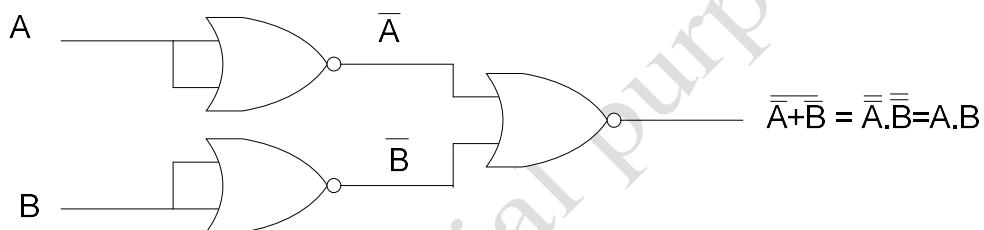
Implementing NOT using NOR gate



Implementing of OR gate using NOR gates

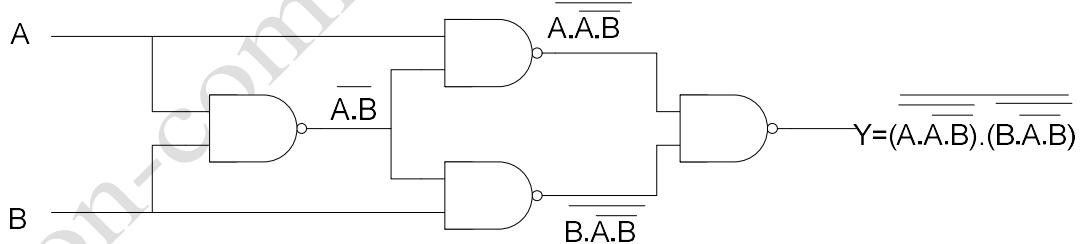


Implementing AND using NOR gates



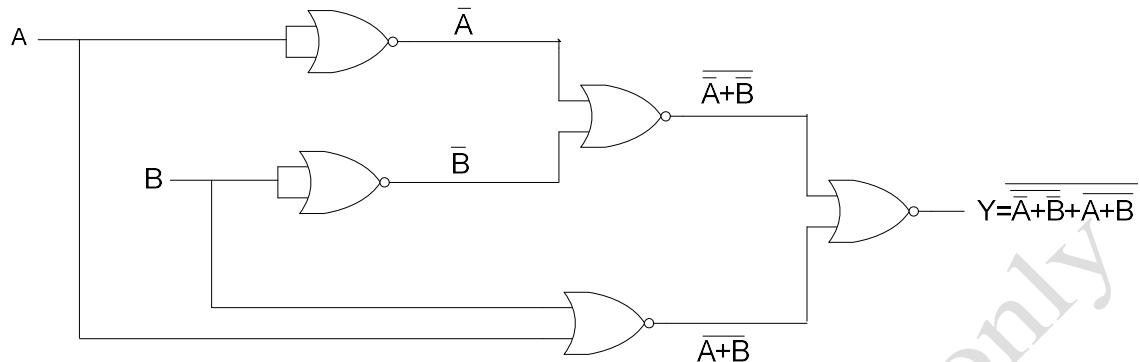
Q8. Realize the XOR gate using (i) NAND gate (ii) NOR gate.

Answer: (i) The following figure shows the realization of XOR gate with NAND gates:



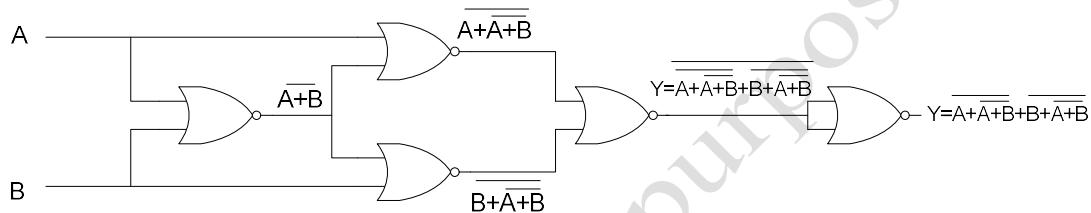
$$Y = (\overline{A} \cdot \overline{A} \cdot B) + (B \cdot \overline{A} \cdot \overline{B}) = \overline{A} \cdot \overline{A} \cdot B + B \cdot \overline{A} \cdot \overline{B} = A \cdot \overline{A} + B \cdot \overline{B} = A \cdot (\overline{A} + \overline{B}) + B \cdot (\overline{A} + \overline{B}) = A \cdot \overline{B} + B \cdot \overline{A} = A \oplus B$$

(ii) The following figure shows the realization of XOR gate with NOR gates:



$$Y = \overline{\overline{A} + \overline{B}} + \overline{A + \overline{B}} = (\overline{A} + \overline{B})(\overline{A} + \overline{B}) = (\overline{A} + \overline{B})(A + B) = \overline{A} \cdot \overline{A} + \overline{A} \cdot B + \overline{B} \cdot A + \overline{B} \cdot B = A \cdot \overline{B} + \overline{A} \cdot B = A \oplus B$$

Alternately,

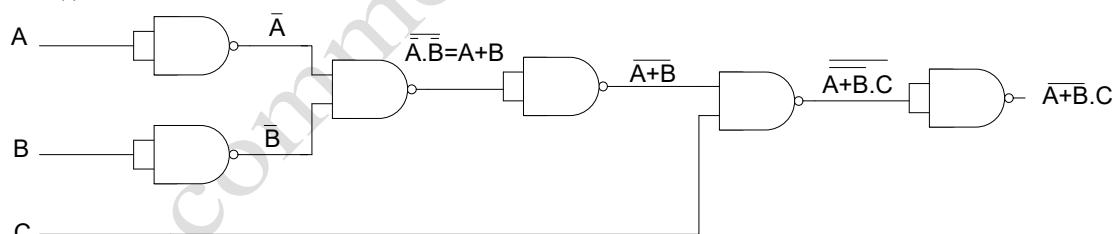


$$Y = \overline{A + \overline{A} + B} + \overline{B + \overline{A} + B} = \overline{A \cdot \overline{A} + B} + \overline{B \cdot \overline{A} + B} = \overline{A} \cdot (A + B) + \overline{B} \cdot (A + B) = \overline{A} \cdot B + A \cdot \overline{B} = A \oplus B$$

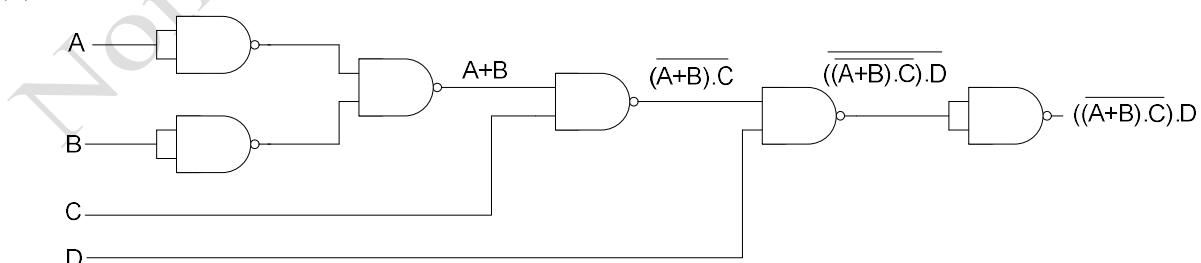
Q9. Implement the following functions using NAND gate only:

- (i) $((\overline{A} + B) \cdot C)$
- (ii) $Y = ((\overline{A} + B) \cdot C) \cdot D$
- (iii) $((A + B) \cdot (\overline{A} + \overline{B})) \cdot D$

Answer: (i)

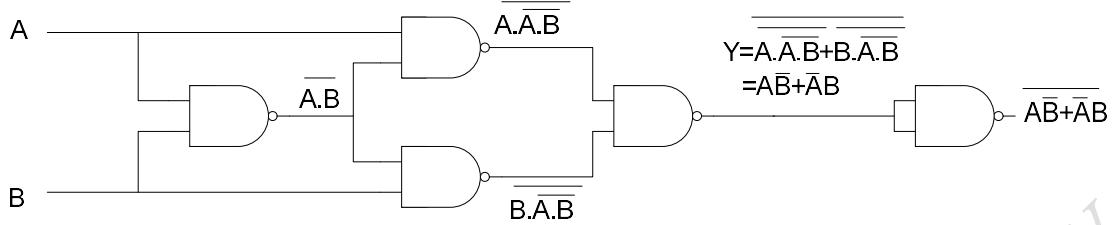


(ii)



(iii)

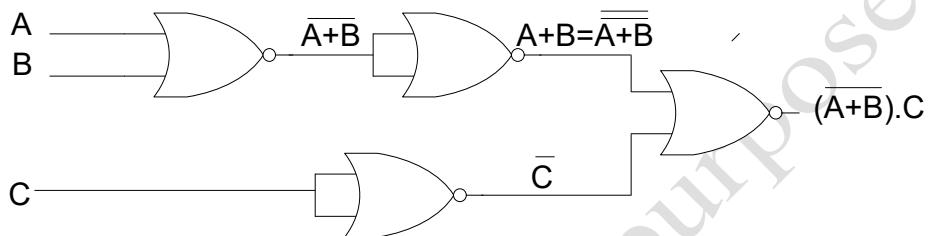
$$\overline{(A+B) \cdot (\bar{A}+\bar{B})} = \overline{\bar{A}\bar{B} + \bar{A}B}$$



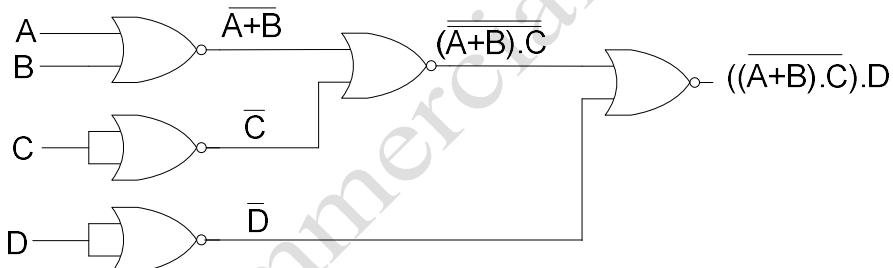
Q10. Implement the following functions using NOR gate only:

$$(i) ((\overline{A+B}).C) \quad (ii) Y = ((\overline{A+B}).C).D \quad (iii) ((A+B).(\overline{A}+\overline{B}))$$

Answer: (i)

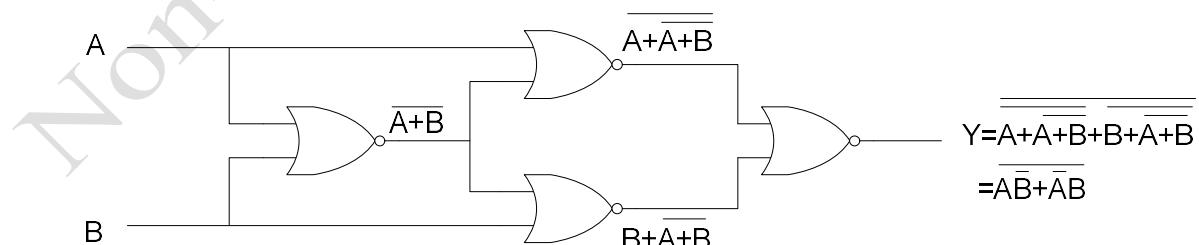


(ii)



(iii)

$$\overline{(A+B) \cdot (\bar{A}+\bar{B})} = \overline{\bar{A}\bar{B} + \bar{A}B}$$



$$Y = \overline{\overline{\overline{A+A+B}} + \overline{B+A+B}} = \overline{\overline{\overline{A+A+B}} + \overline{B} \cdot \overline{\overline{A+B}}} = \overline{\overline{A} \cdot (A+B) + \overline{B} \cdot (A+B)} = \overline{\overline{A} \cdot \overline{B} + \overline{A} \cdot B}$$

Q11. Define canonical Minterm form and canonical Maxterm form.

Answer: Minterm: A minterm, denoted by m_i , $0 \leq i < 2^n$, is a product of n variables in which each variable is complemented if the value assigned to it is 0.

Let us consider a Boolean function $F = f(x, y, z) = x'yz + xy'z + xyz' + xyz$.

Truth table of the above function along with the minterms is shown below:

x	y	z	Minterm	F
0	0	0	$m_0=x'y'z'$	0
0	0	1	$m_1=x'y'z$	0
0	1	0	$m_2=x'yz'$	0
0	1	1	$m_3=x'yz$	1
1	0	0	$m_4=xy'z'$	0
1	0	1	$m_5=xy'z$	1
1	1	0	$m_6=xyz'$	1
1	1	1	$m_7=xyz$	1

The above function can be expressed in term of minterms as $F=m_3+m_5+m_6+m_7=\Sigma m(3,5,6,7)$

The inverse of the function can be expressed as $F'=\Sigma m(0,1,2,4)$

Maxterm: A maxterm, denoted by M_i , $0 \leq i < 2^n$, is a sum of n variables in which each variable is complemented if the value assigned to it is 1.

Let us consider a Boolean function $F = f(x, y, z) = (x + y + z)(x + y + z')(x + y' + z)(x' + y + z)$

Truth table of the above function along with maxterm is shown below:

x	y	z	Maxterm	F
0	0	0	$M_0=x+y+z$	0
0	0	1	$M_1=x+y+z'$	0
0	1	0	$M_2=x+y'+z$	0
0	1	1	$M_3=x+y'+z'$	1
1	0	0	$M_4=x'+y+z$	0
1	0	1	$M_5=x'+y+z'$	1
1	1	0	$M_6=x'+y'+z$	1
1	1	1	$M_7=x'+y'+z'$	1

The above function can be expressed in term of maxterms as $F=M_0.M_1.M_2.M_4=\Pi M(0,1,2,4)$

The inverse of the function can be expressed as $F'=\Pi M(3,5,6,7)$

.Q12. Express the function $F=x+yz$ as the sum of its minterms and product of maxterms.

Answer : $F = x + yz = x(y + y')(z + z') + yz(x + x') = xyz + xyz' + xy'z + xy'z' + xyz + x'yz$

$$\Rightarrow F = xyz + xyz' + xy'z + xy'z' + x'yz = m_7 + m_6 + m_5 + m_4 + m_3 = \sum m(3, 4, 5, 6, 7)$$

Again, $F = x + yz = (x + y)(x + z) = (x + y + zz')(x + z + yy')$

$$\Rightarrow F = (x + y + z)(x + y + z')(x + z + y)(x + z + y') = (x + y + z)(x + y + z')(x + y' + z) = M_0.M_1.M_2 = \Pi M(0,1,2)$$

Q13. Express the function $F=(x+yz)'$ as the sum of its minterms and product of maxterms.

Answer : $F = (x + yz)' = (x + (yz))' = x'.(yz)' = x'.(y' + z') = x'y' + x'z' = x'y'(z + z') + x'z'(y + y')$

$$\Rightarrow F = x'y'z + x'y'z' + x'yz' + x'y'z' = x'y'z + x'y'z' + x'yz' = m_1 + m_0 + m_2 = \sum m(0,1,2)$$

Again, $F = (x + yz)' = (x + (yz))' = x'.(yz)' = x'.(y' + z') = (x' + yy' + zz')(y' + z' + xx')$

$$\Rightarrow F = (x' + yy' + z)(x' + yy' + z')(y' + z' + x)(y' + z' + x')$$

$$\Rightarrow F = (x' + y + z)(x' + y' + z)(x' + y + z')(x' + y' + z')(x + y' + z')(x' + y' + z')$$

$$\Rightarrow F = (x' + y + z)(x' + y' + z)(x' + y + z')(x' + y' + z')(x + y' + z')$$

$$\Rightarrow F = M_4.M_6.M_7.M_3 = \Pi M(3,4,5,6,7)$$

Q14. Convert the following 3-variable SOP to POS form.

- (i) $\Sigma m(3,5,6,7)$ (ii) $\Sigma m(0,2,5,6)$

Answer: (i) $\Sigma m(3,5,6,7) = \Pi M(0,1,2,4)$ (ii) $\Sigma m(0,2,5,6) = \Pi M(1,3,4,7)$

Q15. Convert the following 4-variable POS to SOP form.

- (i) $\Pi M(1,3,4,7)$ (ii) $\Pi M(0,1,2,4,10,13,15)$

Answer: (i) $\Pi M(1,3,4,7) = \Sigma m(0,2,5,6,8,9,10,11,12,13,14,15)$

(ii) $\Pi M(0,1,2,4,10,13,15) = \Sigma m(3,5,6,7,8,9,11,12,14)$

Q16. Use K-Map to simplify the following functions:

$$(i) f(A,B,C,D) = \sum m(0,2,6,10,11,12,13) + d(3,4,5,14,15)$$

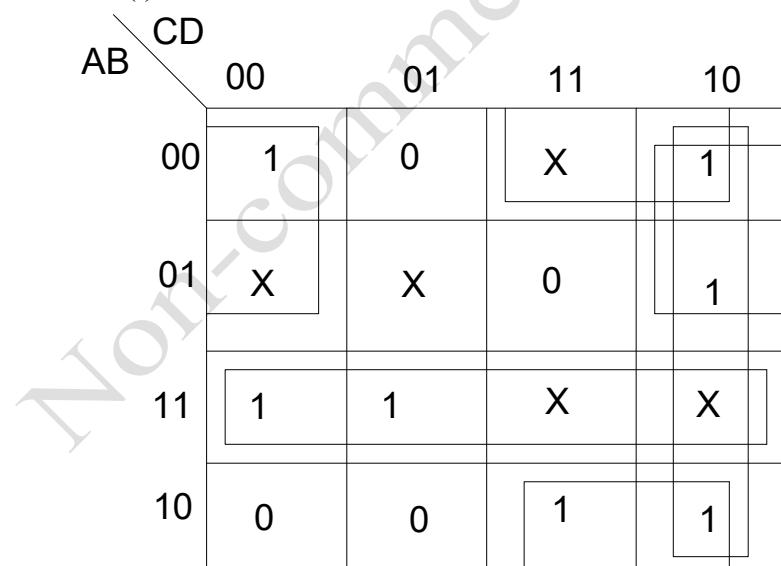
$$(ii) f = \sum m(1,2,6,7,8,13,14,15) + d(3,5,12)$$

$$(iii) f = \sum m(1,3,4,5,13,15) + \sum d(8,9,10,11)$$

$$(iv) f(A,B,C,D) = (A + B + \bar{C})(\bar{B} + \bar{D})(\bar{A} + C)(B + C)$$

$$(v) f(A,B,C,D) = \pi(1,2,4,5,7,8,10,11,13,14)$$

Answer: (i)



$$f(A,B,C,D) = AB + C\bar{D} + \bar{B}C + \bar{A}\bar{D}$$

(ii) Let us consider the variables as A, B, C and D.

		CD	00	01	11	10
		AB	00	01	11	10
00	00	0	1	X		1
00	01	0	X	1		1
01	11	X	1	1	1	
01	10	1	0	0	0	
11	00					
11	01					
11	11					
10	10					

$$f(A, B, C, D) = \overline{AD} + \overline{AC} + AB + A\overline{CD}$$

(iii) Let us consider the variables as A, B, C and D.

		CD	00	01	11	10
		AB	00	01	11	10
00	00	0	1	1	0	
00	01	1	1	0	0	
01	11	0	1	1	0	
01	10	X	X	X	X	
11	00					
11	01					
11	11					
10	10					

$$f(A, B, C, D) = AD + \overline{BD} + \overline{ABC}$$

$$(iv) f(A, B, C, D) = (A + B + \overline{C})(\overline{B} + \overline{D})(\overline{A} + C)(B + C)$$

$$= (A + B + \overline{C} + \overline{D})(A + B + \overline{C} + D)(\overline{A} + \overline{B} + \overline{C} + \overline{D})(\overline{A} + \overline{B} + C + \overline{D})(A + \overline{B} + \overline{C} + \overline{D})(A + \overline{B} + C + \overline{D})$$

$$(\overline{A} + \overline{B} + C + \overline{D})(\overline{A} + \overline{B} + C + D)(\overline{A} + B + C + \overline{D})(\overline{A} + B + C + D)(\overline{A} + B + C + \overline{D})(\overline{A} + B + C + D)$$

$$(A + B + C + \overline{D})(A + B + C + D)$$

$$= M_3 \cdot M_2 \cdot M_{15} \cdot M_{13} \cdot M_7 \cdot M_5 \cdot M_{12} \cdot M_9 \cdot M_8 \cdot M_1 \cdot M_0 = M_0 \cdot M_1 \cdot M_2 \cdot M_3 \cdot M_5 \cdot M_7 \cdot M_8 \cdot M_9 \cdot M_{12} \cdot M_{13} \cdot M_{15}$$

AB \ CD	00	01	11	10
00	0	0	0	0
01	1	0	0	1
11	0	0	0	1
10	0	0	1	1

$$f(A, B, C, D) = (A + B)(C + \bar{D})(\bar{B} + \bar{D})(\bar{A} + C)$$

(v)

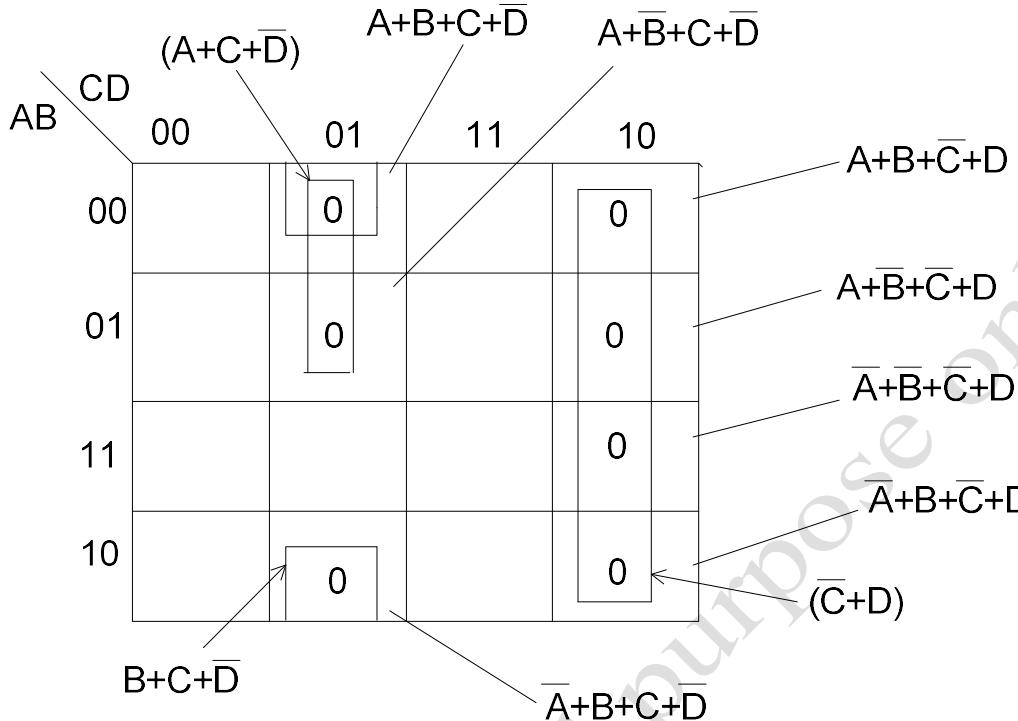
AB \ CD	00	01	11	10
00	1	0	1	0
01	0	0	0	1
11	1	0	1	0
10	0	1	0	0

$$f = (A + \bar{B} + C)(A + \bar{B} + \bar{D})(\bar{B} + C + \bar{D})(A + C + \bar{D})(\bar{A} + B + \bar{C})(\bar{A} + \bar{C} + D)(\bar{A} + B + D)(B + \bar{C} + D)$$

Q17, Simplify the Product of Sum expression below and provide the result in POS form.

$$\begin{aligned} F(A, B, C, D) &= (A + B + C + \bar{D})(A + B + \bar{C} + D)(A + \bar{B} + C + \bar{D})(A + \bar{B} + \bar{C} + D)(\bar{A} + \bar{B} + \bar{C} + D) \\ &\quad (\bar{A} + B + C + \bar{D})(\bar{A} + B + \bar{C} + D) \end{aligned}$$

Answer:

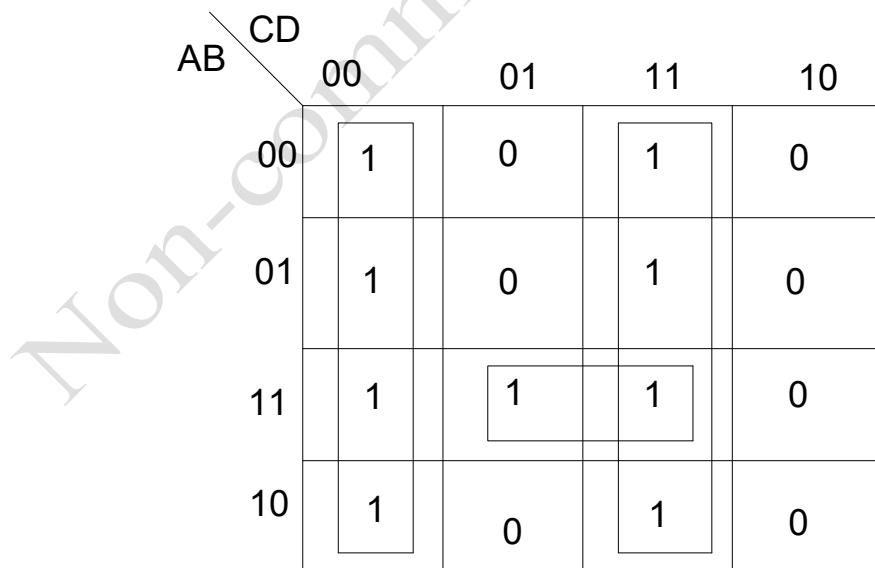


$$\text{Therefore, the result in POS, } F = (\bar{C} + D)(A + C + \bar{D})(B + C + \bar{D})$$

Q18. Simplify the Product Of Sum expression below and provide the result in SOP form.

$$F(A, B, C, D) = (A + B + C + \bar{D})(A + B + \bar{C} + D)(A + \bar{B} + C + \bar{D})(A + \bar{B} + \bar{C} + D)(\bar{A} + \bar{B} + \bar{C} + D) \\ (\bar{A} + B + C + \bar{D})(\bar{A} + B + \bar{C} + D)$$

Answer:



$$\text{Therefore, the result in SOP, } F = \bar{C}\bar{D} + CD + ABD$$

Q19. Find the minimal SOP and minimal POS of the following Boolean function using K-Map.

$$f(a,b,c,d) = \sum m(6,7,9,10,13) + d(1,4,5,11)$$

Answer:

		cd	00	01	11	10
		ab	00	01	11	10
00	01	00	0	X	0	0
		01	X	X	1	1
11	10	00	0	1	0	0
		01	0	1	X	1

$$\text{Minimal SOP is given by } f(a,b,c,d) = \bar{a}b + \bar{c}d + \bar{a}\bar{b}c$$

		cd	00	01	11	10
		ab	00	01	11	10
00	01	00	0	X	0	0
		01	X	X	1	1
11	10	00	0	1	0	0
		01	0	1	X	1

$$\text{Minimal POS is given by } f(a,b,c,d) = (a+b)(c+d)(\bar{a}+\bar{b}+\bar{c})$$

Q20. Reduce the following Boolean function using K-Map and realize the simplified expression using NAND gates.

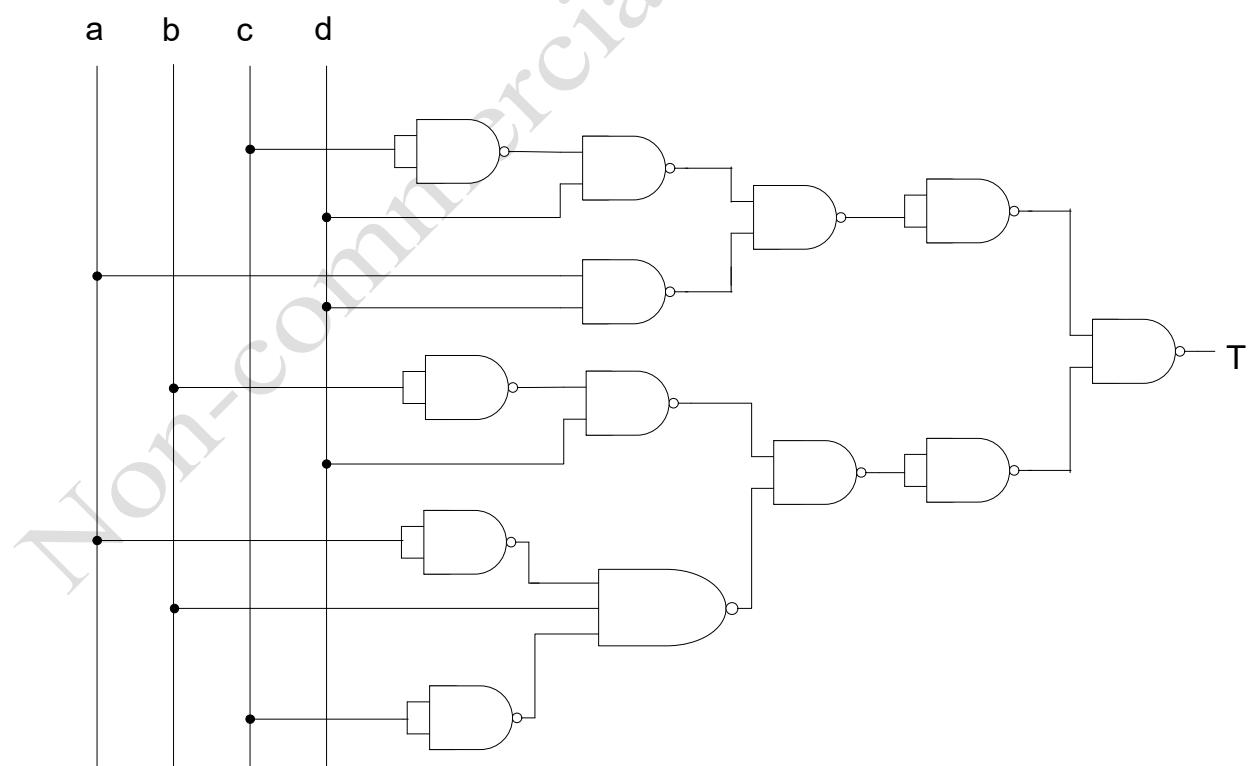
$$T = f(a,b,c,d) = \sum m(1,3,4,5,13,15) + \sum d(8,9,10,11)$$

Answer:

ab \ cd	00	01	11	10
00	0	1	1	0
01	1	1	0	0
11	0	1	1	0
10	X	X	X	X

$$T = f(a,b,c,d) = \bar{c}\bar{d} + ad + \bar{b}d + \bar{a}\bar{b}\bar{c}$$

Following diagram shows the realization of the above expression with NAND gates



Q21. Simplify the following expressions using Karnaugh map. Implement the simplified circuit using the gates as indicated:

$$(i) f(w, x, y, z) = \sum m(1, 5, 7, 9, 10, 13, 15) + d(8, 11, 14) \text{ using NAND gates.}$$

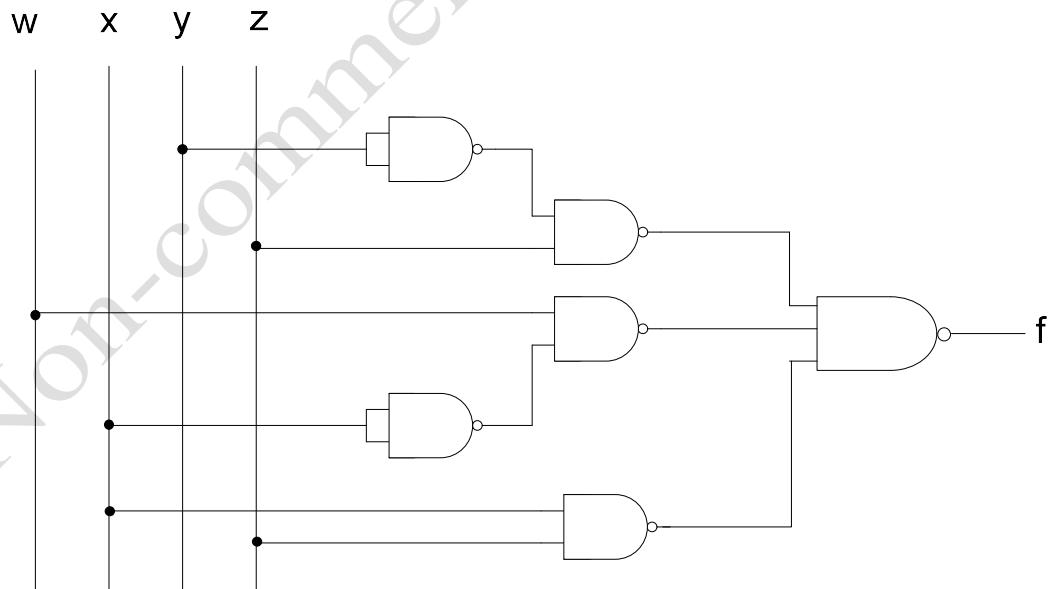
$$(ii) f(A, B, C, D) = \prod M(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14) \text{ using NOR gates.}$$

Answer: (i)

		yz	00	01	11	10
		wx	00	1	0	0
		yz	01	1	1	0
		wx	11	1	1	X
		yz	10	X	1	1

$$f(w, x, y, z) = \bar{y}z + \bar{w}\bar{x} + xz$$

Following is the implementation of the simplified circuit with NAND gates.

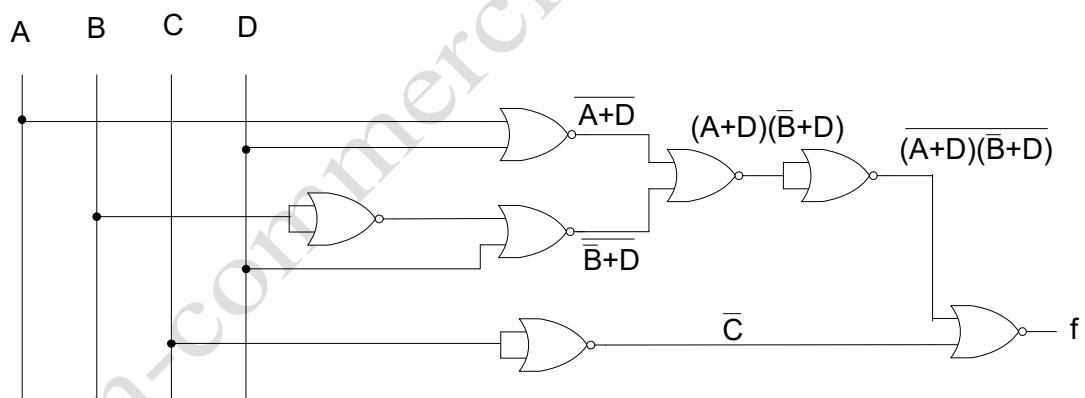


(ii)

AB \ CD	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	0	0	1	0
10	0	0	1	1

$$f(A, B, C, D) = C(A + D)(\bar{B} + D)$$

Following is the implementation of the simplified circuit with NOR gates.



Q22. Simplify the following using Quine McClusky minimization technique:

$$(i) P = f(w, x, y, z) = \sum m(7, 9, 12, 13, 14, 15) + \sum d(4, 11)$$

$$(ii) Y = f(a, b, c, d) = \sum (0, 1, 2, 6, 7, 9, 10, 12) + d(3, 5). \text{ Verify the result using K-map.}$$

$$(iii) f(A, B, C, D) = \sum m(0, 1, 2, 3, 10, 11, 12, 13, 14, 15)$$

$$(iv) f(W, X, Y, Z) = \sum m(1, 3, 6, 7, 8, 9, 10, 12, 13, 14)$$

Answer:

(i)

$$f(w, x, y, z) = \sum m(7, 9, 12, 13, 14, 15) + d(4, 11)$$

wxyz	Stage 1	wxyz	Stage 2	wxyz	Stage 3
0100	(4)✓	-100	(4, 12)	1--1	(9, 11, 13, 15)
1001	(9)✓	10-1	(9, 11)✓	1--1	(9, 13, 11, 15)
1100	(12)✓	1-01	(9, 13)✓	11--	(12, 13, 14, 15)
0111	(7)✓	110-	(12, 13)✓	11--	(12, 14, 13, 15)
1011	11)✓	11-0	(12, 14)✓		
1101	(13)✓				
1110	1(4)✓				
1111	(15)✓	-111	(7, 15)		
		1-11	(11, 15)✓		
		11-1	(13, 15)✓		
		111-	(14, 15)✓		

	7	9	12	13	14	15
wz (9, 11, 13, 15)		✓		✓		✓
wx (12, 13, 14, 15)			✓	✓	✓	✓
xy'z' (4, 12)			✓			
xyz (7, 15)	✓					✓

$$P = f(w, x, y, z) = wz + wx + xyz$$

Verification:

wx \ yz	00	01	11	10
00	0	0	0	0
01	X	0	1	0
11	1	1	1	1
10	0	1	X	0

$$P = f(w, x, y, z) = wz + wx + xyz$$

(ii)

$$Y = f(a, b, c, d) = \Sigma m(0, 1, 2, 6, 7, 9, 10, 12) + d(3, 5)$$

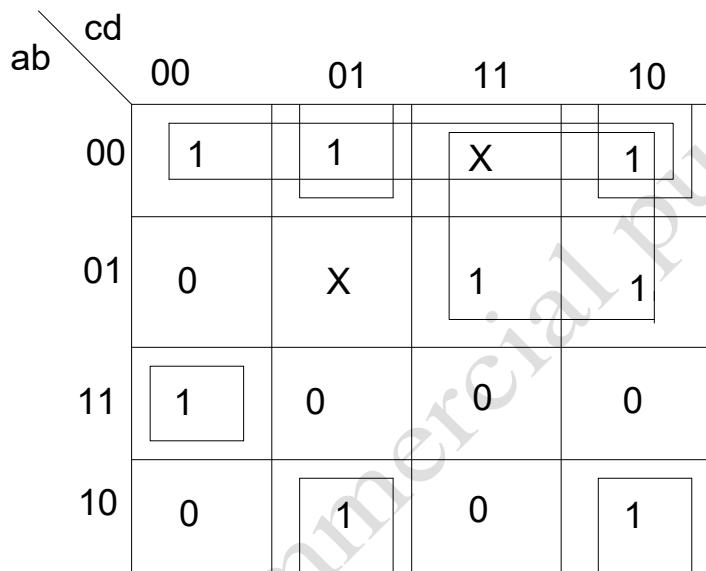
Stage 1		Stage 2		Stage 3	
abcd		abcd		abcd	
0000	(0)✓	000-	(0,1)✓	00 - -	(0,1,2,3)
0001	(1)✓	00-0	(0,2)✓	00 - -	(0,2,1,3)
0010	(2)✓	00-1	(1,3)✓	0 - - 1	(1,3,5,7)
0011	(3)✓	0-01	(1,5)✓	0 - - 1	(1,5,3,7)
0101	(5)✓	-001	(1,9)	0 - 1 -	(2,3,6,7)
0110	(6)✓	001-	(2,3)✓	0 - 1 -	(2,6,3,7)
1001	(9)✓	0-10	(2,6)✓		
1010	(10)✓	-010	(2,10)		
1100	(12)	0-11	(3,7)✓		
0111	(7)✓	01-1	(5,7)✓		
		011-	(6,7)✓		

	0	1	2	6	7	9	10	12
--	---	---	---	---	---	---	----	----

$abc'd'(12)$								✓
$b'c'd(1,9)$		✓					✓	
$b'cd'(2,10)$			✓				✓	
$a'b'(0,1,2,3)$	✓	✓	✓					
$a'd(1,3,5,7)$		✓				✓		
$a'c(2,3,6,7)$			✓	✓	✓			

$$Y = abc'd' + b'c'd + b'cd' + a'b' + a'c$$

Verification:



$$Y = abc'd' + b'c'd + b'cd' + a'b' + a'c$$

(iii)

$$f(A,B,C,D) = \sum m(0,1,2,3,10,11,12,13,14,15)$$

Stage 1		Stage 2		Stage 3	
ABCD		ABCD		ABCD	
0000	(0)✓	000-	(0,1)✓	00 - -	(0,1,2,3)
0001	(1)✓	00-0	(0,2)✓	00 - -	(0,2,1,3)
0010	(2)✓	00-1	(1,3)✓	-01-	(2,3,10,11)
0011	(3)✓	001-	(2,3)✓	-01-	(2,10,3,11)
1010	(10)✓	-010	(2,10)✓		
1100	(12)✓	-011	(3,11)✓	1-1-	(10,11,14,15)
1011	(11)✓	101-	(10,11)✓	1-1-	(10,14,11,15)
1101	(13)✓	1-10	(10,14)✓	11- -	(12,13,14,15)
1110	(14)✓	110-	(12,13)✓	11- -	(12,14,13,15)
1111	(15)✓	11-0	(12,14)✓		
		1-11	(11,15)✓		
		11-1	(13,15)✓		
		111-	(14,15)✓		

	0	1	2	3	10	11	12	13	14	15
$A'B'(0,1,2,3)$	✓	✓	✓	✓						
$B'C(2,3,10,11)$			✓	✓	✓	✓				
AC (10,11,14,15)					✓	✓			✓	✓
AB (12,13,14,15)							✓	✓	✓	✓

$$f(A,B,C,D) = A'B' + AC + AB \text{ or } f(A,B,C,D) = A'B' + B'C + AB$$

Verification:

AB	CD					
	00	01	11	10		
00	1	1	1	1		
01	0	0	0	0		
11	1	1	1	1		
10	0	0	1	1		

$$f(A,B,C,D) = A'B' + AC + AB$$

(iv)

$$f(W, X, Y, Z) = \Sigma m(1, 3, 6, 7, 8, 9, 10, 12, 13, 14)$$

Stage 1		Stage 2		Stage 3	
WXYZ	WXYZ	WXYZ	WXYZ	WXYZ	WXYZ
0001	(1)✓	00-1	(1,3)	1-0-	(8,9,12,13)
1000	(8)✓	-001	(1,9)	1- -0	(8,10,12,14)
0011	(3)✓	100-	(8,9)✓	1- -0	(8,12,10,14)
0110	(6)✓	10-0	(8,10)✓		
1001	(9)✓	1-00	(8,12)✓		
1010	(10)✓	0-11	(3,7)		
1100	(12)✓	011-	(6,7)		
0111	(7)✓	-110	(6,14)		
1101	(13)✓	1-01	(9,13)		
1110	(14)✓	1-10	(10,14)✓		
		110-	(12,13)✓		
		11-0	(12,14)✓		

	1	3	6	7	8	9	10	12	13	14
$WX'Z(1,3)$	✓	✓								
$X'YZ(1,9)$	✓					✓				
$WYZ(3,7)$		✓		✓						
$WXY(6,7)$			✓	✓						
$XYZ'(6,14)$			✓							✓
$WY'Z(9,13)$						✓			✓	
$WY'(8,9,12,13)$					✓	✓		✓	✓	
$WZ'(8,10,12,14)$					✓		✓	✓		✓

$$f(W, X, Y, Z) = W'X'Z + W'XY + WY' + WZ'$$

Verification:

WX \ YZ	00	01	11	10
00	0	1	1	0
01	0	0	1	1
11	1	1	0	1
10	1	1	0	1

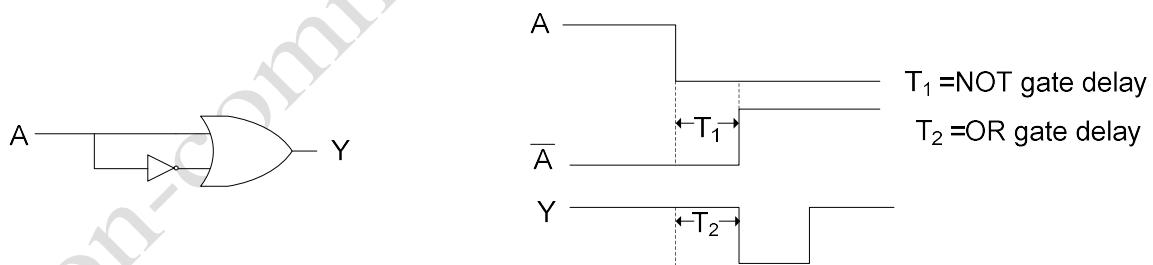
$$f(W, X, Y, Z) = W'X'Z + W'XY + WY' + WZ'$$

Q23. What are static hazards? How to design a hazard free circuit? Explain with an example.

Answer: When the input to a combinational circuit changes, unwanted switching transients may appear in the output. These transients occurs when different paths from input to output have different propagation delays.

Static-1 hazard:

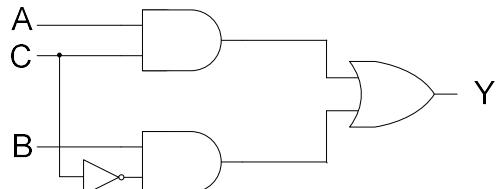
This type of hazard occurs when $Y = A + \bar{A}$ type situation appears for a logic circuit and A makes a transition $1 \rightarrow 0$.



An $A + \bar{A}$ condition should always generate 1 at the output i.e static-1. But the NOT gate output takes finite time to become 1 following $1 \rightarrow 0$ transition of A. Thus for the OR gate there are two zeros appears at the input for that small duration resulting a 0 at the output. The width of this zero is in nanosecond order and is called glitch.

Designing static-1 hazard free circuit:

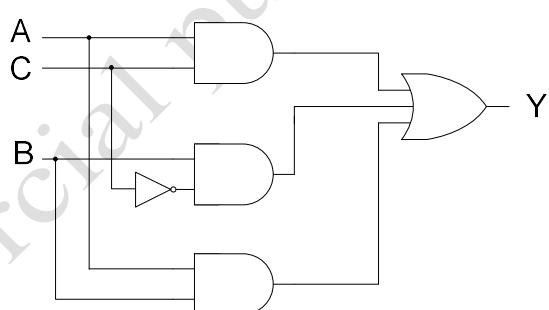
	\bar{C}	C
A B	0 0	
$\bar{A} B$	1	0
A B	1	1
$A \bar{B}$	0	1



The karnaugh map shown above represented by $Y = B\bar{C} + AC$

Consider the circuit input B=1 and A=1 and then C makes transition 1→0. The output shows glitches.
Now, consider the following grouping:

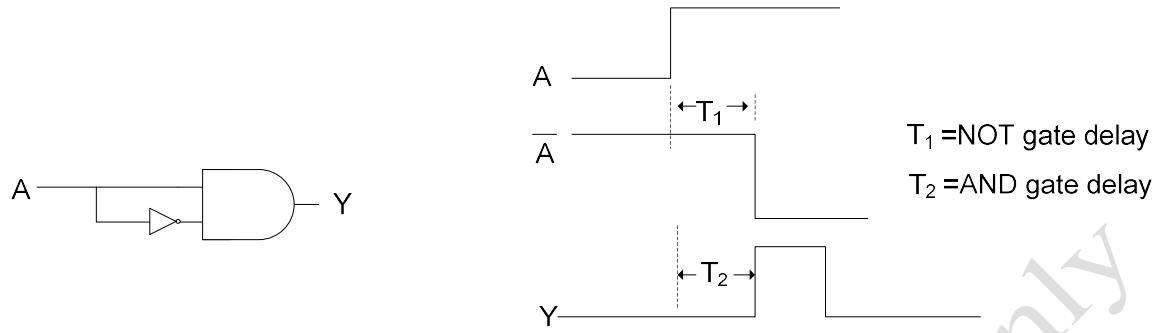
	\bar{C}	C
A B	0 0	
$\bar{A} B$	1	0
A B	1	1
$A \bar{B}$	0	1



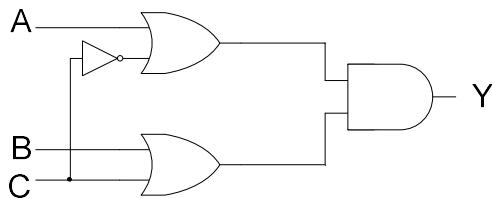
The above circuit includes one additional AB and $Y = B\bar{C} + AC + AB$. The additional ensures free from glitches.

Static-0-hazard:

This type of hazard occurs when $Y = A\bar{A}$ kind of situation occurs in a logic circuit and A makes a transition 0→1. A $A\bar{A}$ condition should always generate 0 at the output i.e static-0. But the NOT gate output takes finite time to become 0 following a 0→1 transition of A. Thus for final AND gate there are two ones appearing at the inputs for small duration resulting a 1 at its output.

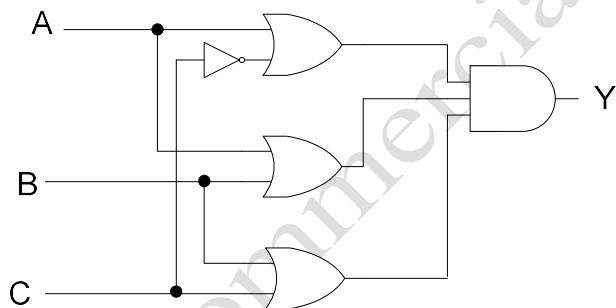


The circuit below is with static-0 hazard:



Consider the circuit input B=0 and A=0 and then C makes transition 0→1. The output shows glitches.

The circuit below is static-0 hazard free

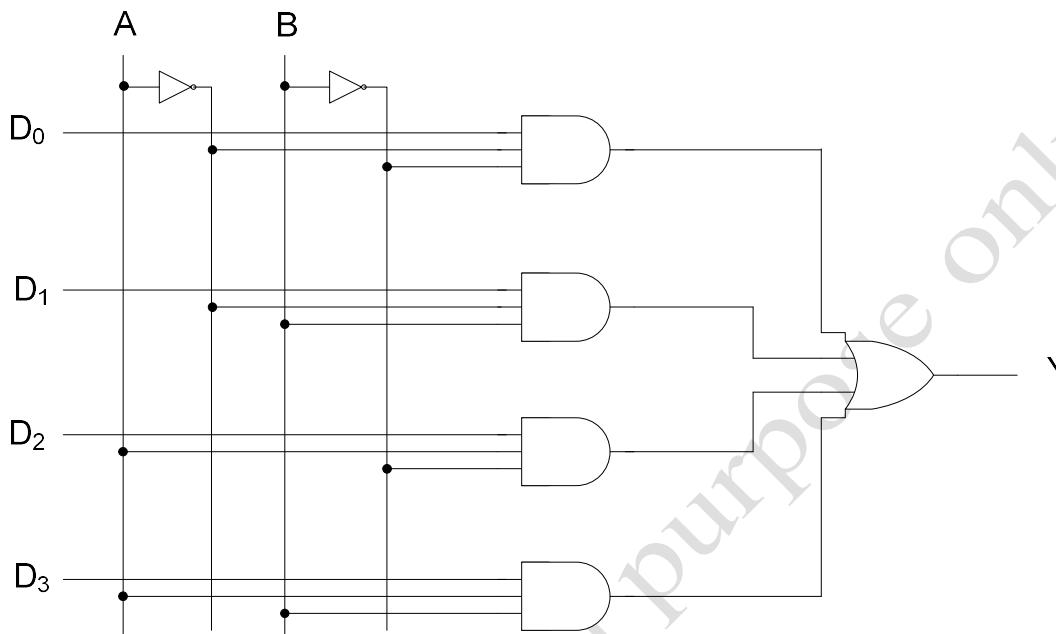


Module 3

Q1. What is a multiplexer? Design a 4 to 1 multiplexer using logic gates. Write the truth table and explain its working principle.

Answer: Multiplexer is a circuit with many inputs but only one output.

Designing of 4 to 1 multiplexer shown below:



Truth table for 4 to 1 MUX:

A	B	Y
0	0	D ₀
0	1	D ₁
1	0	D ₂
1	1	D ₃

Working principle of 4 to 1 multiplexer:

From the above diagram, the Logic Equation for 4 to 1 multiplexer is

$$Y = A'B'D_0 + A'BD_1 + AB'D_2 + ABD_3$$

$$\text{If } A = 0, B = 0 \text{ then, } Y = 0'0'D_0 + 0'0D_1 + 00'D_3 + 00D_3 = 1.1.D_0 + 1.0.D_1 + 0.1.D_2 + 0.0.D_3 = D_0$$

Similarly, if A=0 and B=1 then Y=D₁, if A=1 and B=0 then Y=D₂ and , if A=0 and B=1 then Y=D₃

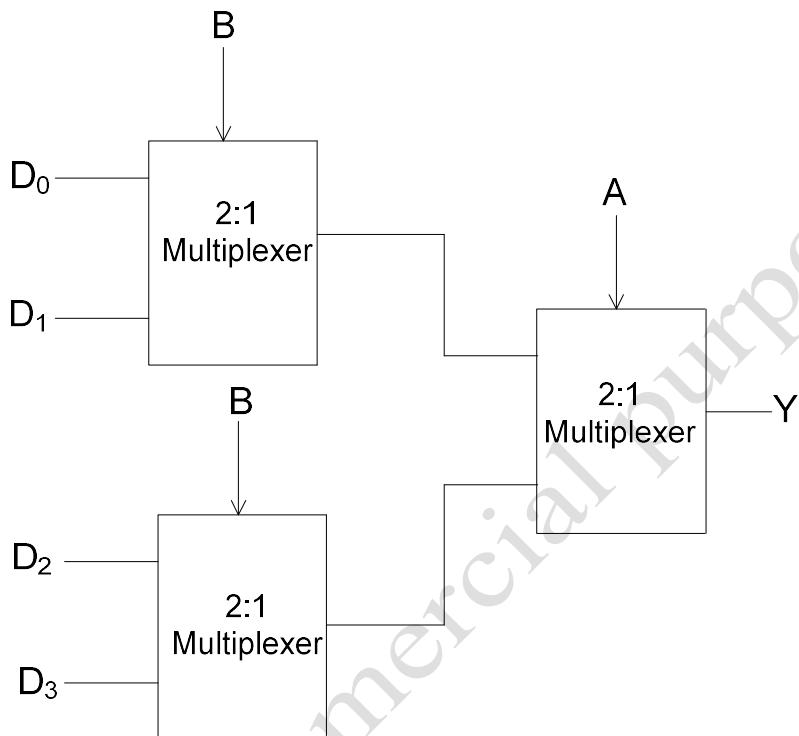
Q2. Construct 4:1 multiplexer using only 2:1 multiplexer.

Answer: Logic Equation for 2:1 Multiplexer is $Y = A'D_0 + AD_1$

Logic equation for 4:1 Multiplexer is $Y = A'B'D_0 + A'BD_1 + AB'D_2 + ABD_3$

$$\Rightarrow Y = A'(B'D_0 + BD_1) + A(B'D_2 + BD_3)$$

We require three 2:1 Multiplexers and the connection is shown below.



Q3. Construct 8:1 multiplexer using only 2:1 multiplexer.

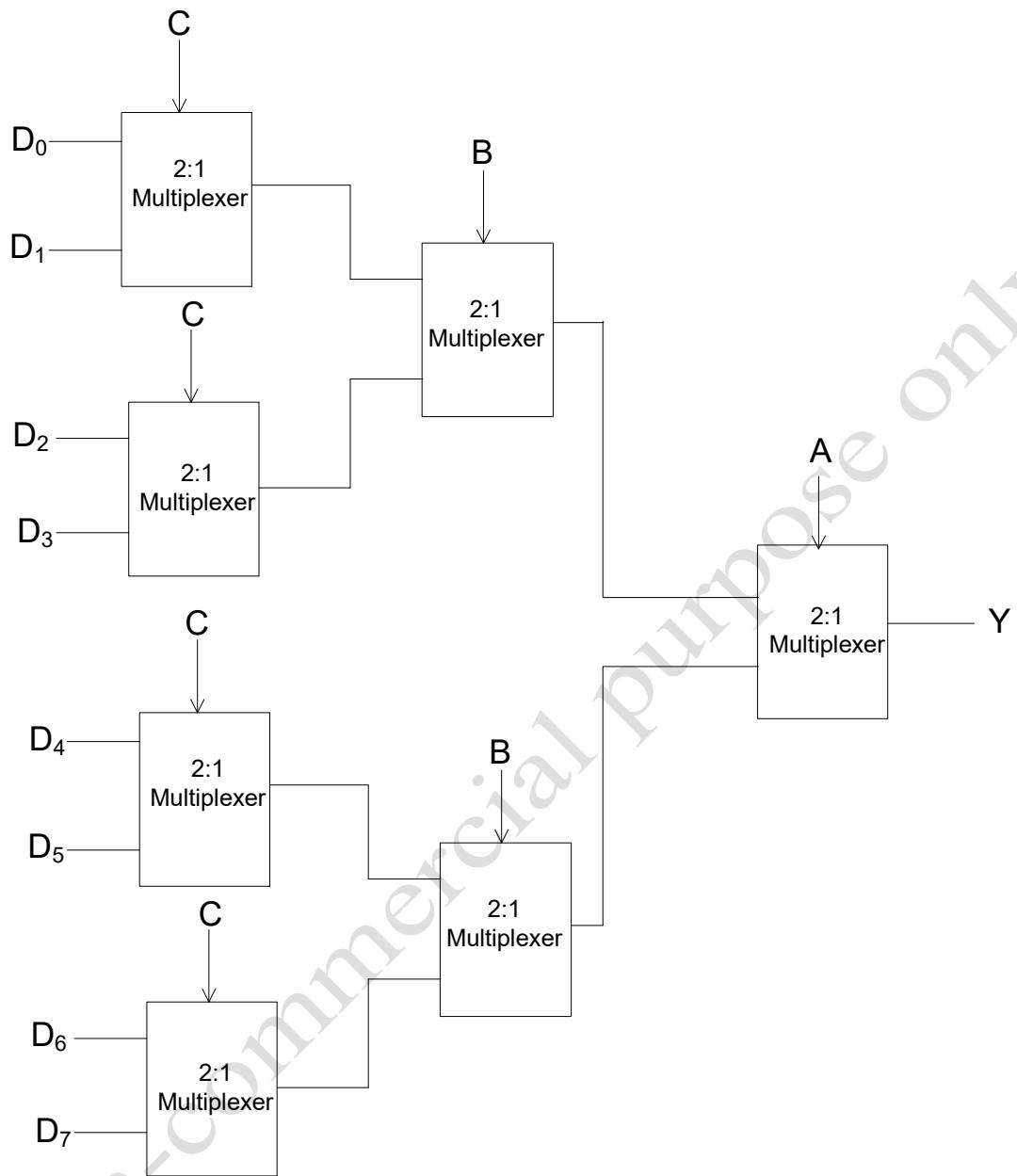
Answer: Logic Equation for 2:1 Multiplexer is $Y = A'D_0 + AD_1$

Logic Equation for 8:1 Multiplexer is

$$Y = A'B'C'D_0 + A'B'CD_1 + A'BC'D_2 + A'BCD_3 + AB'C'D_4 + AB'CD_5 + ABC'D_6 + ABCD_7$$

$$\Rightarrow Y = A'(B'C'D_0 + B'CD_1 + BC'D_2 + BCD_3) + A(B'C'D_4 + B'CD_5 + BC'D_6 + BCD_7)$$

$$\Rightarrow Y = A[B'(C'D_0 + CD_1) + B(C'D_2 + CD_3)] + A[B'(C'D_4 + CD_5) + B(C'D_6 + CD_7)]$$



Q4. Design 16 to 1 multiplexer using 8 to 1 multiplexer and one 2 to 1 multiplexer.

Answer: Logic Equation for 2 :1 Multiplexer is $Y = A'D_0 + AD_1$

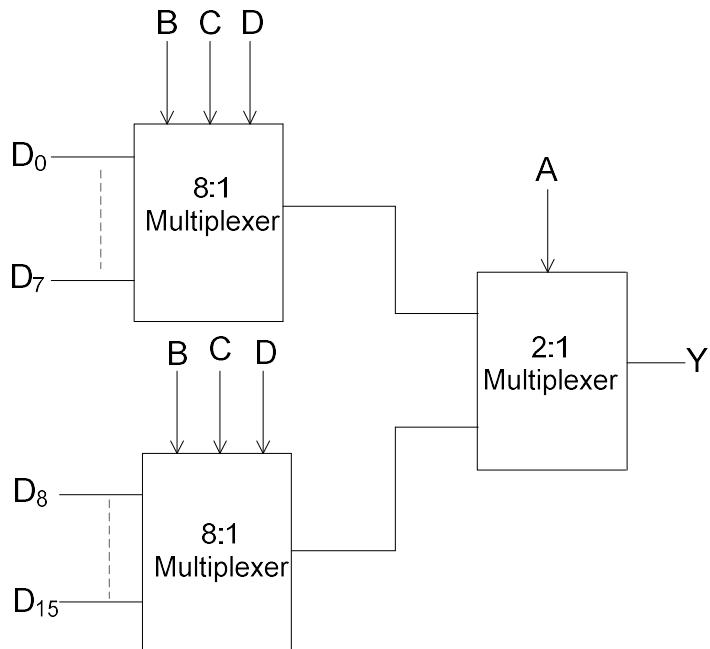
Logic Equation for 8 :1 Multiplexer is

$$Y = A'B'C'D_0 + A'B'CD_1 + A'BC'D_2 + A'BCD_3 + AB'C'D_4 + AB'CD_5 + ABC'D_6 + ABCD_7$$

Logic Equation for 16:1 Multiplexer is

$$Y = A'B'C'D'D_0 + A'B'C'DD_1 + \dots + A'BCD'D_6 + A'BCDD_7 + AB'C'D'_8 + AB'C'D'_9 + \dots + ABCD'D_{14} + ABCDD_{15}$$

$$\Rightarrow Y = A'(B'C'D'D_0 + B'C'DD_1 + \dots + BCD'D_6 + BCDD_7) + A(B'C'D'_8 + B'C'D'_9 + \dots + BCD'D_{14} + BCDD_{15})$$



Q5. Design 32 to 1 multiplexer using 16 to 1 multiplexer and one 2 to 1 multiplexer.

Answer: Logic Equation for 2 :1 Multiplexer is $Y = A'D_0 + AD_1$

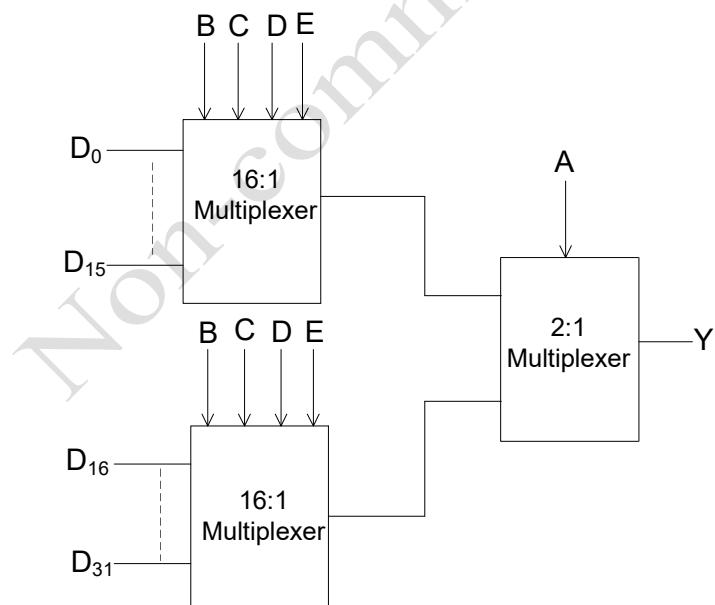
Logic Equation for 16:1 Multiplexer is

$$Y = A'B'C'D'D_0 + A'B'C'DD_1 + \dots + ABCD'D_{14} + ABCDD_{15}$$

Logic Equation for 32 :1 Multiplexer is

$$Y = A'B'C'D'E'D_0 + \dots + A'BCDE'D_{14} + A'BCDED_{15} + AB'C'D'E'D_{16} + \dots + ABCDE'D_{30} + ABCDED_{31}$$

$$\Rightarrow Y = A'(B'C'D'E'D_0 + \dots + BCDE'D_{14} + BCDED_{15}) + A(B'C'D'E'D_{16} + \dots + BCDE'D_{30} + BCDED_{31})$$



Q6. Mention the differences between decoder and demultiplexer.

Answer:

Demultiplexer	Decoder
There is one data input and multiple output. There are selects used as control bits.	There is no data input. The only inputs are the control bit.
The data input appears at one of the output as per the control inputs.	One of the output is high as per the control inputs.
Input appears at the output where subscription of the output is equal to the decimal equivalent to the inputs.	Output becomes high where subscription of the output is equal to the decimal equivalent to the inputs

Q7. (a) Realize $Y = A'B + B'C' + ABC$ using an 8 to 1 Multiplexer.

(b) Can it be realized with a 4 to 1 multiplexer?

Answer : (a) Logic Equation for 8:1 Multiplexer is

$$Y = A'B'C'D_0 + A'B'CD_1 + A'BC'D_2 + A'BCD_3 + AB'C'D_4 + AB'CD_5 + ABC'D_6 + ABCD_7$$

We should express Y as a function of three variables i.e function of minterms.

$$Y = A'B + B'C' + ABC$$

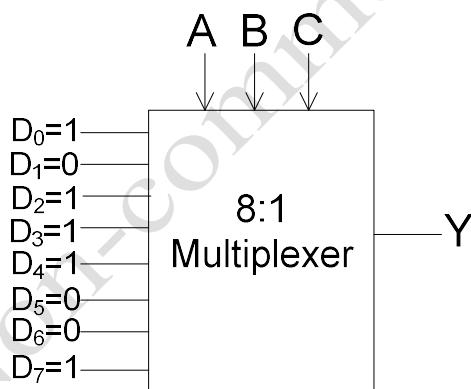
$$\Rightarrow Y = A'B(C + C') + B'C'(A + A') + ABC$$

$$\Rightarrow Y = A'BC + A'BC' + AB'C' + A'B'C' + ABC$$

$$\Rightarrow Y = A'B'C' + A'BC' + A'BC + AB'C' + ABC$$

Comparing with the Logic equation of 8:1 Multiplexer, we have

$$D_0 = D_2 = D_3 = D_4 = D_7 = 1 \text{ and } D_1 = D_5 = D_6 = 0$$



$$(b) Y = A'B + B'C' + ABC$$

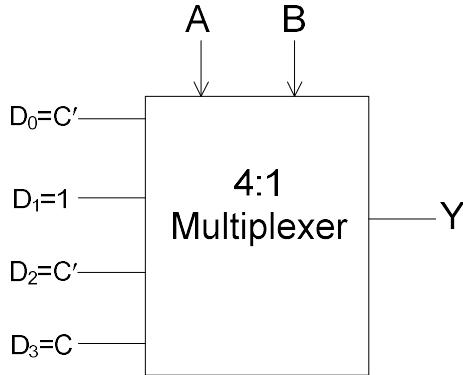
$$\Rightarrow Y = A'B + B'C'(A + A') + ABC$$

$$\Rightarrow Y = A'B + AB'C' + A'B'C' + ABC$$

$$\Rightarrow Y = A'B'C' + A'B.C + AB'C' + ABC$$

Logic equation for 4:1 Multiplexer is $Y = A'B'D_0 + A'BD_1 + AB'D_2 + ABD_3$

We have, $D_0 = C'$, $D_1 = 1$, $D_2 = C'$ and $D_3 = C$



Q8. Implement the following Boolean functions using 4:1 multiplexer (MUX):

$$(i) Y = f(A, B, C, D) = \sum m(0, 1, 2, 4, 6, 9, 12, 14)$$

$$(ii) F(A, B, C) = \sum m(1, 3, 5, 6)$$

Answer: Logic equation for 4:1 Multiplexer is $Y = A'B'D_0 + A'BD_1 + AB'D_2 + ABD_3$

$$Y = f(A, B, C, D) = \sum m(0, 1, 2, 4, 6, 9, 12, 14)$$

$$\Rightarrow Y = A'B'C'D' + A'B'C'D + A'B'CD' + A'BC'D' + A'BCD' + AB'C'D + ABC'D' + ABCD'$$

$$\Rightarrow Y = A'B'(C'D' + C'D + CD') + A'B(C'D' + CD') + AB'C'D + AB(C'D' + CD')$$

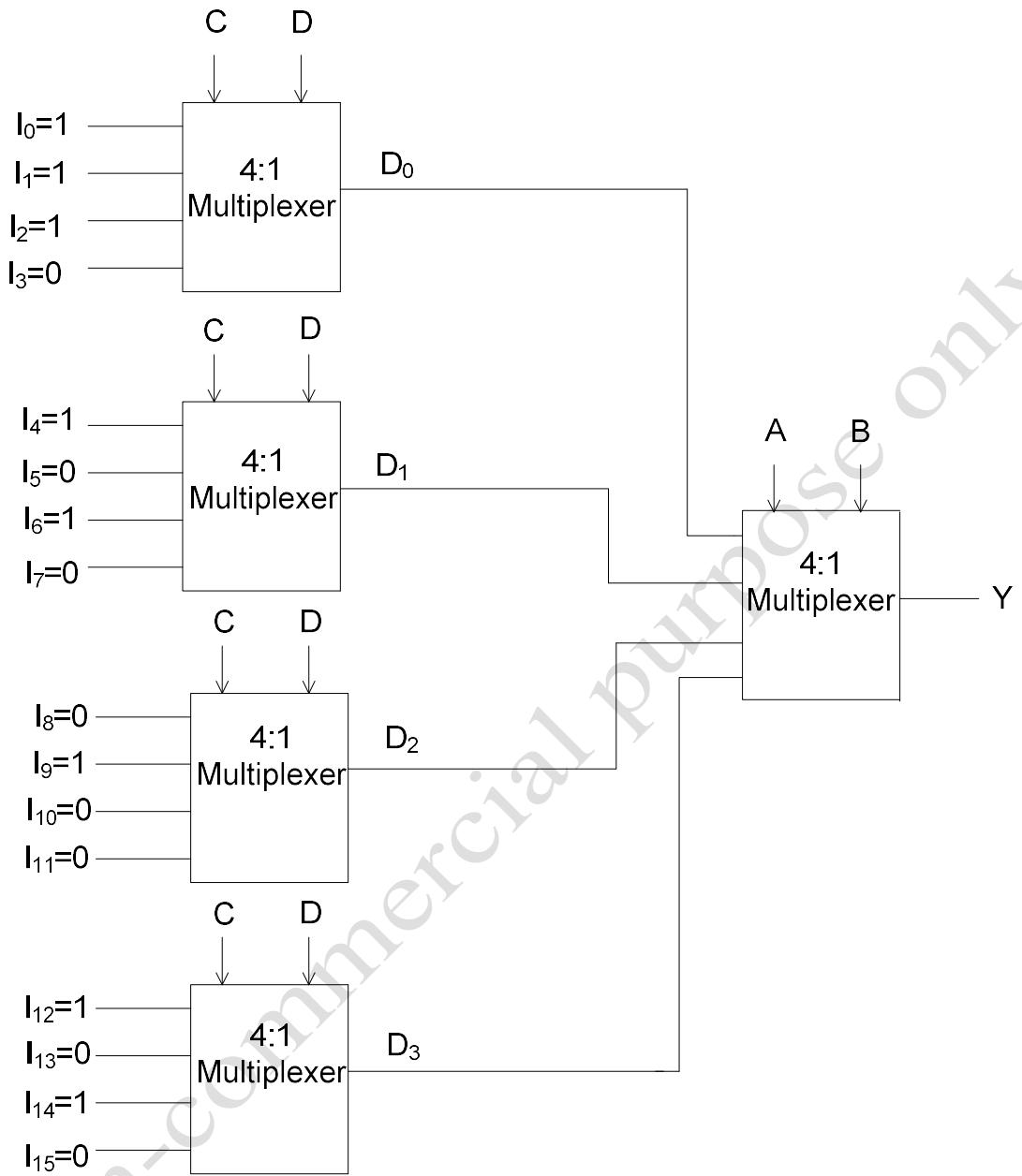
Comparing with Logic Equation of 4:1 Multiplexer, We have

$$D_0 = C'D' + C'D + CD' \Rightarrow D_0 = C'D'.1 + C'D.1 + CD'.1 + CD.0$$

$$D_1 = C'D' + CD' \Rightarrow D_1 = C'D'.1 + C'D.0 + CD'.1 + CD.0$$

$$D_2 = C'D \Rightarrow D_2 = C'D'.0 + C'D.1 + CD'.0 + CD.0$$

$$D_3 = C'D' + CD' \Rightarrow D_3 = C'D'.1 + C'D.0 + CD'.1 + CD.0$$



(ii) Logic equation for 4:1 Multiplexer is $Y = A'B'D_0 + A'BD_1 + AB'D_2 + ABD_3$

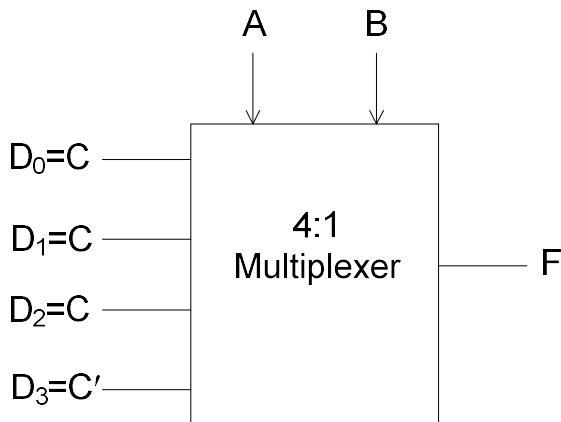
$$F(A, B, C) = \sum m(1, 3, 5, 6)$$

$$\Rightarrow F = A'B'C + A'BC + AB'C + ABC'$$

$$\Rightarrow F = A'B.C + A'B.C + AB.C + AB.C'$$

Comparing with Logic Equation of 4:1 Multiplexer, we have

$$D_0 = C, D_1 = C, D_2 = C \text{ and } D_3 = C'$$



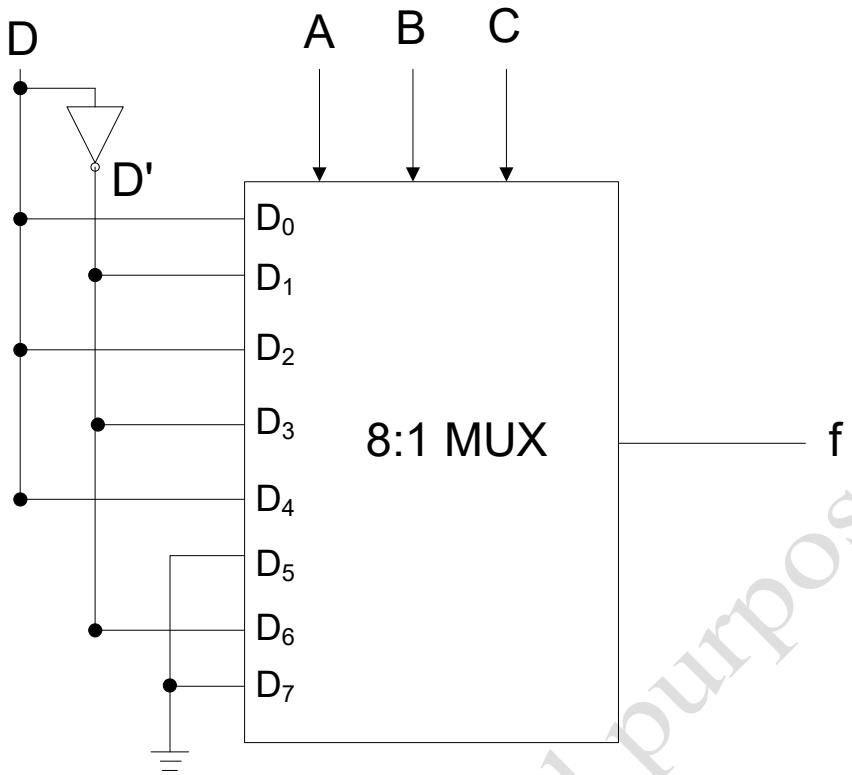
Q9. Implement the Boolean function expressed by SOP:

$$f(A, B, C, D) = \sum m(1, 2, 5, 6, 9, 12)$$

Answer:

ABC	000	001	010	011	100	101	110	111
D=0	0	1	0	1	0	0	1	0
D=1	1	0	1	0	1	0	0	0
f	1	0	d	d'	d'	d'	d'	d
8:1 MUX data input	D ₀ =D	D ₁ =D'	D ₂ =D	D ₃ =D'	D ₄ =D	D ₅ =0	D ₆ =D'	D ₇ =0

Circuit diagram:



Q10. Implement the Boolean function:

$F(A, B, C, D) = \sum m(0, 1, 2, 4, 5, 7, 8, 9)$ using 8 to 1 multiplexers. Draw the logic diagram and explain the operation. Additional gates can be used if required.

Answer : (a) Logic Equation for 8:1 Multiplexer is

$$Y = A'B'C'D_0 + A'B'CD_1 + A'BC'D_2 + A'BCD_3 + AB'C'D_4 + AB'CD_5 + ABC'D_6 + ABCD_7$$

Logic Equation for 2:1 Multiplexer is $Y = A'D_0 + AD_1$

$$F(A, B, C, D) = \sum m(0, 1, 2, 4, 5, 7, 8, 9)$$

$$\Rightarrow F = A'B'C'D' + A'B'C'D + A'B'CD' + A'BC'D' + A'BC'D + A'BCD + AB'C'D' + AB'C'D$$

$$\Rightarrow F = A'(B'C'D' + B'C'D + B'CD' + BC'D' + BC'D + BCD) + A(B'C'D' + B'C'D)$$

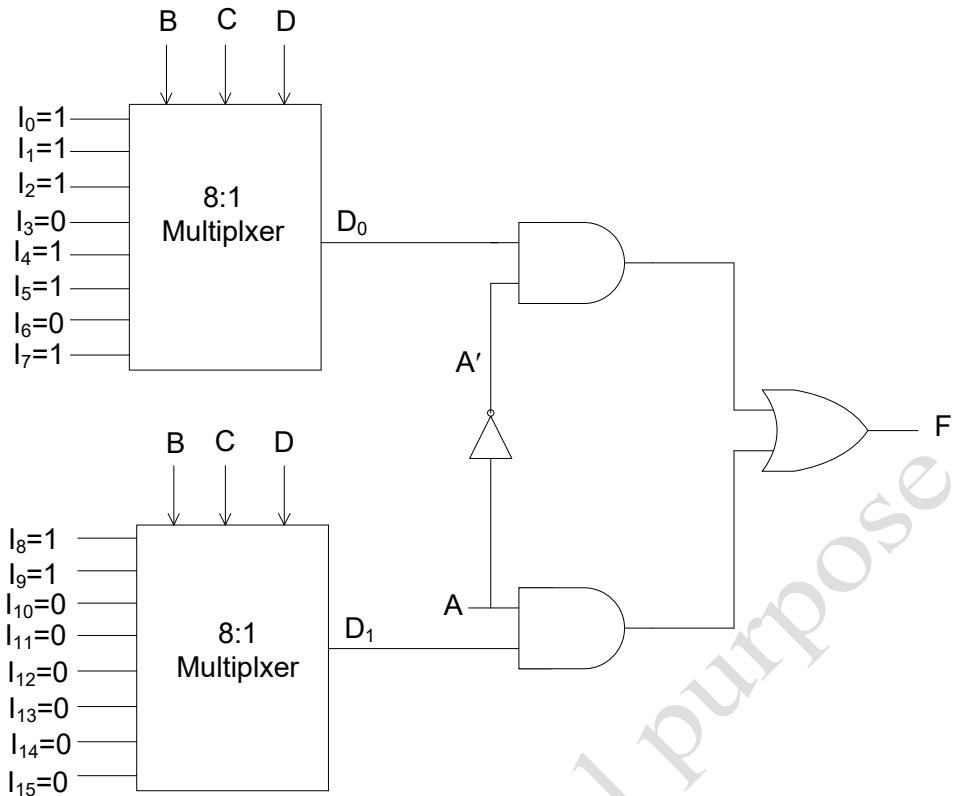
Comparing with 2:1 Logic Equation, we have

$$D_0 = B'C'D' + B'C'D + B'CD' + BC'D' + BC'D + BCD$$

$$\Rightarrow D_0 = B'C'D'.1 + B'C'D.1 + B'CD'.1 + B'CD.0 + BC'D'.1 + BC'D.0 + BCD'.0 + BCD.1$$

$$D_1 = B'C'D' + B'C'D$$

$$\Rightarrow D_1 = B'C'D'.1 + B'C'D.1 + B'CD'.0 + B'CD.0 + BC'D'.0 + BC'D.0 + BCD'.0 + BCD.0$$



(Note: Q9 and Q10 are similar. But method for Q9 is preferable)

Q11. Realize the following Boolean function:

$$P = f(w, x, y, z) = \sum(0, 1, 5, 6, 7, 10, 15) \text{ using (i) 16:1 MUX (ii) 8:1 MUX (iii) 4:1 MUX}$$

Answer : (i) Logic Equation for 16:1 Multiplexer is

$$\begin{aligned} P = & w'x'y'z'.D_0 + w'x'y'z.D_1 + w'x'yz'.D_2 + w'x'yz.D_3 + w'xy'z'.D_4 + w'xy'z.D_5 + w'xyz'.D_6 + w'xyz.D_7 + wx'y'z'.D_8 \\ & + wx'y'z.D_9 + wx'yz'.D_{10} + wx'yz.D_{11} + wxy'z'.D_{12} + wxy'z.D_{13} + wxyz'.D_{14} + wxyz.D_{15} \end{aligned}$$

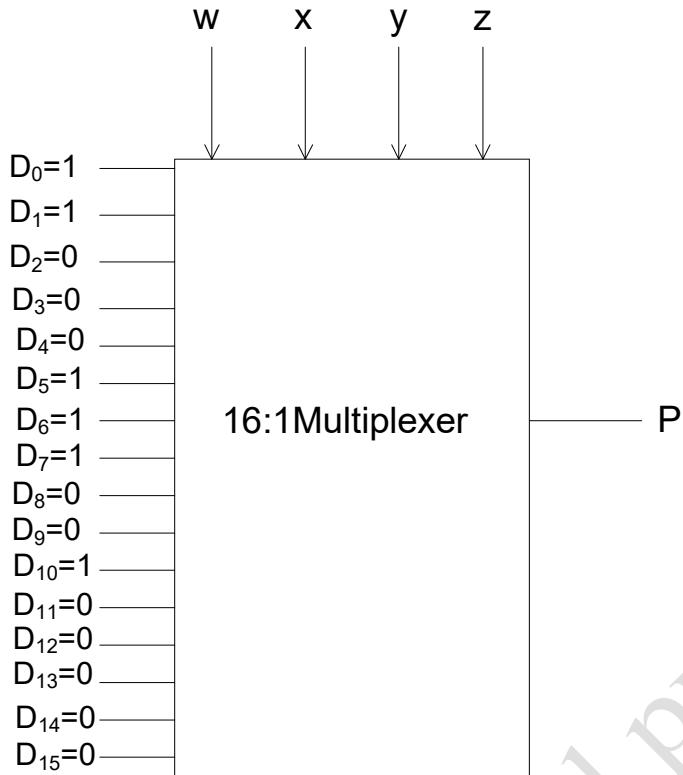
$$P = f(w, x, y, z) = \sum m(0, 1, 5, 6, 7, 10, 15)$$

$$\Rightarrow P = w'x'y'z' + w'x'y'z + w'xy'z + w'xyz' + w'xyz + wx'y'z' + wxyz$$

$$\begin{aligned} \Rightarrow P = & w'x'y'z'.1 + w'x'y'z.1 + w'x'yz'.0 + w'x'yz.0 + w'xy'z'.0 + w'xy'z.1 + w'xyz'.1 + w'xyz.1 + wx'y'z'.0 \\ & + wx'y'z.0 + wx'yz'.1 + wx'yz.0 + wxy'z'.0 + wxy'z.0 + wxyz'.0 + wxyz.1 \end{aligned}$$

Comparing with Logic Equation for 16:1 Multiplexer, we have

$$D_0 = D_1 = D_5 = D_6 = D_7 = D_{10} = D_{15} = 1 \text{ and } D_2 = D_3 = D_4 = D_8 = D_9 = D_{11} = D_{12} = D_{13} = D_{14} = 0$$



(ii) Logic Equation for 8:1 Multiplexer is

$$Y = x'y'z'I_0 + x'y'z'I_1 + x'yz'I_2 + x'yz'I_3 + xy'z'I_4 + xy'z'I_5 + xyz'I_6 + xyz'I_7$$

Logic Equation for 2:1 Multiplexer is $Y = w'D_0 + wD_1$

$$P = f(w, x, y, z) = \sum m(0, 1, 5, 6, 7, 10, 15)$$

$$\Rightarrow P = w'x'y'z' + w'x'y'z + w'xy'z + w'xyz' + w'xyz + wx'y'z' + wxyz$$

$$\Rightarrow P = w'(x'y'z' + x'y'z + xy'z + xyz' + xyz) + w(x'y'z' + xyz)$$

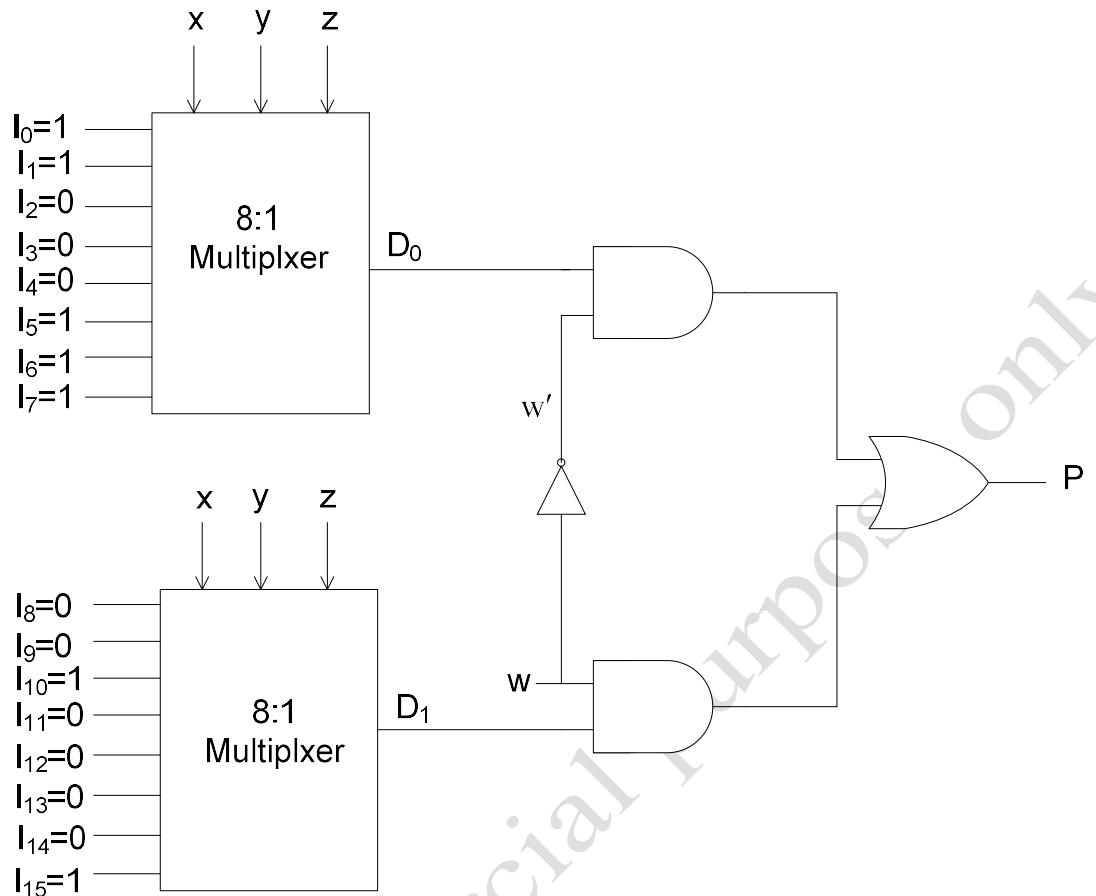
$$\Rightarrow P = w'(x'y'z'.1 + x'y'z.1 + x'yz'.0 + x'yz.0 + xy'z'.0 + xy'z.1 + xyz'.1 + xyz.1)$$

$$+ w(x'y'z'.0 + x'y'z.0 + x'yz'.1 + x'yz.0 + xy'z'.0 + xy'z.0 + xyz'.0 + xyz.1)$$

Comparing with Logic Equation of 2:1 Multiplexer, we have

$$D_0 = x'y'z'.1 + x'y'z.1 + x'yz'.0 + x'yz.0 + xy'z'.0 + xy'z.1 + xyz'.1 + xyz.1$$

$$D_1 = x'y'z'.0 + x'y'z.0 + x'yz'.1 + x'yz.0 + xy'z'.0 + xy'z.0 + xyz'.0 + xyz.1$$



(iii) Logic equation for 4:1 Multiplexer is $Y = w'x'D_0 + w'xD_1 + wx'D_2 + wxD_3$

$$P = f(w, x, y, z) = \sum m(0, 1, 5, 6, 7, 10, 15)$$

$$\Rightarrow P = w'x'y'z' + w'x'y'z + w'xy'z + w'xyz' + w'xyz + wx'yz' + wxyz$$

$$\Rightarrow P = w'x'(y'z' + y'z) + w'x(y'z + yz' + yz) + wx'yz' + wxyz$$

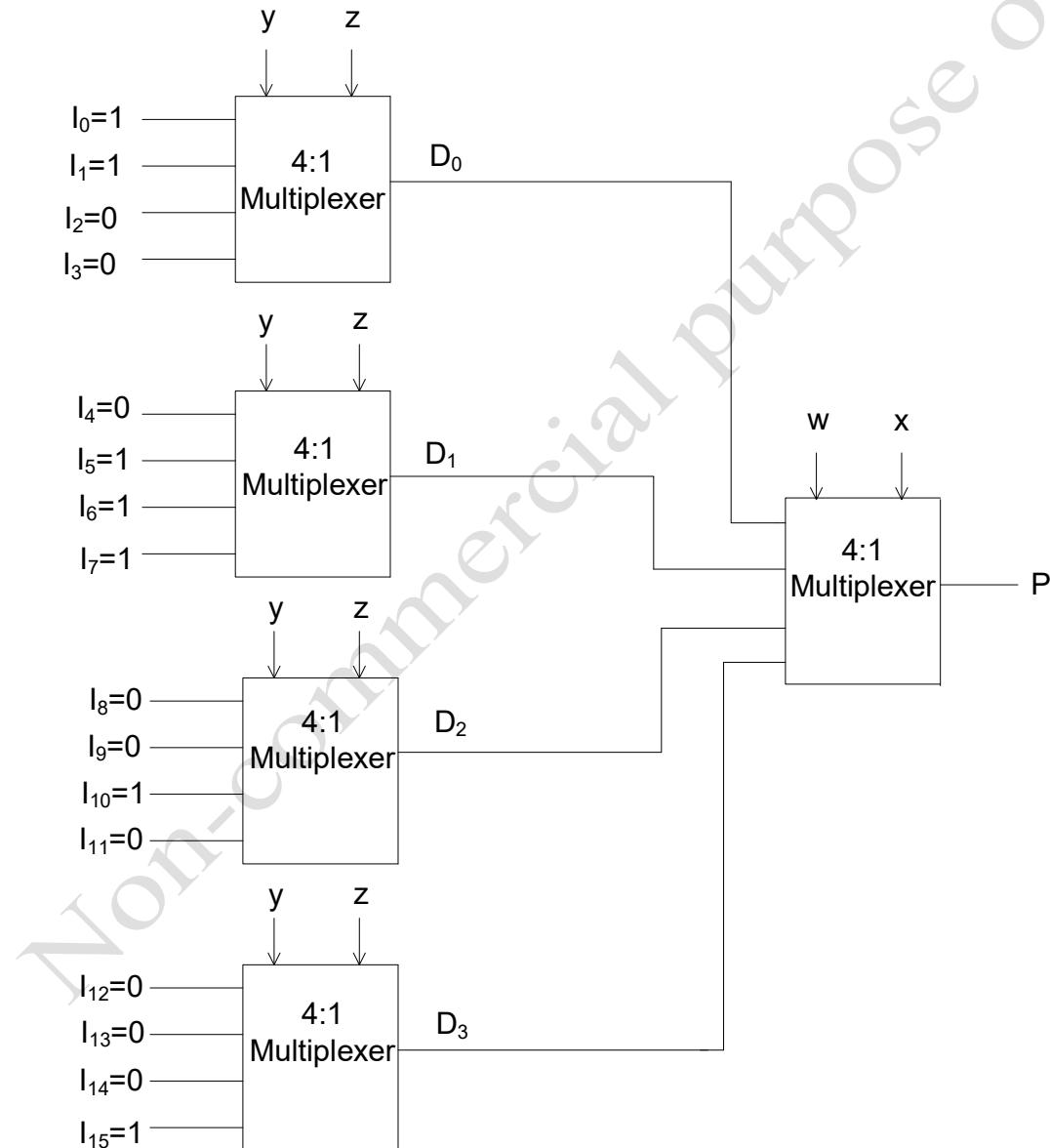
Comparing with Logic Equation for 4:1 Multiplexer, we have

$$D_0 = y'z' + y'z \Rightarrow D_0 = y'z'.1 + y'z.1 + yz'.0 + yz.0$$

$$D_1 = y'z + yz' + yz \Rightarrow D_1 = y'z'.0 + y'z.1 + yz'.1 + yz.1$$

$$D_2 = yz' = y'z'.0 + y'z.0 + yz'.1 + yz.0$$

$$D_3 = yz = y'z'.0 + y'z.0 + yz'.0 + yz.1$$



Q12. Design and implement BCD to excess-3 code converter using four 8:1 multiplexers. Take MSB ‘A’ as main entered variable(input variable) ‘BCD’ lines as select lines, assuming f(A,B,C,D) as BCD input.

Answer: Truth table for converting BCD to Excess-3

BCD				Excess-3			
A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

Designing of the multiplexer whose output is W

BCD	000	001	010	011	100	101	110	111
A=0	0	0	0	0	0	1	1	1
A=1	1	1	X	X	X	X	X	X
W	A	A	0	0	0	1	1	1
8:1 MUX Data Input	D ₀ =A	D ₁ =A	D ₂ =0	D ₃ =0	D ₄ =0	D ₅ =1	D ₆ =1	D ₇ =1

Designing of the multiplexer whose output is X

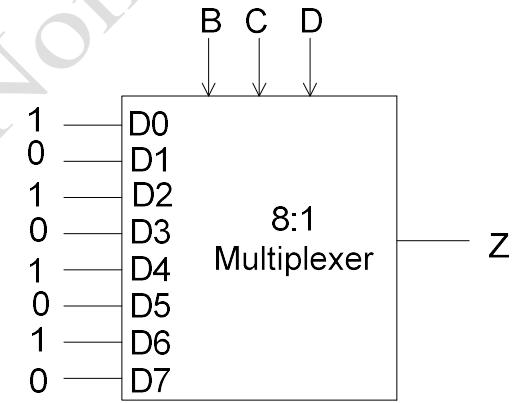
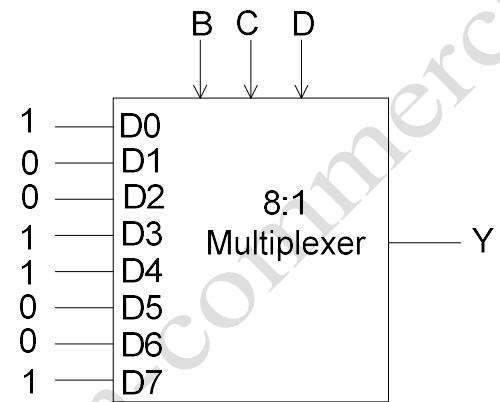
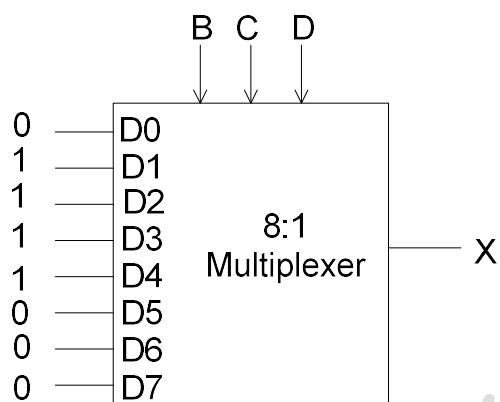
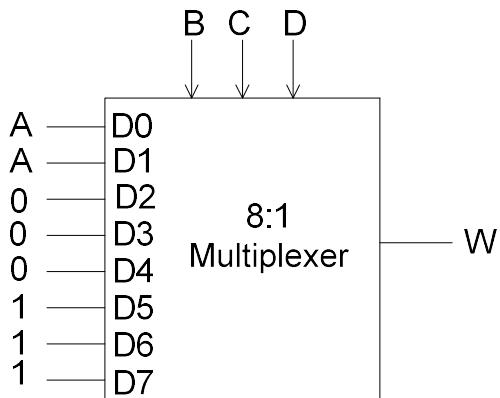
BCD	000	001	010	011	100	101	110	111
A=0	0	1	1	1	1	0	0	0
A=1	0	1	X	X	X	X	X	X
X	0	1	1	1	1	0	0	0
8:1 MUX Data Input	D ₀ =0	D ₁ =1	D ₂ =1	D ₃ =1	D ₄ =1	D ₅ =0	D ₆ =0	D ₇ =0

Designing of the multiplexer whose output is Y

BCD	000	001	010	011	100	101	110	111
A=0	1	0	0	1	1	0	0	1
A=1	1	0	X	X	X	X	X	X
Y	1	0	0	1	1	0	0	1
8:1 MUX Data Input	D ₀ =1	D ₁ =0	D ₂ =0	D ₃ =1	D ₄ =1	D ₅ =0	D ₆ =0	D ₇ =1

Designing of the multiplexer whose output is Z

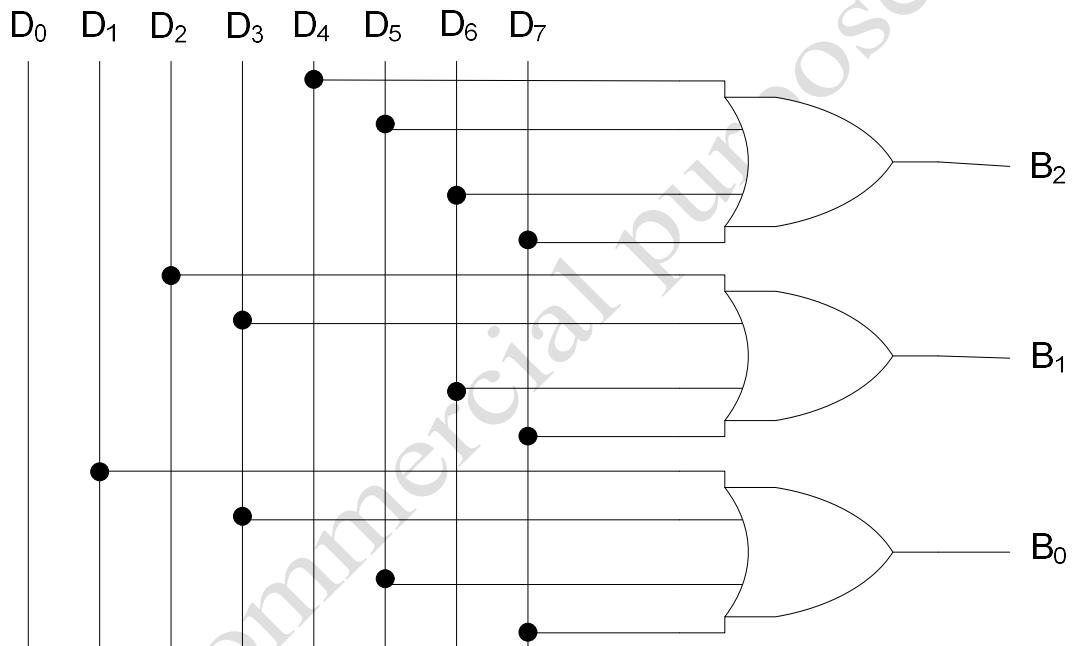
BCD	000	001	010	011	100	101	110	111
A=0	1	0	1	0	1	0	1	0
A=1	1	0	X	X	X	X	X	X
Z	1	0	1	0	1	0	1	0
Data Input	D ₀ =1	D ₁ =0	D ₂ =1	D ₃ =0	D ₄ =1	D ₅ =0	D ₆ =1	D ₇ =0



Q13. Realize a logic circuit for octal to binary encoder.

Answer: Truth table for octal to binary encoder

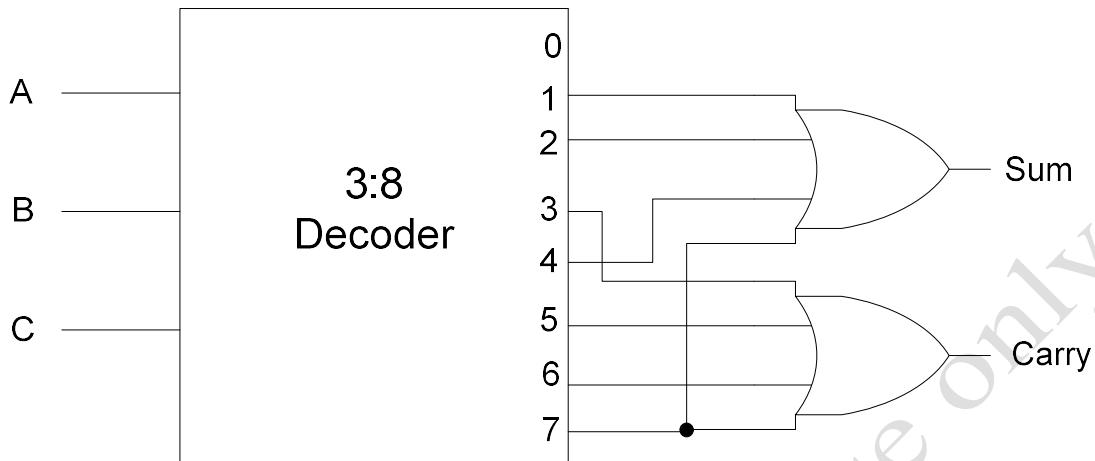
Input								Output		
D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	B ₂	B ₁	B ₀
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1



Q14. Implement a full adder using a 3 to 8 decoder.

Answer: Truth table for full adder

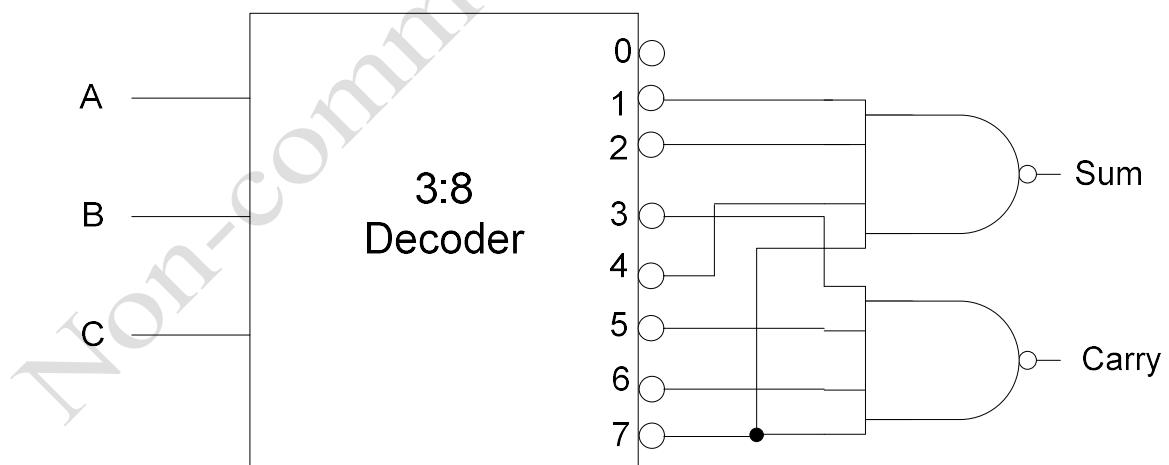
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Q15. Implement full adder using IC 74138

Answer: Truth table for full adder

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

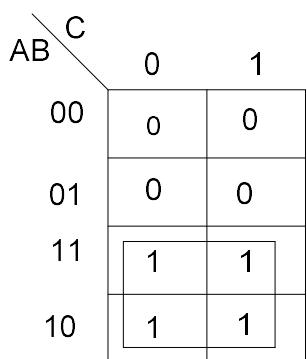


Q16. Implement 3 bit binary to gray code conversion by using IC 74139.

Answer: Truth table for converting 3 bit binary to gray code

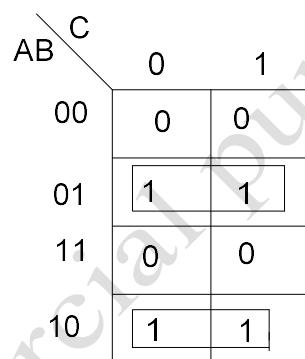
Binary code			Gray code		
A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

K-Map for X:



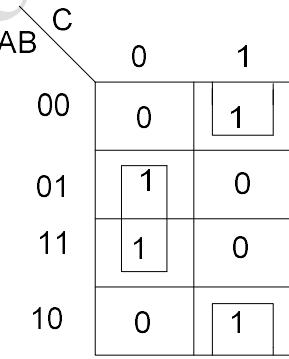
$$X=A$$

K-Map for Y:

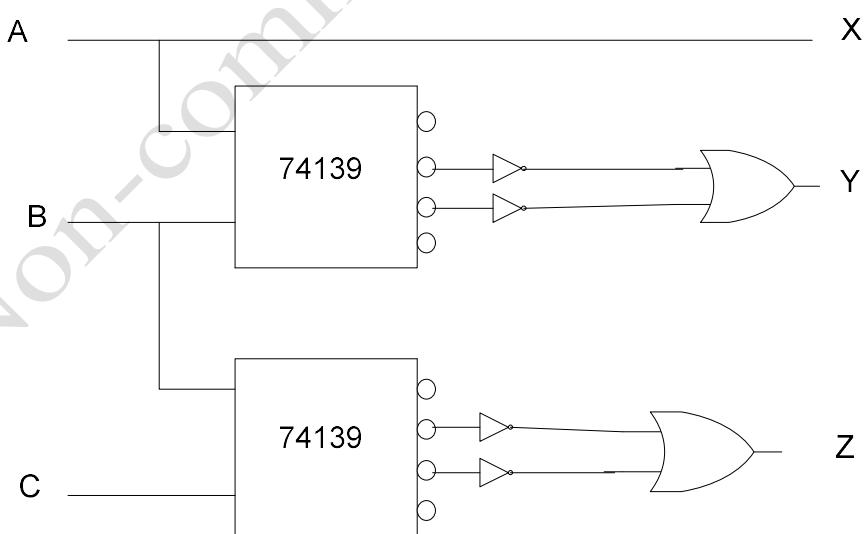


$$Y=\bar{A}B+A\bar{B}$$

K-Map for Z:



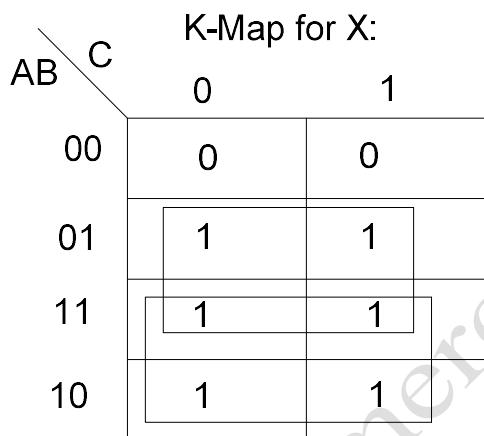
$$Z=B\bar{C}+\bar{B}C$$



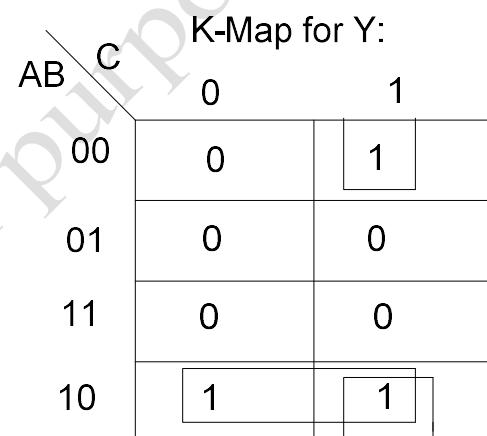
Q17. Design a priority encoder for a system with 3 inputs, the middle bit with highest priority encoding to 10, the MSB with the next priority encoding to 11, while the LSB with least priority encoding to 01.

Answer: Truth table of the priority encoder

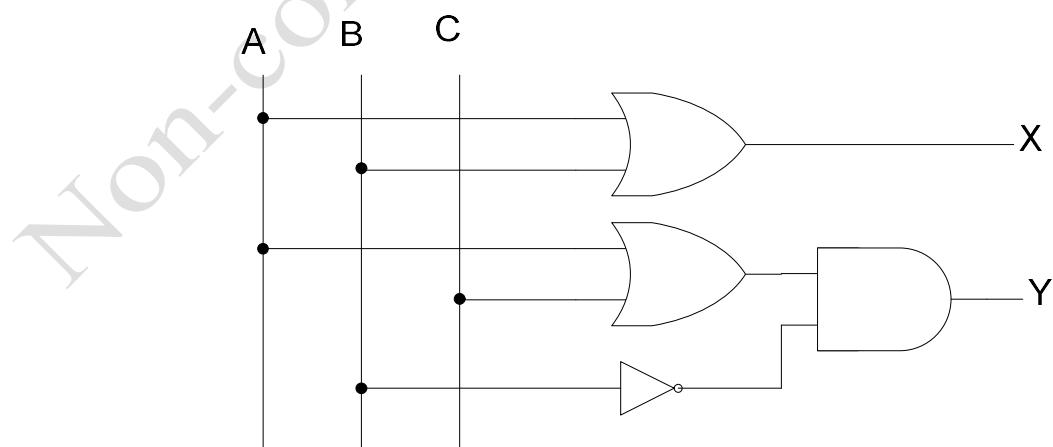
Input			Output	
A	B	C	X	Y
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	0
1	1	1	1	0



$$X = A + B$$

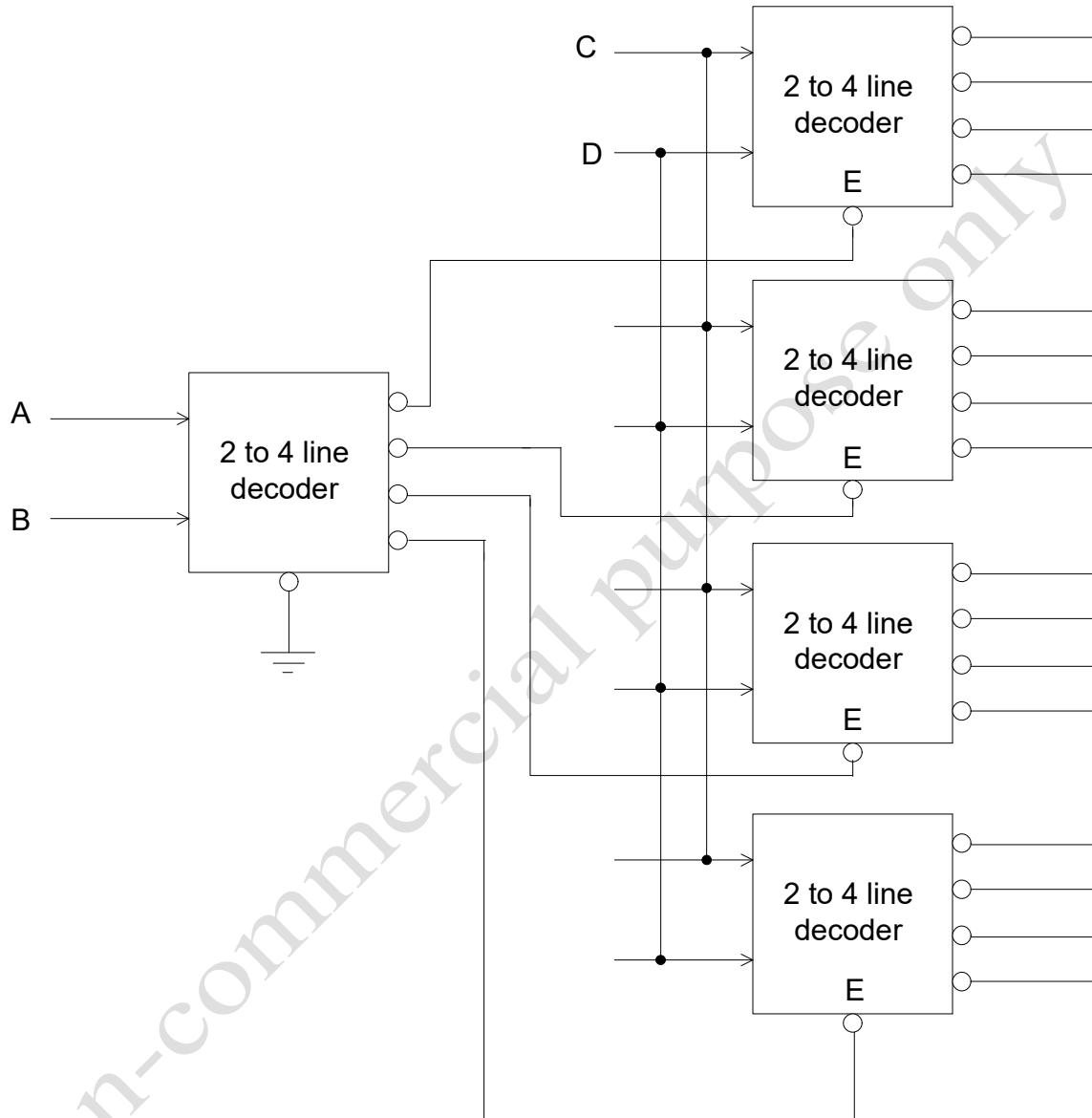


$$Y = \bar{A}\bar{B} + \bar{B}C = \bar{B}(A + C)$$



Q18. Design a 4 to 16 line decoder using 2 to 4 line decoder which has the active low outputs as active low enable input. Explain its operation.

Answer:



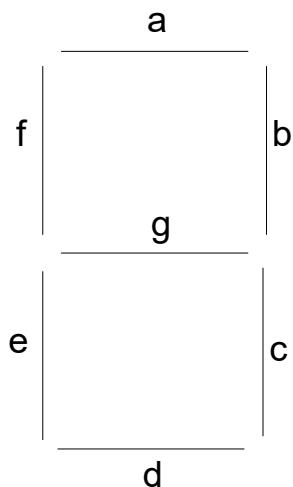
Q19. Write the comparisons between PLA and PAL.

Answer:

PAL	PLA
The output OR-gate array is fixed while the input AND gate array is fusible linked and thus programmable.	Both output OR-gate array and input AND gate array are fusible linked.
PAL is easier to program.	PLA is more complicated since the number fusible links are more compared to PAL
PAL is less expensive.	PLA is more expensive compared to PAL.

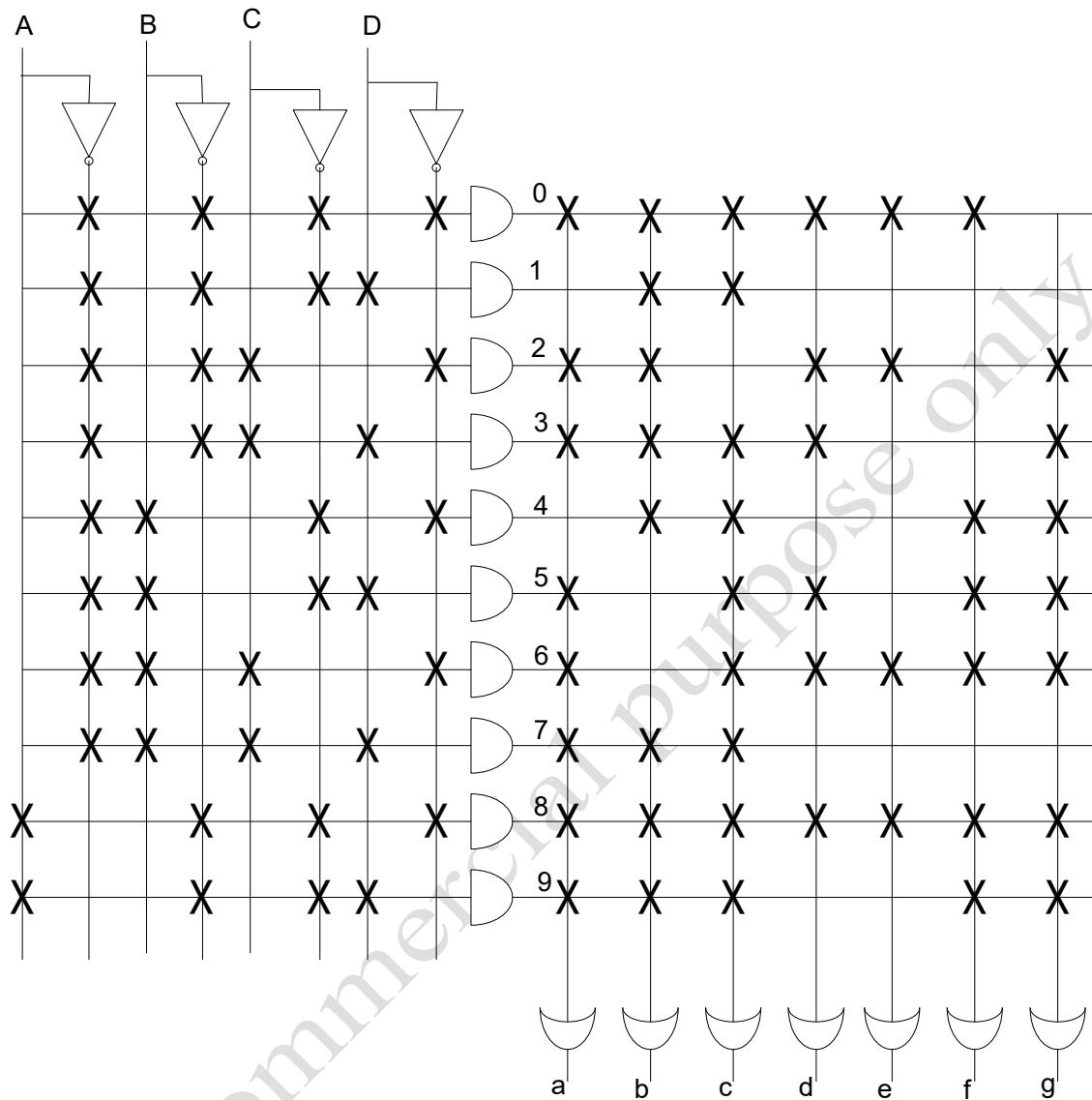
Q20. Design 7-segments decoder using PLA.

Answer: Seven segment indicator:



Following table shows the segments should light up to display a number.

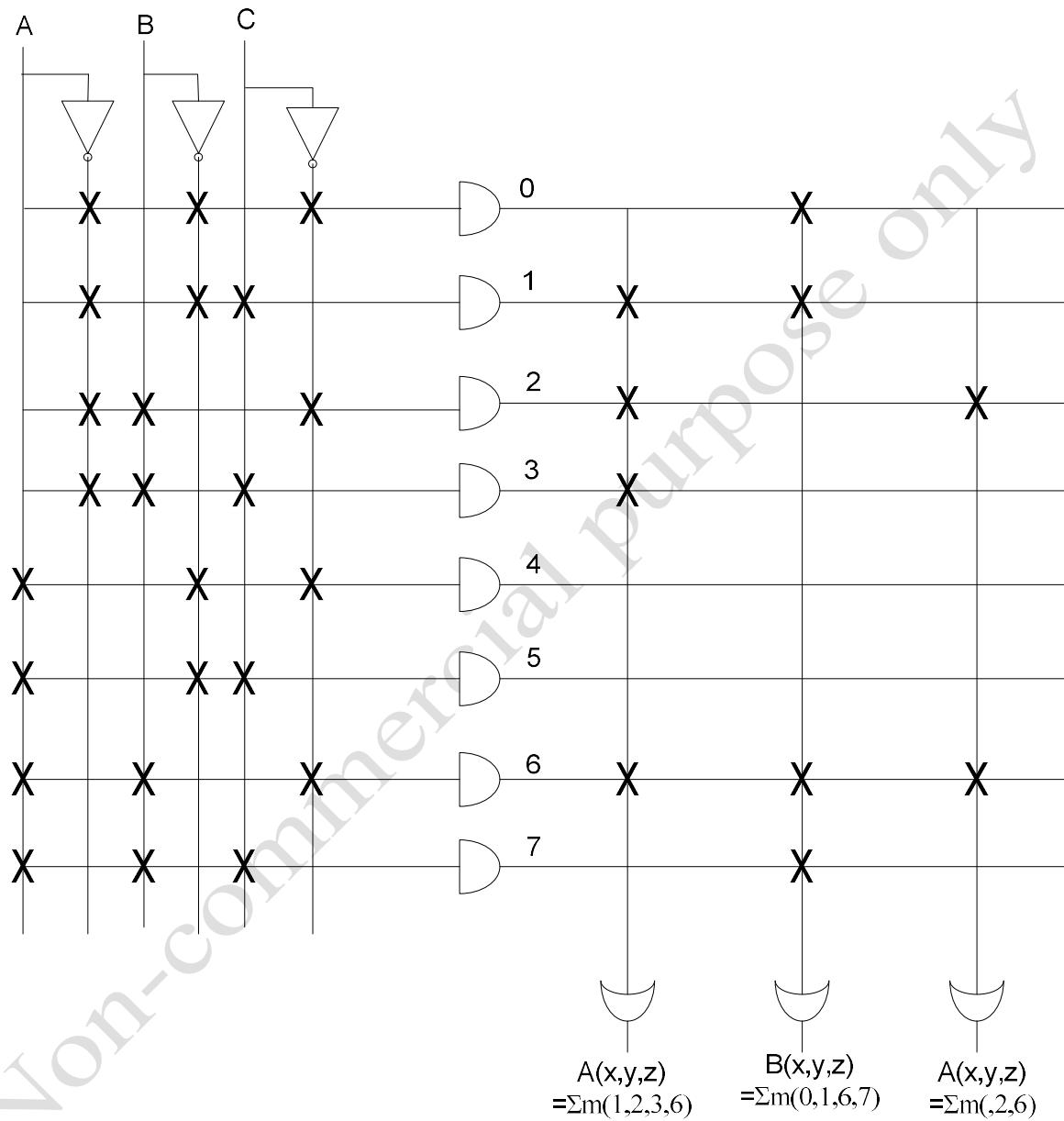
Number to display	Segments to light up
0	a,b,c,d,e,f
1	b,c
2	a,b,d,e,g
3	a,b,c,d,g
4	b,c,f,g
5	a,c,d,f
6	a,c,d,e,f,g
7	a,b,c
8	a,b,c,d,e,f,g
9	a,b,c,f,g



Q21. Implement the following function using PLA:

$$A(x,y,z) = \sum m(1,2,3,6); B(x,y,z) = \sum m(0,1,6,7); C(x,y,z) = \sum m(2,6)$$

Answer:



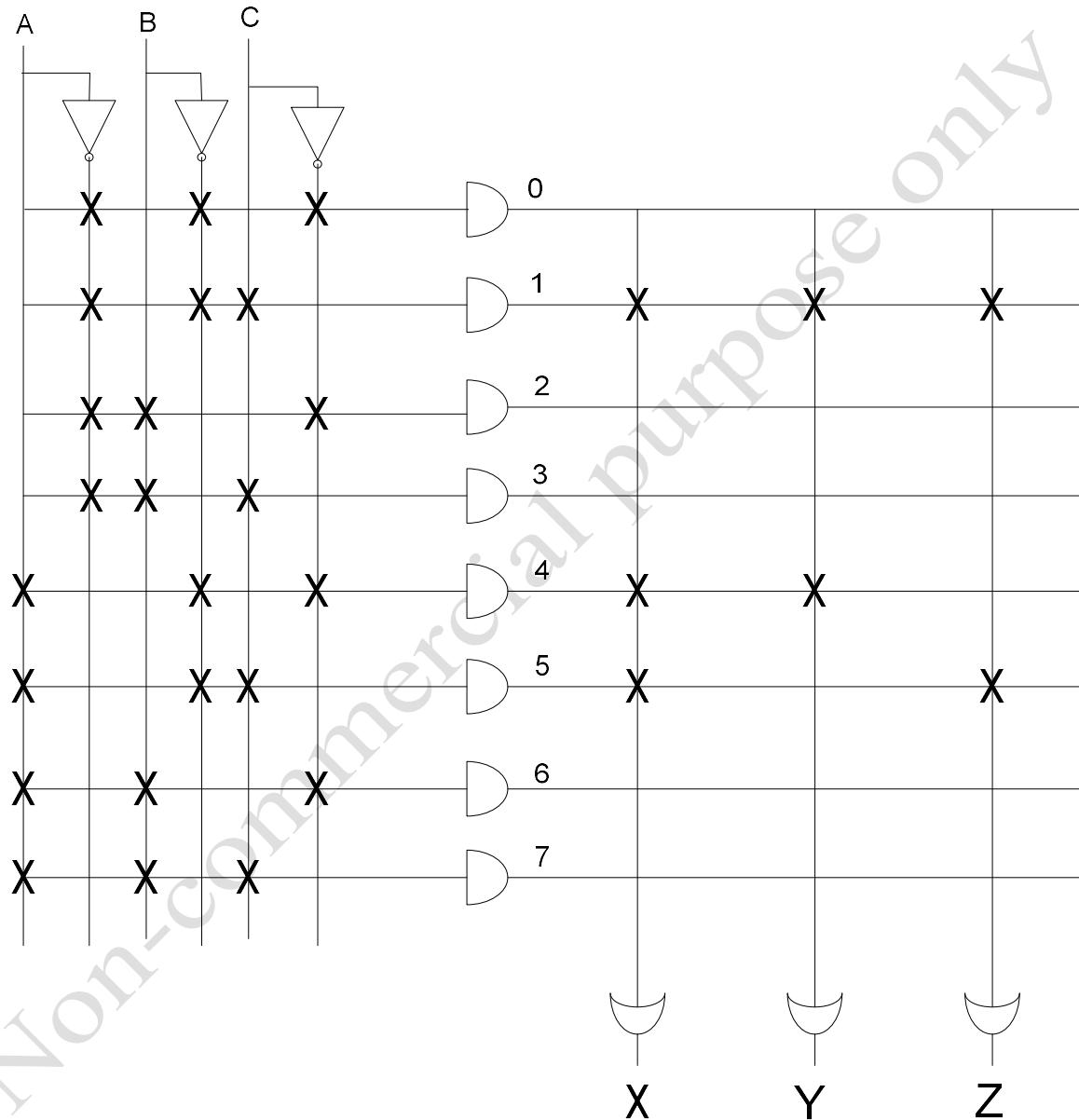
Q22. Draw the PLA circuit and realize the Boolean functions:

$$X = A'B'C + AB'C' + B'C, Y = A'B'C + AB'C', Z = B'C$$

$$\text{Answer : } X = A'B'C + AB'C' + B'C = A'B'C + AB'C' + B'C(A + A') = A'B'C + AB'C' + AB'C$$

$$Y = A'B'C + AB'C'$$

$$Z = B'C = B'C(A + A') = AB'C + A'B'C$$



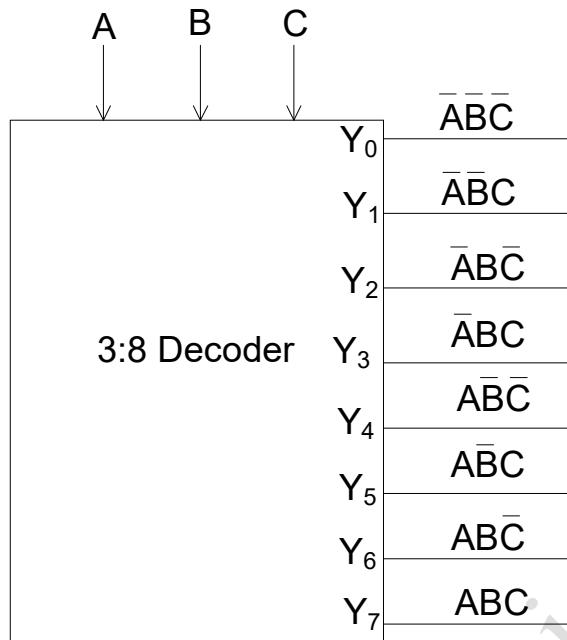
Q23. Describe the working principle of 3:8 decoder. Design a circuit that realizes the following

functions using a 3:8 decoder and multi input OR gates.

$$(i) F_1(A, B, C) = \sum m(1, 3, 7) \quad (ii) F_2(A, B, C) = \sum m(2, 3, 5)$$

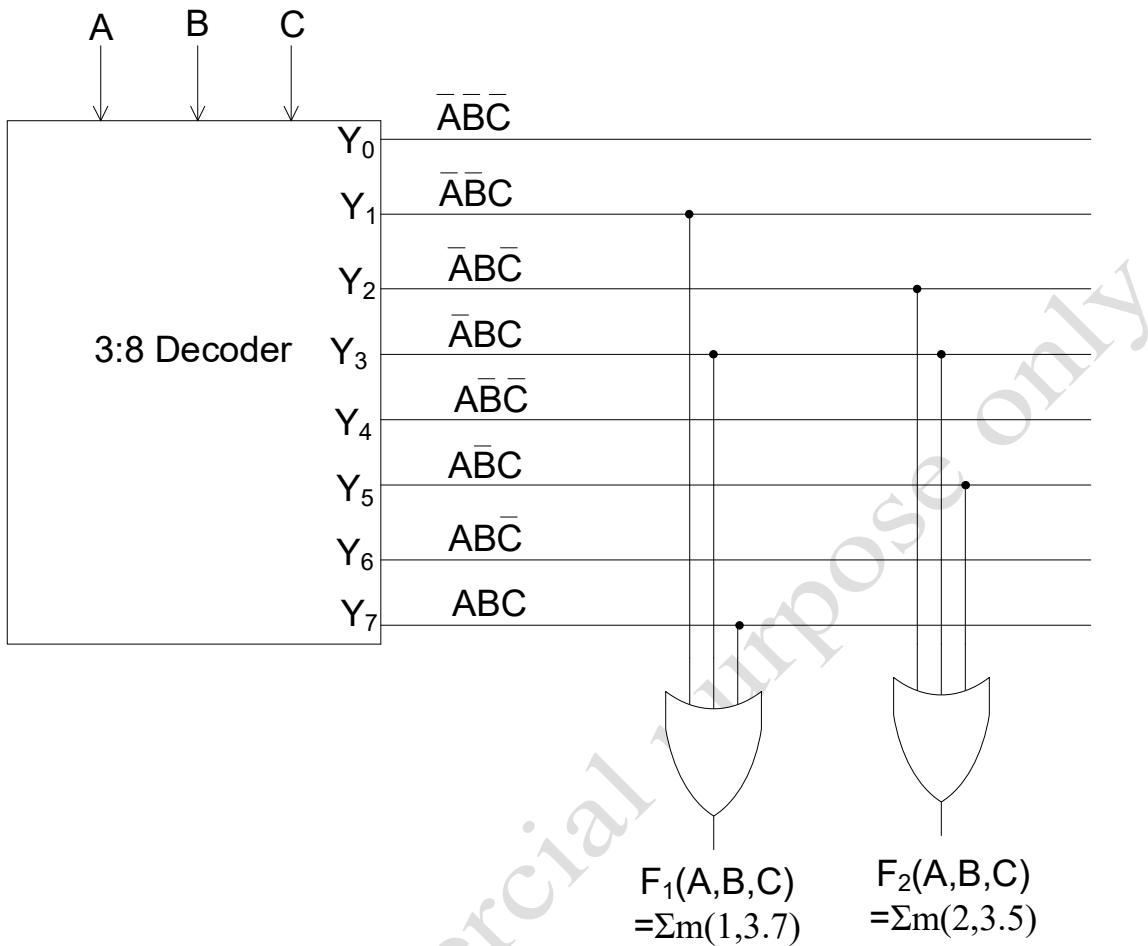
Answer: Working principle of 3:8 decoder:

There are 3 inputs and 8 outputs in a 3:8 decoder. One of the output is HIGH and remaining seven are LOW according to inputs. This is shown in truth table.



Truth table of 3:8 Decoder :

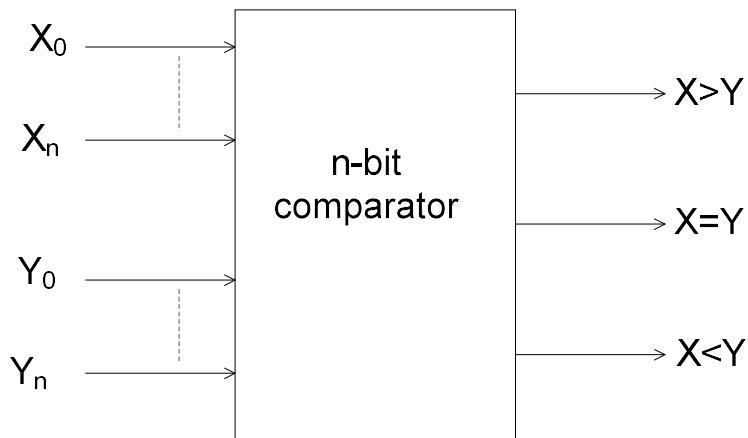
A	B	C	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	0	0	1	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1



Q24. What is magnitude comparator? Design one bit comparator and write the truth table, logic circuit using basic gates.

Answer: A magnitude comparator compares two binary numbers and it produces an output showing the comparison of the two input numbers.

For example, two n-bit binary numbers X=X₀X₁...X_n and Y=Y₀Y₁...Y_n are compared. There are three outputs. The outputs are for X>Y, X=Y and X<Y as shown in the figure below.



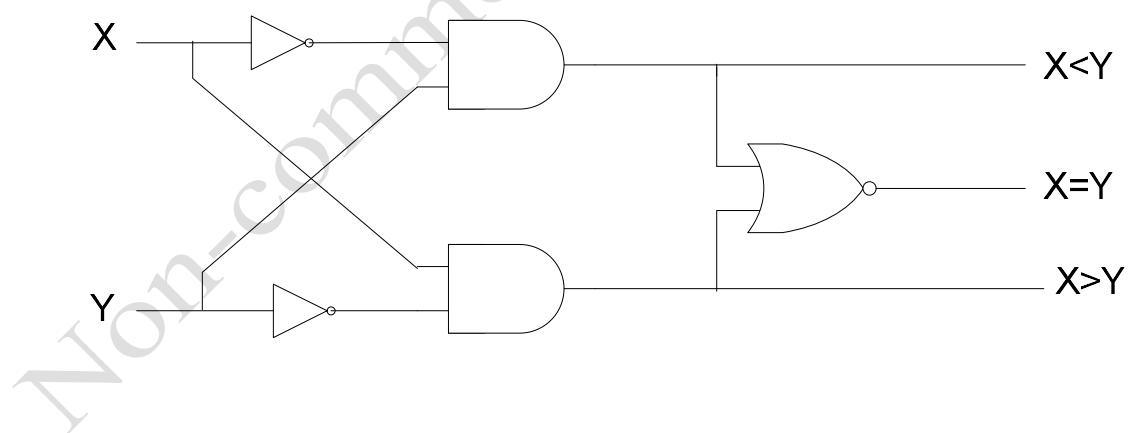
Designing of one bit comparator:

Truth table

Input		Output		
X	Y	$X > Y$	$X = Y$	$X < Y$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

If G, L, E stand for greater than, less than and equal to respectively, then

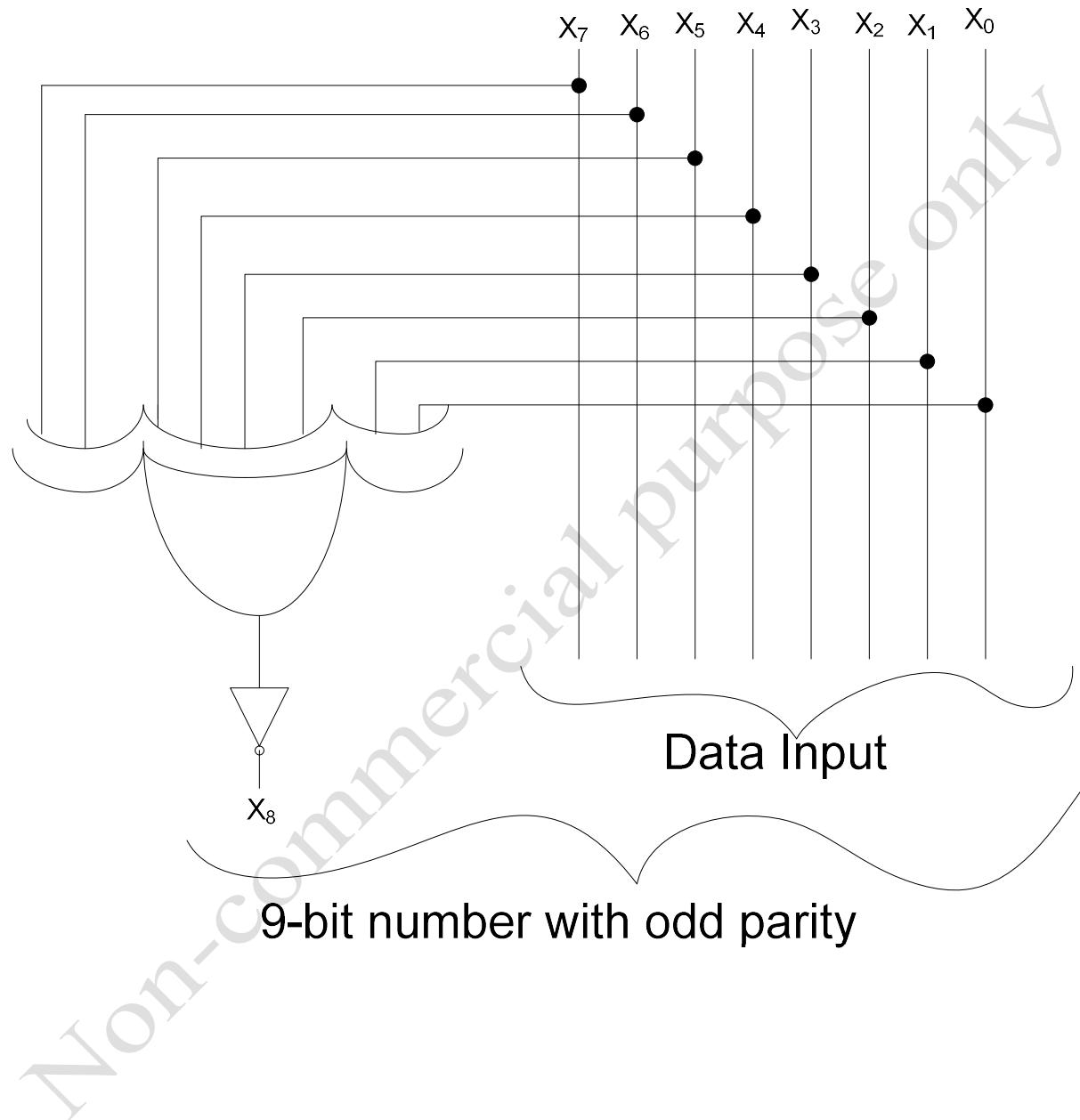
$$(X > Y): G = XY'; (X < Y): L = X'Y; (X = Y): E = X'Y' + XY = (XY' + X'Y)' = (G + L)'$$



Q25. What is parity generator? Explain with an example.

Answer: A parity generator is a logic circuit which produces either even parity number or odd parity number as per requirement.

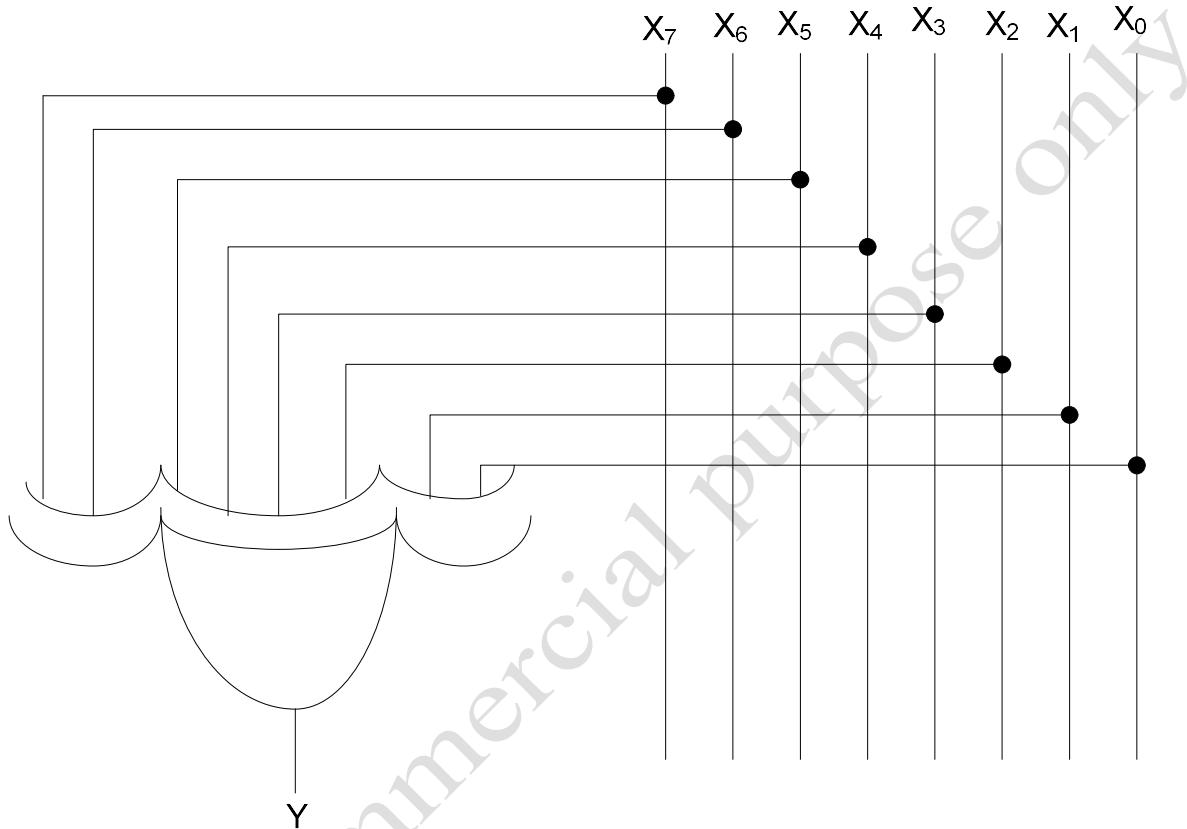
For example:



Q26. What is parity checker? Explain with example.

Answer: A parity checker check the parity of a number whether the number is of even parity or odd parity.

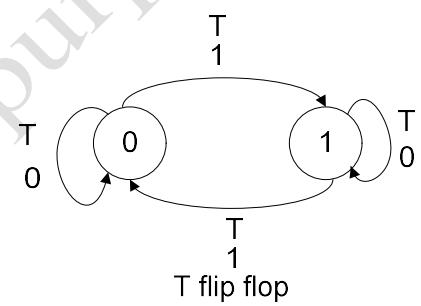
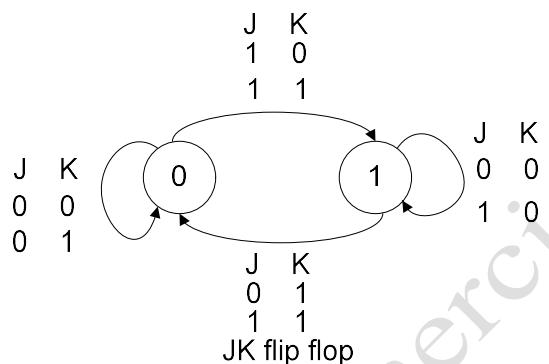
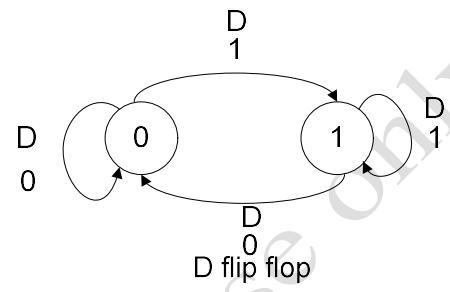
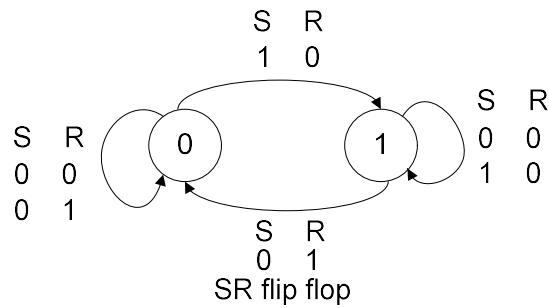
For example: The exclusive OR gate produces an output 1 when the input ($X_0 \dots X_7$) is of odd parity and produces 0 when the input is of even parity.



Q27. Give state transition diagram of SR, D, JK and T flip flops.

Answer:

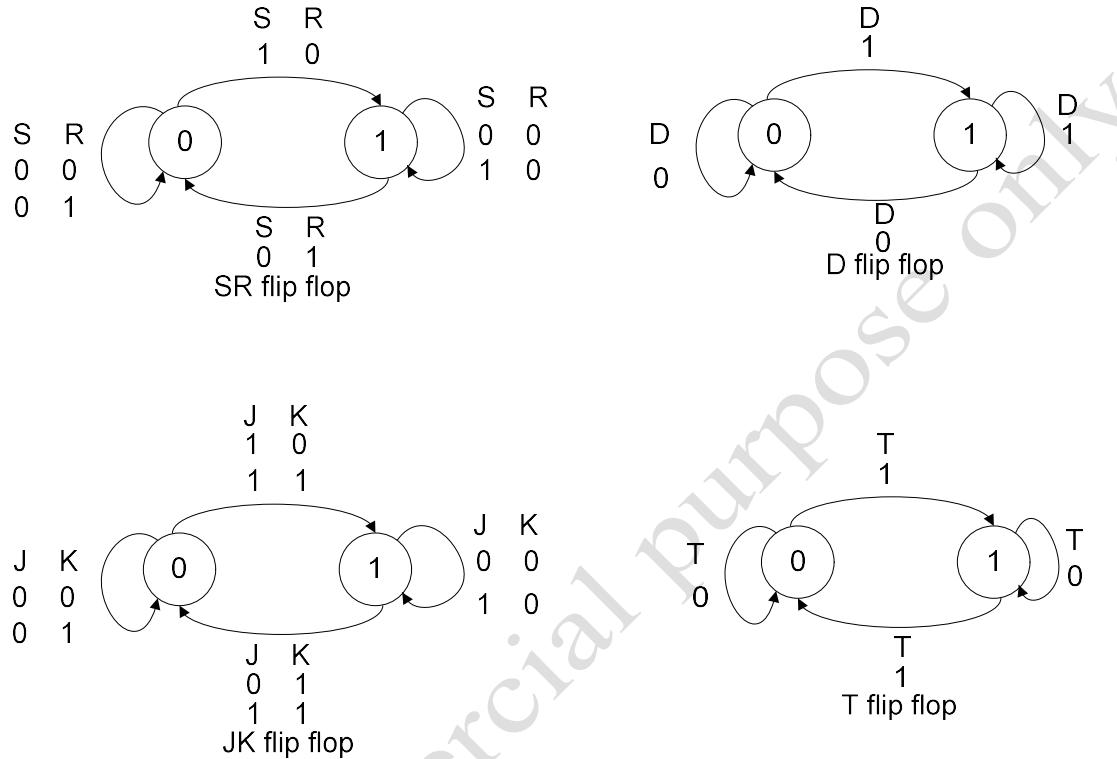
State Transition Diagram



Q28. Obtain the characteristic equation of SR, JK, D and T flip flops.

Answer:

State Transition Diagram



Excitation Table for SR, JK, D and T flip flop is given below is prepared State Transition Diagram above

$Q_n \rightarrow Q_{n+1}$	S R	J K	D	T
0 0	0 X	0 X	0	0
0 1	1 0	1 X	1	1
1 0	0 1	X 1	0	1
1 1	X 0	X 0	1	0

From the Excitation Table, K-map is formed and then the characteristic equation is determined.

		SR		Q _n	
		00	01	11	10
0		0	0	x	1
1		1	0	x	1

Characteristic Equation for SR flip flop is

$$Q_{n+1} = S + \bar{R}Q_n$$

		JK		Q _n	
		00	01	11	10
0		0	0	1	1
1		1	0	0	1

Characteristic Equation for JK flip flop is

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

		D		Q _n	
		0	1		
0		0	1		
1		0	1		

Characteristic Equation for D flip flop is

$$Q_{n+1} = D$$

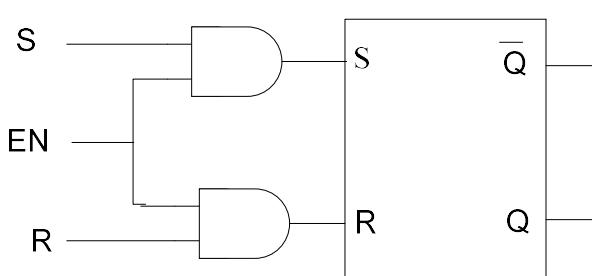
		T		Q _n	
		0	1		
0		0	1		
1		1	0		

Characteristic Equation for T flip flop is

$$Q_{n+1} = T\bar{Q}_n + \bar{T}Q_n$$

Q29. Explain the operation of a gated SR latch with a logic diagram and truth table.

Logic diagram and truth table of gated SR flip flop is shown below:



Logic Diagram

EN	S	R	Q_{n+1}
1	0	0	Q_n (No Change)
1	0	1	0
1	1	0	1
1	1	1	Illegal
0	x	x	Q_n (No Change)

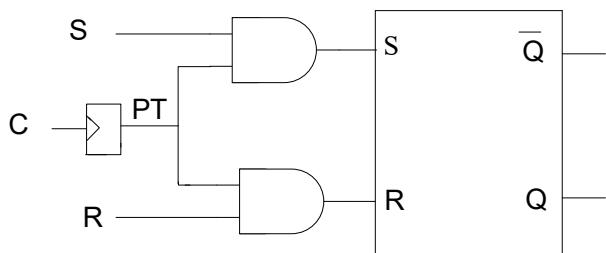
Truth table

When the Enable (EN) input is high, information at the R and S inputs will be transmitted directly to the outputs. The latch is said to be enabled. When the Enable (EN) input is low, the outputs of the AND gates are low and information at the R and S inputs will not be transmitted to the outputs. The latch is said to be disabled.

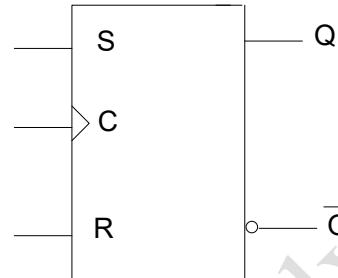
It is possible to strobe or clock the flip flop in order to store information at any time and then hold the stored information for any desired period of time. This flip flop is called a gated or clocked RS flip flop.

Q30. Explain the operation of edge triggered ‘SR’ flip flop with the help of a logic diagram and truth table. Also draw the relevant waveforms.

Answer: Positive edge triggered ‘SR’ flip flop



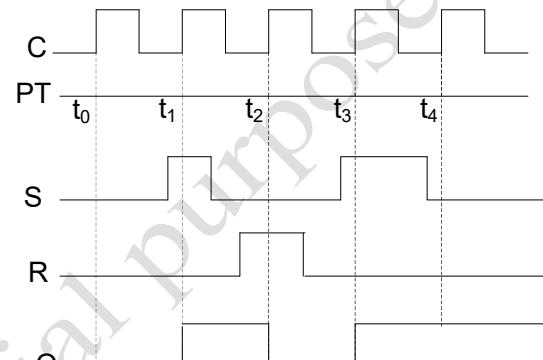
Logic Diagram



IEEE Symbol

C	S	R	Q_{n+1}
↑	0	0	Q_n (No Change)
↑	0	1	0 (Reset)
↑	1	0	1 (Set)
↑	1	1	Illegal

Truth table



Waveform of positive edge triggered RS flip flop

Positive edges occur at t_0, t_1, t_2, t_3 and t_4 .

At t_0 , $S=0$ and $R=0$, hence no change in the output and $Q=0$.

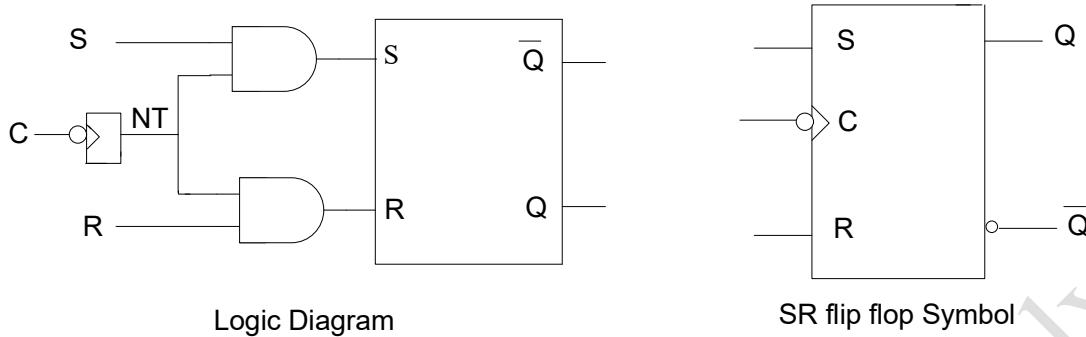
At t_1 , $S=1$ and $R=0$, hence the output is set and $Q=1$.

At t_2 , $S=0$ and $R=1$, hence the output is reset and $Q=0$.

At t_3 , $S=1$ and $R=0$, hence the output is set and $Q=1$

At t_4 , $S=0$ and $R=0$, hence no change in the output and $Q=1$.

Negative edge triggered ‘SR’ flip flop

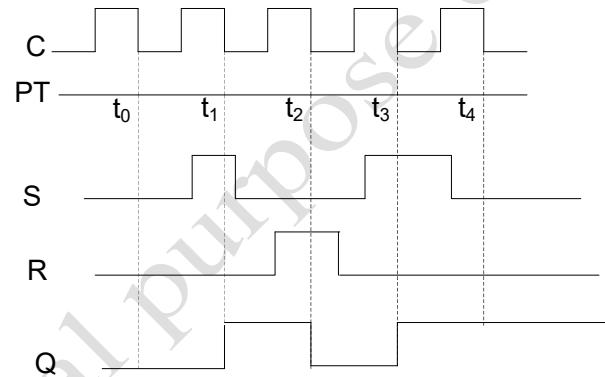


Logic Diagram

SR flip flop Symbol

C	S	R	Q_{n+1}
↓	0	0	Q_n (No Change)
↓	0	1	0 (Reset)
↓	1	0	1 (Set)
↓	1	1	Illegal

Truth table



Waveform of negative edge triggered SR flip flop

Negative edges occur at t_0, t_1, t_2, t_3 and t_4 .

At t_0 , S=0 and R=0, hence no change in the output and Q=0.

At t_1 , S=1 and R=0, hence the output is set and Q=1.

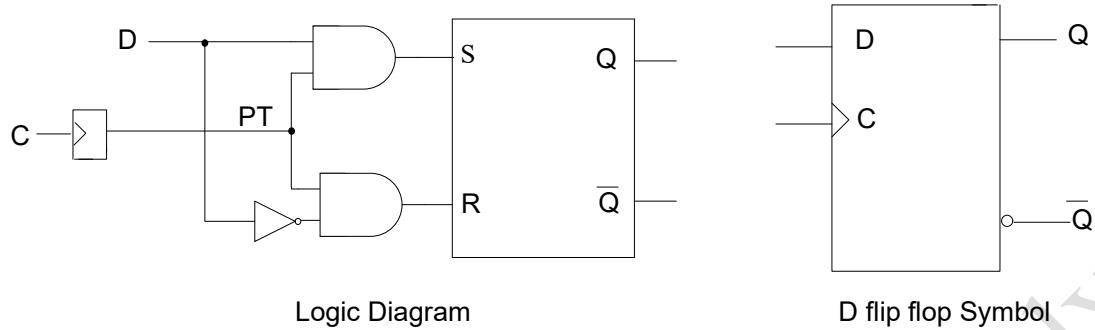
At t_2 , S=0 and R=1, hence the output is reset and Q=0.

At t_3 , S=1 and R=0, hence the output is set and Q=1

At t_4 , S=0 and R=0, hence no change in the output and Q=1.

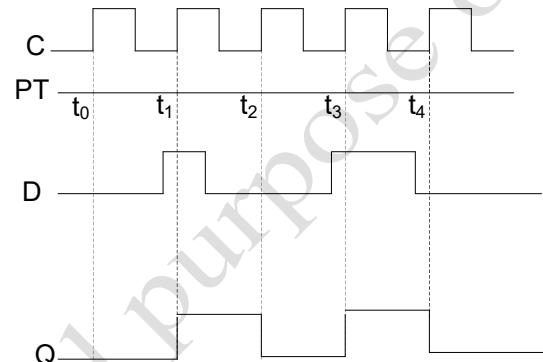
Q31. Explain the operation of edge triggered ‘D’ flip flop with the help of a logic diagram and truth table. Also draw the relevant waveforms.

Answer: Positive edge triggered ‘D’ flip flop



C	D	Q_{n+1}
0	x	Q_n (No Change)
↑	0	0
↑	1	1

Truth table



Waveform of positive edge triggered D flip flop

Positive edges occur at t_0, t_1, t_2, t_3 and t_4 .

At t_0 , D=0, hence the output is low and Q=0.

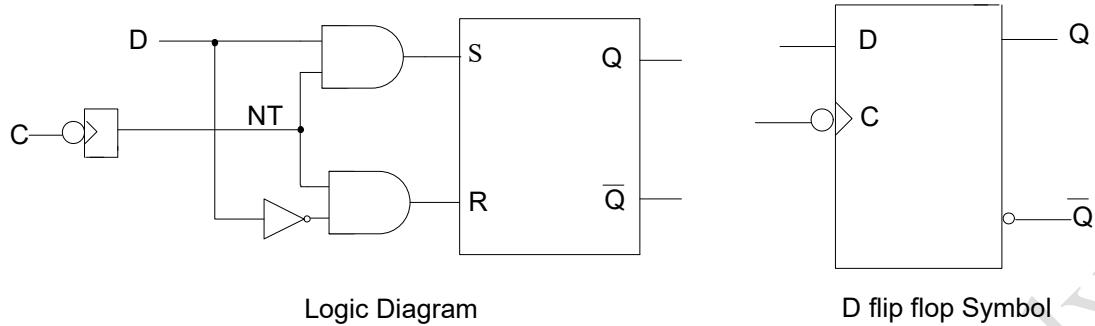
At t_1 , D=1, hence the output is high and Q=1.

At t_2 , D =0, hence the output is low and Q=0.

At t_3 , D=1, hence the output is high and Q=1

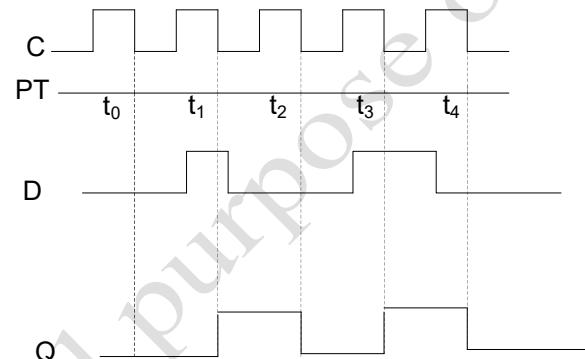
At t_4 , D=0, hence no change in the output and Q=1.

Negative triggered D flip flop



C	D	Q_{n+1}
0	x	Q_n (No Change)
↓	0	0
↓	1	1

Truth table



Waveform of positive edge triggered D flip flop

Negative edges occur at t_0, t_1, t_2, t_3 and t_4 .

At t_0 , D=0, hence the output is low and Q=0.

At t_1 , D=1, hence the output is high and Q=1.

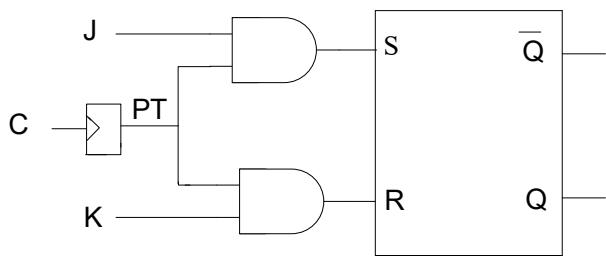
At t_2 , D =0, hence the output is low and Q=0.

At t_3 , D=1, hence the output is high and Q=1

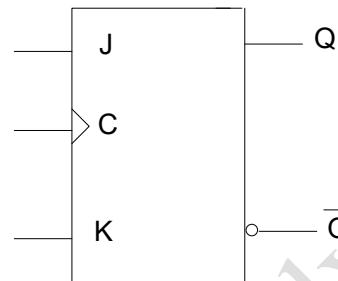
At t_4 , D=0, hence no change in the output and Q=1.

Q32. Explain the working of pulse triggered JK flip flop with typical JK flip flop waveform.

Answer: Positive Edge Triggered JK flip flop



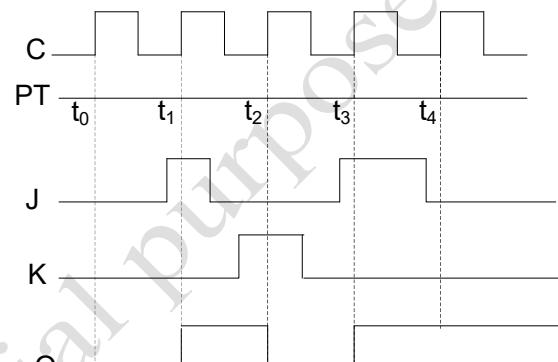
Logic Diagram



JK flip flop Symbol

C	J	K	Q_{n+1}
↑	0	0	Q_n (No Change)
↑	0	1	0
↑	1	0	1
↑	1	1	Toggle

Truth table



Waveform of positive edge triggered JK flip flop

Positive edges occur at t_0, t_1, t_2, t_3 and t_4 .

At t_0 , $J=0$ and $K=0$, hence no change in the output and $Q=0$.

At t_1 , $J=1$ and $K=0$, hence the output is high and $Q=1$.

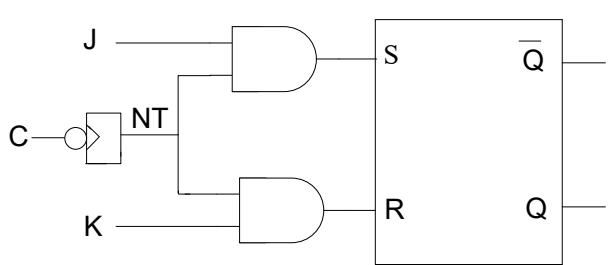
At t_2 , $J=0$ and $K=1$, hence the output is low and $Q=0$.

At t_3 , $J=1$ and $K=0$, hence the output is high and $Q=1$

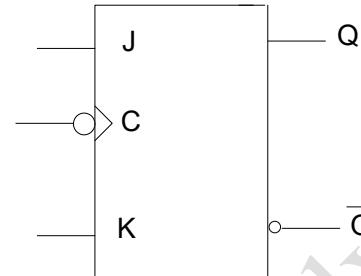
At t_4 , $J=0$ and $K=0$, hence no change in the output and $Q=1$.

:

Negative Edge Triggered JK flip flop



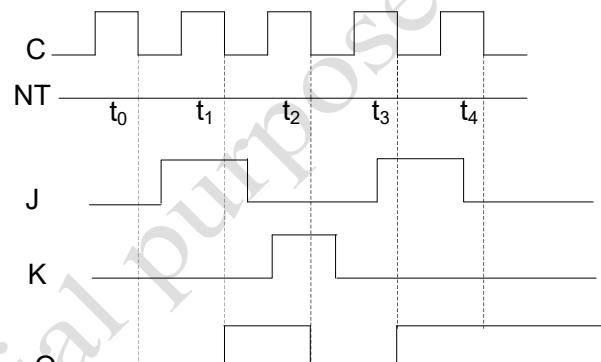
Logic Diagram



JK flip flop Symbol

C	J	K	Q_{n+1}
↓	0	0	Q_n (No Change)
↓	0	1	0
↓	1	0	1
↓	1	1	Toggle

Truth table



Waveform of positive edge triggered JK flip flop

Negative edges occur at t_0, t_1, t_2, t_3 and t_4 .

At t_0 , $J=0$ and $K=0$, hence no change in the output and $Q=0$.

At t_1 , $J=1$ and $K=0$, hence the output is high and $Q=1$.

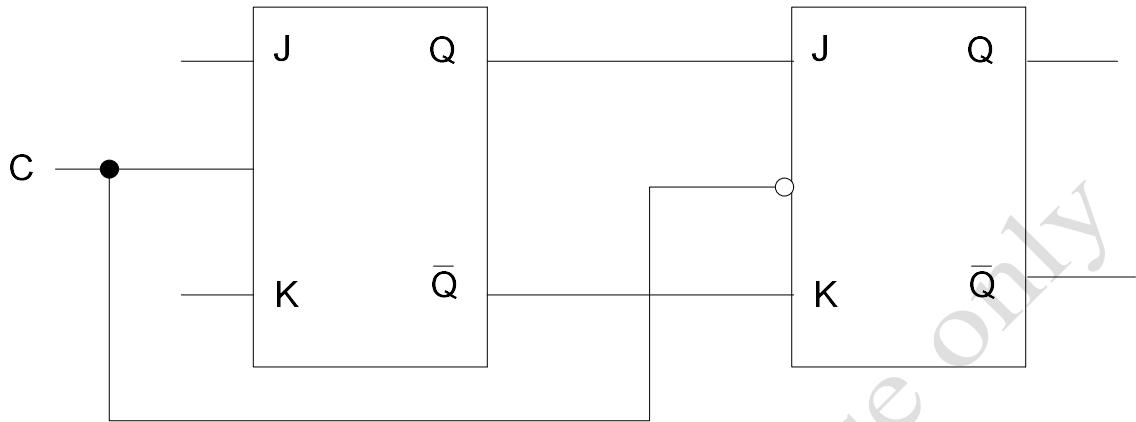
At t_2 , $J=0$ and $K=1$, hence the output is low and $Q=0$.

At t_3 , $J=1$ and $K=0$, hence the output is high and $Q=1$

At t_4 , $J=0$ and $K=0$, hence no change in the output and $Q=1$.

Q33. Explain the working of Master Slave J K flip flops with logic diagram.

Answer:



Master Slave flip flop

Master is positive-level-triggered and the slave is negative-level-triggered. The master responds to its J and K inputs before the slave.

If $J=1$ and $K=0$, the master sets on the positive clock transition. The high Q output of the master drives the J input of the slave. So, on the negative clock transition, the slave sets, thus copying the action of the master.

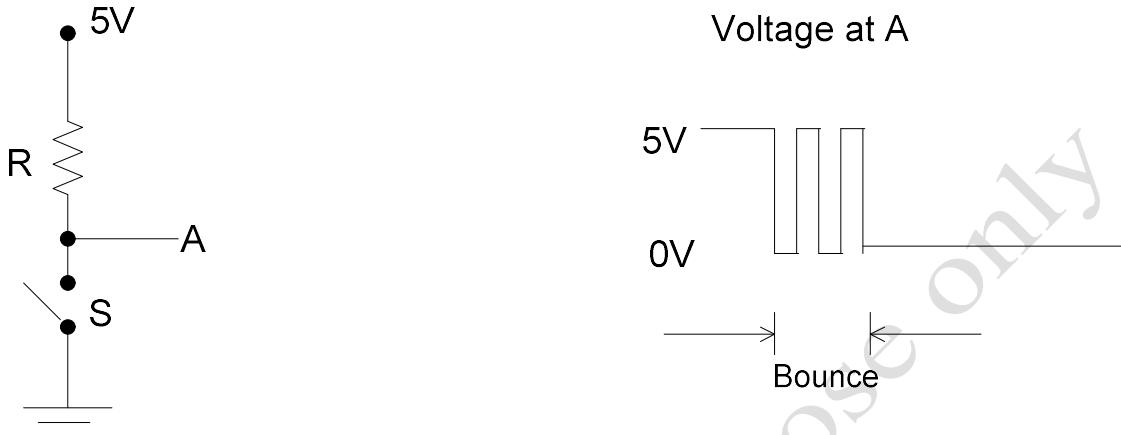
If $J=0$ and $K=1$, the master resets on the positive clock transition. The high \bar{Q} output of the master drives the K input of the slave. So, on the negative clock transition, the slave resets, thus copying the action of the master.

If $J=1$ and $K=1$, the master toggles on the positive clock transition. The slave also toggles at the negative clock transition thus copying the action of the master.

If $J=0$ and $K=0$, the master and the slave both are disabled, thus copying the action of the master.

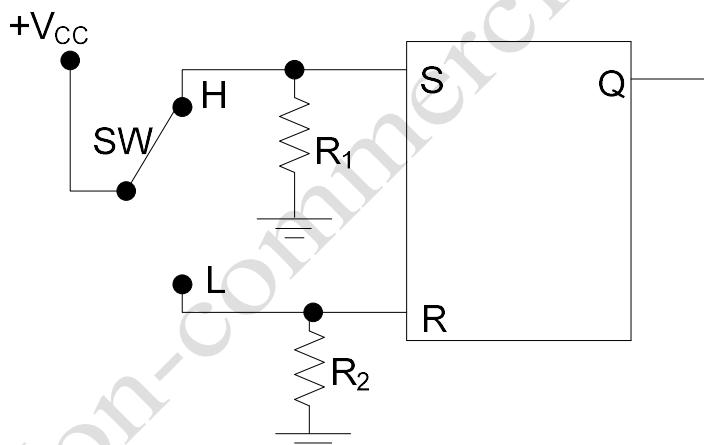
Q34. What is contact bounce? With neat diagram, explain the working principles of Switch Debounce circuit.

Answer:



Any mechanical switching device consists of a moving contact arm restrained by some spring system. As a result, when a mechanical switch is closed, the arm is moved from one stable position to other and the arm bounces much as a hard ball bounces when dropped on a hard surface. This phenomenon is known as contact bounce. When switch S is closed, due to contact bounce the voltage at the A is shown in the above figure.

RS Latch Debounce Circuit

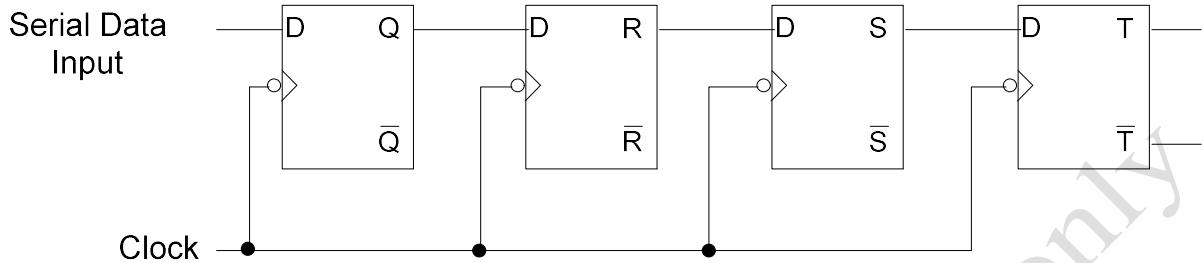


When switch(SW) is moved to the position H, R=0 and S=1. Bouncing occurs at S due to contact bounce of the switch. The flip flop treats as high and low inputs. The flip flop will be set with Q=1 at the first high of the contact bounce. When the switch continues to bounce, losing contact, the input signals are R=S=0, thus the flip flop remains at Q=1. As a result, the flip flop responds only to the first high of the contact bounce.

MODULE 4

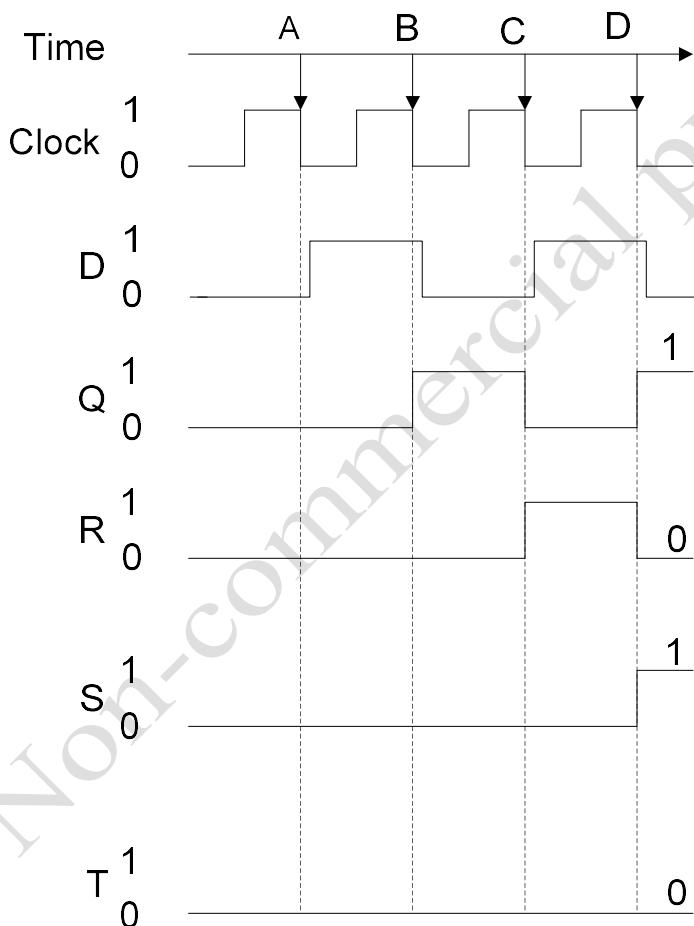
Q1. Explain 4-bit Serial in-Serial out register.

Answer: 4-bit serial in-serial out register is shown below:



The waveform for the above circuit is shown below:

It has been assumed that initially $Q=0$, $R=0$, $S=0$ and $T=0$.



At clock edge A: $DQRS=0000$. As the clock trigger at A, the values at DQRS is transferred to QRST and $QRST=0000$.

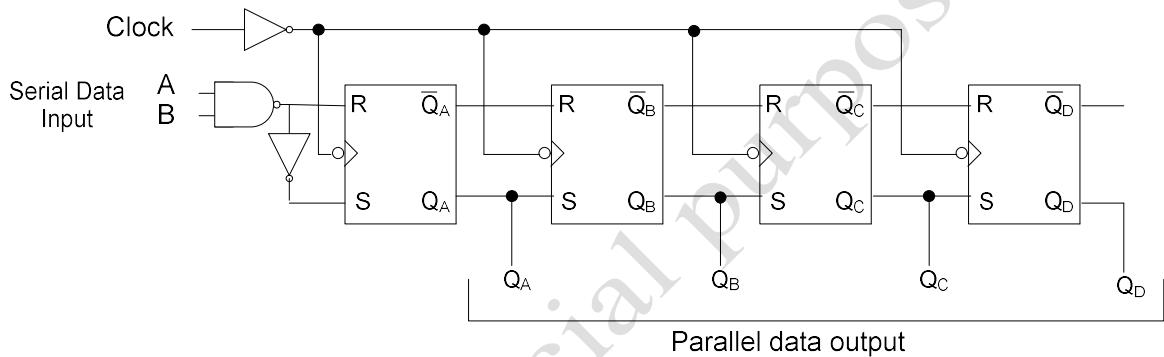
At clock edge B: DQRS=1000. As the clock trigger at B, the values at DQRS is transferred to QRST and QRST=1000.

At clock edge C: DQRS=0100. As the clock trigger at C, the values at DQRS is transferred to QRST and QRST=0100.

At clock edge D: DQRS=1010. As the clock trigger at B, the values at DQRS is transferred to QRST and QRST=1010.

Q2. Explain 4-bit Serial in-parallel out register.

Answer: 4-bit serial in-parallel out register is shown below:



Data shifted in serially, but shifted out in parallel as shown in the figure above. In order to shift the data out in parallel, output of each flip flop is connected to output pin.

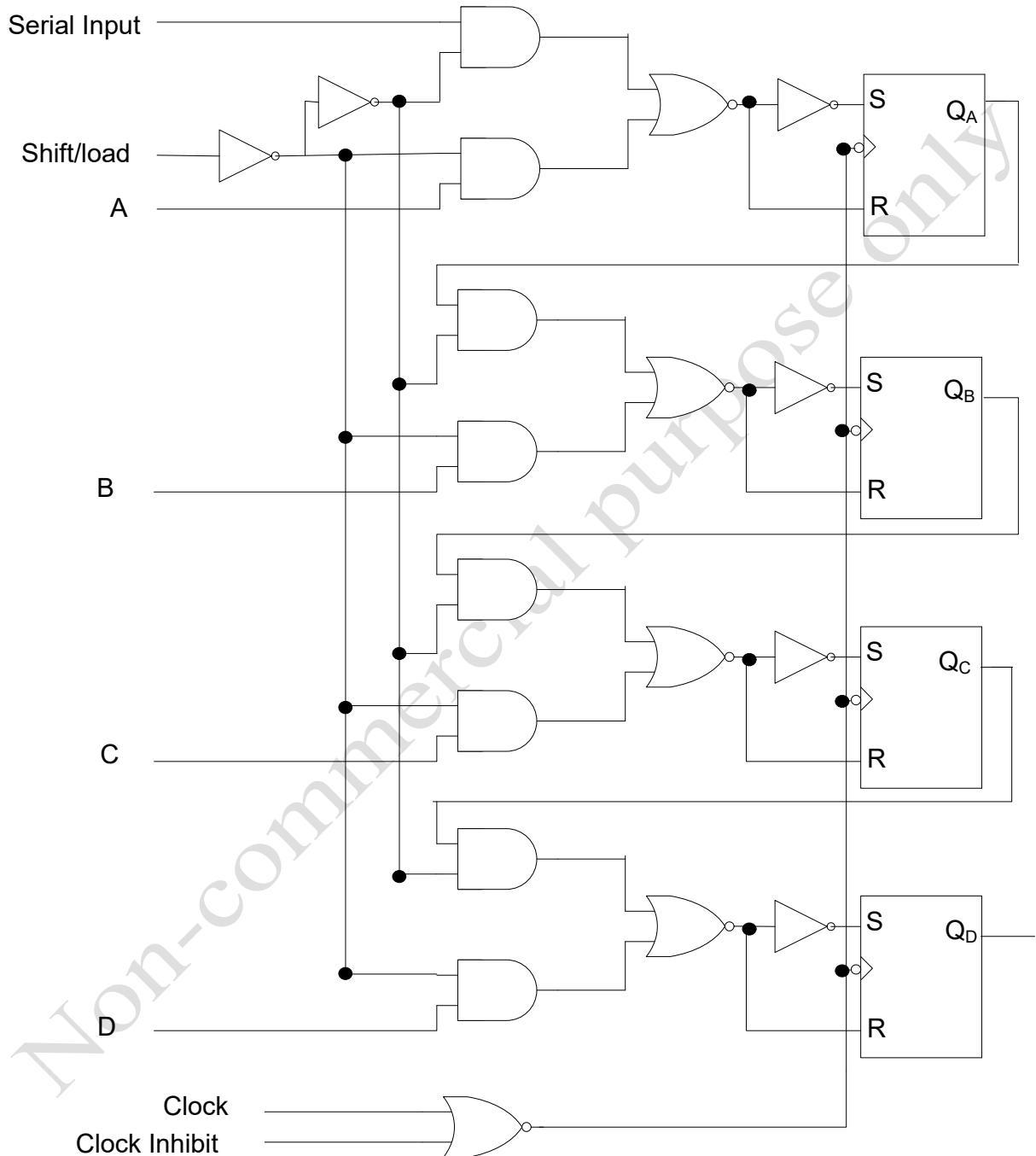
Suppose that the serial data is connected to A, and then B can be used as a control line.

If B is held high, then the NAND gate is enabled and the serial input data passes through the NAND gate is inverted. The input data is shifted serially into the register.

If B is held low, then the NAND gate output is high irrespective of input data.

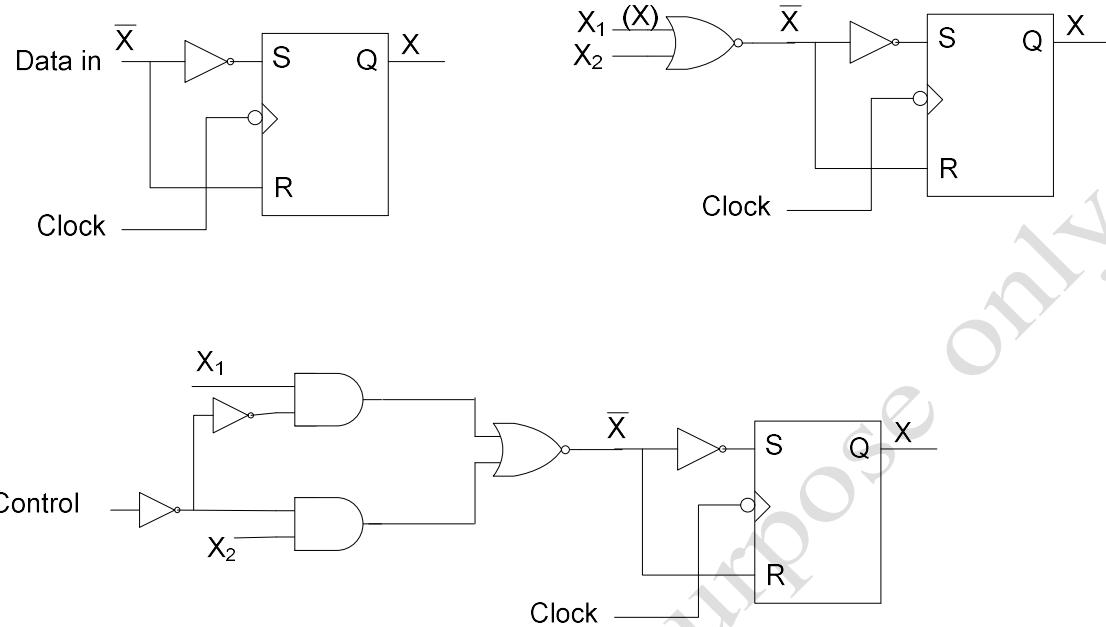
Q3. Explain 4-bit parallel in-Serial out register.

Answer: 4-bit parallel in serial out is shown below.



The above logic block diagram shows 4-bit parallel in (A, B, C and D) and serial out register. This can also be used as serial in if data is entered at Serial Input terminal as shown.

Analysis of the above circuit is given below:



The clocked RS flip flop and the attached inverter form a type D flip flop. If a data bit X is to be clocked into the, the complement of X must be present at the input.

If one leg of the NOR gate is at ground level, a data bit X at the other leg is inverted. This NOR gate provide option of entering data from two different sources, either X_1 or X_2 .

Addition of two AND gates and two inverters allow the selection of data selection of data X_1 or data X_2 .

If the control line is high, the upper AND gate is enabled and lower AND gate is disabled.

If the control line is low, upper AND gate is disabled and the lower AND gate is enabled.

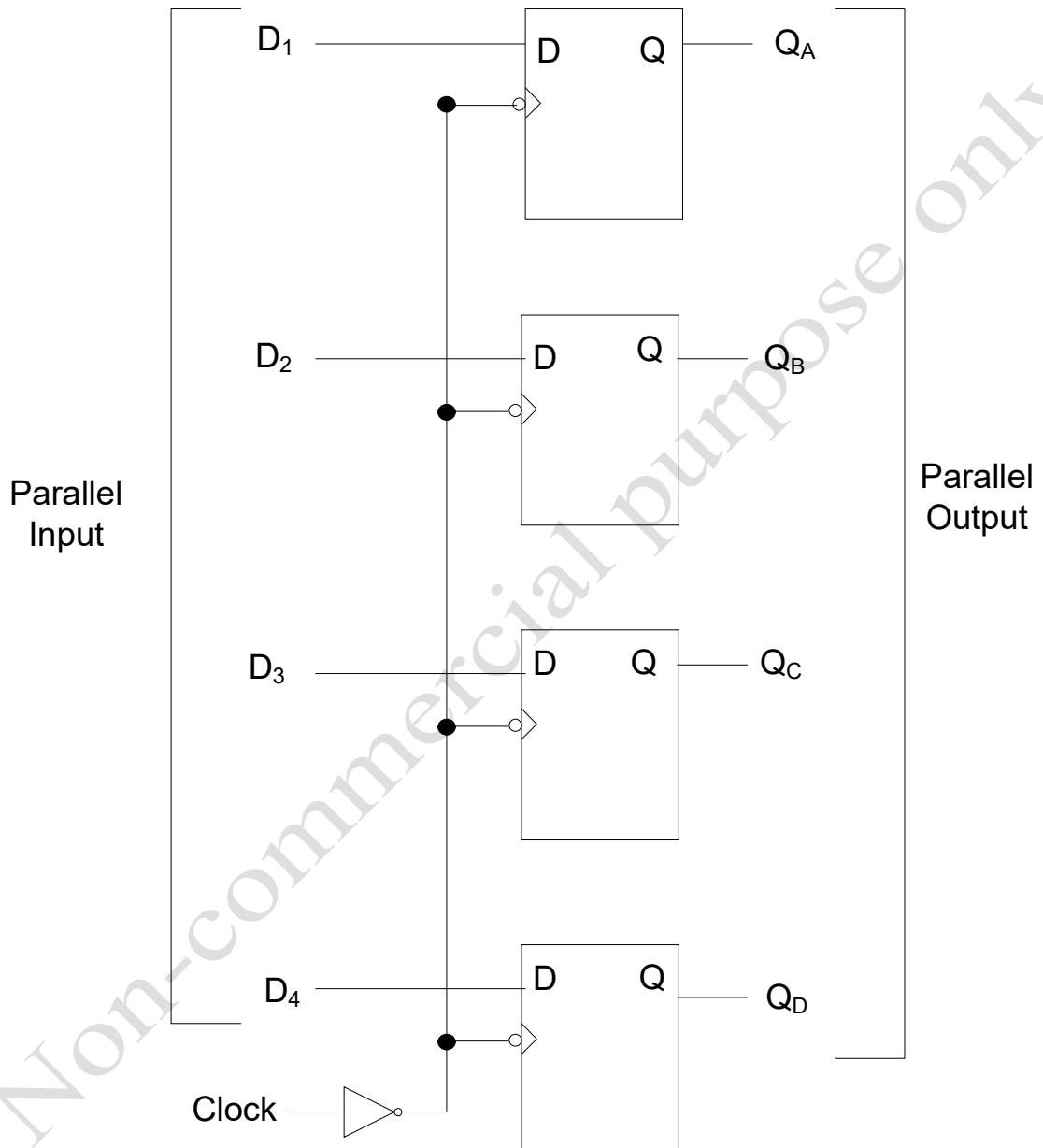
Control line is high: Data bit at X_1 will be shifted into the flip flop at the next clock pulse.

Control line is low: Data bit at X_2 will be shifted into the flip flop at the next clock pulse.

Shift/Load is low: A single clock transition load data into the register in parallel.

Q4. Explain 4-bit parallel in-parallel out register.

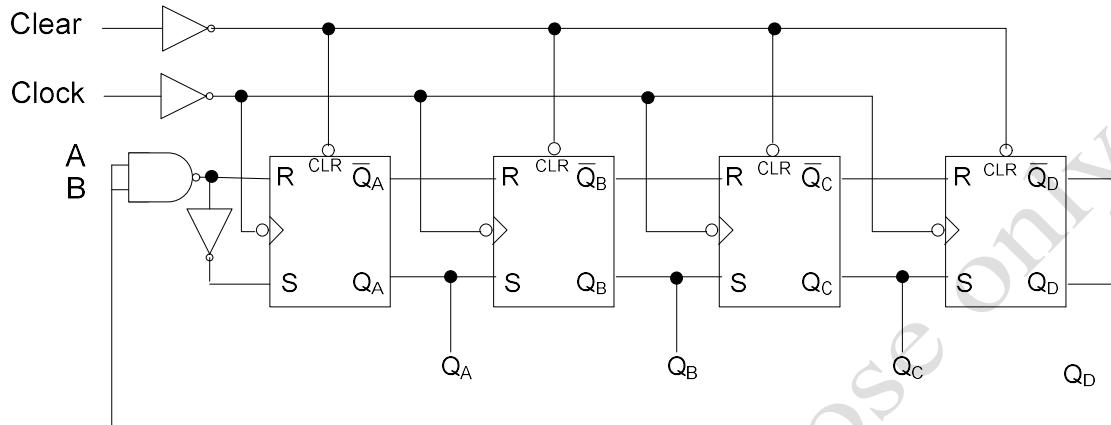
Answer: 4-bit parallel in parallel out is shown below.



Data D_1 through D_4 are shifted into the register with clock pulse. The stored data is immediately available in parallel at the output Q_1 through Q_4 . This type of register is used to store data is called data latch or data register..

Q5. Explain 4-bit Ring Counter.

Answer: Following is the 4-bit ring counter.



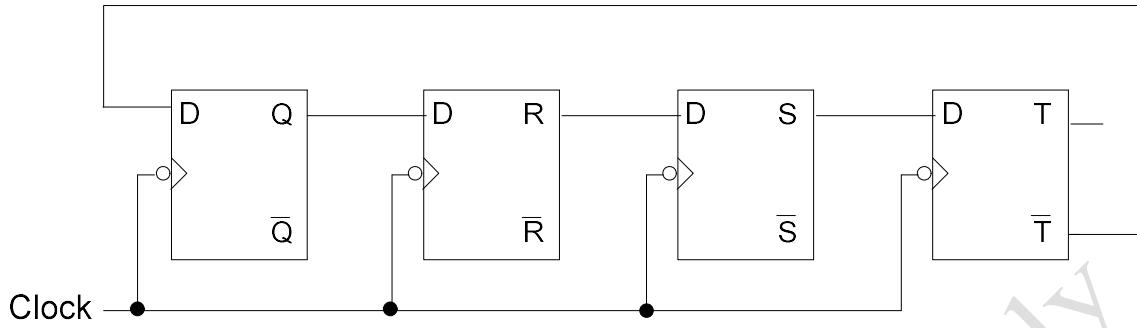
Output of the last flip flop Q_D is feedback to the input of the first flip flop.

State table of Ring Counter is shown below:

Clock	Q_A	Q_B	Q_C	Q_D
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0
5	0	1	0	0
6	0	0	1	0
7	0	0	0	1
8	1	0	0	0

Q6. Design 4-bit Johnson counter (Switch Tail Counter) with state table.

Answer: 4-bit Johnson counter is shown below.



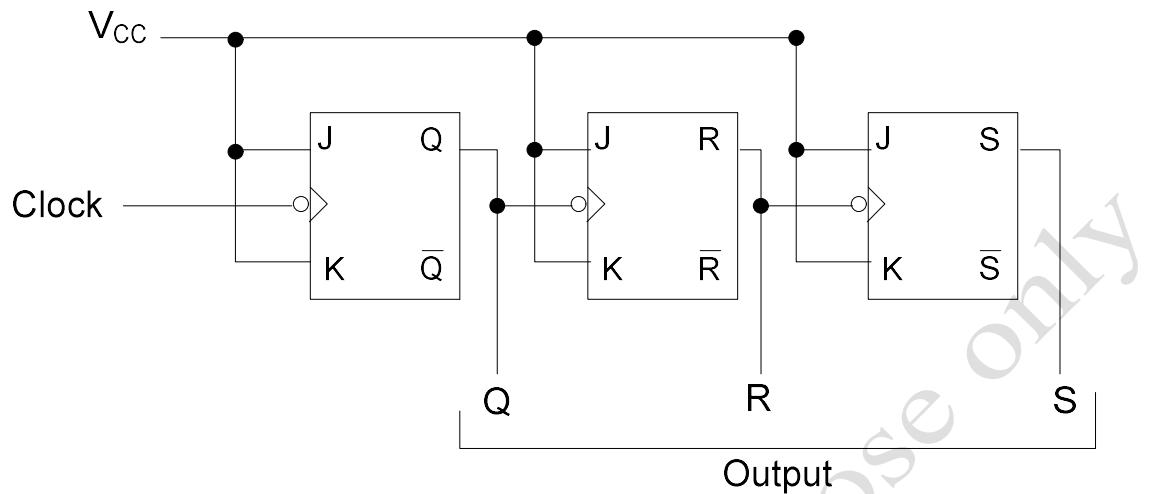
Inverting output of the last flip flop is feedback to the first flip flop.

State table of Johnson Counter is shown below:

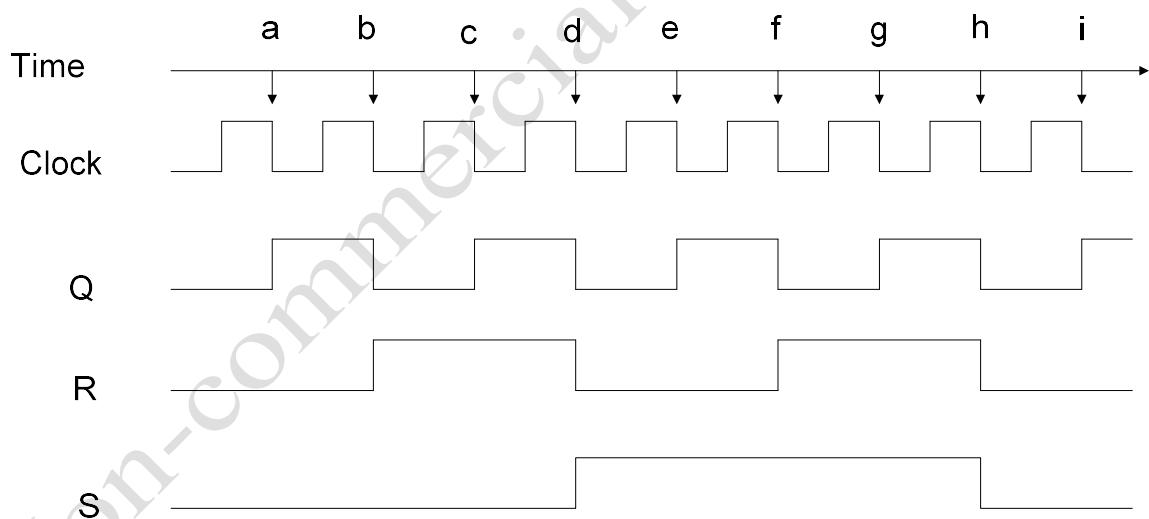
Clock	Serial in= T'	Q	R	S	T
0	1	0	0	0	0
1	1	1	0	0	0
2	1	1	1	0	0
3	1	1	1	1	0
4	0	1	1	1	1
5	0	0	1	1	1
6	0	0	0	1	1
7	0	0	0	0	1
8	1	0	0	0	0
9	1	1	0	0	0

Q7. Explain a 3-bit binary Ripple up counter, give the block diagram, truth table and output waveforms.

Answer: Following is a Ripple Up Counter (or Asynchronous UP Counter).



Waveforms:



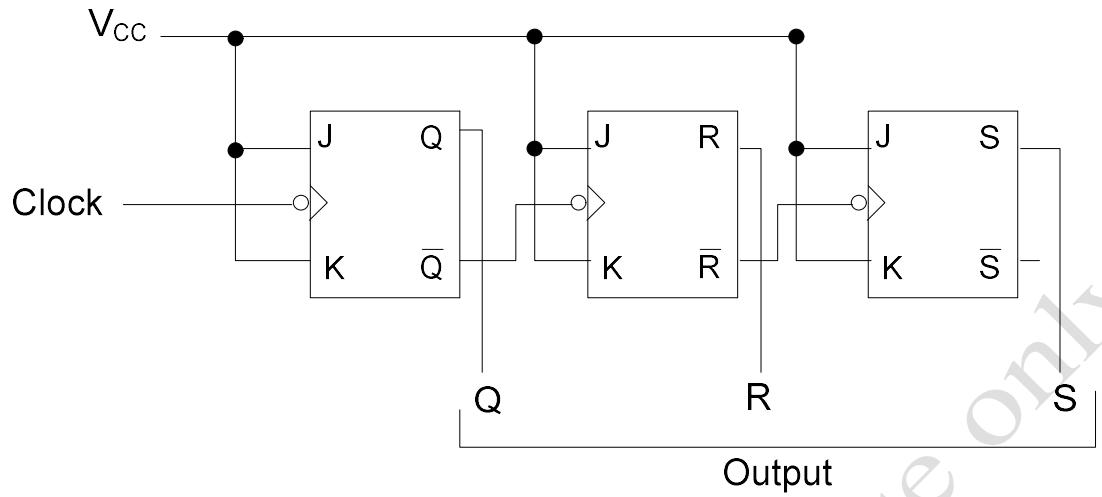
Truth Table:

Negative Edge Triggered Clock	Q	R	S	Count
---	0	0	0	0

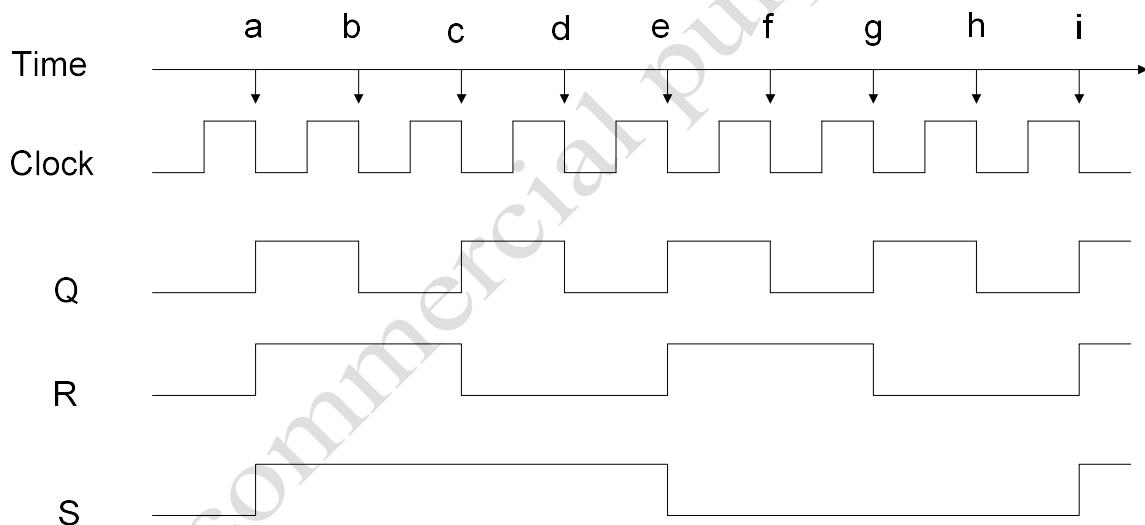
a	0	0	1	1
b	0	1	0	2
c	0	1	1	3
d	1	0	0	4
e	1	0	1	5
f	1	1	0	6
g	1	1	1	7
h	0	0	0	0
i	0	0	1	1

Q8. Explain a 3-bit binary Ripple down counter, give the block diagram, truth table and output waveforms.

Answer: Following is a Ripple Down Counter (or Asynchronous Down Counter).



Waveforms:



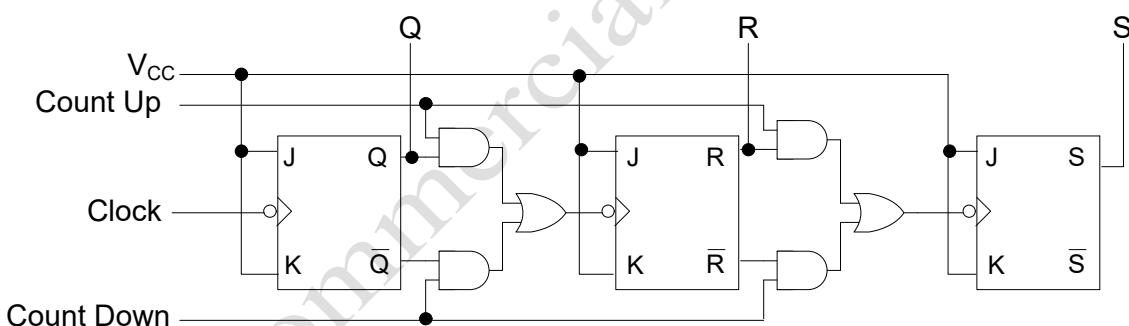
Truth Table:

Negative Edge Triggered Clock	Q	R	S	Count
---	0	0	0	0

a	1	1	1	7
b	1	1	0	6
c	1	0	1	5
d	1	0	0	4
e	0	1	1	3
f	0	1	0	2
g	0	0	1	1
h	0	0	0	0
i	1	1	1	7

Q9. Explain a 3-bit Ripple Up Down Counter.

Answer: Following is a Ripple Up Down Counter.



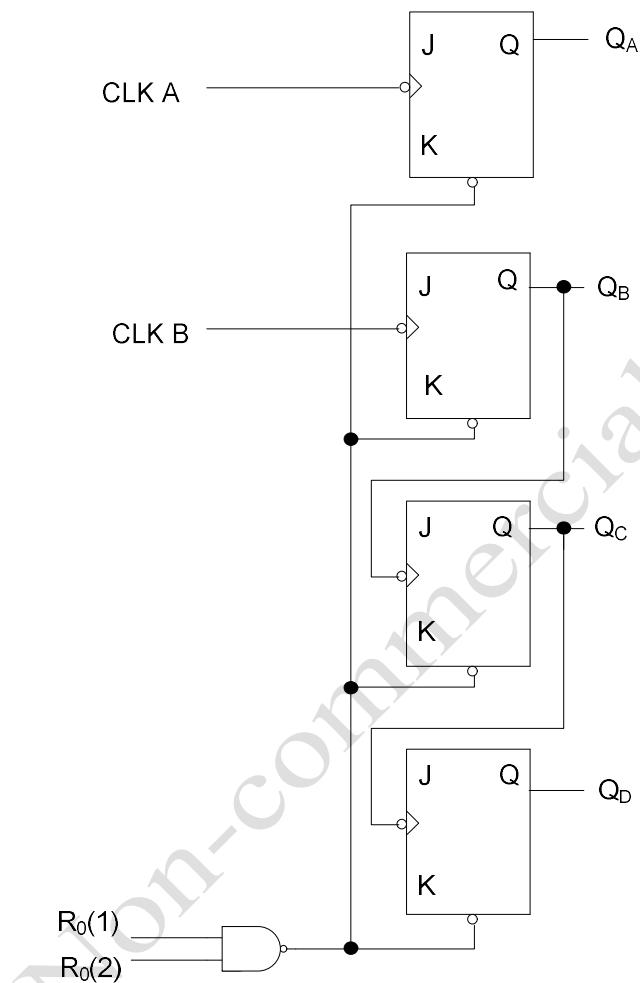
Ripple Up Down Counter is combination Ripple Up Counter and Ripple Down Counter.

If Count Up control is high and Count Down control is low, the above counter will be Up Counter.

If Count Up control is low and Count Down control is high, the above counter will be Down Counter.

Q10. Explain the 7493 IC.

Answer: Following is the 7493 IC



7493 IC is a 4 bit binary counter that can be used in either mod-8 or mod-16.

If the clock is applied at CLK B, the counter will be mod-8 counter and the output appear at Q_B, Q_C and Q_D.

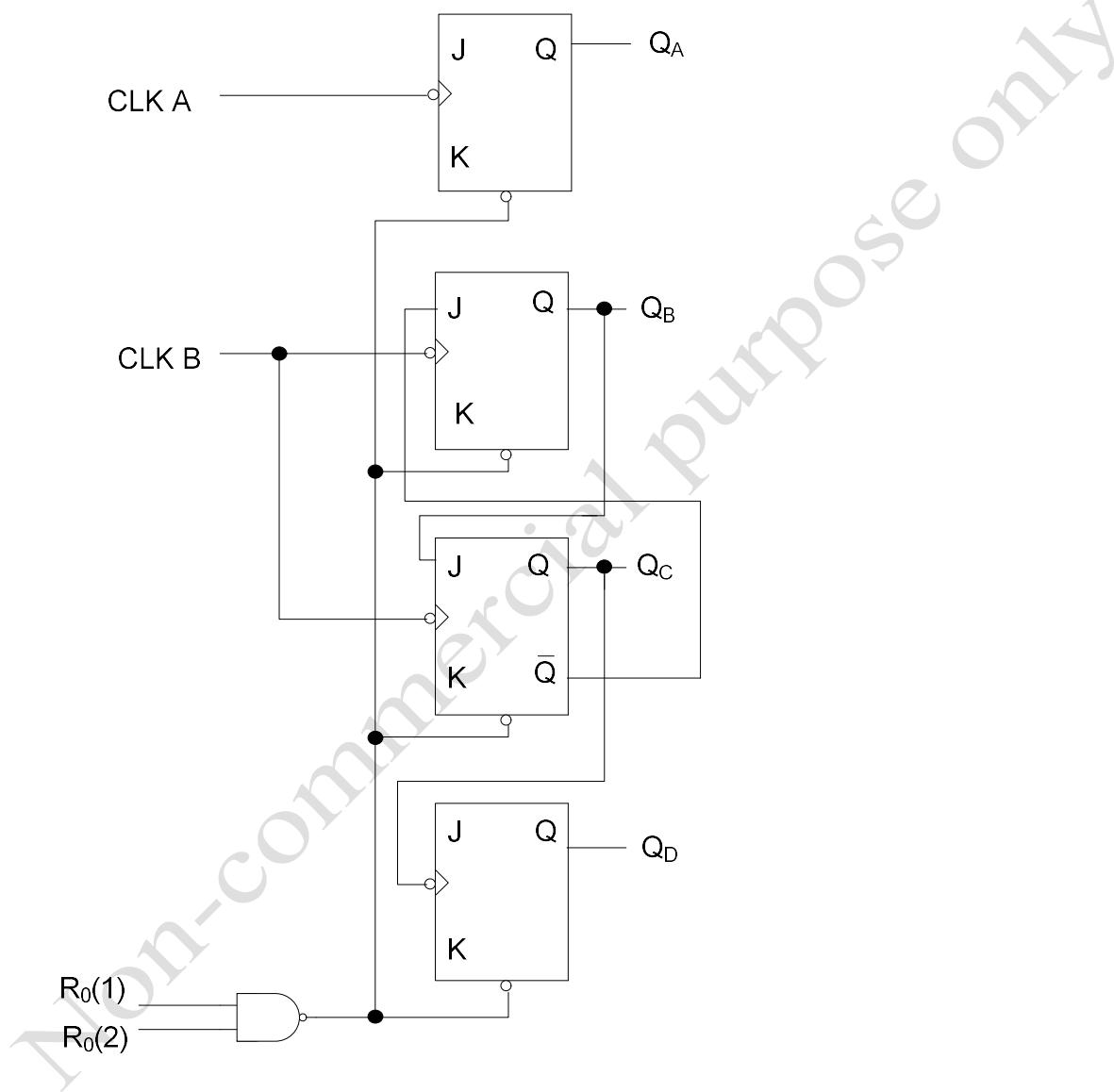
If the clock is applied at CLK A and Q_A is connected to CLK B, the counter will be mod-16

Counter and the output appear at Q_A , Q_B , Q_C and Q_D .

$R_0(1)$ and $R_0(2)$ are used to reset all flip flops simultaneously.

Q11. Explain IC 7492.

Answer: Following is the logical diagram for IC 7492



IC 7492 can be used as divide by 12 counter or as divide by 6 counter.

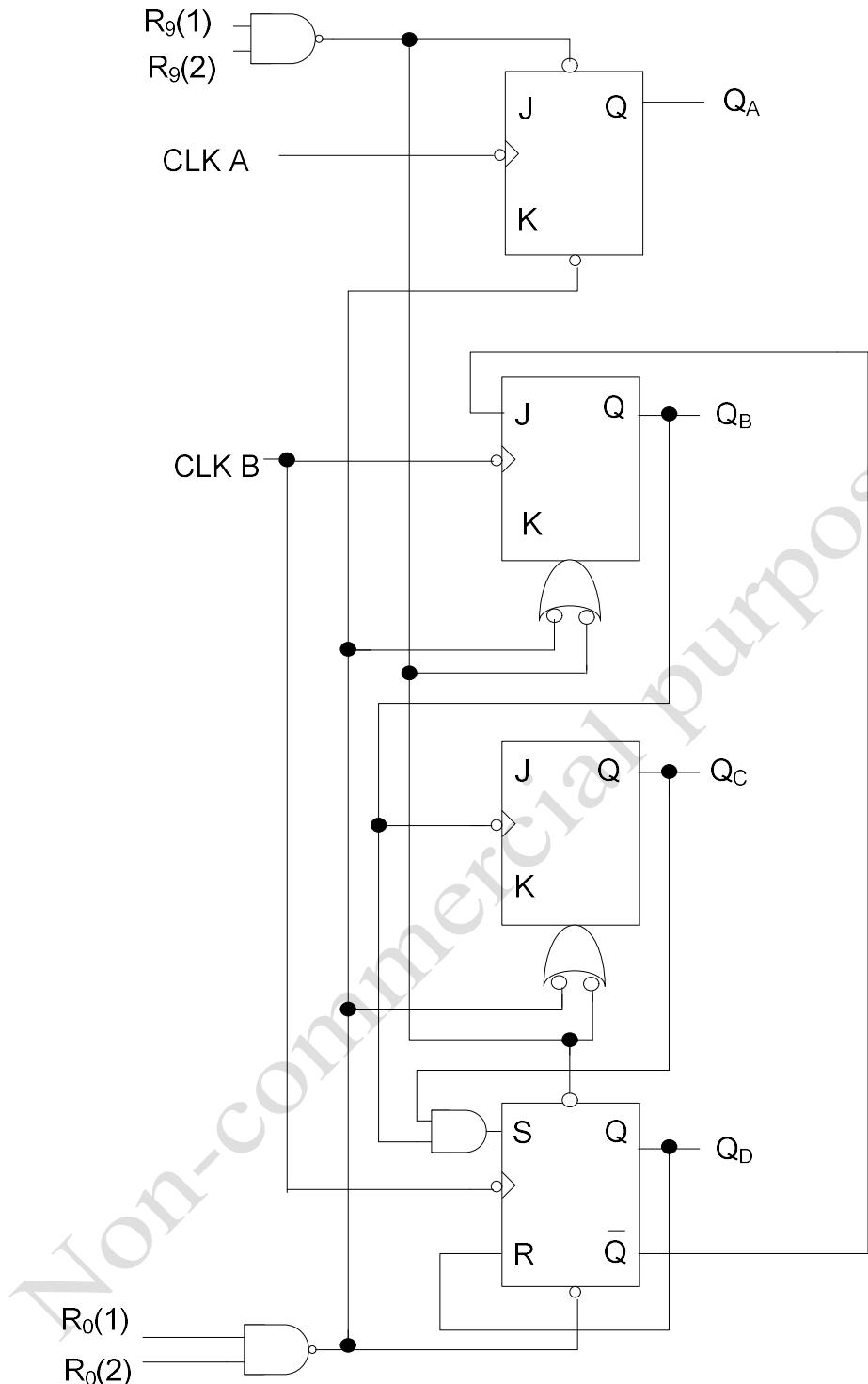
If the clock is applied at input B and the outputs are taken at Q_B , Q_C and Q_D , then the counter is divide by 6 counter.

If the clock is applied at input A, Q_A is connected to input CLK B and the outputs are taken at Q_A , Q_B , Q_C and Q_D , then the counter is divide by 12 counter.

$R_0(1)$ and $R_0(2)$ are used to reset all flip flops simultaneously.

Q12. Explain IC 7490.

Answer: Following is the logical diagram for IC 7490

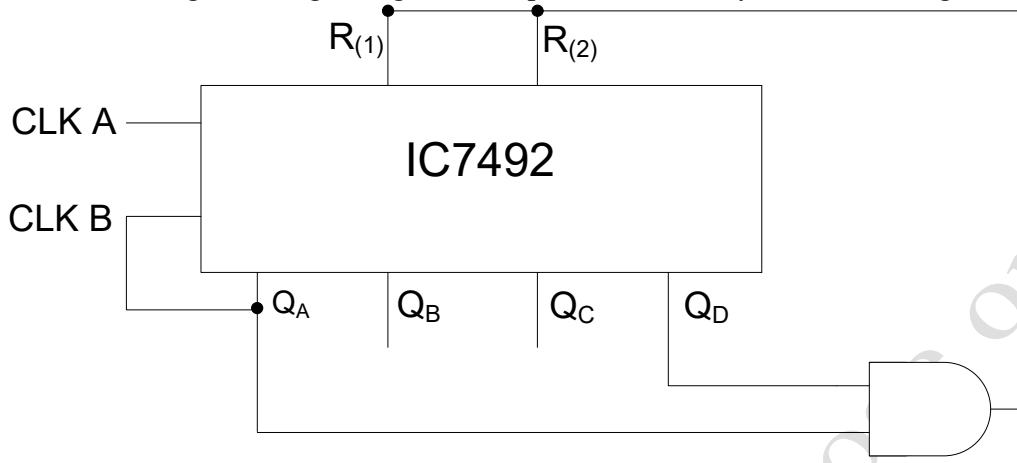


IC 7490 is a decade counter. If the system clock is applied at CLK A and Q_A is connected to CLK B, then the counter is a decade counter.

R₀₍₁₎ and R₀₍₂₎ are used to reset all flip flops simultaneously.

Q13. Design divide by 9 counter using IC 7492.

Answer: Following is the logic diagram to implement divide by 9 counter using IC 7492.



IC 7492 is a mod-12 counter when Q_A is connected to CLK B.

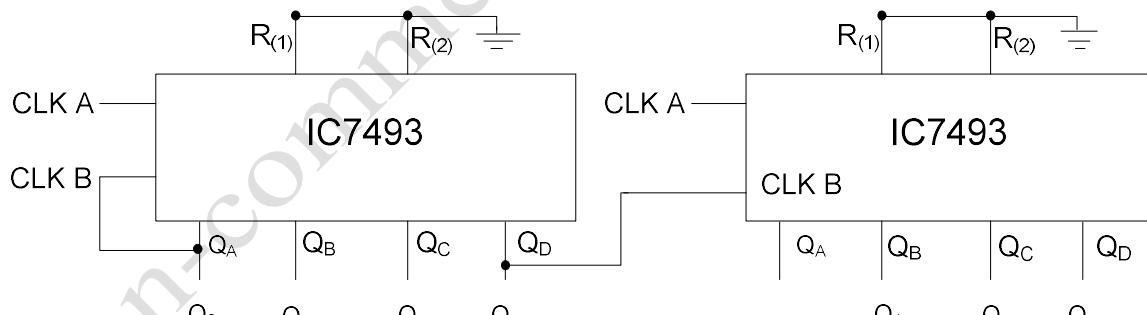
In the above diagram, when Q_DQ_CQ_BQ_A=1001, output of the AND gate is high and as a result, the counter reset as Q_DQ_CQ_BQ_A=0000. Thus, the above circuit is a divide by 9 counter.

Q14. Design a divide by 128 counter using 7493 ICs.

Answer: Following is the logic diagram divide by 128 counter.

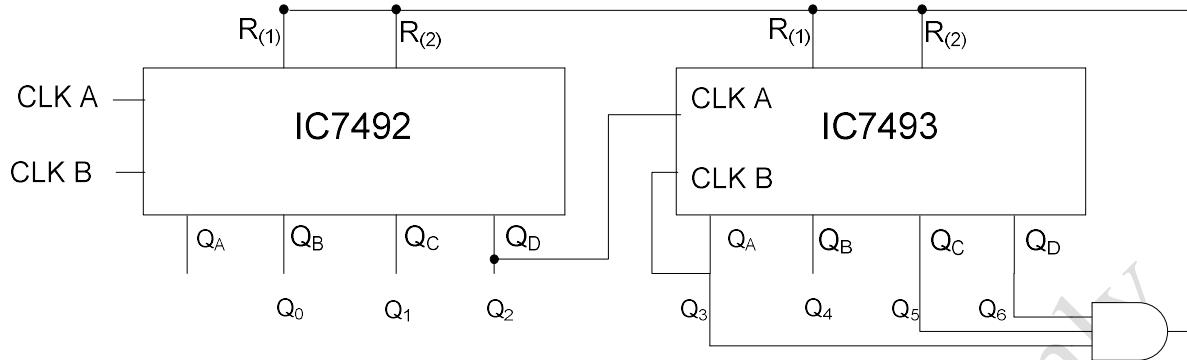
$128 = 16 \times 8$. First IC 7493 is used as divide by 16. The CLK B is input from Q_A and the external clock is applied at CLK A.

Second IC 7493 is used as divide by 8. CLK A is unused. CLK B is input from Q_D of the first IC.



Q15. Design a divide by 78 counter using 7493 and 7492 counter ICs.

Answer: Following is the logic diagram divide by 78 counter.



$$78=6 \times 13.$$

IC 7492 is used as divide by 6 counter. CLK A is unused and the external clock is applied to the CLK B.

IC 7493 is to be used as divide by 13 counter. To make this as divide by 13 counter, Q_D of IC 7492 is connected to the CLK A of IC 7493. Q_A, Q_C and Q_D are connected as input to a AND gate and output of the AND gate is connected reset pins.

Q16. Design mod-3 synchronous counter.

Answer:

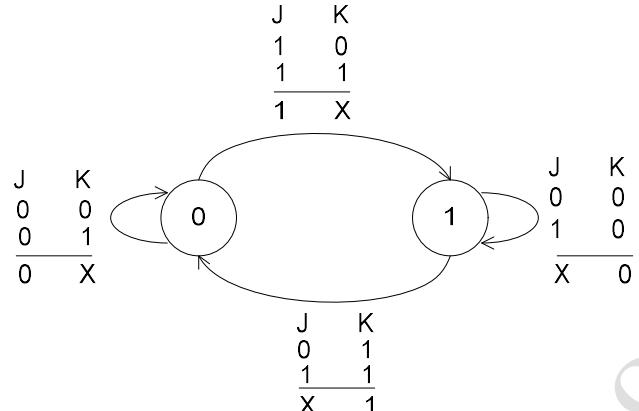
Truth Table

Clock	Counter Output	
	Q ₂	Q ₁
0	0	0
1	0	1
2	1	0
3	0	0

Truth Table for JK Flip Flop

J	K	Q_{n+1}	Action
0	0	Q_n	No Change
0	1	0	Reset
1	0	1	Set
1	1	\bar{Q}_n	Toggle

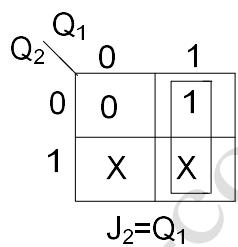
State Transition Diagram for JK Flip Flop



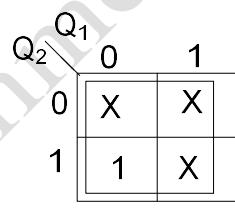
State table for the design of Modulo-3 synchronous counter

Present State		Next State		J_2	K_2	J_1	K_1
Q_2	Q_1	Q_2^+	Q_1^+				
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	0	0	X	1	0	X

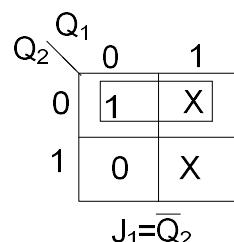
K- Map for J_2



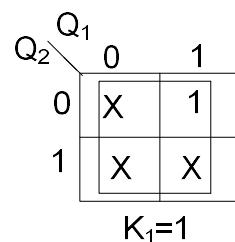
K- Map for K_2



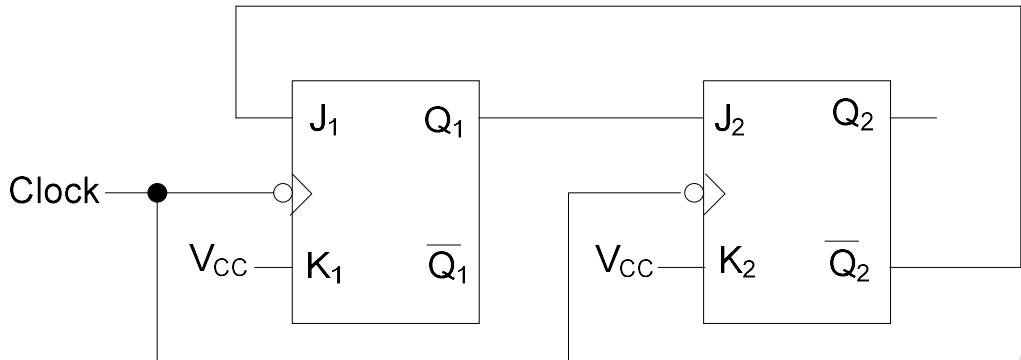
K- Map for J_1



K- Map for K_1



Logic diagram:



Q17. Design mod-5 synchronous counter.

Answer:

Truth Table:

Clock	Counter Output		
	Q ₃	Q ₂	Q ₁
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	0	0	0

Truth Table for JK Flip Flop

J	K	Q_{n+1}	Action
0	0	Q_n	No Change
0	1	0	Reset
1	0	1	Set
1	1	\bar{Q}_n	Toggle

State Transition Diagram for JK Flip Flop

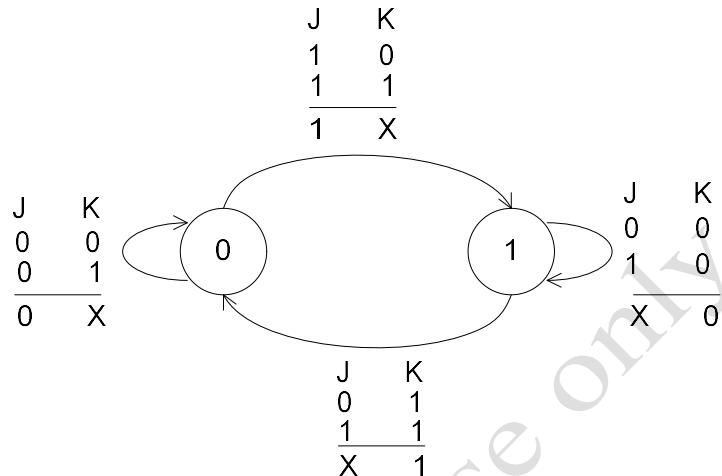
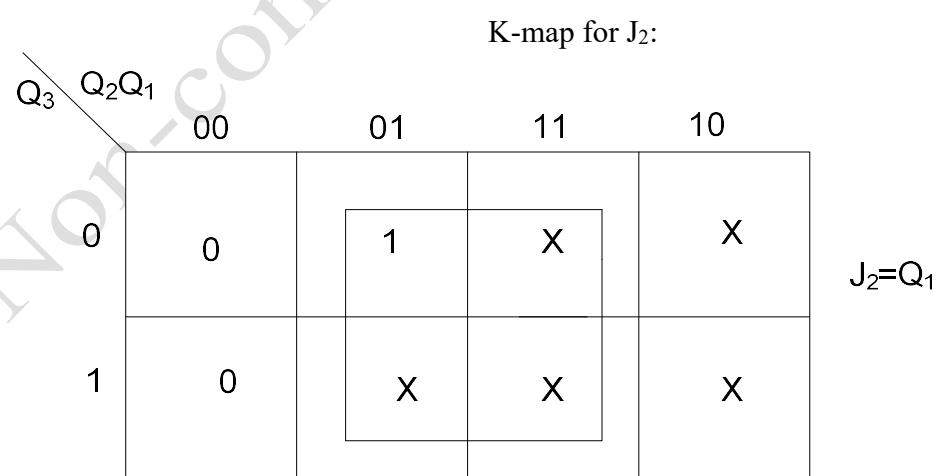
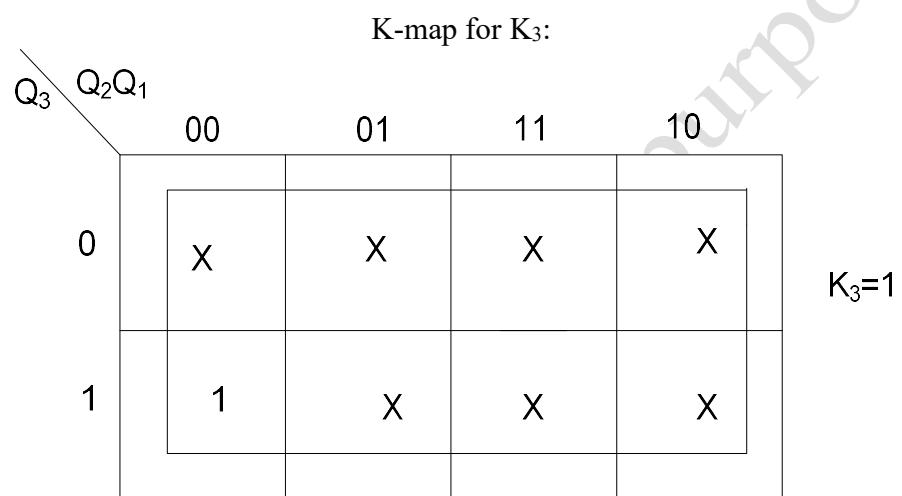
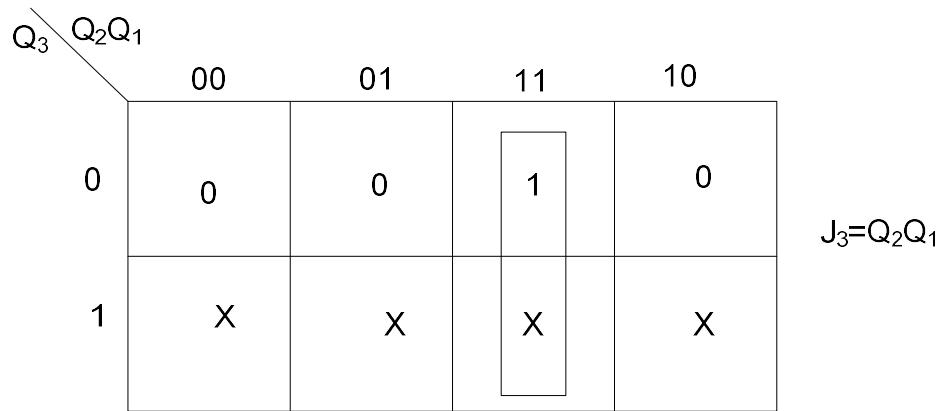
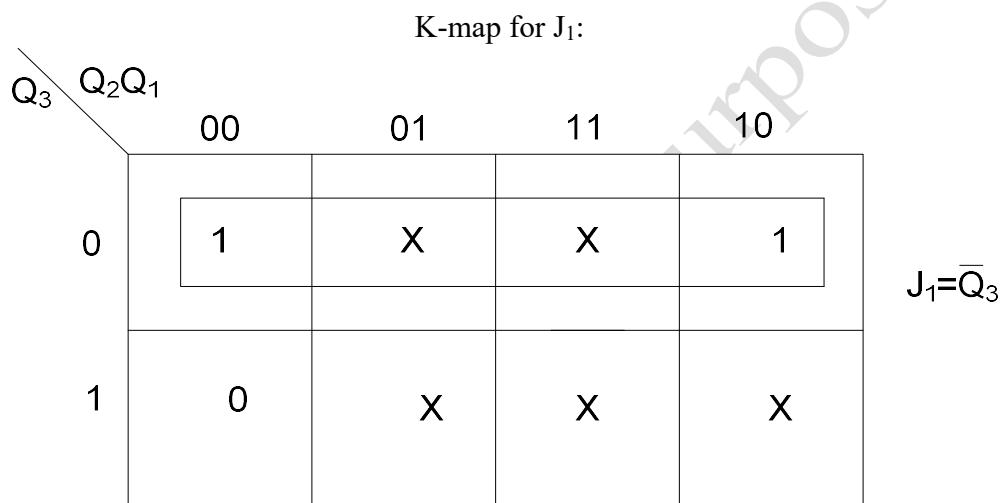
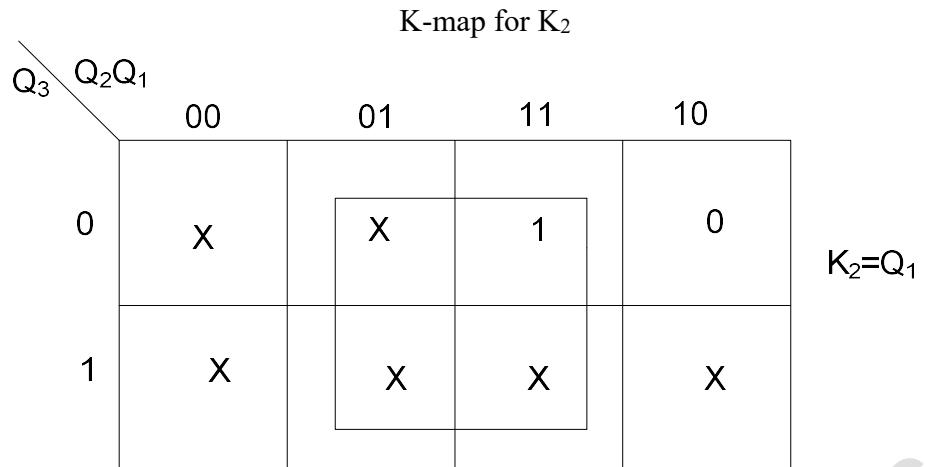


Table for the design of Modulo-5 synchronous counter

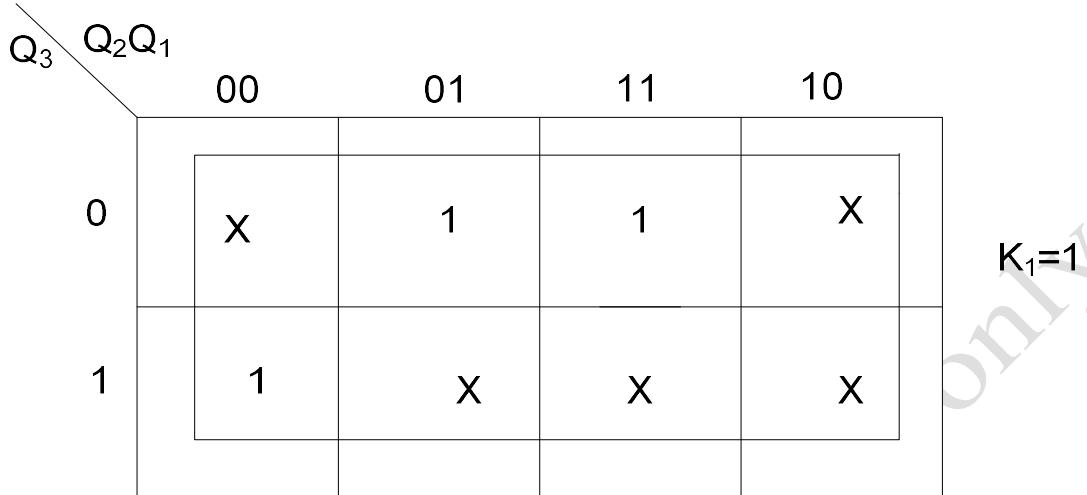
Present State			Next State			J_3	K_3	J_2	K_2	J_1	K_1
Q_3	Q_2	Q_1	Q_3^+	Q_2^+	Q_1^+						
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X

K-map for J_3 :

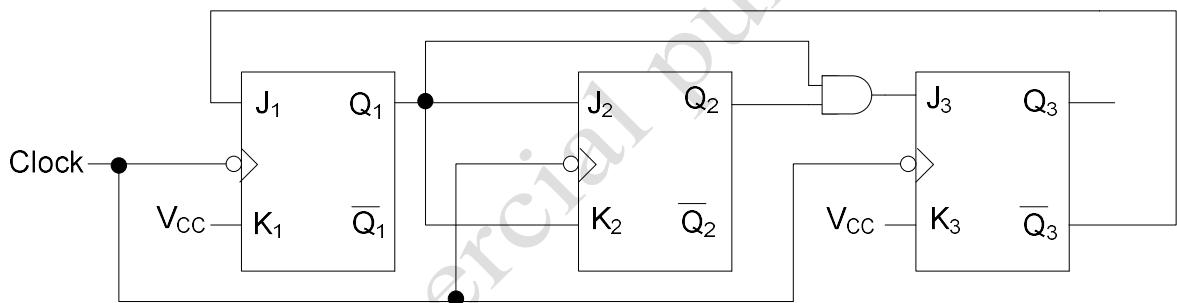




K-map for K₁:



Logic Diagram:



Q18. Design synchronous mod-6 counter.

Answer:

Truth Table:

Clock	Counter Output		
	Q ₃	Q ₂	Q ₁
0	0	0	0
1	0	0	1
2	0	1	0

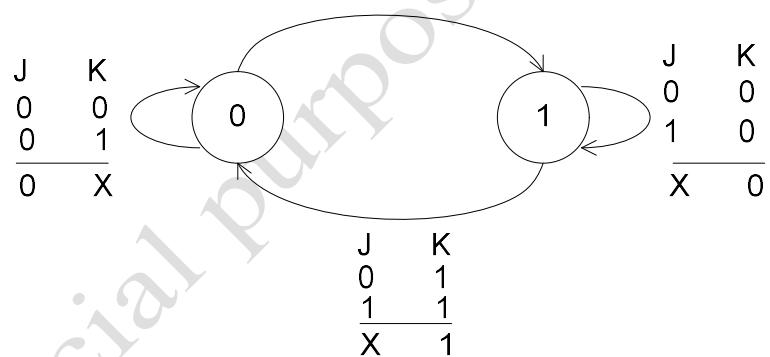
3	0	1	1
4	1	0	0
5	1	0	1
6	0	0	0

State Transition Diagram for JK Flip Flop

J	K
1	0
1	1
1	X

Truth Table for JK Flip Flop

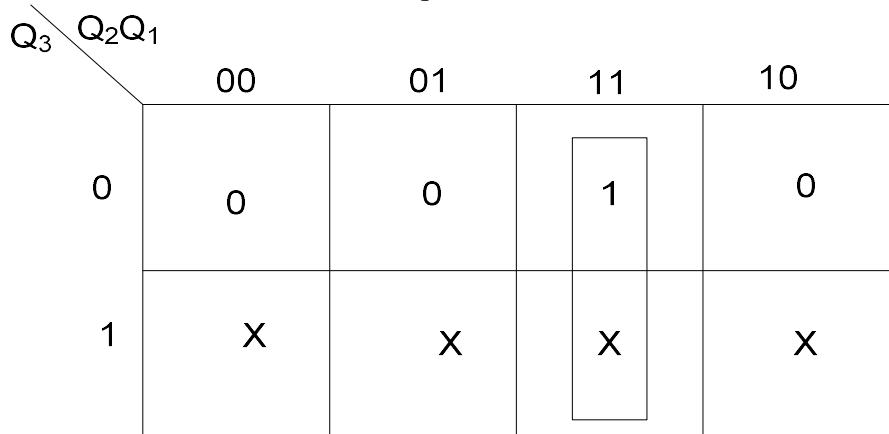
J	K	Q_{n+1}	Action
0	0	Q_n	No Change
0	1	0	Reset
1	0	1	Set
1	1	\bar{Q}_n	Toggle



State Table for the design of Modulo-5 synchronous counter

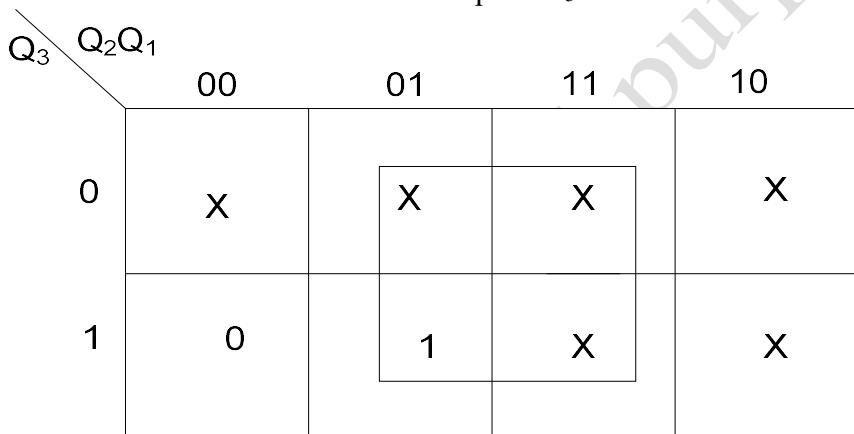
Present State			Next State			J_3	K_3	J_2	K_2	J_1	K_1
Q_3	Q_2	Q_1	Q_3^+	Q_2^+	Q_1^+						
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1

K-map for J_3 :



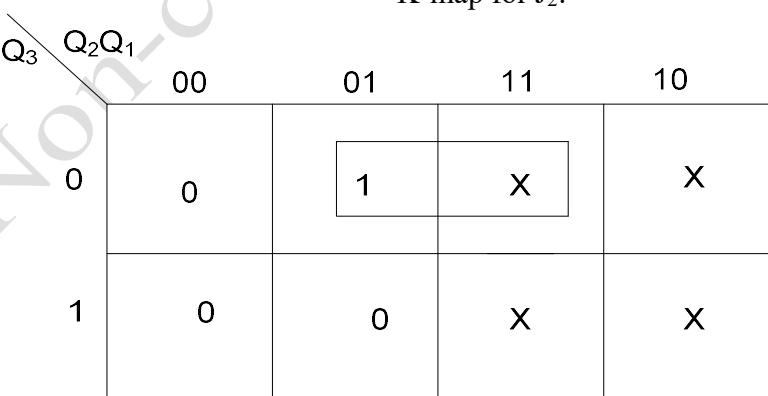
$$J_3 = Q_2Q_1$$

K-map for K_3 :



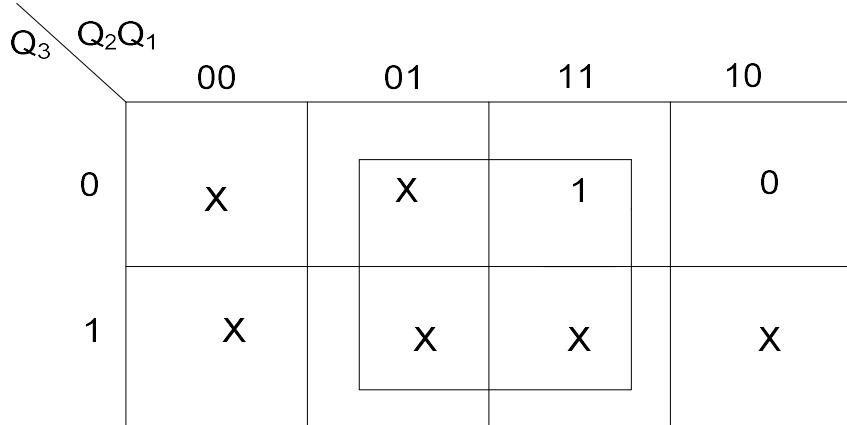
$$K_3 = Q_1$$

K-map for J_2 :



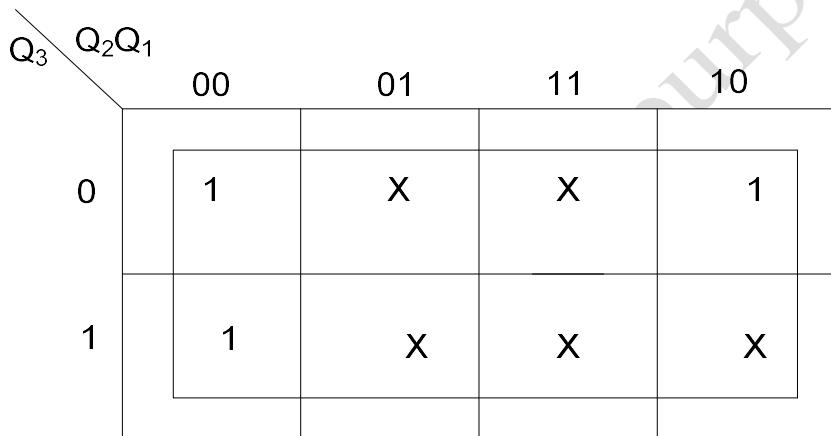
$$J_2 = \bar{Q}_3Q_1$$

K-map for K_2 :



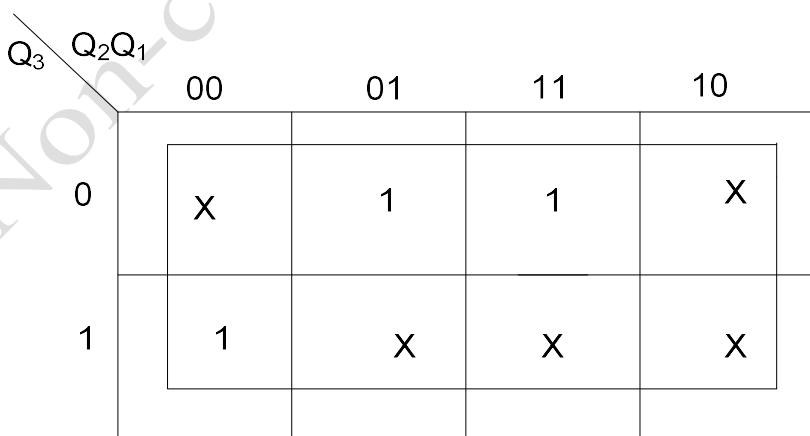
$$K_2 = Q_1$$

K-map for J_1 :



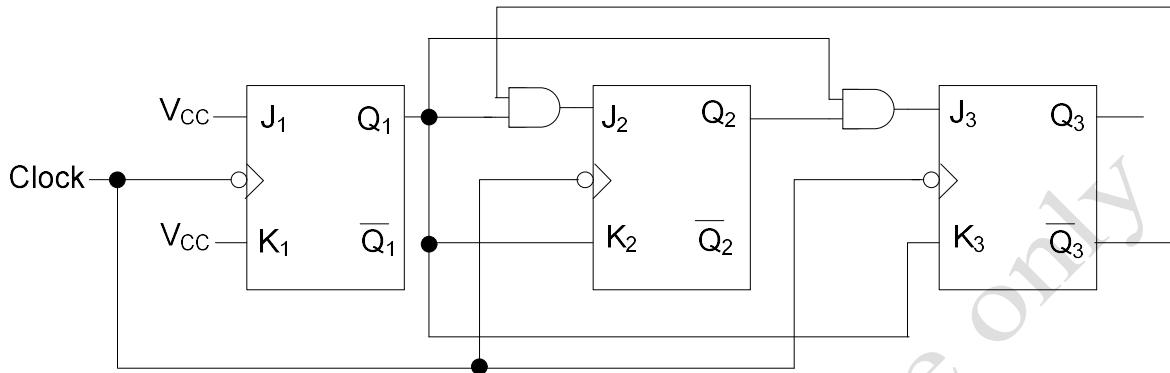
$$J_1 = 1$$

K-map for K_1 :



$$K_1 = 1$$

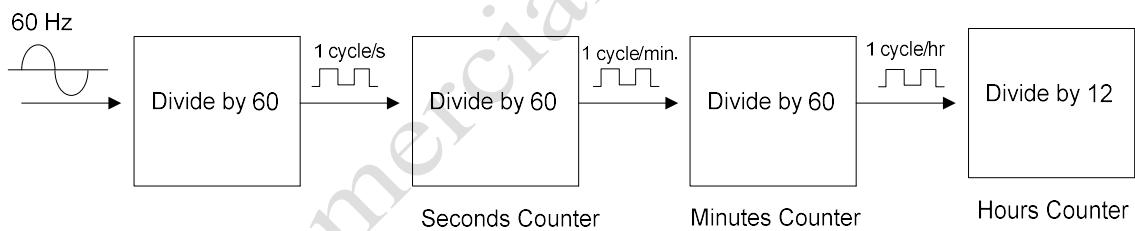
Circuit diagram:



Q19. Explain Digital Clock with block diagram.

Answer: In several countries power supply is 50Hz. There one can use standard variable frequency signal generator to get 60Hz.

Block diagram of a digital clock:



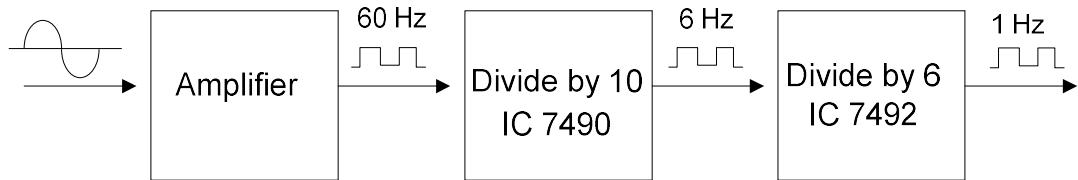
Block diagram shows the functions to be performed. The first divide by 60 counter divides the 60 Hz power signal down to a 1 Hz square wave. This 1 Hz square wave is the input to the second counter.

The second divide by 60 counter changes its state once each second and has 60 discrete states. It can be decoded to provide signal to display second. This counter produces output square wave of 1 cycle per minute and this is the input to the third counter.

The third divide by 60 counter changes its state once each minute and has 60 discrete states. It can be decoded to provide signal to display minute. This counter produces output square wave of 1 cycle per hour and this is input to the fourth counter.

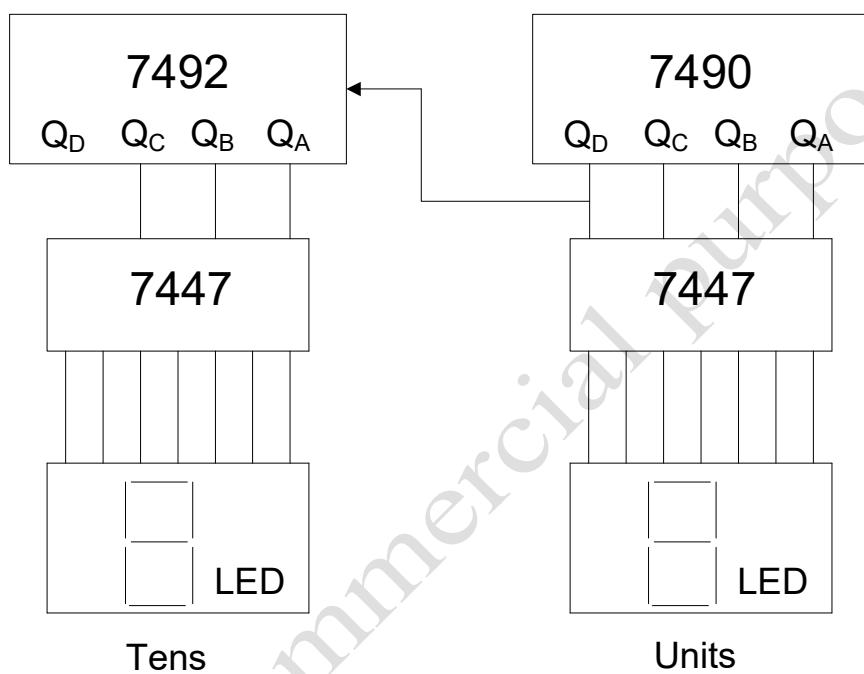
The last counter changes its state once each hour and has 12 discrete states. It can be decoded to provide signal to display hour. The last counter reset at every 12 hours.

Divide by 60 counter can be implemented by cascading divide by 10 counter (IC 7490) and divide by 6 counter (IC 7492). This is in the block diagram below.



.Display of Second, Minute and Hour can be implemented by the IC 7447 and 7 segment display.

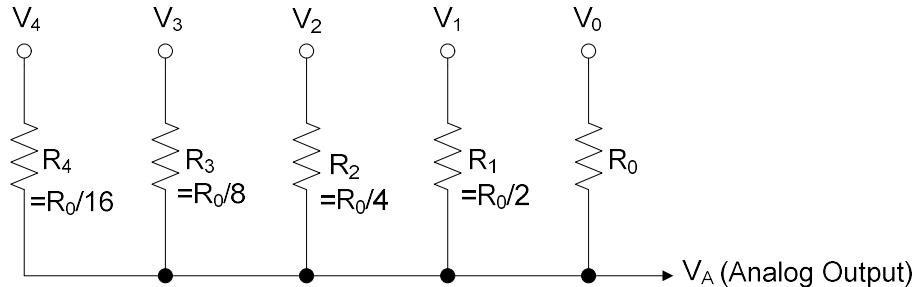
This is shown below in the following diagram.



MODULE 5

Q1. Explain 5-bit resistive divider with diagram.

Answer: 5-bit resistive divider is shown below:



A resistive divider can be built to change a digital voltage to an equivalent analog voltage.

The following criterion can be applied to resistive divider.

- There must be one input resistor for each digital bit.
- Beginning with the LSB, each following resistor value is one half of the previous resistor.
- The LSB has weight of $\frac{1}{2^n - 1}$, where n is the number of input bits.
- The change in output voltage due to a change in the LSB is equal to $\frac{V}{2^n - 1}$ where V is the digital input voltage.
- The output voltage can be obtained for any digital input signal by following equation.

$$V_A = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2 + V_3 2^3 + \dots + V_{n-1} 2^{n-1}}{2^n - 1}$$
, where $V_0, V_1, V_2, \dots, V_{n-1}$ are the digital voltage (0 or V) and n is the number of input bits.

Q2. For a 5-bit resistive divider, determine the following (a) the weight assigned to the LSB

(b) the weight assigned to the second and the third LSB (c) the change in output voltage due to a change in the LSB, the second LSB, and the third LSB (d) the output voltage for a digital input 10101. Assume 0= 0 V and 1=+10 V.

Answer:

(a) The LSB weight is $\frac{1}{2^5 - 1} = \frac{1}{31}$

(b) The second LSB weight is $\frac{2}{31}$ and third LSB weight is $\frac{4}{31}$

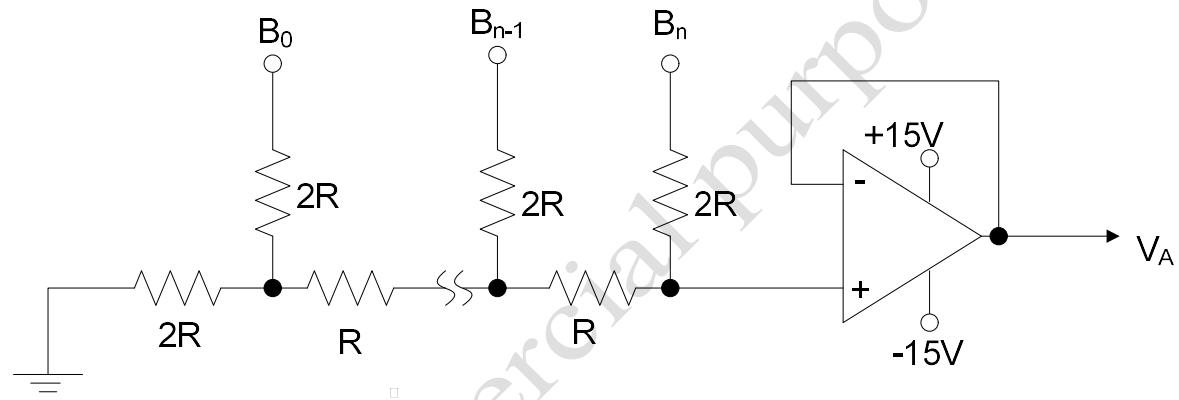
(c) The LSB causes a change in the output voltage of $\frac{10}{31}$ V. The second LSB causes an output voltage change of $\frac{20}{31}$ V and third LSB causes an output voltage change of $\frac{40}{31}$ V.

(d) The output voltage for a digital input of 10101 is

$$V_A = \frac{10 \times 2^0 + 0 \times 2^1 + 10 \times 2^2 + 0 \times 2^3 + 10 \times 2^4}{2^5 - 1} = \frac{10(1+4+16)}{31} = \frac{210}{31} = 6.77 \text{ V}$$

Q3. Explain binary ladder with diagram.

Answer: Binary ladder is shown below.



B_n, B_{n-1}, \dots, B_0 are the digital inputs, whose values are either 0 (0 Volt) or 1(V Volt).

B_n is MSB and B_0 is the LSB.

$$V_A = V \left(B_n \times \frac{1}{2} + B_{n-1} \times \frac{1}{4} + \dots + B_0 \times \frac{1}{2^n} \right)$$

Q4. Find the output voltage from a 5-bit ladder that has a digital input of 11010. Assume that

0=0 V and 1=+10 V.

Answer:

$$V_A = 10 \left(1 \times \frac{1}{2} + 1 \times \frac{1}{4} + 0 \times \frac{1}{8} + 1 \times \frac{1}{16} + 0 \times \frac{1}{32} \right) = 10 \left(\frac{1}{2} + \frac{1}{4} + \frac{1}{16} \right) = 8.125 \text{ V}$$

Q5. Explain the terms accuracy and resolution for D/A converter.

Answer:

Accuracy is a measure of how close the actual output voltage is to the theoretical output value. For example, suppose the theoretical output voltage for a particular input is +10 V. For accuracy of 1 percent, the actual output voltage must lie between +9.9 V and +10.1 V. Resolution defines the smallest increment in voltage that can be recognized. Resolution is a function of number of bits in the digital input signal. In a 4-bit ladder system, the LSB weight of $1/16$. This means that the smallest increment in output voltage is $1/16$ of the input voltage. If the input voltage is +16 V, then the output voltage changes in steps of 1 V. This converter cannot resolve voltages smaller than 1 V. This converter is not capable of distinguishing voltages finer than 1 V which is the resolution of the converter.

Q6. What is the resolution of a 9-bit D/A converter which uses a ladder network? What is the resolution expressed as a percentage? If the full scale output voltage of this converter is +5 V, What is the resolution in volts?

Answer:

In a 9-bit system, the LSB has a weight of $\frac{1}{2^9} = \frac{1}{512}$.

Hence, the resolution of the converter expressed in percentage = $\frac{1}{512} \times 100\% \approx 0.2\%$

The resolution in volt = $\frac{1}{512} \times 5 \approx 10mV$

Q7. How many bits are required at the input of a converter if it is necessary to resolve voltage to 5 mV and the ladder has +10 V full scale?

Answer:

Resolution = $\frac{1}{2^n} \times$ full scale voltage where n is the number of bits

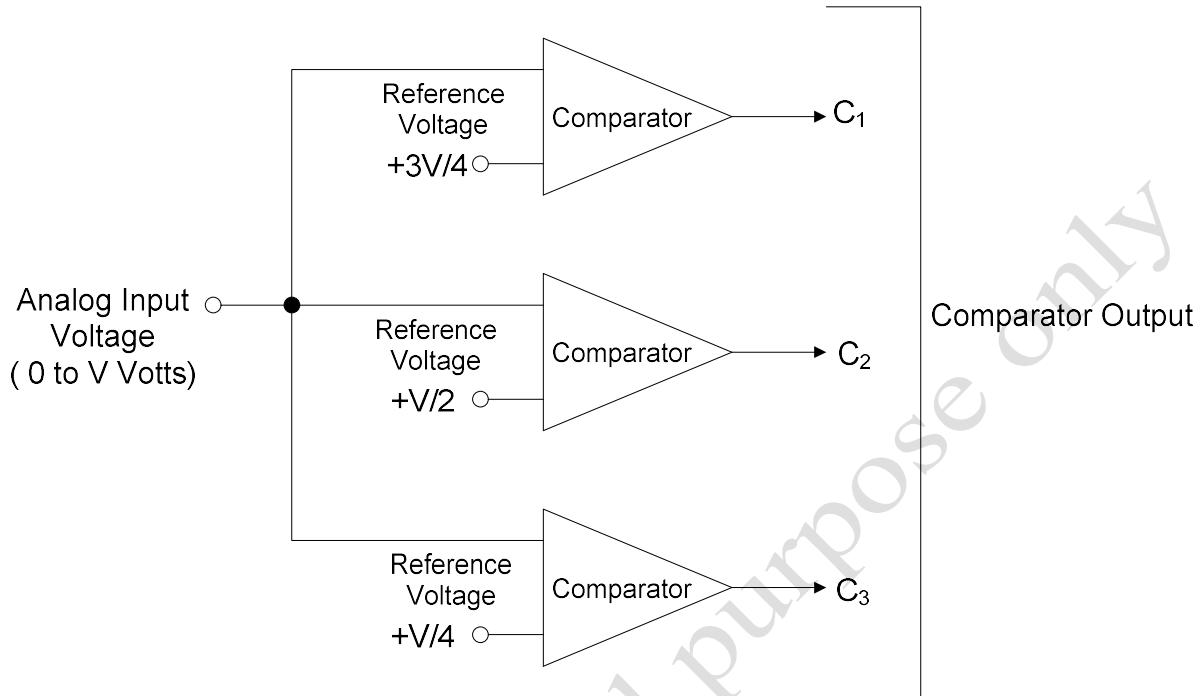
$$\Rightarrow 5 \times 10^{-3} = \frac{1}{2^n} \times 10$$

$$\Rightarrow 2^n = 2000$$

$$\Rightarrow n \approx 11$$

Q8. Explain simultaneous A/D converter with diagram.

Answer: Following is the logical diagram for 2-bit simultaneous A/D converter.



Following table shows the comparator output for input voltage ranges

Input Voltage	Comparator Output		
	C_3	C_2	C_1
0 to $+V/4$	Low	Low	Low
$+V/4$ to $+V/2$	Low	Low	High
$+V/2$ to $+3V/4$	Low	High	High
$+3V/4$ to V	High	High	High

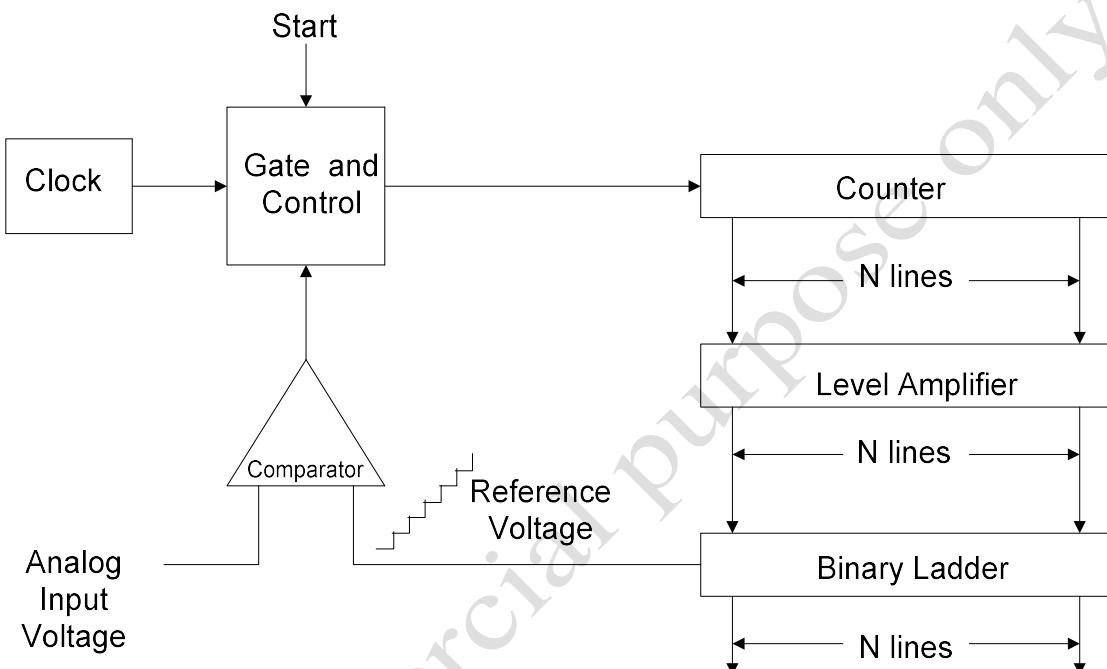
The simultaneous method of A/D conversion using three comparators is shown in the above figure. The analog signal to be digitized serves as one of the inputs to each comparator. The second input is a standard reference voltage. The reference voltages used are $+V/4$, $+V/2$ and $+3V/4$. The system is then capable of accepting an analog input voltage between 0 and $+V$.

If the analog signal exceeds the reference voltage to any comparator, that comparator turns on. Now, if all the comparators are off, the analog input signal must be between 0 and $+V/4$. If C_1 is high and C_2 and C_3 are low, the input must be between $+V/4$ and $+V/2$. If C_1 and C_2 are high and C_3 is low, the input must be between $+V/2$ and $+3V/4$. If all the

comparator outputs are high, the input signal must be between $+3V/4$ and $+V$.

Q9. Explain counter type A/D converter with diagram.

Answer: Following is the counter type A/D converter



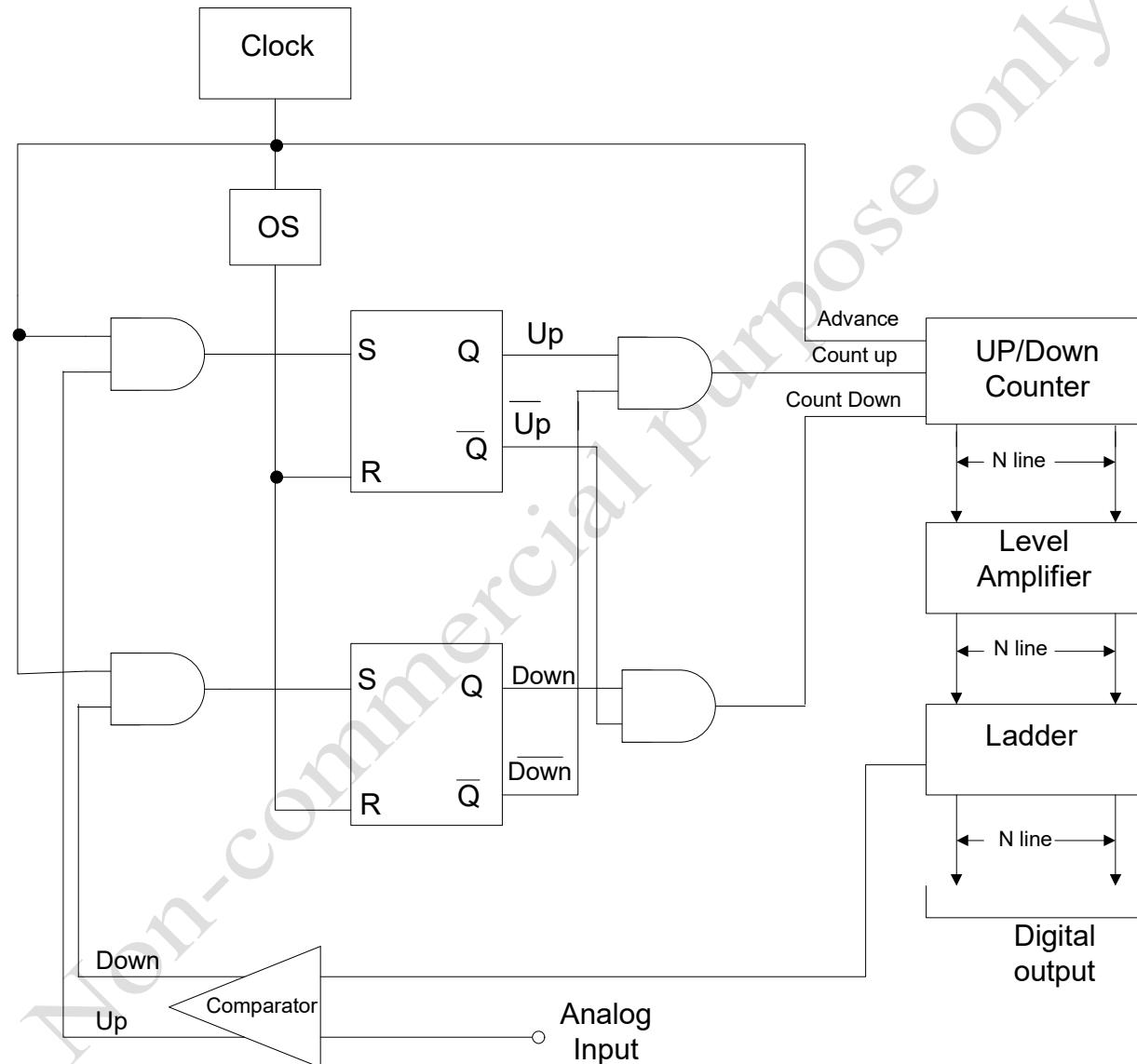
This type of A/D converter consists of binary counter. The digital output signal of this counter is connected to a standard binary ladder D/A converter. If a clock is applied to the input of the counter, the output of the binary ladder D/A converter is the staircase waveform. This waveform is the reference voltage signal for the comparator.

First, the counter is reset to all 0s. Then, when a convert signal appears on the START line, the gate opens and the clock pulses are allowed to pass through to the input of the counter.

The counter advances through a normal binary count sequence, and the staircase waveform is generated at the output of the ladder. This waveform is applied to one side of the comparator and analog input voltage is applied to the other side. When the reference voltage equals (or exceeds) the input analog voltage, the gate is closed, the counter stops and the conversion is complete. The number stored in the counter is now the digital equivalent of the analog input voltage.

Q10. Explain continuous A/D converter with diagram.

Answer: Following is the continuous A/D converter:



This type of A/D converter consists of binary up/down counter. The digital output signal of this counter is connected to a standard binary ladder to form a D/A converter. Output of the ladder is

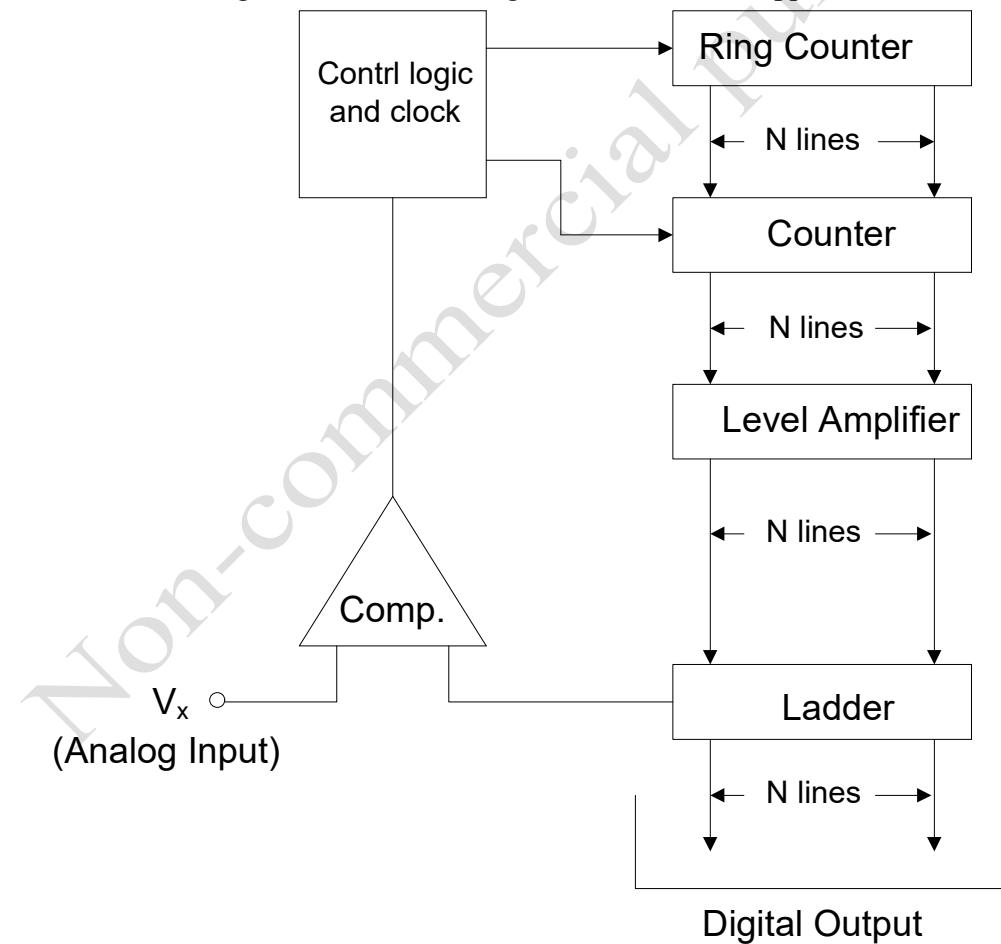
fed into a comparator which has two outputs. When the input analog voltage is more positive than the ladder output, Up output of the comparator is high. When the input analog voltage is more negative than the ladder output, the down output is high.

If the Up output of the comparator is high, the AND gate at the input of the Up flipflop open, and the first time the clock goes positive, the flipflop is set. At moment down flipflop is reset, the AND gate which controls the count-up line of the counter will be true and the counter advance one count. As long as the Up line out of the comparator is high, the converter continues to operate and advances its count.

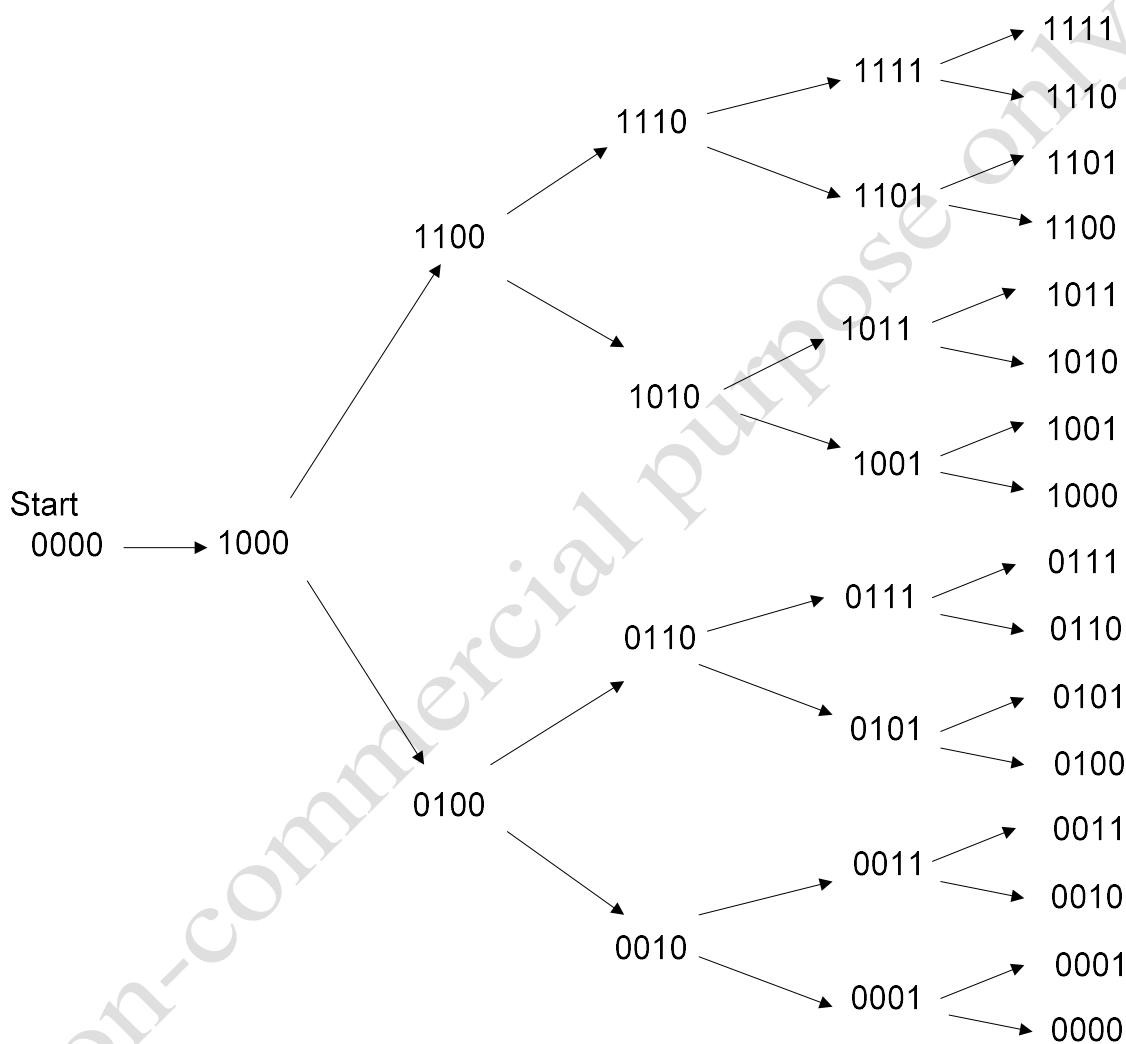
At the point where the ladder voltage becomes more positive than the input voltage, the Up line of the comparator goes low and the Down line goes high. The converter then goes through a count-down conversion cycle.

Q11. Explain successive approximation converter with diagram.

Answer: Following shows the block diagram for successive approximation converter.



Following shows the operation performed in successive approximation converter



Successive approximation converter consists of counter which is first reset to all 0s. The MSB of the counter is then set. The MSB is then left in or taken out (by resetting the MSB flipflop) depending on the output of the comparator. Then the second MSB is set in, and comparator is made to determine whether to reset the second MSB flipflop. The process is repeated down to LSB and at this time desired number is in the counter. The converter operates by successive dividing the voltage ranges in half. The successive approximation method is the process of approximating the analog voltage by trying 1 bit at a time beginning with MSB. The operation is shown in the above diagram.

VERILOG

Q1. What is the need for HDL? Explain the structure of VHDL/Verilog program.

Answer: Need for HDL:

- (i) HDL is able to describe a large complex design requiring hundreds of logic gates in a convenient manner.
- (ii) HDL is able to use software test-bench to detect functional error if any and correct it called simulation.
- (iii) HDL is used to get hardware implementation details called synthesis.

Structure of Verilog HDL:

```
module testcircuit (x,y,a,b,c); //module name with port list  
input a,b,c; //defines input ports  
output x,y; // defines output port  
// module body begins  
.....  
// module body ends  
endmodule
```

Q2. Write verilog code for two-input AND gate in (i) Structural Model (ii) Dataflow Model

(iii) Behavioral Model

Answer: (i) Structural Model:-

```
module and_gate (A,B,Y);  
input A,B; //defines two input port  
output Y; //defines one output port  
and g1(Y,A,B); // g1 is optional user defined gate identifier  
endmodule
```

(ii) Dataflow Model:-

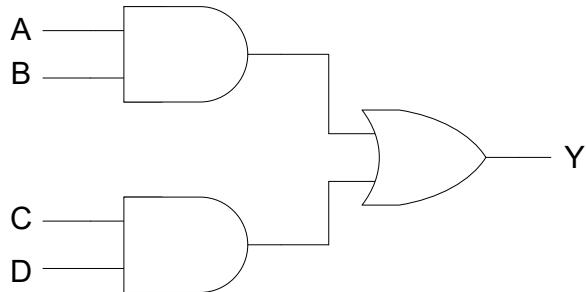
```
module and_gate (A,B,Y);  
input A,B; //defines two input port  
output Y; //defines one output port  
assign Y=A&B;  
endmodule
```

(iii) Behavioral Model:-

```
module and_gate (A,B,Y);  
input A,B; //defines two input port  
output Y; //defines one output port  
reg Y;  
always @ (A or B)  
if ((A==1) && (B=1))  
Y=1;  
else  
Y=0;
```

endmodule

Q3. Write a verilog code for the following figure in (i) Structural Model (ii) Dataflow Model
(iii) Behavioral Model



(i) Structural Model:

```
module figure(A,B,C,D,Y)
input A,B,C,D;
output Y;
wire and_op1, and_op2; //Internal connection
and g1(and_op1,A,B);
and g2(and_op2,C,D);
or g3(Y, and_op1, and_op2);
endmodule
```

(ii) Dataflow Model:

```
module figure(A,B,C,D,Y)
input A,B,C,D;
output Y;
assign Y=(A & B) | (C & D);
endmodule
```

(iii) Behavioral Model:

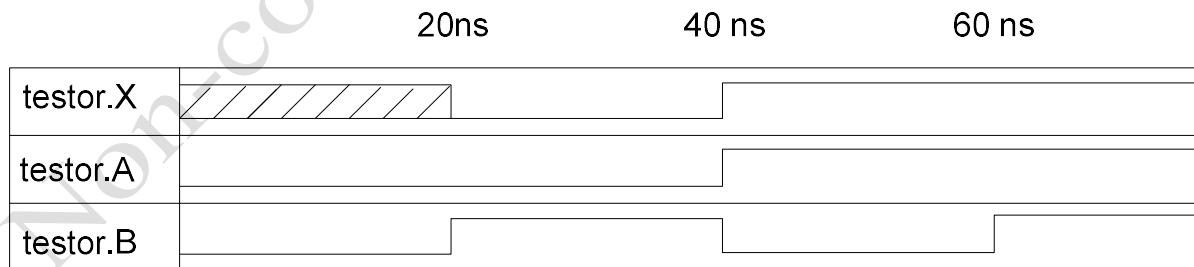
```
module figure(A,B,C,D,Y);
input A,B,C,D;
output Y;
reg Y;
always @ (A or B or C or D) //A,B,C,D form sensitivity list
if ((A==1) && (B==1))
Y=1;
else if ((C==1) && (D==1))
Y=1;
else //for all other combination of A,B,C,D
Y=0;
```

endmodule

Q4. Prepare test bench in verilog to simulate OR gate. Draw the timing diagram generated by simulating the verilog code. Assume 20ns holding time of each input combination.

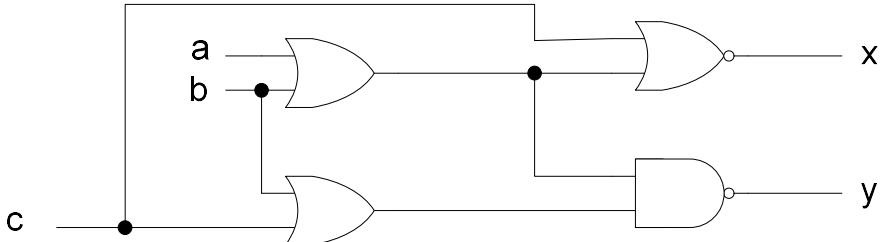
Answer:

```
module testor; // Simulation module is given a name testor
reg A,B;
wire X;
or_gate org(A,B,X); //Circuit is instantiated with the name or_gate
initial // start simulation
begin // Input is generated to test the circuit and simulation begins
A=1'b0; B=1'b0; // 1'b0 signifies an binary digit with a value 0
#20 // Delay of 20 ns
A=1'b0; B=1'b1;
#20 // Another delay 20 ns
A=1'b1; B=1'b0;
#20
A=1'b1; B=1'b1;
#20 $finish;
end
endmodule
module or_gate(A,B,X); // OR gate used as a procedure in simulation
input A,B;
output X;
or #(20) g1(X,A,B); // Gate declaration with a gate delay of 20 ns
endmodule
```



The input AB is given by testor.A and testor.B and taking the values 00,01,10 and 11. Retain these values for 20ns. The output of OR gate, testor.X changes according to input but after a delay of 20ns. For first 20ns, OR gate output is unknown as it needs 20ns respond.

Q5. Write the structural code for figure shown below and also prepare a test bench for the circuit.



Structural code:

```

module figure (a,b,c,x,y);
input a,b,c;
output x,y;
wire or_op1,or_op2; // internal connection of upper and lower OR gates
or g1(or_op1,a,b); //g1 represents the upper OR gate
or g2(or_op1,b,c); //g2 represents the lower OR gate
nor g3(x,c,or_op1); // g3 represents NOR gate
nand g4(y,or_op1,or_op2); // g4 represents NAND gate
endmodule
  
```

Test Bench:

```

module testfigure;
reg a,b,c;
wire or_op1, or_op2, x, y;
figure org(a,b,c,x,y);
initial
begin
a=1' b0; b=1' b0; c=1' b0;
# 50
a=1' b0; b=1' b0; c=1' b1;
# 50
a=1' b0; b=1' b1; c=1' b0;
# 50
a=1' b0; b=1' b1; c=1' b1;
# 50
a=1' b1; b=1' b0; c=1' b0;
# 50
a=1' b1; b=1' b0; c=1' b1;
# 50
  
```

```
a=1' b1; b=1' b1; c=1' b0;
```

```
# 50
```

```
a=1' b1; b=1' b1; c=1' b1;
```

```
# 50 $ finish;
```

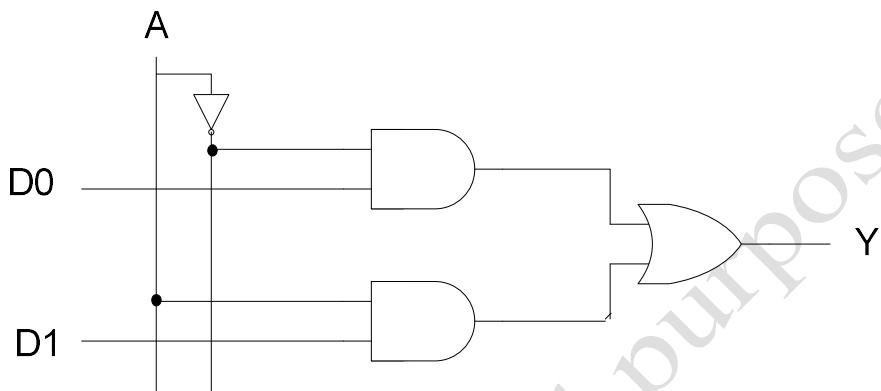
```
end
```

```
endmodule
```

Q6. Write verilog code for 2:1 Multiplexer.

Answer:

2:1 Multiplexer with the basic gates as shown below:



Verilog code for 2:1 multiplexer: Dataflow model

```
module mux2to1(A,D0,D1,Y);
input A,D0,D1;
output Y;
assign Y=(~A&D0) | (A&D1); // Alternately, assign Y= A ? D1 : D0;
endmodule
```

Alternately: Behavioral Model

```
module mux2to1(A,D0,D1,Y);
input A,D0,D1;
output Y;
reg Y;
always @ (A or D0 or D1)
if (A==1) Y=D1;
else Y=D0;
endmodule
```

Q7. Write verilog code for 4:1 Multiplexer.

Answer:

Verilog code for 4:1 multiplexer: Dataflow model

```
module mux4to1(A,B,D0,D1,D2,D3,Y);
input A,B,D0,D1,D2,D3;
output Y;
assign Y=A ? (B ? D3 :D2) : (B ? D1 :D0);
endmodule
```

Verilog code for 4:1 multiplexer: Behavioral model

```
module mux4to1(A,B,D0,D1,D2,D3,Y);
input A,B,D0,D1,D2,D3;
output Y;
reg Y;
always @ (A or B or D0 or D1 or D2 or D3)
case ({A,B}) //Concatenation of A and B where A is MCB.
0: Y=D0;
1: Y=D1;
2: Y=D2;
3: Y=D3;
endcase
endmodule
```

Q8. Write verilog code for 1:4 Demultiplexer

Answer:

Verilog code for 1:4 Demultiplexer : Behavioral model

```
module demux1to4 (S,D,Y);
input [1:0] S;
input D;
output [3:0] Y;
reg [3:0] Y;
always @ (D or S)
case ( {D,S}) // Concatenation of D and S to give 3 bits , D is MSB
3' b100 : Y=4' b0001;
3' b101 : Y=4' b0010;
3' b110 : Y=4' b0100;
3' b111: Y=4' b1000;
default: Y=4' b0000;
endcase
endmodule
```

Q9. Write verilog code for D latch.

Answer:

```
module Dlatch (D,EN,Q);
input D,EN;
output Q;
reg Q;
always @ (EN or D)
if (EN) Q=D;
endmodule
```

Q10. Write verilog code for SR latch.

Answer:

```
module SRlatch (S,R,EN,Q);
input S,R,EN;
output Q;
reg Q;
always @ (EN or S or R)
if (EN) Q=S | (~R & Q);
endmodule
```

Q11. Write verilog code for D flipflop. (+ve edge trigger)

Answer:

```
module DFFpos (D,C,Q);
input D,C;
output Q;
reg Q;
always @ (posedge C)
Q=D;
endmodule
```

Q12. Write a verilog code that converts a D flipflop to SR flipflop.

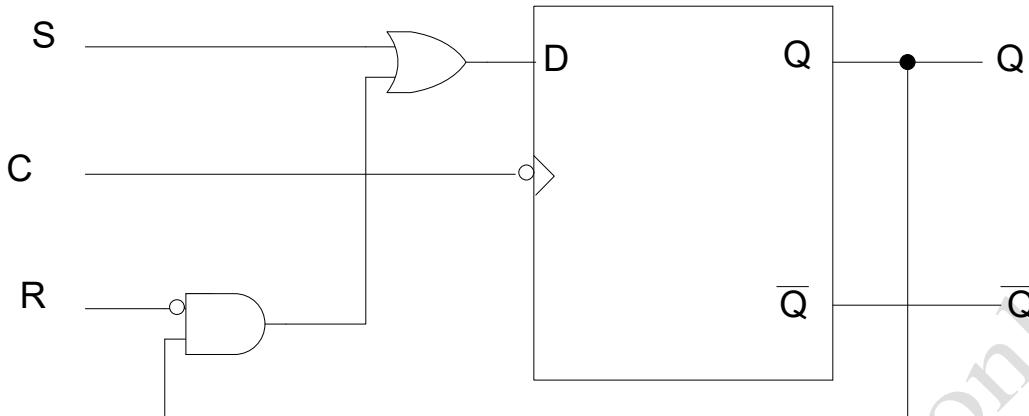
Answer:

Characteristic equation for D flipflop is $Q_{n+1}=D$

Characteristic equation for SR flipflop is $Q_{n+1}=S+R'Q_n$

Therefore, $D= S+R'Q_n$

The circuit diagram for converting D flipflop to SR flipflop is



Verilog code for the above circuit to convert D flipflop to SR flipflop:

```
module SRFFneg (S,R,C,Q);
input S,R,C;
output Q;
wire DSR;
assign DSR= S | (~R & Q);
DFFneg D1(DSR,C,Q); // Instantiate negative edge triggered D flipflop
endmodule
```

```
module DFFneg (D,C,Q);
input D,C;
output Q;
reg Q;
always @ (negedge C)
Q=D;
endmodule
```

Q13. Write a verilog code for IC 74174 (parallel in parallel out)

Answer:

```
module reg74174 (D, clock, clear, Q);
input clock, clear;
input [5:0] D;
output [5:0] Q;
reg [5:0] Q;
always @ ( negedge clock or negedge clear)
if (~clear) Q=6'b0;
else Q=D;
endmodule
```

Q14. Write a verilog code for shift register.

Answer: Following is the code for right shift register where T is the final output and Q,R,S are internal outputs.

```
module SR1 (D,clock,T);
input clock, D;
output T;
reg T;
reg Q,R,S;
always @ (negedge clock)
begin
Q<=D;
R<=Q;
S<=R;
T<=S;
End
endmodule
```

Q15. Write a verilog code for serial in serial out right shift register.

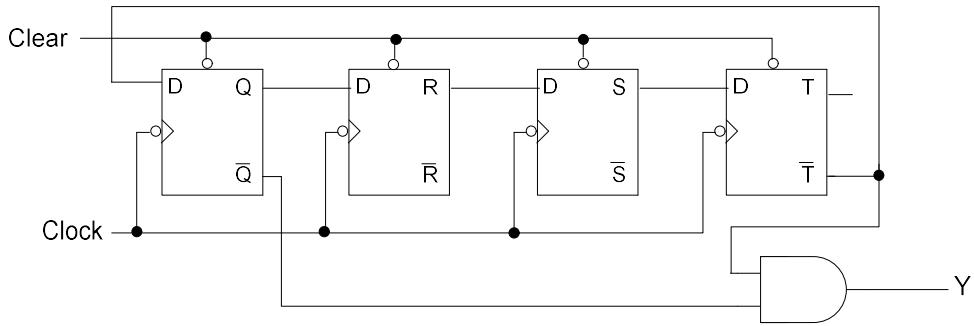
Answer:

```
module SR2 (D,clock,Q);
input clock,D;
output [3:0] Q;
reg [3:0] Q;
always @ (negedge clock)
begin
Q[0]<=D;
Q[1]<=Q[0];
Q[2]=Q[1];
Q[3]=Q[2];
end
endmodule
```

Q16. Write a verilog code switched tail counter.

Answer:

Switch tail circuit is shown below:



Verilog code for Switch tail counter:

```
module STC (clock, clear,Y);
input clock, clear;
output Y;
reg Q,R,S,T; // internal outputs of flipflops
assign Y= (~Q) & (~T);
always @ (negedge clock)
begin
if (~clear) Q= 6' b0;
else
begin
Q <= ~T;
R <=Q;
S <=R;
T <=S;
end
endmodule
```

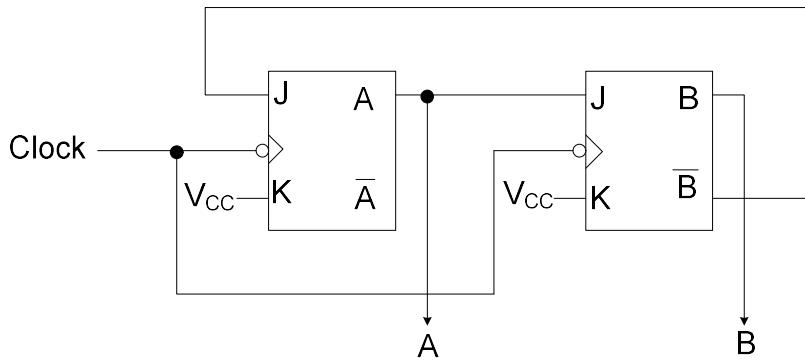
Q17. Write a verilog code for module 8 up counter.

Answer:

```
module UC (clock, reset, Q);
input clock, reset;
output [2:0] Q;
reg [2:0] Q;
always @ (negedge clock or negedge reset)
if (~reset) Q=3'b0;
else Q=Q+1;
endmodule
```

Q18. Write a verilog code for module 3 up counter using J K flip flop.

Answer: Circuit diagram for module 3 up counter is shown below:



Verilog code for module 3 up counter using JK flipflops:

```
module UCJK(A,B,clock,reset);
    input clock, reset;
    output A,B;
    wire JA, JB, KA, KB;
    assign JA=~B;
    assign KA=1'b1;
    assign JB=A;
    assign KB=1'b1;
    JKFF JK1(A,JA,KA,clock,reset);
    JKFF JK2(B, JB,KB,clock,reset);
endmodule

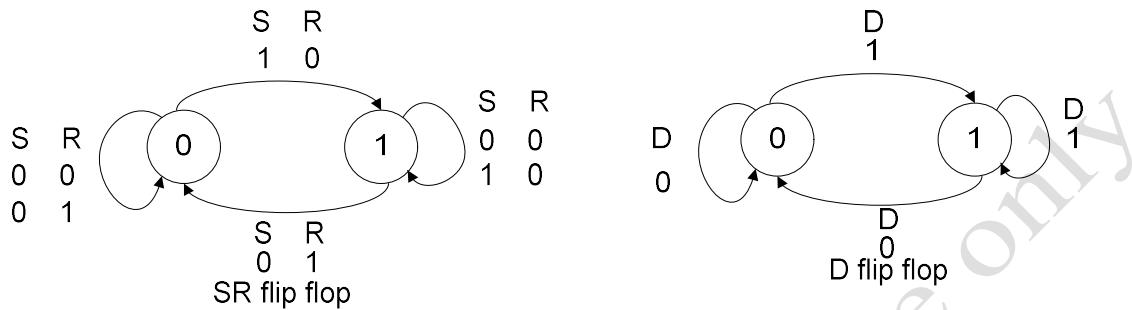
module JKFF( Q,J,K,clock,reset);
    input J,K,clock,reset;
    output Q;
    reg Q;
    always @ (negedge clock or negedge reset)
        if (~reset) Q=1'b0;
        else Q<=(J & ~Q) | (~K & Q);
endmodule
```

ADDITIONAL

Q1. Show how a D flip flop can be converted to SR flip flop.

Answer:

State Transition Diagram



Excitation Table for SR and D flip flop is given below is prepared State Transition Diagram above

$Q_n \rightarrow Q_{n+1}$	S R	D
1 0	1 X	0
2 1	1 0	1
3 0	0 1	0
2 1	X 0	1

$Q_n \setminus SR$	00	01	11	10
0	0	0	x	1
1	1	0	x	1

Characteristic Equation for SR flip flop is

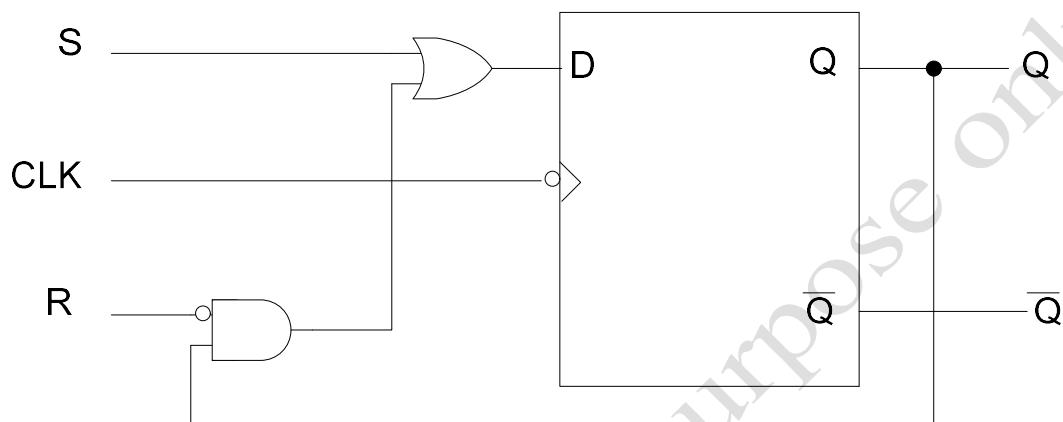
$$Q_{n+1} = S + \bar{R}Q_n$$

$Q_n \setminus D$	0	1
0	0	1
1	0	1

Characteristic Equation for D flip flop is

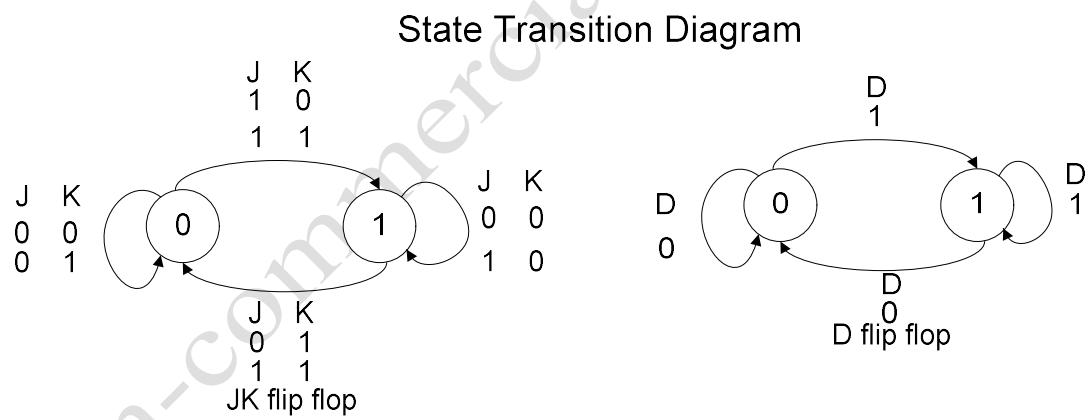
$$Q_{n+1} = D$$

Therefore, with $D = S + \overline{R}Q_n$, we get the circuit below behave like SR flipflop.



Q2. Show how a D flip flop can be converted to JK flip flop.

Answer



Excitation Table for JK and D flip flop is given below is prepared State Transition Diagram above

$Q_n \rightarrow Q_{n+1}$	J	K	D
0 0	0	X	0
0 1			
1 0	1	X	1

1	1	X	1	0
		X	0	1

JK

Q_n	00	01	11	10
0	0	0	1	1
1	1	0	0	1

Characteristic Equation for JK flip flop is

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

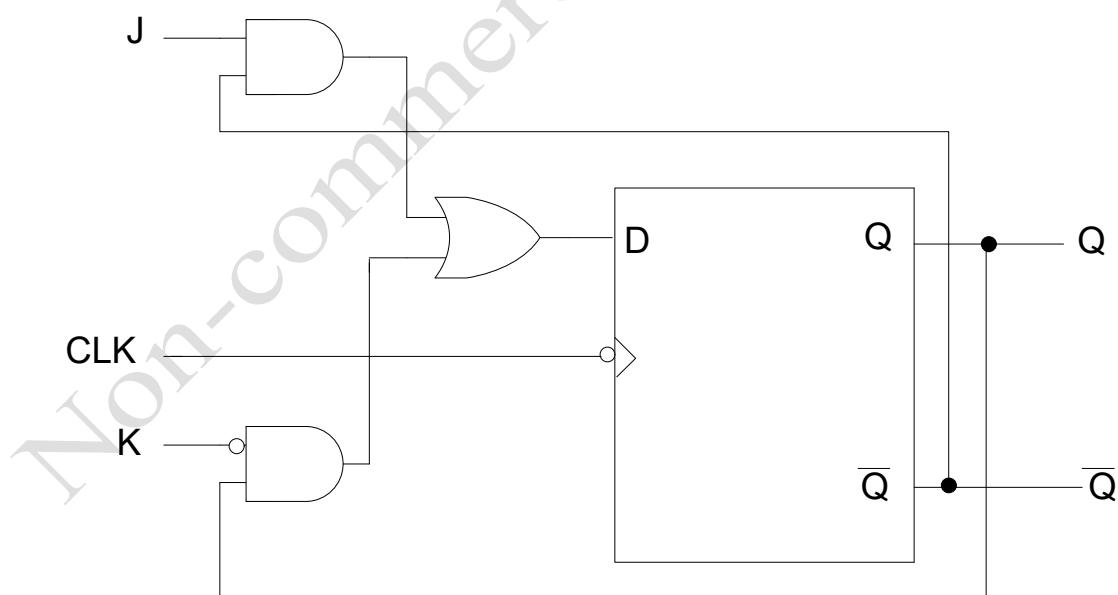
D

Q_n	0	1
0	0	1
1	0	1

Characteristic Equation for D flip flop is

$$Q_{n+1} = D$$

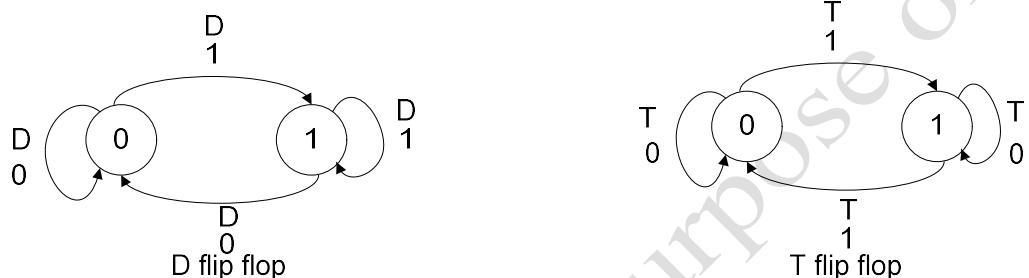
Therefore, with $D = J\bar{Q}_n + \bar{K}Q_n$, we get the circuit below behave like JK flipflop.



Q3. Show how a D flip flop can be converted to T flip flop.

Answer:

State Transition Diagram



Excitation Table for D and T flip flop is given below is prepared State Transition Diagram above

$Q_n \rightarrow Q_{n+1}$	D	T
0 0	0	0
0 1	1	1
1 0	0	1
1 1	1	0

Q_n	D	Q_{n+1}
0	0	1
1	0	1

Characteristic Equation for D flip flop is

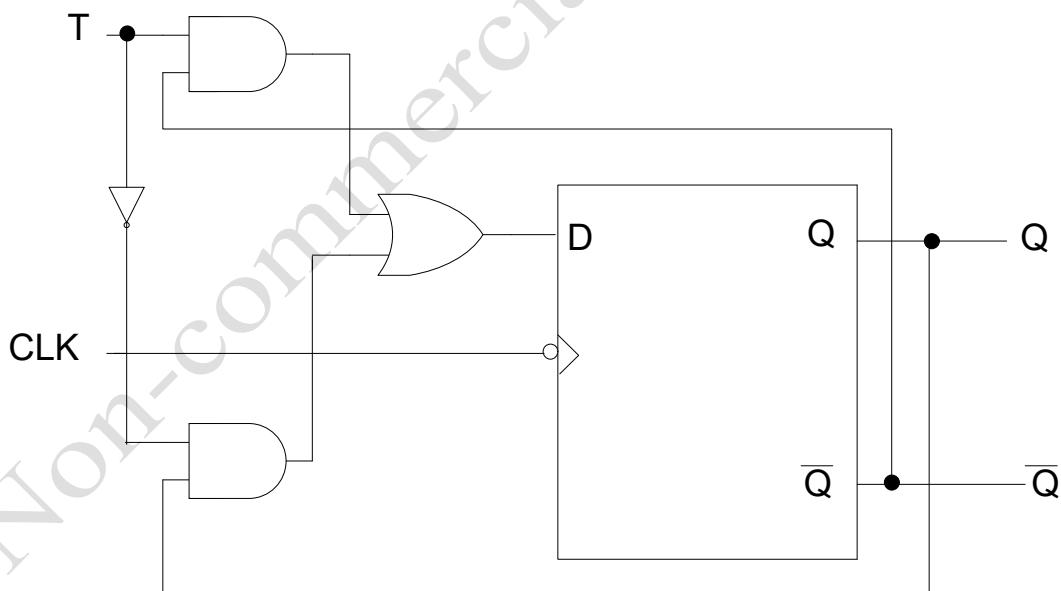
$$Q_{n+1} = D$$

Q_n	T	Q_{n+1}
0	0	1
1	1	0

Characteristic Equation for T flip flop is

$$Q_{n+1} = T\bar{Q}_n + \bar{T}Q_n$$

Therefore, with $D = T\bar{Q}_n + \bar{T}Q_n$, we get the circuit below behave like T flipflop.



Q4. Show how SR flip flop can be converted to JK flip flop.

Answer: State Synthesis table for SR to JK flip flop conversion.

J_n	K_n	Q_n	Q_{n+1}	S_n	R_n
0	0	0	0	0	x
0	0	1	1	x	0
0	1	0	0	0	x
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	x	0
1	1	0	1	1	0
1	1	1	0	0	1

$J_n K_n$	00	01	11	10
Q_n	0	0	1	1
0	0	0	X	X
1	X	0	0	X

$$S_n = J_n \bar{Q}_n$$

$J_n K_n$	00	01	11	10
Q_n	0	X	X	0
0	X	X	0	0
1	0	1	1	0

$$R_n = K_n Q_n$$

We get the circuit below behave like JK flipflop.

