# Adders and Digital Logic Circuits

Dr. J. K. Denny

August 28, 2017

## 1 Adding Binary Digits

## 2 The Half-Adder

Consider adding two binary numbers. For example, add 1101 and 1001. This gives:

$$\begin{array}{r} 1101 \\ +1001 \\ \hline 10110 \end{array}$$

More abstractly, consider adding just two binary digits, $P$ and $Q$. This will result in a sum digit $S$ and a carry digit $C$. That is,

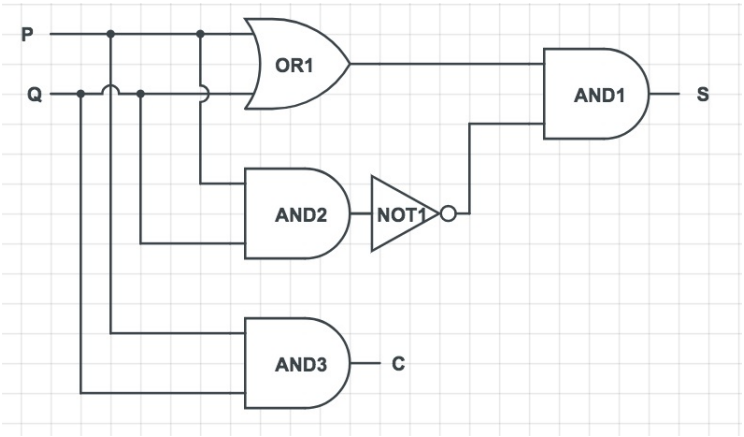
$$\begin{array}{r} P \\ +Q \\ \hline CS \end{array}$$

To write a circuit for this operation, we first build an I/O table.

| P | Q | C | S |
|---|---|---|---|
| 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 |

Thus, we see that $S \equiv (P \vee Q) \wedge \neg(P \wedge Q) \equiv P \oplus Q$ and $C \equiv P \wedge Q$. This combination of equivalences for adding binary digits is called a *half-adder*.

The half-adder circuit is given by:




# 3 The Full-Adder

Next, we wish to add three binary digits, $P$, $Q$, and $R$, and produce the sum, $S$, and carry, $C$. This often happens in a situation as seen in the second digit of the following addition in which the computation includes $1 + 1 + 0 = 10$.

$$\begin{array}{r} 1 \\ 11 \\ \underline{+01} \\ 100 \end{array}$$

Abstractly, we want to add:

$$\begin{array}{r} P \\ Q \\ \underline{+R} \\ CS \end{array}$$

We do this by breaking it down into further additions.

First, we use a half-adder to do the following:

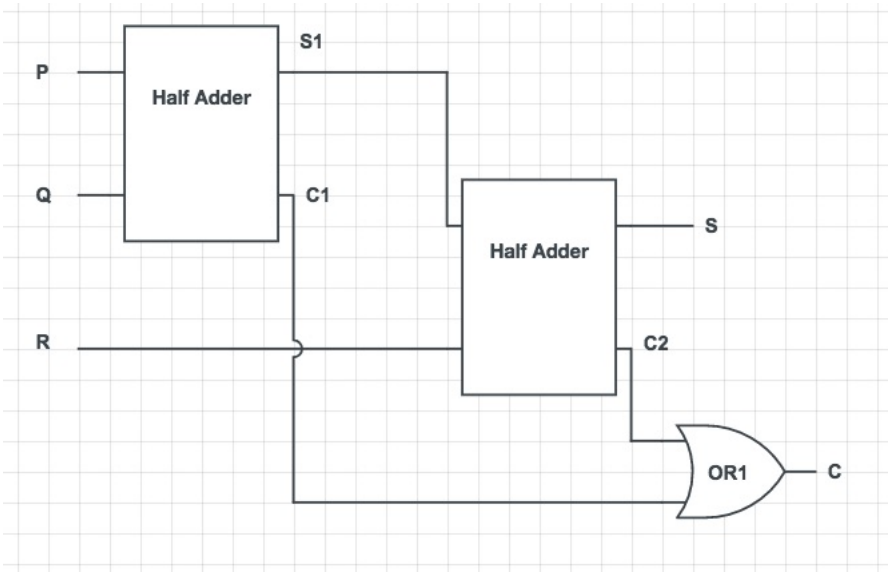
$$\begin{array}{r} P \\ \underline{+Q} \\ C_1 S_1 \end{array}$$

Then, another half-adder to find:

$$\begin{array}{r} S_1 \\ \underline{+R} \\ C_2 S \end{array}$$

Finally, we need to compute $C = C_1 + C_2$. However, $C_1$ and $C_2$ cannot both be 1. (Look at all possible cases to verify.) Thus, $C = C_1 \vee C_2$.

The full-adder circuit is given by:




# 4 The Parallel Adder

Finally, we want to add two 3-digit binary numbers. The digits will be $P, Q, R, T, U, V$ with the result $C, S_1, S_2, S_3$.

$$\begin{array}{r} PQR \\ \underline{+TUV} \\ CS_3S_2S_1 \end{array}$$

This is performed by one half-adder and two full-adders in series.

First, $R$ and $V$ feed into a half-adder and produce $S_1, C_1$. Then, $Q$ and $U$ and $C_1$ feed into a half-adder and produce $S_2, C_2$. Next, $P$ and $T$ and $C_2$ feed into a half-adder and produce $S_3, C$.