Bhavana Mehta

bhavanam@upenn.edu | bmehta5 | bhavanamehta | Google Scholar | Website

Education

University of Pennsylvania
Ph.D. + M.S., Computer & Information Science *Sept 2019 – Aug 2025*
Advisor: Dr. Boon Thau Loo

Nirma Institute of Technology, India
B.Tech., Electronics & Communication Engineering *July 2014 – May 2018*

Selected Publications

Paper on Adaptive Distributed Systems *(Submitted to SIGMOD'26)*
Bhavana Mehta, Nupur Baghel, Mohammad J Amiri, Ryan Marcus, Boon Thau Loo

Towards Full Stack Adaptivity in Permissioned Blockchains *(VLDB '24)*
Chenyuan Wu, Mohammad J Amiri, Haoyun Qin, **Bhavana Mehta**, Ryan Marcus, Boon Thau Loo

Towards Adaptive Fault-Tolerant Sharded Databases *(AIDB @ VLDB '23)*
Bhavana Mehta, Neelesh CA, Prashanth Iyer, Mohammad J Amiri, Boon Thau Loo, Ryan Marcus

AdaChain: A Learned Adaptive Blockchain *(VLDB '23)*
Chenyuan Wu, **Bhavana Mehta**, Mohammad J Amiri, Ryan Marcus, Boon Thau Loo

Human Action Recognition System using Good Features and Multilayer Perceptron Network *(ICCSP '17)*
Jonti Talukdar, **Bhavana Mehta**

Research & Work Experience

University of Pennsylvania, Philadelphia
Research Assistant *Sept 2019 – Present*

- Built *AdaChain*, a reinforcement-learning blockchain that dynamically selects transaction-processing paradigms using contextual bandits, improving throughput by 17–22% vs. static baselines. Integrated runtime protocol-switching logic developed as part of the *BFTBrain* consensus agent.
- Developed forecasting and RL-based shard-placement strategies to minimize cross-shard traffic under Byzantine faults, sustaining >10K TPS in adversarial settings.
- Designed adaptive control logic and ML pipelines to optimize dataflow and consensus selection in distributed databases and permissioned blockchains to achieve high throughput and fault tolerance.
- Conducted independent research on volatility-driven strategies across equities, options, and crypto, and achieved 43% ROI over 18 months.

Bluespec Inc., Boston, MA
Design Engineer *Jan 2018 – June 2019*

- Architected and optimized RISC-V processor cores (32/64-bit), focusing on pipeline design, hazard resolution, and timing closure to meet target clock frequency requirements.
- Automated the generation and deployment of 500+ RISC-V core variants from high-level specifications to final *tape-out*, streamlining the hardware design cycle and reducing time-to-market by 30%.

RISE Lab, Indian Institute of Technology Madras
Research Intern *May 2017 – July 2017*

- Implemented a parameterizable 64-bit SRT divider on FPGA (Bluespec SystemVerilog) for high-speed arithmetic operations, achieving a 281 ns execution latency on a Xilinx UltraScale device and informing subsequent RISC-V core design optimizations.

Skills

Programming: Python (PyTorch, NumPy), C/C++, SQL, Bash, Verilog, MATLAB
Statistics: Probability, Time-series Analysis, Machine Learning (Supervised, Unsupervised, Reinforcement Learning)
Systems: Distributed Systems, Consensus Protocols, Fault-Tolerance, Algorithmic Optimization, High-Performance Computing
Tools: PyTorch, scikit-learn, NumPy, Pandas, Docker, Git