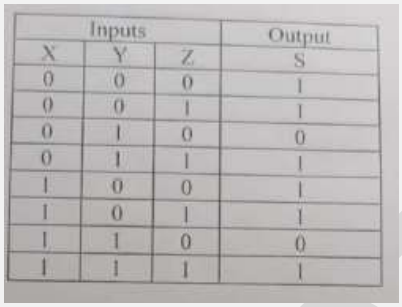
PART A (MODULE I/II/III/IV/V)		
3 Marks Questions ***(Prepare maximum no of questions possible, covering all topics prescribed as 5 modules in the syllabus)***		
1.		Express the decimal number -23 as an8 bit number in the l's and 2's complement form
2.		Design a 4:1 MUX with the help of a truth table and logic diagram
3.		Represent -45 in sign magnitude, l's complement and 2's complement form
4.		Implement a Full adder by deriving expressions from its truth table.
5.		Convert the decimal number 3.248 x 10‘ to a single precision floating point binary number.
6.		Express +19 and -19 in 2’s complement form
7.		Implement a full adder using 8:1 MUX.
8.		Distinguish between Combinational and Sequential circuits.
9.		With the help of logic and timing diagram, design an Asynchronous Two bit Up-counter using positive edge triggered JK Flip-Flop
10.		Implement a JK flip flop and explain its working
11.		How can you convert JK Flip flop to D Flip flop?
12.		Explain Serial in Serial out shift register with the help of circuit diagram.
13.		A program runs in 10 second on computer A, which has a 2 GHz clock. You are trying to help a computer designer build a computer, B, which will run this program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer B to require 1.2 times as many clock cycles as computer A for this program. What clock rate should you tell the designer to target?
14.		Describe the code sequence of C=A+B in Single Accumulator organization and Stack organization of instruction set architecture

15.		Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time of 250 ps and a CPI of 2.0 for some program, and computer B has a clock cycle time of 500 ps and a CPI of 1.2 for the same program. Which computer is faster for this program and by how much?
16.		Briefly describe the 5 key components of a Computer System
17.		Write the code sequence for B = A + C in stack and accumulator instruction set architecture.
18.		Differentiate between Big-endian and Little-endian address assignments.
19.		Explain any one of the bus arbitration schemes in DMA.
20.		How to calculate branch target address in branch on equal(beq) instruction?
21.		What are the MIPS Datapath components required to construct a Branch (beq) Datapath? Represent their symbols and the control signals associated with them.
22.		Briefly explain the different types of Pipeline hazards.
23.		Explain the use of Vectored Interrupts.
24.		What is Bus Arbitration? List out and explain two approaches to Bus Arbitration
25.		Write a short note on memory operations: a)Write back b) Write through
26.		Explain different types of Read Only Memory (ROM).
27.		Define Temporal locality and Spatial locality
28.		What is a Semi-conductor Memory?
29.		Explain the operation of a static RAM cell with the help of a diagram
30.		Differentiate between PROM and EPROM?

		6 Marks Questions ***(Prepare maximum no of questions possible, covering all topics prescribed in the module assigned)***
1		Minimize the Boolean expression f(A,B,C,D)=>(0,1,3,5,7,8,9, 11,13, 15)using Karnaugh map and realize it using NAND gate.
2		Using Boolean algebra techniques, simplify the expression AB+A(B+C)+B(B+C)
3		Design an Octal to Binary encoder with the help of a truth table and logic diagram.
4		Reduce the Boolean function specified in the truth table to its minimum SOP form by using a K -Map 
5	[	Minimize the Boolean expression RA,B,C,D)=Em(1,5,6,7,9,15)+d(2,3,11,13) using Kamaugh map and realize it using Logic gates
6		Convert the decimal number 3.257 * 10^4 into IEEE-754 Single Precision Floating Point binary representation.
1		Explain the working of an edge triggered SR Flip flop in detail.
2		Design a 3 bit UP/DOWN synchronous counter
3		Construct a Mod-5 Asynchronous Counter
4		Implement and explain the working of a 4-bit Parallel-In Serial-Out [PM] Shifter.
5		What are the basic functions of a shift register? Explain 4 bit SIPO shift register with a neat diagram

Inputs			Output
X	Y	Z	S
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

1		What you meant by addressing modes? Explain any three addressing modes that have been used in recent computers.
2		Explain the five classic components of a computer with figure
3		List down and briefly explain the 8 great ideas in Computer Architecture.
4		Describe the code sequence of C=A+B in different types of instruction set architecture
1		Draw a single data path representation for R-type instruction.
2		How should two or more simultaneous interrupt requests be handled? Explain with figure
3		Draw the Single Cycle Datapath for implementing Memory Reference instructions and R-Format instructions
4		Write notes on: Direct Memory Access & Interupt handling
5		With a neat diagram, explain the operation of DMA controllers in a computer system
6		What is pipeline hazard? Explain any three hazards in pipelined processors with examples
1		How the virtual address is converted into real address in a paged virtual memory system? Explain.
2		A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct mapped manner with 64 bytes per cache block. Assume that the size of each memory word is | byte. Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.
3		Explain the various Cache Mapping Techniques.
4		Explain virtual memory address translation using page table with the help of a neat diagram.
5		What is cache memory? Explain different cache mapping techniques with examples

6	a)	Construct a IKB Memory 1C using 1024x4 Memory chips.
	b)	What do you understand by Virtual Memory?