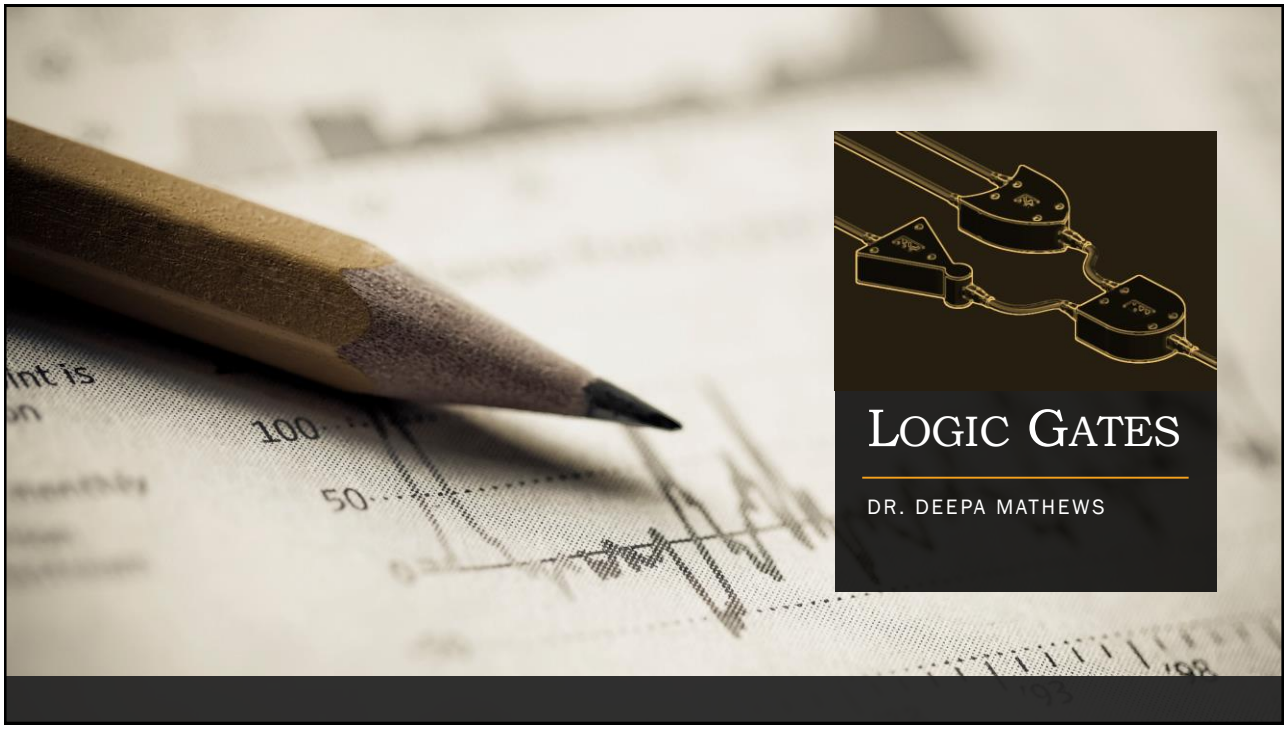
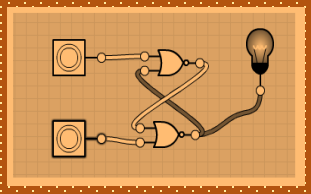


LOGIC GATES

DR. DEEPA MATHEWS

INTRODUCTION



Transistor - It is just a **switch**. It is either switched on (current can flow), or switched off (no current flow)

Gate - A device that performs basic operation on electrical signals

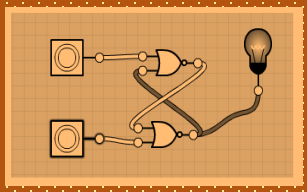
Circuits - Gates combined to perform more complicated tasks

Logic diagrams - A graphical representation of a circuit; each gate has its own symbol

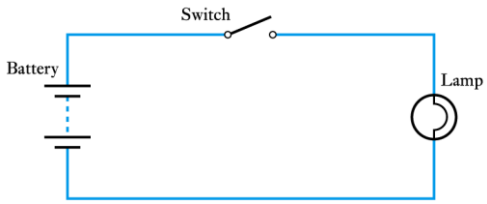
Truth tables - A table showing all possible input value and the associated output values

Boolean expressions - Uses Boolean algebra, a mathematical notation for expressing two-valued logic

INTRODUCTION



- Digital systems are concerned with digital signals.
- **Binary signals** are the most common form of digital signals. They can be used individually to represent a single binary quantity or the state of a single switch.



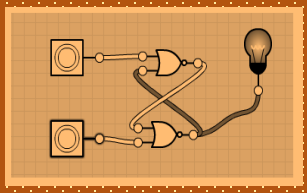
A simple binary arrangement

S	*L*
OPEN	OFF
CLOSED	ON

S	*L*
0	0
1	1

truth table

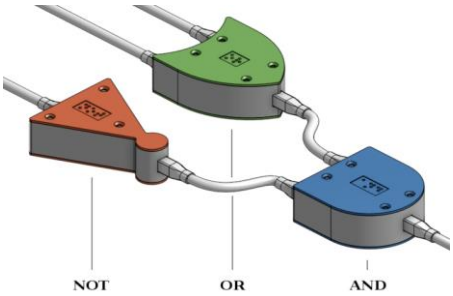
INTRODUCTION



- The building blocks used to create digital circuits are **logic gates.**
- The name is derived from the ability of such a device to **make decisions**. They produce a logic-1 or logic-0 output signal, if input logic requirements are satisfied.
- In most logic gates, the **low (0)** state is approximately zero volts (0 V), while the **high (1)** state is approximately five volts positive (+5 V).
- Most logic gates have **two inputs and one output.** There are seven basic logic gates: **AND, OR, NOT, NAND, NOR, XOR, and XNOR**.
- Each gate has its own **logic symbol** which allows complex functions to be represented by a logic diagram.
- The function of each gate can be represented by a **truth table** or using **Boolean notation.**

Logic Gates

- Inverter (NOT Gate)
- AND Gate
- OR Gate
- Exclusive-OR (XOR) Gate



- NAND Gate = AND Gate + Inverter
- NOR Gate = OR Gate + Inverter
- Exclusive-NOR Gate = XOR Gate + Inverter

Inverter (NOT) Gate

The NOT gate (or inverter)

(a) Circuit symbol

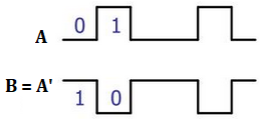
A	B
0	1
1	0

(b) Truth table

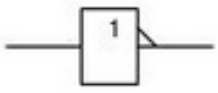
B = A' or B = ~A or

$$B = \overline{A}$$

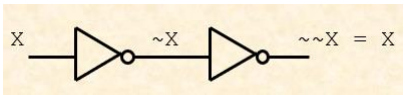
(c) Boolean expression



(d) Timing Diagram



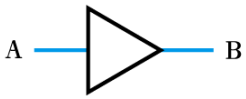
(e) IEEE Symbol



Effect of Double Inversion

X	~X	~~X
0	1	0
1	0	1

Buffer Gate



(a) Circuit symbol

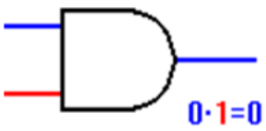
A	B
0	0
1	1

(b) Truth table

$B = A$

(c) Boolean expression

AND Gate



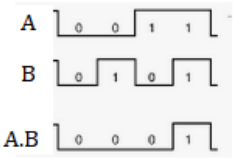
(a) Circuit symbol

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

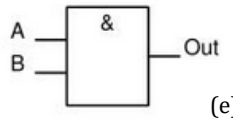
(b) Truth table

$C = A \cdot B$

(c) Boolean expression



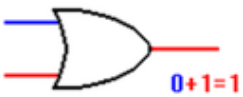
(d) Timing Diagram



(e) IEEE Symbol

OR Gate

The OR gate



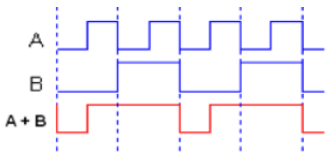
(a) Circuit symbol

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

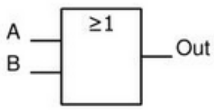
(b) Truth table

$C = A + B$

(c) Boolean expression

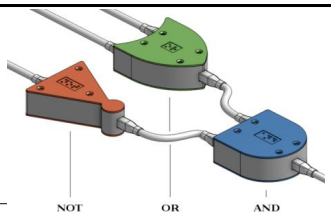


(d) Timing Diagram



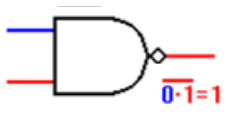
(e) IEEE Symbol

Basic Logic Gates



AND	OR	NOT
Two or more inputs but only one output	Two or more inputs but only one output.	One input, one output; Unary operation
Algebraic Function: **Y = A.B** Logical Multiplication	Algebraic Function: **Y = A+B** Logical Addition	Algebraic Function: **Y = A'** Complement
All or nothing gate **Output is 1, if and only if all its inputs are 1.**	***Any* or *all* gate** **Output is LOW only when all of the inputs are LOW.**	**Inverter gate**

NAND Gate



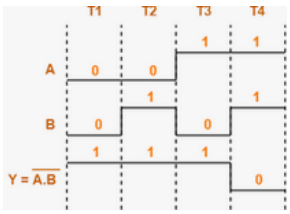
(a) Circuit symbol

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

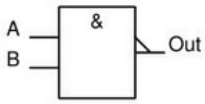
(b) Truth table

$C = \overline{A \cdot B}$

(c) Boolean expression



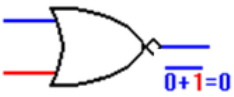
(d) Timing Diagram



(e) IEEE Symbol

NOR Gate

The NOR gate



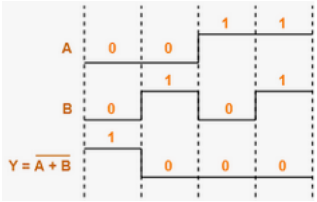
(a) Circuit symbol

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

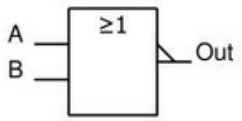
(b) Truth table

$C = \overline{A + B}$

(c) Boolean expression



(d) Timing Diagram

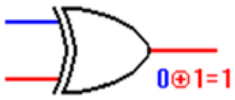


(e) IEEE Symbol

XOR Gate

"Odd but not even gate"

The Exclusive OR gate



(a) Circuit symbol

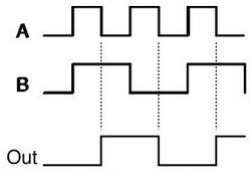
A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

(b) Truth table

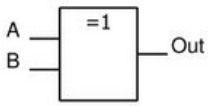
$C = A \oplus B$

$= \overline{A}B + A\overline{B}$

(c) Boolean expression



(d) Timing Diagram

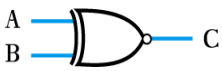


(e) IEEE Symbol

Complement of a variable is represented by an overbar or ' Thus, complement of variable B is represented as B'.

XNOR Gate

The Exclusive NOR gate



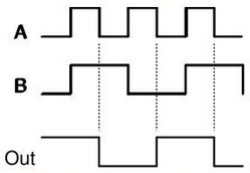
(a) Circuit symbol

A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

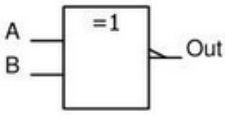
(b) Truth table

$C = \overline{A \oplus B}$

(c) Boolean expression

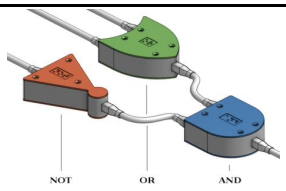


(d) Timing Diagram



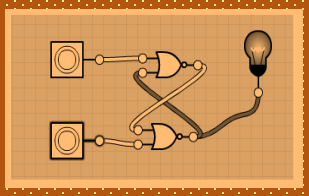
(e) IEEE Symbol

Derived Logic Gates



NAND	NOR	XOR	XNOR
Not AND	NOT OR	Odd, but not even gate; HIGH when odd no. of HIGH inputs	Exclusive NOR gate; Inverted XOR gate
Algebraic Function: **Y = (A.B)'**	Algebraic Function: **Y = (A+B)'**	Algebraic Function: **Y = A'B + AB'**	Algebraic Function: **Y = AB + A'B'**
The unique output from the NAND gate is 0 only when all inputs are 1.	The unique output from the NOR gate is 1 only when all inputs are 0.	**Anticoincidence gate/ inequality detector –** produces an output 1 only when the inputs are not equal	**coincidence gate/ equality detector –** since produces an output 1 only when the inputs are equal

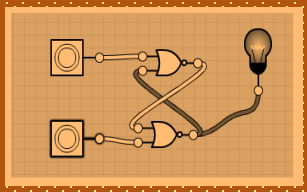
Quiz



1. How many AND gates are required to realize Y = CD + EF + G?
   a) 4
   b) 5
   c) 3
   d) 2

2. The NOR gate output will be high if the two inputs are _____
   a) 00
   b) 01
   c) 10
   d) 11

QUIZ



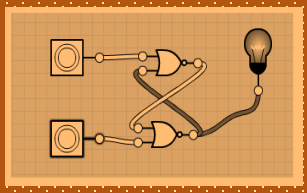
3. An OR gate has 4 inputs. One input is high and the other three are low. The output is …….

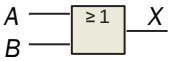
a) Low
b) High
c) alternately high and low
d) may be high or low depending on relative magnitude of inputs

4. How many two input AND gates and two input OR gates are required to realize Y = ST+PQ+RS?

a) 3, 2
b) 4, 2
c) 1, 1
d) 2, 3

QUIZ



5. The symbol 

is for

a. OR gate
b. AND gate
c. NOR gate
d. XOR gate

6. Function of NOT gate is to ……..

a) Stop signal
b) Invert input signal
c) Act as a universal gate
d) None of the above