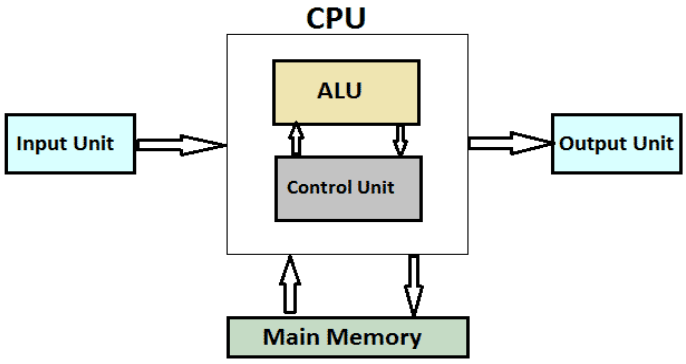
MODULE 4

The Processor - Introduction, Logic design conventions, Building a datapath, A simple implementation scheme, An overview of pipelining - Pipelined datapath and control - Structural hazards - Data hazards - Control hazards, I/O organization - Accessing I/O devices, interrupts - handling multiple devices, Direct memory access

The Processor

- *Processor (CPU)* is the active part of the computer, which does all the work of data manipulation and decision making.
- *Datapath* is the hardware that performs all the required operations, for example, ALU, registers, and internal buses.



- *Control* is the hardware that tells the datapath what to do, in terms of switching, operation selection, data movement between ALU components, etc.

MIPS (Microprocessor without Interlocked Pipelined Stages) is a reduced instruction set computer (RISC), instruction set architecture developed by MIPS Computer Systems.

For every instruction, the first two steps are identical:

1. Send the *program counter* (PC) to the memory that contains the code and fetch the instruction from that memory.

2. Read one or two registers, using fields of the instruction to select the registers to read. For the load word instruction, we need to read only one register, but most other instructions require reading two registers.

After these two steps, the actions required to complete the instruction depend on the instruction class. Fortunately, for each of the three instruction classes (memory-reference, arithmetic-logical, and branches), the actions are largely the same, independent of the exact instruction. The simplicity and regularity of the MIPS instruction set simplifies the implementation by making the execution of many of the instruction classes similar.

The value written into the PC can come from one of two adders, the data written into the register file can come from either the ALU or the data memory, and the second input to the ALU can come from a register or the immediate field of the instruction.

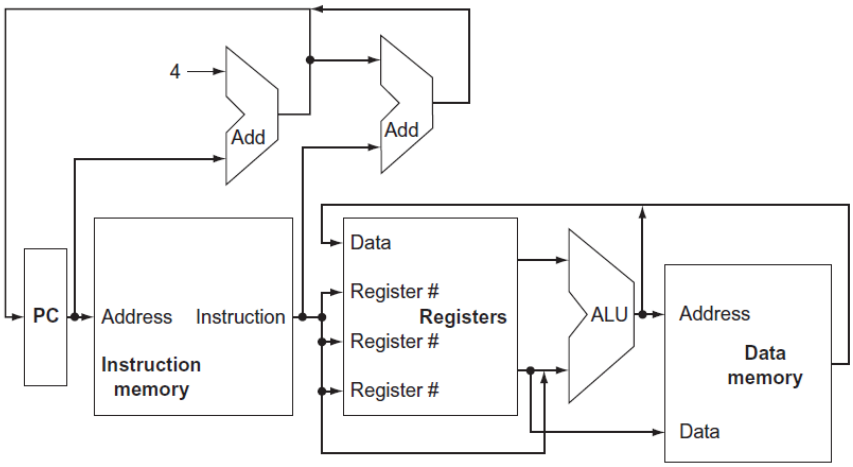


FIGURE 4.1 An abstract view of the implementation of the MIPS subset showing the major functional units and the major connections between them. All instructions start by using

In practice, these data lines cannot simply be wired together; we must add a logic element that chooses from among the multiple sources and steers one of those sources to its destination. This selection is commonly done with a device called a multiplexor, although this device might better be called a data selector.

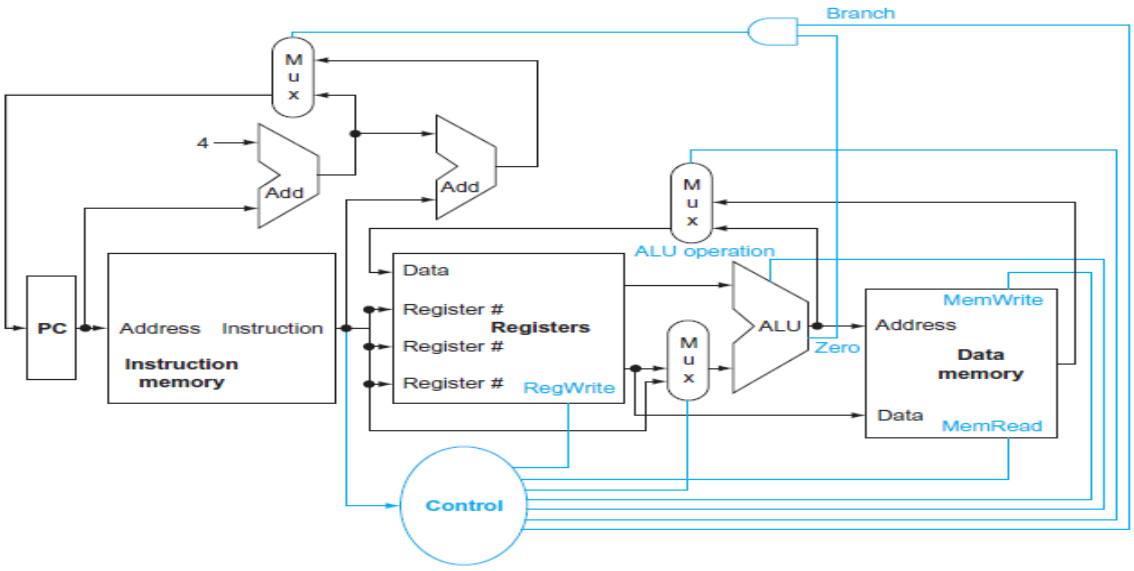
All instructions start by using the program counter to supply the instruction address to the instruction memory. After the instruction is fetched, the register operands used by an instruction are specified by fields of that instruction. Once the register operands have been fetched, they can be operated on to compute a memory address (for a load or store), to compute an arithmetic result (for an integer arithmetic-logical instruction), or a compare (for a branch). If the instruction is an arithmetic-logical instruction, the result from the ALU must be written to a register.

If the operation is a load or store, the ALU result is used as an address to either store a value from the registers or load a value from memory into the registers. The result from the ALU or memory is written back into the register file. Branches require the use of the ALU output to determine the next instruction address, which comes either from the ALU (where the PC and branch off set are summed) or from an adder that increments the current PC by 4. Generally, LDR is used to load something from memory into a register, and STR is used to store something from a register to a memory address.

The basic implementation of the MIPS subset, including the necessary multiplexors and control lines.

The single-cycle MIPS processor is a simplified processor that completes the execution of each instruction in one clock cycle. It consists of essential components like the **Program Counter (PC)**, **Instruction Memory**, **Registers**, **ALU**, and **Data Memory**, all controlled by the **Control Unit**.

The process begins with the **Program Counter (PC)**, which holds the address of the next instruction. This address is sent to the **Instruction Memory** to fetch the instruction. The instruction is then decoded to identify the operation type and the required registers.



The **Registers** unit reads the specified registers' values, which are sent as inputs to the **ALU**. The ALU performs arithmetic or logical operations based on the instruction type, such as addition for R-type or address calculations for load and store instructions. For branch instructions, the ALU checks for equality, and if conditions are met, the PC is updated to a new target address.

For **load word (LW)** and **store word (SW)** instructions, the **Data Memory** is accessed. The calculated memory address determines where data is read (LW) or written (SW). Results are then either stored back into registers or used for further operations.

The **Control Unit** generates control signals (like RegWrite, MemRead, and MemWrite) to ensure that each component behaves as required. Multiplexers (MUX) help select between multiple inputs, such as ALU input sources or the next PC value.

- The **top multiplexor** ("Mux") controls what value replaces the PC (PC + 4 or the branch destination address); the multiplexor is controlled by the gate that "ANDs" together the Zero output of the ALU and a control signal that indicates that the instruction is a branch.
- The middle multiplexor, whose output returns to the register file, is used to steer the output of the ALU (in the case of an arithmetic-logical instruction) or the output of the data memory (in the case of a load) for writing into the register file.
- Finally, the bottommost multiplexor is used to determine whether the second ALU input is from the registers (for an arithmetic-logical instruction or a branch) or from the off set field of the instruction (for a load or store).
- The added control lines are straightforward and determine the operation performed at the ALU, whether the data memory should read or write, and whether the registers should perform a write operation.

Logic design conventions

The Datapath elements in the MIPS implementation consist of two different types of logic elements: elements that operate on data values and elements that contain state.The elements that operate on data values are all combinational, which means that their outputs depend only on the current inputs.An element contains state if it has some internal storage.A state element has at least two inputs and one output. The required inputs are the data value to be written into the

element and the **clock**, which determines when the data value is written.The **output** from a state element provides the value that was written in an earlier clock cycle.Logic components that contain state are also called ***sequential***, because their outputs depend on both their inputs and the contents of the internal state.

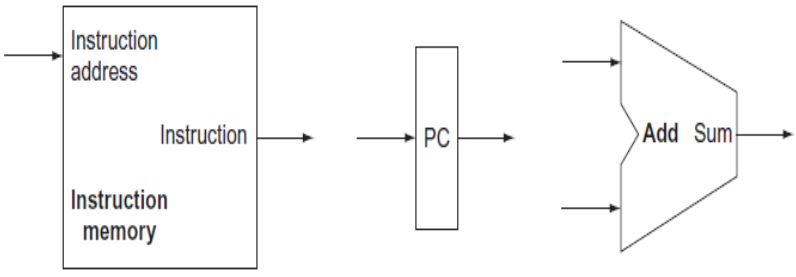
Building a datapath

Major components required to execute each class of MIPS instructions.

The first element we need: **a memory unit** to store the instructions of a program and supply instructions given an address. The **program counter (PC)** is a register that holds the address of the current instruction.An **adder** to increment the PC to the address of the next instruction. To execute any instruction, we must start by fetching the instruction from memory. To prepare for executing the next instruction, we must also increment the program counter so that it points at the next instruction, 4 bytes later.

A **register file** is a collection of registers in which any register can be read or written by specifying the number of the register in the file. The **register file** contains the register state of the computer. In addition, we will need an ALU to operate on the values read from the registers. **R-format instructions have three register** operands, so we will need to read two data words from the register file and write one data word into the register file for each instruction.

For each data word **to be read from the registers**, we need an **input to the register file** that specifies the ***register number*** to be read and an output from the register file that will **carry the value** that has been read from the registers. **To write a data word**, we will need two inputs: one to specify the register number to be written and one to supply the *data* to be written into the register. The register file always outputs the contents of whatever register numbers are on the Read register inputs. Writes, however, are controlled by the write control signal, which must be asserted for a write to occur at the clock edge.



a. Instruction memory b. Program counter c. Adder

Two state elements are needed to store and access instructions, and an adder is needed to compute the next instruction address.

The state elements are the **instruction memory** and the **program counter**. The **instruction memory** need **only provide read access** because the datapath does not write instructions. Since the **instruction memory only reads**, we treat it as **combinational logic**: the output at any time reflects the contents of the location specified by the address input, and no read control signal is needed.The **program counter** is a 32-bit register that is written at the end of every clock cycle and thus does not need a write control signal. The **adder** is an ALU wired to always add its two 32-bit inputs and place the sum on its output.

Consider the R-format instructions,

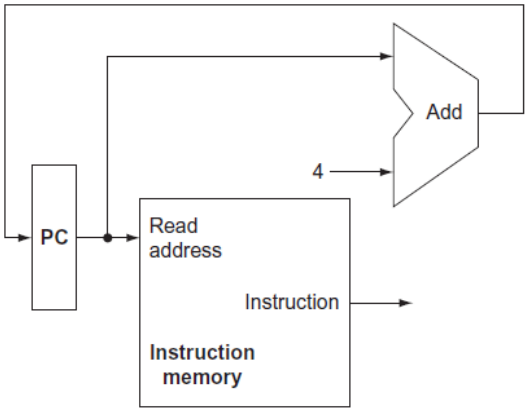


FIGURE 4.6 A portion of the datapath used for fetching instructions and incrementing the program counter. The fetched instruction is used by other parts of the datapath.

They all read two registers, perform an ALU operation on the contents of the registers, and write the result to a register.call these instructions either ***R-type instructions*** or *arithmetic-logical instructions* . This instruction class includes add, sub, AND, OR.The processor's 32 general-purpose registers are stored in a structure called a **register file**

The two elements needed to implement R-format ALU operations are the register file and the ALU..

The register file contains all the registers and has two read ports and one write port.The register file always outputs the contents of the registers corresponding to the Read register inputs on the outputs; no other control inputs are needed.In contrast, a register write must be explicitly indicated by asserting the write control signal. Remember that writes are edge-triggered, so that all the write inputs (i.e., the value to be written, the register number, and the write control signal) must be valid at the clock edge.

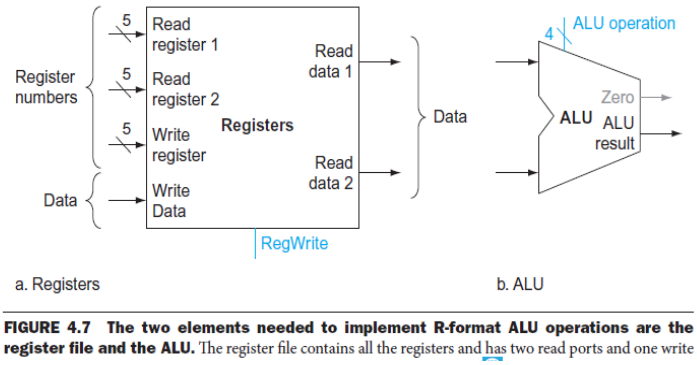


FIGURE 4.7 The two elements needed to implement R-format ALU operations are the register file and the ALU. The register file contains all the registers and has two read ports and one write

MIPS load word and store word instructions

General form **lw $t1,offset_value($t2)** or **sw $t1,offset_value ($t2)**. These instructions compute a memory address by adding the base register, which is $t2, to the 16-bit signed offset field contained in the instruction. If the instruction is a store, the value to be stored must also be read from the register file where it resides in $t1. If the instruction is a load, the value read from memory must be written into the register file in the specified register, which is $t1.

Thus, we will need both the register file and the ALU.In addition, we will need a unit to **sign-extend** the 16-bit off set field in the instruction to a 32-bit signed value,and a **data memory** unit to read from or write to.

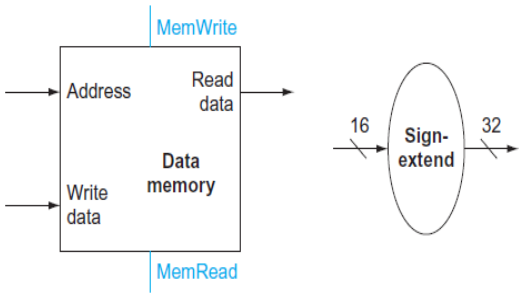


FIGURE 4.8 The two units needed to implement loads and stores, in addition to the register file and ALU of Figure 4.7, are the data memory unit and the sign extension unit.

The **data memory** must be written on store instructions; hence, data memory has read and write control signals, an address input, and an input for the data to be written into memory.

Branching Instruction

The **beq** instruction has three operands, **two registers** that are compared for equality, and a **16-bit off set** used to compute the **branch target address** relative to the branch instruction address.

Its form is **beq $t1,$t2,offset**.

To implement this instruction, we must compute the **branch target address** by adding the **sign-extended off set field of the instruction to the PC**. The instruction set architecture specifies that the base for the branch address calculation is the address of the instruction following the branch. Since we compute PC + 4 (the address of the next instruction) in the instruction fetch datapath, it is easy to use this value as the base for computing the branch target address.

The architecture also states that the **off set** field is **shifted left 2 bits** so that it is a **word off set**; this shift increases the effective range of the off set field by a factor of 4.As well as computing the branch target address, we must also determine whether the next instruction is the instruction that follows sequentially or the instruction at the branch target address.

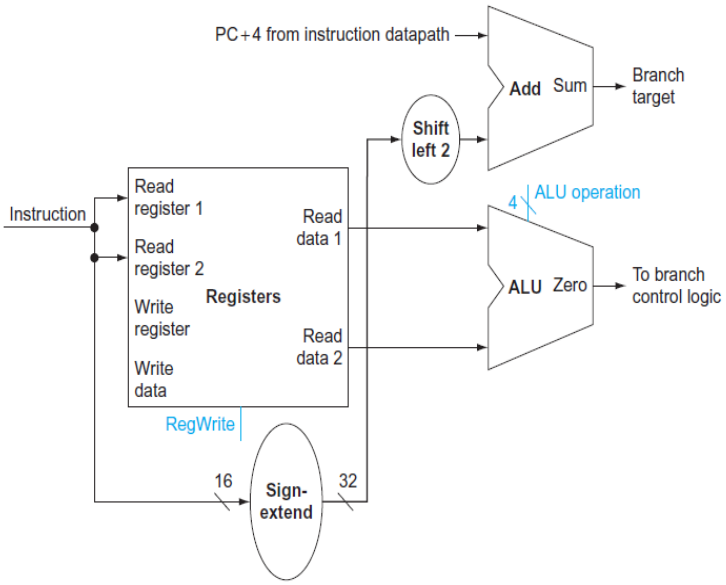
When the condition is true (i.e., the operands are equal), the branch target address becomes the new PC, and we say that the **branch** is **taken**. If the operands are not equal, the incremented PC should replace the current PC (just as for any other normal instruction); in this case, we say that the **branch** is **not taken**.Thus, the branch datapath must **do two operations**: compute the branch target address and compare the register contents.

To compute the **branch target address**, the branch datapath includes a **sign extension unit** and an **adder.** To perform the compare, we need to use the register file to supply the two register operands (although we will not need to write into the register file).

In addition, the comparison can be done using the ALU , Since that ALU provides an output signal that indicates whether the result was 0, we can send the two register operands to the ALU with the control set to do a subtract. If the Zero signal out of the ALU unit is asserted, we know that the two values are equal. Although the Zero output always signals if the result is 0, we will be using it only to implement the equal test of branches.

The memory unit is a state element with inputs for the address and the write data, and a single output for the read result. There are separate read and write controls, although only one of these may be asserted on any given clock.The sign extension unit has a 16-bit input that is sign-extended into a 32-bit result appearing on the output .**The datapath** for a branch uses the ALU to evaluate the branch condition and a separate adder to compute the branch target as the sum of the incremented PC and the sign-extended, lower 16 bits of the instruction (the branch displacement), shifted left 2 bits.

The unit labeled ***Shift left 2*** is simply a routing of the signals between input and output that **adds 00 to the low-order end of the sign-extended off set field**; no actual shift hardware is needed, since the amount of the "shift " is constant. Control logic is used to decide whether the incremented PC or branch target should replace the PC, based on the Zero output of the ALU.



Creating a Single Datapath

This simplest datapath will attempt to execute all instructions in one clock cycle. To share a datapath element between two different instruction classes, we may need to allow multiple connections to the input of an element, using a multiplexor and control signal to select among the multiple inputs. To create a datapath with only a single register file and a single ALU, we must support two different sources for the second ALU input, as well as two different sources for the data stored into the register file. Thus, one multiplexor is placed at the ALU input and another at the data input to the register file.

(Explain each component)

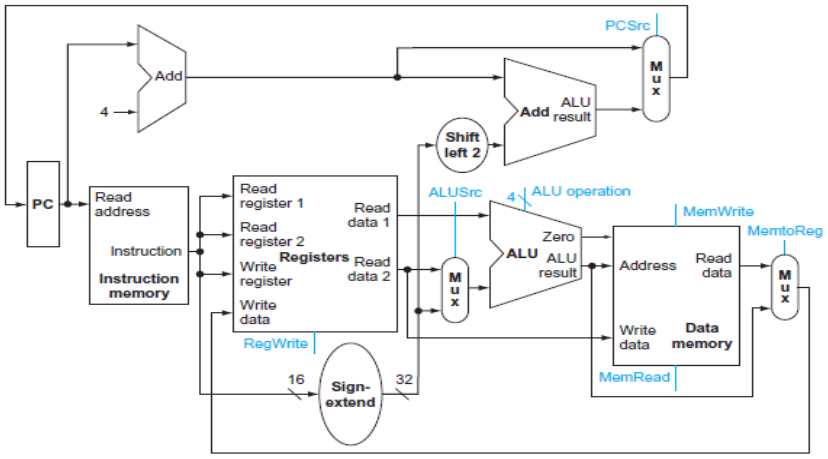


FIGURE 4.11 The simple datapath for the core MIPS architecture combines the elements required by different instruction classes. The components come from Figures 4.6, 4.9, and 4.10. This datapath can execute the basic instructions (load-store word, ALU operations, and branches) in a single clock cycle. Just one additional multiplexor is needed to integrate branches. The support for jumps will be added later.

A simple implementation scheme

The simple implementation covers *load word* (lw), *store word* (sw), *branch equal* (beq), and the arithmetic-logical instructions add, sub, AND, OR, and set on less than.

For **load word and store word instructions**, we use the ALU to compute the memory address by addition. For **the R-type instructions**, the ALU needs to perform one of the five actions (AND, OR, subtract, add, or set on less than), depending on the value of the 6-bit function field in the low-order bits of the instruction.**For branch equal**, the ALU must perform a subtraction.The ALU control block has also been added. The PC does not require a write control, since it is written once at the end of every clock cycle; the **branch control logic** determines whether it is written with the incremented PC or the branch target address.

- Opcode (bits [31:26]): Specifies the instruction type.
- rs (bits [25:21]): Source register. (source 1)
- rt (bits [20:16]): Target register. (source 2)
- rd (bits [15:11]): Destination register (used in R-type instructions).
- Immediate/offset (bits [15:0]): Used in I-type instructions (e.g., branch offset or immediate value).s
- hamt and funct (bits [10:6] and [5:0]): Used in R-type instructions for shift amount and operation details.

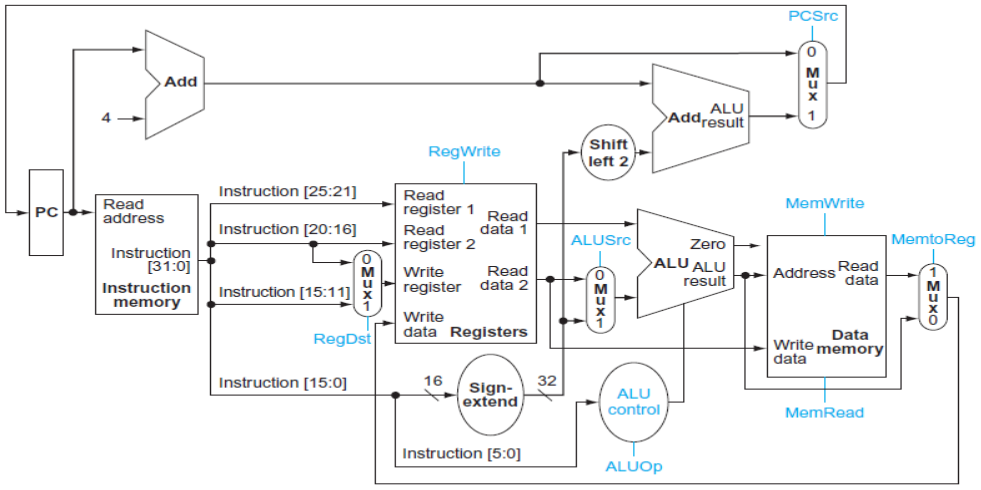


FIGURE 4.15 The datapath of Figure 4.11 with all necessary multiplexors and all control lines identified. The control lines are shown in color. The ALU control block has also been added. The PC does not require a write control, since it is written once at the end of every clock cycle; the branch control logic determines whether it is written with the incremented PC or the branch target address.

Pipelining

Pipelining is an implementation technique in which multiple instructions are overlapped in execution.advanced pipelining techniques used in recent processors such as the Intel Core i7 and ARM Cortex-A8..

Pipelining is a technique where multiple instructions are overlapped during execution. Pipeline is divided into stages and these stages are connected with one another to form a pipe like structure. Instructions enter from one end and exit from another end.Pipelining increases the overall instruction throughput.

Pipeline Instruction-Execution

1. Fetch instruction from memory.
2. Read registers while decoding the instruction. The regular format of MIPS, instructions allows reading and decoding to occur simultaneously.
3. Execute the operation or calculate an address.
4. Access an operand in data memory.
5. Write the result into a register.

As with the single-cycle and multi-cycle implementations, we will start by looking at the datapath for pipelining. pipelining involves breaking up instructions into five stages:

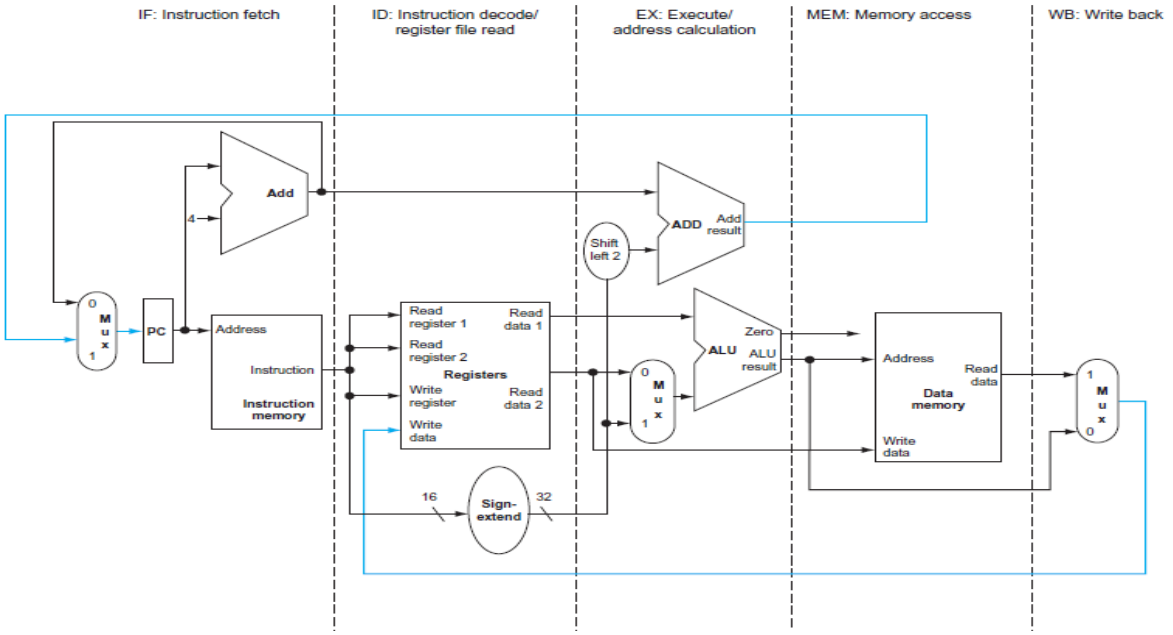
1. IF: Instruction fetch
2. ID: Instruction decode and register file read
3. EX: Execution or address calculation

4. MEM: Data memory access

5. WB: Write back

Pipelining increases the number of simultaneously executing instructions and the rate at which instructions are started and completed. Pipelining does not reduce the time it takes to complete an individual instruction, also called the latency. For example, the five-stage pipeline still takes 5 clock cycles for the instruction to complete. pipelining improves instruction throughput rather than individual instruction execution time or latency.

Single-cycle datapath, divided into stages



Each step of the instruction can be mapped onto the datapath from left to right. The only exceptions are the update of the PC and the write-back step which sends either the ALU result or the data from memory to the left to be written into the register file.

The two exceptions are:

• The WB stage places the result back into the register file in the middle of the datapath - > leads to data hazards.

• The selection of the next value of the PC – either the incremented PC or the branch address - > leads to control hazards.

MIPS Instructions and Pipelining

In order to implement MIPS instructions effectively on a pipeline processor, we must ensure that the instructions are the same length (*simplicity favors regularity*) for easy IF and ID, similar to the multicycle datapath. We also need to have few but consistent instruction formats, to avoid deciphering variable formats during IF and ID, which would prohibitively increase pipeline

segment complexity for those tasks. Thus, the register indices should be in the same place in each instruction.

Datapath Partitioning for Pipelining

Recall the single-cycle datapath, which can be partitioned (subdivided) into functional unit. The single-cycle datapath contains separate Instruction Memory and Data Memory units, this allows us to directly implement in hardware the IF-ID-EX-MEM-WB representation of the MIPS instruction sequence.Observe that several control lines have been added, for example, to route data from the ALU output (or memory output) to the register file for writing. Also, there are again three ALUs, one for ALUop, another for JTA (Jump Target Address) computation, and a third for adding PC+4 to compute the address of the next instruction.

In summary, pipelining improves efficiency by first regularizing the instruction format, for simplicity. We then divide the instructions into a fixed number of steps, and implement each step as a pipeline segment. During the pipeline design phase, we ensure that each segment takes about the same amount of time to execute as other segments in the pipeline. Also, we want to keep the pipeline full wherever possible, in order to maximize utilization and throughput, while minimizing set-up time.

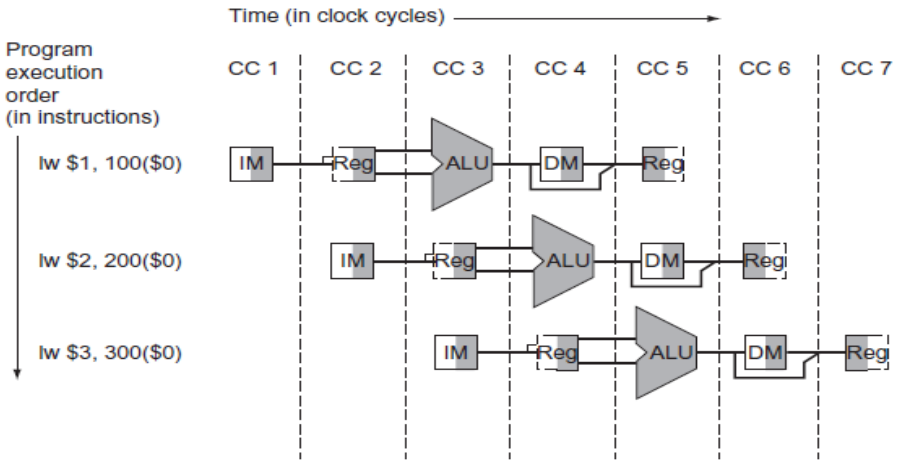


FIGURE 4.34 Instructions being executed using the single-cycle datapath in Figure 4.33, Active portions of the datapath highlighted as a load instruction goes through the five stages of pipelined execution.

- 1. *Instruction fetch*
- *2. Instruction decode and register file read:*
- 3. *Execute or address calculation:*
- 4. *Memory access:*
- 5. *Write-back:*

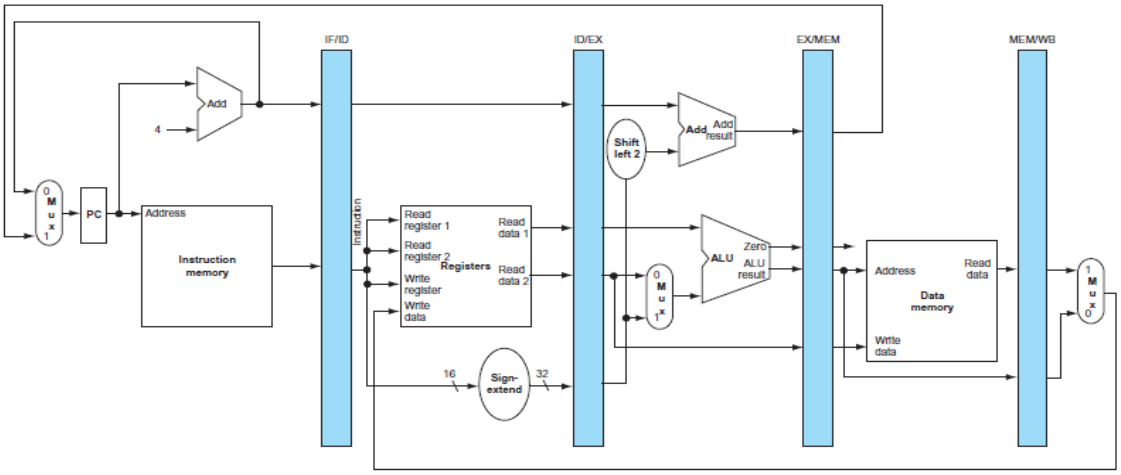


FIGURE 4.35 The pipelined version of the datapath in Figure 4.33. The pipeline registers, in color, separate each pipeline stage. They are labeled by the stages that they separate; for example, the first is labeled *IF/ID* because it separates the instruction fetch and instruction decode stages. The registers must be wide enough to store all the data corresponding to the lines that go through them. For example, the IF/ID register must be 64 bits wide, because it must hold both the 32-bit instruction fetched from memory and the incremented 32-bit PC address. We will expand these registers over the course of this chapter, but for now the other three pipeline registers contain 128, 97, and 64 bits, respectively.

Instruction fetch

The top portion of instruction being read from memory using the address in the PC and then being placed in the IF/ID pipeline register. The PC address is incremented by 4 and then written back into the PC to be ready for the next clock cycle. This incremented address is also saved in the IF/ID pipeline register in case it is needed later for an instruction, such as beq. The computer cannot know which type of instruction is being fetched, so it must prepare for any instruction, passing potentially needed information down the pipeline.

Instruction decode and register file read:

The bottom portion of the instruction portion of the IF/ID pipeline register supplying the 16-bit immediate field, which is sign-extended to 32 bits, and the register numbers to read the two registers. All three values are stored in the ID/EX pipeline register, along with the incremented PC address. We again transfer everything that might be needed by any instruction during a later clock cycle.

Execute or address calculation

The load instruction reads the contents of register 1 and the sign-extended immediate from the ID/EX pipeline register and adds them using the ALU. That sum is placed in the EX/MEM pipeline register.

Memory access:

The top portion shows the load instruction reading the data memory using the address from the EX/MEM pipeline register and loading the data into the MEM/WB pipeline register.

Write-back:

The bottom portion o shows the final step: reading the data from the MEM/WB pipeline register and writing it into the register file in the middle.

Pipeline Hazards

There are situations in pipelining when the next instruction cannot execute in the following clock cycle. These events are called *hazards*, and there are three different types.

- Structural hazards
- Data hazards
- Control hazards

Structural hazards

The first hazard is called a structural hazard. It means that the hardware cannot support the combination of instructions that we want to execute in the same clock cycle.

Eg: A structural hazard in the laundry room would occur if we used a washer dryer combination instead of a separate washer and dryer, or if our roommate was busy doing something else and wouldn't put clothes away. Our carefully scheduled pipeline plans would then be foiled.

Data hazards

Data Hazards occur when an instruction depends on the result of a previous instruction still in the pipeline, which result has not yet been computed. The simplest remedy inserts stalls in the execution sequence, which reduces the pipeline's efficiency.In a computer pipeline, data hazards arise from the dependence of one instruction on an earlier one that is still in the pipeline.

For example, suppose we have an add instruction followed immediately by a subtract instruction that uses the sum ($s0):

add $s0, $t0, $t1

sub $t2, $s0, $t3

Without intervention, a data hazard could severely stall the pipeline. The add instruction doesn't write its result until the fifth stage, meaning that we would have to waste three clock cycles in the pipeline.The primary solution is based on the observation that we don't need to wait for the instruction to complete before trying to resolve the data hazard. For the code sequence above, as soon as the ALU creates the sum for the add, we can supply it as an input for the subtract.

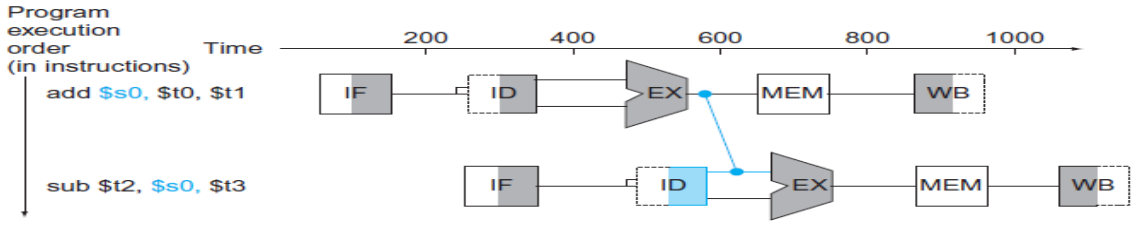


FIGURE 4.29 Graphical representation of forwarding. The connection shows the forwarding path from the output of the EX stage of `add` to the input of the EX stage for `sub`, replacing the value from register `$s0` read in the second stage of `sub`.

Control Hazards

Control Hazards can result from branch instructions. Here, the branch target address might not be ready in time for the branch to be taken, which results in *stalls* (dead segments) in the pipeline that have to be inserted as local wait events, until processing can resume after the branch target is executed. Control hazards can be mitigated through accurate branch prediction (which is difficult), and by *delayed branch* strategies.

I/O organization

One of the basic features of a computer is its ability to exchange data with other devices. This communication capability enables a human operator, for example, to use a keyboard and a display screen to process text and graphics.

Single Bus Arrangement

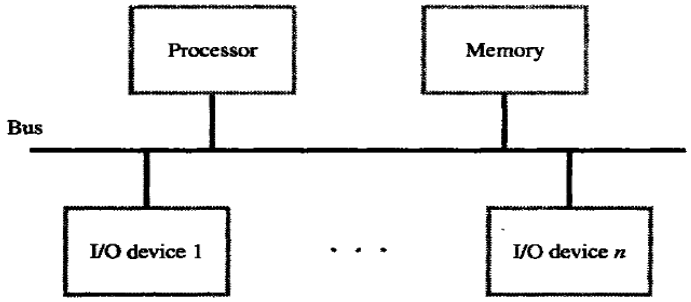


Figure 4.1 A single-bus structure.

- Multiple I/O devices may be connected to the processor and the memory via a single bus Each I/O device is assigned an unique address.Bus enables all the connected devices to exchange information. Bus consists of three sets of lines to carry address, data and control signals.
- To access an I/O device, the processor places the address on the address lines
- The device recognizes the address, and responds to the commands issued on the control lines
- The requested data are transferred over the data lines

1. Memory-Mapped I/O Interfacing :

In this kind of interfacing, we assign a memory address that can be used in the same manner as we use a normal memory location.Any machine instruction that can access memory can be used to transfer data to or from an I/O device

2. I/O Mapped I/O Interfacing :

A kind of interfacing in which we assign an 8-bit address value to the input/output devices which can be accessed using IN and OUT instruction is called I/O Mapped I/O Interfacing.

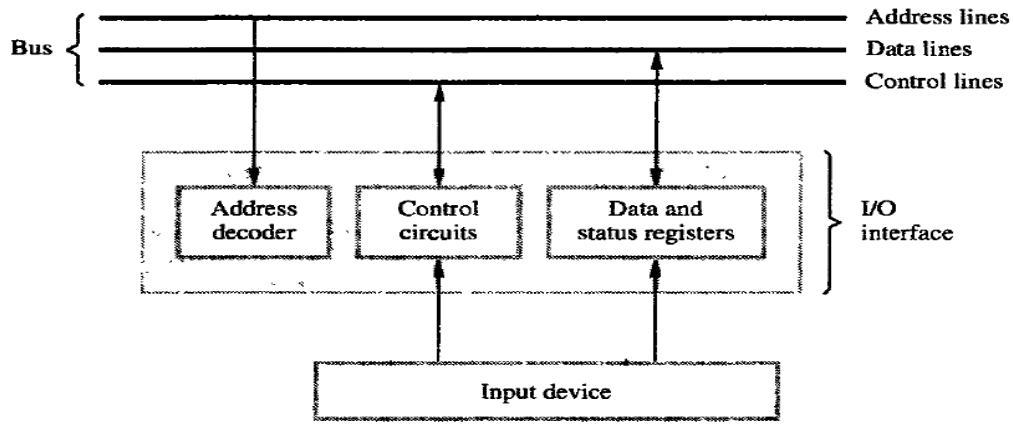


Figure 4.2 I/O interface for an input device.

- I/O device is connected to the bus using an I/O interface circuit which has: - Address decoder, control circuit, and data and status registers.
- **Address decoder** ,decodes the address placed on the address lines thus enabling the device to recognize its address.
- **Data register** holds the data being transferred to or from the processor
- **Status register** holds information necessary for the operation of the I/O device.
- Data and status registers are connected to the data lines, and have unique addresses.
- I/O interface circuit coordinates I/O transfers

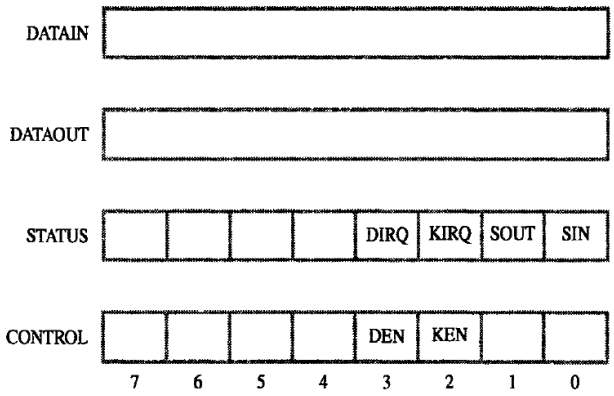


Figure 4.3 Registers in keyboard and display interfaces.

DATAIN:

This register is used for receiving data from the peripheral (keyboard or display).Typically, it contains an 8-bit data bus that is used to send the data to the CPU.The contents of this register would be read by the CPU when it needs to process input from the device.

DATAOUT:

This register is used for sending data to the peripheral.It sends data from the CPU to the peripheral, typically when the system needs to display something on the screen.

STATUS:

The STATUS register indicates the status of the device.If the device is ready -DIRQ (Data Ready Interrupt Request),If there is data to be read -KIRQ (Keyboard Interrupt Request), or If the device is busy -SOUT (Serial Output, SIN - Serial Input)

CONTROL:

The CONTROL register is used to control the operations of the device.It includes control signals like DEN (Device Enable) and KEN (Keyboard Enable).

Synchronization between the processor and an I/O device

- Two other mechanisms used for synchronizing data transfers between the processor and memory:
    - **Interrupts**
    - **Direct Memory Access**

Interrupts

In **computer architecture**, an **interrupt** is a signal to the processor emitted by hardware or software indicating an event that needs immediate attention.Our processor repeatedly keeps on checking for the SIN and SOUT bits for the synchronization in the program. Hence, the processor does not do any things useful other than running the infinite loop. To avoid this situation input/output devices can have the concept of interrupts . When the input/output device is ready it could signal the processor on a separate line called **interrupt request line**.

On receiving the interrupt the processor reads the input output device and hence removing the infinite loop waiting mechanism.

For example , let us take a task that involves two activities :

1. *Perform some computation*
2. *Print the result*

*Repeat the above two steps several times in the program, let the program contain 2 routines **COMPUTE** and **PRINT** routine.*

Method #1 :

The COMPUTE routine passes N lines to the PRINT routine and the PRINT routine then prints the N lines one by one on a printer. All this time the COMPUTE routine keeps on waiting and does not do anything useful.

Method #2 :

The COMPUTE routine passes N lines to the PRINT routine. The PRINT routine then sends one line to the printer and instead of printing that line it execute itself and passes the control to

the COMPUTE routine . The COMPUTE routine continuous it activity, once the line has been printed the printers sends an interrupt to the processor of the computer. At this point the COMPUTE routine is suspended and the PRINT routine is activated and the PRINT routine send second line to the printer so that the printer can keep on printing the lines and the process continues.

Types Of Interrupts

- Hardware Interrupts
- Software Interrupts

Hardware Interrupts

If the signal for the processor is from external device or hardware is called hardware interrupts.

Example: from keyboard we will press the key to do some action this pressing of key in keyboard will generate a signal which is given to the processor to do action, such interrupts are called hardware interrupts.

Hardware interrupts can be classified into two types ->

Maskable Interrupt: The hardware interrupts which can be delayed when a much highest priority interrupt has occurred to the processor.

Non Maskable Interrupt: The hardware which cannot be delayed and should process by the processor immediately.

Software Interrupts

Software interrupt can also divided in to two types they are ->

Normal Interrupts: the interrupts which are caused by the software instructions are called Normal Interrupts.

Exception: unplanned interrupts while executing a program is called Exception. For example: while executing a program if we got a value which should be divided by zero is called a exception.

Need For Interrupts

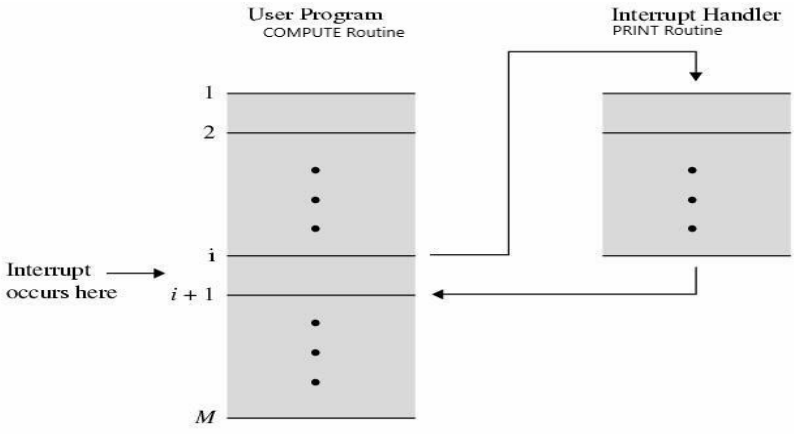
The operating system is a reactive program

1. When you give some input it will perform computations and produces output but meanwhile you can interact with the system by interrupting the running process or you can stop and start another process
- This reactiveness is due to the interrupts
- Modern operating systems are interrupt driven

Interrupt Service Routine (ISR)

The routine that gets executed when an interrupt request is made is called as INTERRUPT SERVICE ROUTINE (ISR).

- **Step 1:** When the interrupt occurs the processor is currently executing **i'th** instruction and the program counter will be currently pointing to **(i + 1)th** instruction.
- **Step 2:** When the interrupt occurs the program counter value is stored on the processes stack.
- **Step 3:** The program counter is now loaded with the address of interrupt service routine.
- **Step 4:** Once the interrupt service routine is completed the address on the processes stack is pop and place back in the program counter.
- **Step 5:** Execution resumes from **(i + 1)th** line of COMPUTE routine.

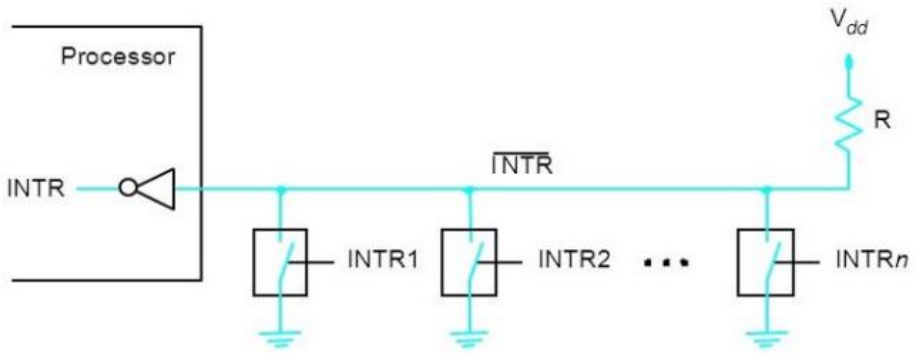


Interrupt Hardware

Many computers have facility to connect two or more input and output devices.A single interrupt request line may be used to serve n devices.All devices are connected to the line via switches to ground.To request an interrupt a device closes its associated switch.

Thus if all interrupt request signals INTR1 to INTRn are inactive, that is, if all switches are open, the voltage on the interrupt request line will be equal to Vdd. This is the inactive state of the line. When a device request an interrupt by closing its switch, the voltage on the line drops to 0, causing the interrupt request signal, INTR, received by the processor to go to 1.

Since the closing of one or more switches will cause the line voltage to drop to 0, the value of INTR is the logical OR of the requests from individual devices, that is, INTR = INTR1 + …….+ INTRn.There is a common interrupt line for all N input/output devices .



An interrupt can stop the currently executed program temporarily and branch to an interrupt service routine.An interrupt can occur at any time during the execution of a program.Because of the above reasons it may be some time necessary to disable the interrupt and enable it later on in the program. For this reason some processor may provide special machine instructions such as **interrupt enable** an **interrupt disable** that performs these tasks.

The **first possibility** is to have the processor hardware ignore the interrupt request line until the execution of the first instruction of the interrupt service routine has been completed. Also note that the program written for the interrupt service routine has to enable and disable the interrupts in this case. This is done explicitly **by the programmer.**

The second option, which is suitable for a **simple processor** with only one interrupt request line, is to have the processor automatically disable interrupts before starting the execution of the interrupt service routine.

After saving the contents of the PC and the processor status register (PS) on the stack, the processor performs the equivalent of executing an **Interrupt disable instruction.** It is often the case that **one bit** in **the PS register** called **Interrupt enable**.An interrupt request received while this bit is equal to **1** will be accepted.

After saving the contents of the PS on the stack, with the Interrupt enable bit equal to 1, the processor **clears the Interrupt-enable** bit in its PS register, thus disabling further interrupts. When a Return from interrupt is executed, the contents of the PS are **restored** from the stack, setting the Interrupt enable bit back to 1. Hence, interrupts are **again enabled**.In the **third option**, the processor has a special interrupt-request line for which the interrupt handling circuit responds only to **the leading edge** of the signal. Such a line is said to be **edge triggered**. In this case the processor will receive only one request.

Handling an interrupt requests from a single device

- The device raise an interrupt request.
- The processor interrupts the program currently being executed.
- Interrupts are disabled by changing the control bits in the PS.
- The device is informed that its request has been recognized, and in response, it deactivates the interrupt request signal.
- The action requested by the interrupt is performed by the interrupt service routine.
- Interrupts are enabled and execution of the interrupted program is resumed.

Handling interrupt requests from a Multiple device

There could be scenarios when there are multiple input/output devices connected to the CPU that could be raising interrupts, since these interrupts are raised at a random time there can be several issues like->

- How will the processor identify the device using the interrupt
- How will the processor handle two simultaneous interrupts

- Should the device be allowed to raise an interrupt while another interrupt service routine is already being executed

Four Methods :

1. Polling
2. Vectored Interrupts
3. Priority-Based Interrupt Handling
4. Dasisy Chain Mechanism

Polling

The status register can be used to identify the device using an interrupt. When a device raises an interrupt it will set a specific bit to one . That bit is called **IRQ(Interrupt ReQuest) .IRQs** are hardware lines over which devices can send interrupt signal to the microprocessor.When you add a new device to a PC you sometime need to set its **IRQ.**The simplest way to identify the interrupting device is to have the interrupt service routine **poll all the I/O devices connected to the bus.**

The **first device encountered with its IRQ bit set** is the device that should be serviced.

- **Disadvantages ->**
- A lot of time spent in checking for the IRQ bits of all the devices, considering that most of devices are generating interrupts at a random time.

Vectored Interrupts

To reduce the time involved in the polling process, a device requesting an interrupt may identify itself directly to the processor. This approach is called vectored interrupts.A device requesting an interrupt can identify itself by sending **a special code to the processor over the bus**. This enables the processor to identify individual devices even if they share a single interrupt request line. The code supplied by the device may represent the **starting address of the interrupt service routine for that device**. The code length is typically in the range of 4 to 8 bits. **The remainder of the address** is supplied by the processor based on the area in the memory where the address for interrupt service routines are located.

The location pointed to by the interrupting device is used to store the **starting address of the interrupt service routine**. The processor reads this address called the **interrupt vector** and **loads it into the PC**. The interrupt vector may also include a new value for the processor status register.In most computers, I/O devices send the **interrupt-vector code** over the data bus, using the bus control signals to ensure that devices do not interfere with each other. When a device sends an interrupt request, the processor may not be ready to receive the interrupt-vector code immediately.

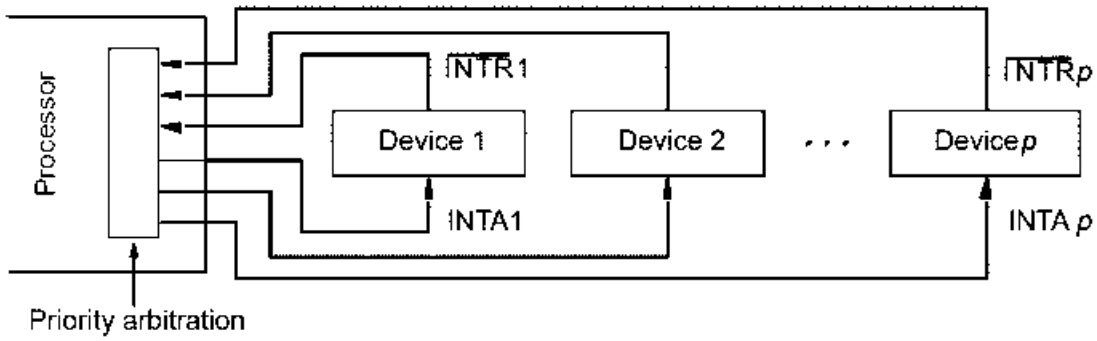
For example, it must first complete the execution of the current instruction, which may require the use of the bus. There may be further delays if interrupts happen to be disabled at the time the request is raised. The interrupting device must wait to put data on the bus only when the

processor is ready to receive it. When the processor is ready to receive the interrupt-vector code, it activates the interrupt-acknowledge line**, INTA**. The I/O device responds by sending its interrupt- vector code and turning off the INTR signal.

Priority-Based Interrupt Handling (Interrupt Nesting)

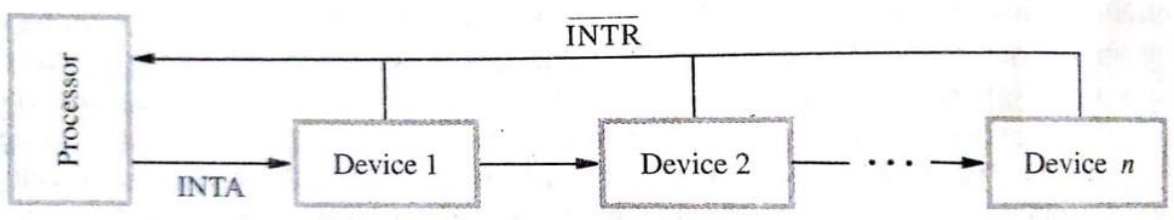
I/O devices should be organized in a priority structure. An interrupt request from a highpriority device should be accepted while the processor is servicing another request from a lowerpriority device. A multiple-level priority organization means that during execution of an interruptservice routine, interrupt requests will be accepted from some devices but not from others, depending upon the device's priority. To implement this scheme, priority level can be assigned to the processor that can be changed by the program. The processor's priority is usually encoded in a few bits of the processor status word. It can be changed by program instructions that write into the PS.

A multiple-priority scheme can be implemented easily by using **separate interrupt- request and interrupt-acknowledge lines for each device**, Each of the interrupt request lines is assigned a **different priority level**. Interrupt requests received over these lines are sent to a priority arbitration circuit in the processor. A request is accepted only if it has a higher priority level than that currently assigned to the processor.



Daisy Chain Mechanism

Suppose when there are multiple input/output devices raising an interrupt simultaneously then it is straight forward for us to select which interrupt to handle depending on the interrupt having the highest priority.



(a) Daisy chain

- Step 1: Multiple devices try to raise an interrupt by trying to pull down the interrupt request line(INTR).

- Step 2 : The processes realises that there are devices trying to raise an interrupt ,so it makes the INTA line goes high, is that it is set to 1.
- Step 3 : The INTA Line is connected to a device, device one in this case.

1. If this device one had raised an interrupt then it goes ahead and passes the identifying code to the data line.
2. If device one had not raise an interrupt then it passes the INTA signal to device two and so on.

So priority is given to device nearest to the processor. This method ensures that multiple interrupt request are handled properly, even when all the devices are connected to a common interrupt request line. **Simultaneous request**: When simultaneous interrupt requests are arrived **from two or more I/O devices to the processor,** the processor must have some means of deciding which request to service first.The processor simply accepts the request having the **highest priority**. If several devices share one interrupt-request line,, some other mechanism is needed**.**

The interrupt request line INTR is common to all devices. The interrupt-acknowledge line, INTA, is connected in a daisy-chain fashion, such that the INTA signal propagates serially through the devices. When several devices raise an interrupt request and the INTR line is activated, the processor responds by setting the INTA line to 1. This signal is received by device 1. Device 1 passes the signal on to device 2 only if it does not require any service.

If device 1 has a pending request for interrupt, it blocks the INTA signal and proceeds to put its identifying code on the data lines. Therefore, in the daisy-chain arrangement, the device that is electrically closest to the processor has the highest priority. The second device along the chain has second highest priority, and so on.

DMA-Direct Memory Access

To transfer large blocks of data at high speed, a special control unit may be provided between an external device and the main memory, without continuous intervention by the processor. This approach is called direct memory access (DMA).Control unit which performs these transfers is a part of the I/O device's interface circuit. This control unit is called as a DMA controller. DMA controller performs functions that would be normally carried out by the processor.For each word, it provides the memory address and all the control signals.To transfer a block of data, it increments the memory addresses and keeps track of the number of transfers.

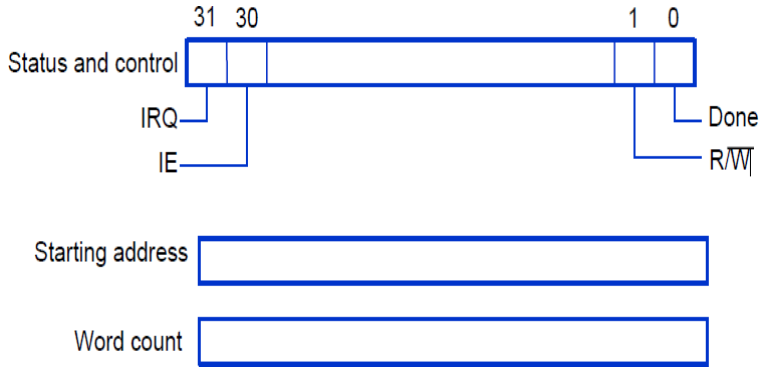
The operation of the DMA controller must be under the control of a program executed by the processor. The processor must initiate the DMA transfer.To initiate the DMA transfer, the processor informs the DMA controller of:

- Starting address
- Number of words in the block.

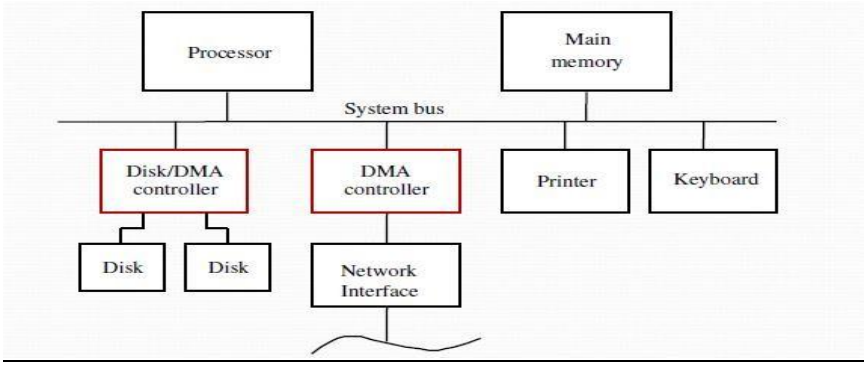
- Direction of transfer (I/O device to the memory, or memory to the I/O device).

Once the DMA controller completes the DMA transfer, it informs the processor by raising an interrupt signal.

Registers in DMA Controller :-



Use of DMA Controller in a computer system



DMA controller connects a high-speed network to the computer bus.Disk controller, which controls two disks also has DMA capability. It can perform two independent DMA operations, as if each disk has its own DMA controller. The registers to store the memory address, word count and status and control information are duplicated.To start a DMA transfer, a program writes the address and word count information into the registers of the disk controller.

The DMA controller proceeds independently to implement the operation and once it is completed, the Done bit is set to 1.At the same time the if the IE bit is set, the controller sends an interrupt request and sets the IRQ bit .The status register also contains other information such as whether the transfer took place correctly or not.

Processor and DMA controllers have to use the bus in an interwoven fashion to access the memory.DMA devices are given higher priority than the processor to access the bus.Among different DMA devices, high priority is given to high-speed peripherals such as a disk or a graphics display device.

The DMA transfers the data in three modes which include the following.

a) Burst Mode: In this mode DMA handover the buses to CPU only after completion of whole data transfer. Meanwhile, if the CPU requires the bus it has to stay ideal and wait for data transfer.

b) Cycle Stealing Mode: In this mode, DMA gives control of buses to CPU after transfer of every byte. It continuously issues a request for bus control, makes the transfer of one byte and returns the bus. By this CPU doesn't have to wait for a long time if it needs a bus for higher priority task.
c) Transparent Mode: Here, DMA transfers data only when CPU is executing the instruction which does not require the use of buses.

A conflict may arise if both the processor and a DMA controller or two DMA controllers try to use the bus at the same time.To resolve these conflicts, an arbitration procedure is implemented on the bus.

The device that is allowed to initiate transfers on the bus at any given time is called the bus master. When the current bus master relinquishes its status as the bus master, another device can acquire this status.The process by which the next device to become the bus master is selected and bus mastership is transferred to it is called bus arbitration.

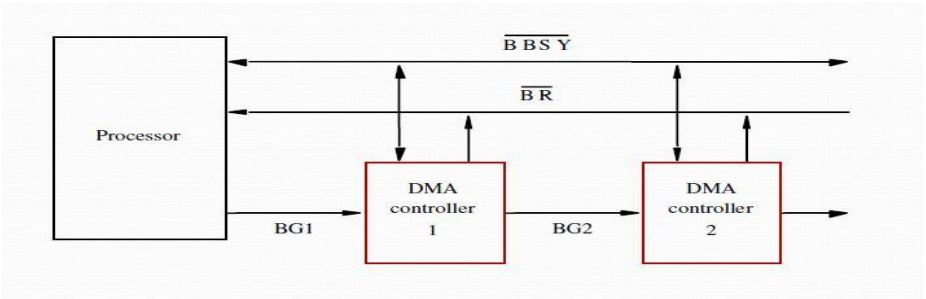
Bus Arbitration

- Centralized arbitration:
  A single bus arbiter performs the arbitration.
- Distributed arbitration:
  All devices participate in the selection of the next bus master

Centralized Bus Arbitration :

Bus arbiter may be the processor or a separate unit connected to the bus.Normally, the processor is the bus master, unless it grants bus membership to one of the DMA controllers.DMA controller requests the control of the bus by asserting the Bus Request (BR) line.In response, the processor activates the Bus-Grant (BG1) line, indicating that the controller may use the bus when it is free.

The bus grant signal is connected to all DMA controllers in a daisy chain fashion.The current bus master indicates to all devices that it is using the bus by activating another signal called BBSY.BBSY signal is 0, it indicates that the bus is busy. When BBSY becomes 1, the DMA controller which asserted BR can acquire control of the bus.



Distributed arbitration

All deviceswaitingto use the bus share the responsibility of carrying out the arbitration process.Arbitration process does not depend on a central arbiter and hence

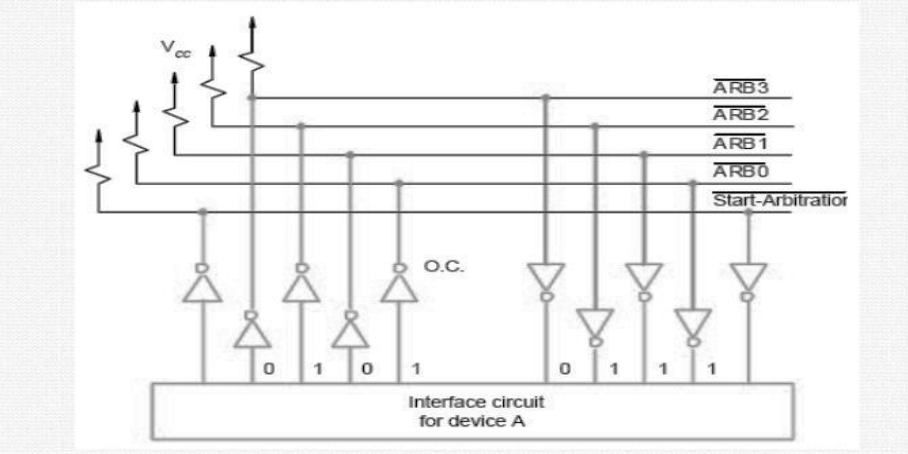
distributed arbitration has higher reliability. Each device is assigned a 4-bit ID number.All the devices are connected using 5 lines, 4 arbitration lines to transmit the ID, and one line for the Start-Arbitration signal.

To request the bus a device:

- Asserts the Start-Arbitration signal.
- Places its 4-bit ID number on the arbitration lines.

The pattern that appears on the arbitration lines is the logical-OR of all the 4-bit device IDs placed on the arbitration lines.The winner is selected based on the net outcome of the 4 lines It is the device with the highest ID among the requested devices.

Each device compares the pattern that appears on the arbitration lines to its own ID, starting with MSB.If it detects a difference, it transmits 0's on the arbitration lines for that bit and all lower bit positions.



Example

- Device A has the ID 5 and wants to request the bus:
  - Transmits the pattern 0101 on the arbitration lines.
- Device B has the ID 6 and wants to request the bus:
  - Transmits the pattern 0110 on the arbitration lines.
- Pattern that appears on the arbitration lines is the logical OR of the patterns:
  - Pattern 0111 appears on the arbitration lines.

Example

- Device A compares its ID 5 with a pattern 0101 to pattern 0111. It detects a difference at bit position 3 as a result, it transmits a pattern 0100 on the arbitration lines.
- The pattern that appears on the arbitration lines is the logical-OR of 0100 and 0110, which is 0110.
- This pattern is the same as the device ID of B, and hence B has won the arbitration.