PROJECT PART II

DVB-S2X RECEIVER IMPLEMENTATION

DIGITAL BASEBAND RECEIVER ON RFSOC

An EDL Project by

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WHAT IS DVB-S2X?

OVERVIEW

DVB-S2X (Digital Video Broadcasting – Satellite – Second Generation Extension) is an advanced standard optimized for high-throughput broadcast systems.

KEY EXTENSIONS OVER DVB-S2

- **Efficiency:** Higher spectral efficiency for modern transponders.
- **Modulation:** Support for higher-order modulations (up to 256APSK).
- **Robustness:** Improved performance under low Signal-to-Noise Ratio (SNR).

Next-Gen Satellite Tech

PROJECT OBJECTIVE

CORE OBJECTIVE

Design and implement a complete **DVB-S2X digital baseband receiver** capable of real-time video output.

- **Input:** Constellation-demapped soft bits / LLRs.
- **Output:** Valid Transport Stream (TS).

IMPLEMENTATION STRATEGY

Leverage modern hardware description languages and high-performance FPGA platforms.

- **RTL Design:** Verilog or Chisel.
- **Hardware:** AMD Xilinx RFSoC 4x2 (Zynq UltraScale+).

SYSTEM ARCHITECTURE

STAGE 1

INPUT INTERFACE

Receives soft bits/LLRs from Part I.

STAGE 2

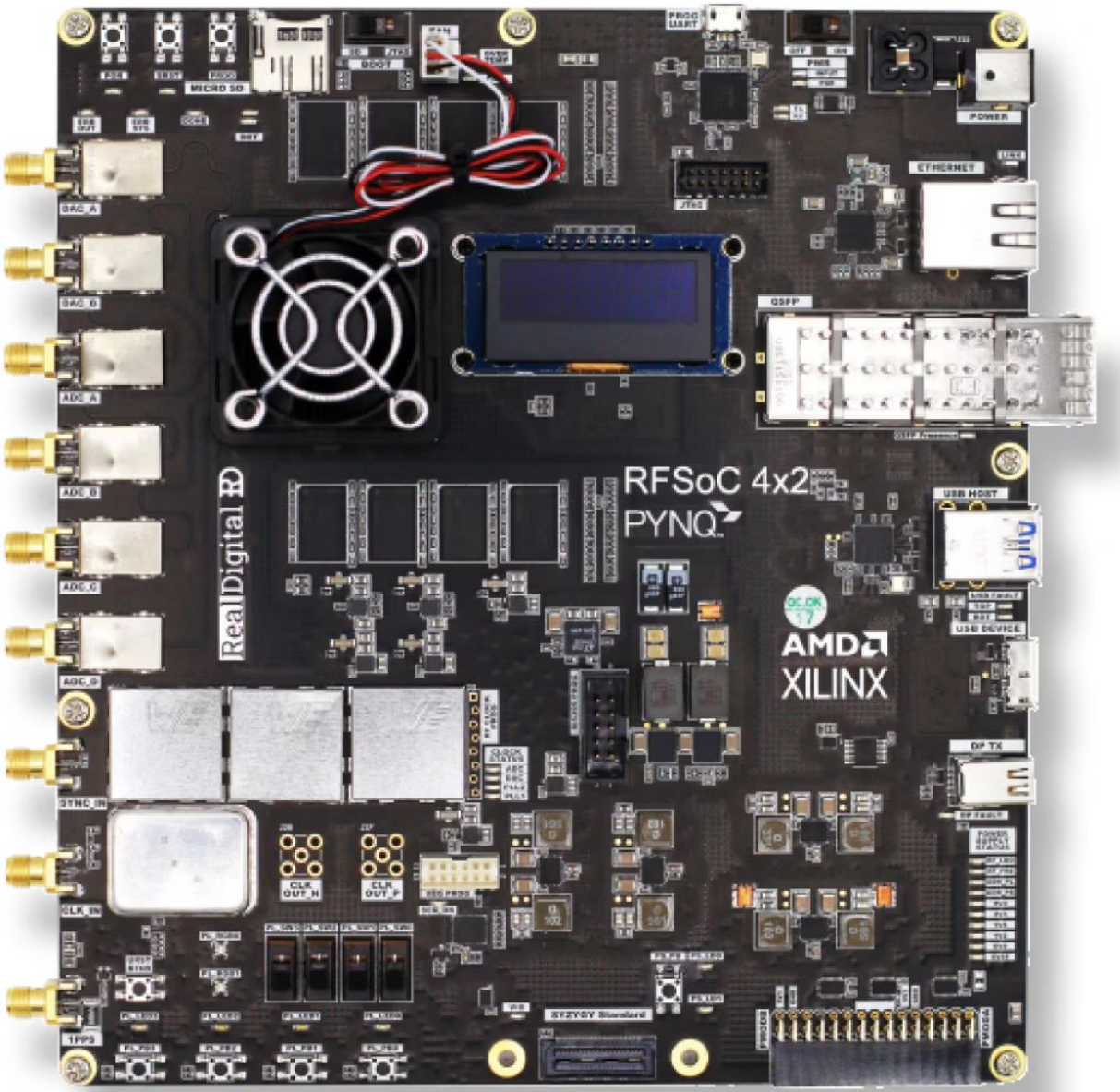
RECEIVER PIPELINE

LDPC → BCH → Descrambling → BBFRAME → CRC

STAGE 3

HARDWARE OUTPUT

Video display directly driven by the RFSoC logic.



RECEIVER BLOCK CHAIN

FRONT-END (PART I)

- Baseband AGC
- Symbol Timing Recovery
- Carrier Frequency Recovery
- Carrier Phase Recovery
- Pilot Detection & Removal
- PLFRAME Synchronization
- Physical Layer Descrambling
- Soft-Output Constellation Demapping

BACK-END (OUR RESPONSIBILITY)

- **LDPC Decoding** (Error Correction)
- **BCH Decoding** (Error Floor Removal)
- Baseband Descrambling
- BBFRAME Extraction
- CRC-8 Verification
- Transport Stream Generation
- **Video Display Interface**

TEAM RESPONSIBILITY

DECODING & DESCRAMBLING

- **LDPC Decoding:** Advanced error correction for high-noise environments.
- **BCH Decoding:** Supplemental coding to clean up residual errors.
- **Baseband Descrambling:** Restoring original baseband frame data.

FRAMING & OUTPUT

- **BBFRAME Extraction:** Identifying valid frames from the stream.
- **CRC-8 Verification:** Ensuring data integrity per frame.
- **Transport Stream Generation:** Formatting data for standard video interfaces.
- **Video Output:** Direct drive display from FPGA logic.

FINAL DELIVERABLE

End-to-end real-time DVB-S2X receiver with video display on RFSoC, integrated with Part I.

DELIVERABLES

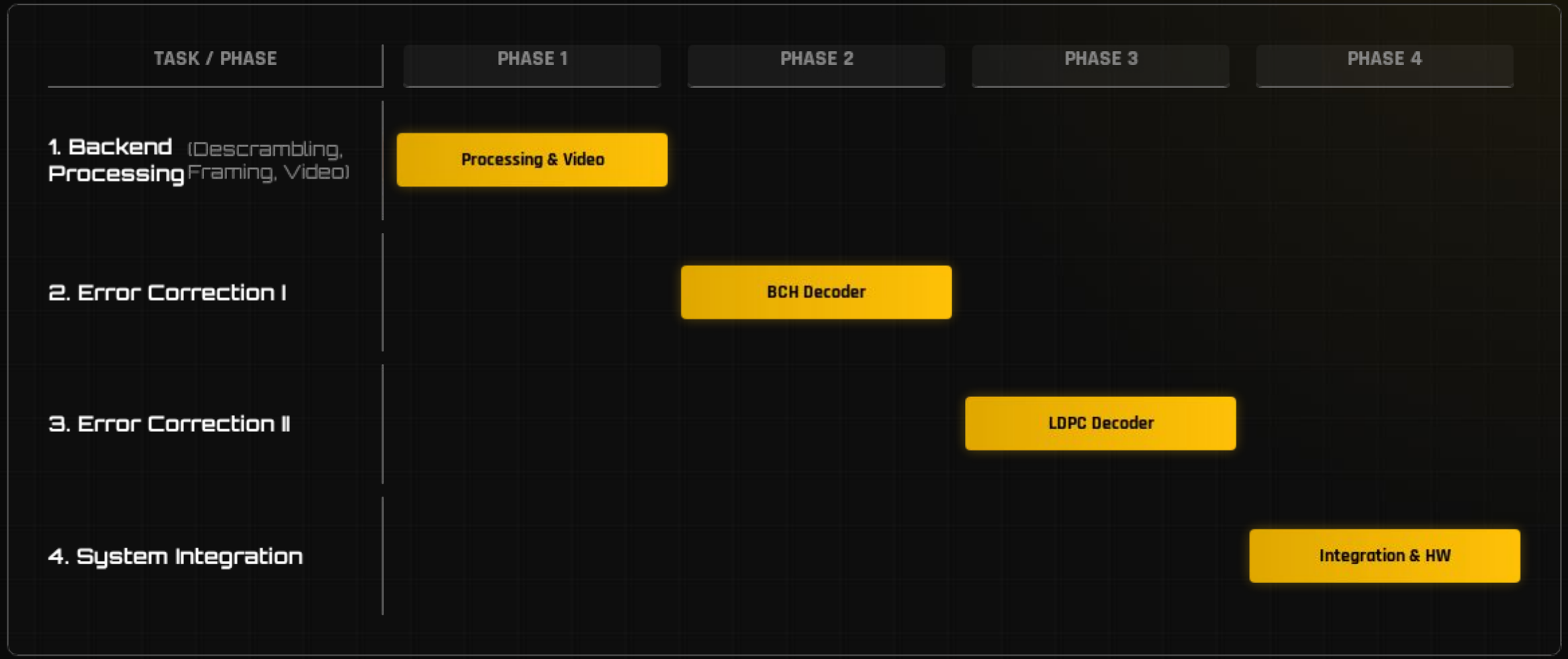
MINIMUM DELIVERABLES

- Functional LDPC & BCH Decoders.
- Baseband Descrambling.
- BBFRAME & CRC-8 Verification.
- Valid TS Generation.
- **Hardware Video Display.**

DESIRED DELIVERABLES

- All DVB-S2X code rates & frame sizes.
- Full rate real-time throughput.
- Robust video playback across configurations.

IMPLEMENTATION TIMELINE



TEAM PLAN (NEXT 3 WEEKS)

EXECUTION STRATEGY

- Collaborative 3-Person Team per block
- One Major Block per Week
- RTL + RFSoC Validation before moving on

WEEK 1

DESCRAMBLING BLOCK

- Baseband Descrambler
- RTL Development & Sim
- **RFSoC Integration** (w/ LDPC/BCH)

WEEK 2

FRAMING & ERROR DETECTION

- BBFRAME Extraction
- CRC-8 Verification
- RTL Test Case Validation
- **RFSoC Hardware Testing**

WEEK 3

OUTPUT & INTEGRATION

- Transport Stream (TS) Gen
- Video Output Interface
- End-to-End Integration
- **Final Video Display Demo**

Thank You!