FF No.: 654

COURSE CODE: IT2201

COURSE NAME: COMPUTER ORGANIZATION AND ARCHITECTURE

Course Prerequisites:

Basics of computer system and any programming language.

Course Objectives:

1. To study the fundamental concepts of structural Computer system and Computer Arithmetic
2. To understand the basic concepts and functions of Microprocessor
3. To gain knowledge of Computer Memory System
4. To get familiar with GPU and CPU architecture
5. To identify solutions for real world design issues using processors.

Credits: 5

Teaching Scheme Theory: 3 Hours/Week
Tut: 1 Hours/Week
Lab: **2** Hours/Week

Course Relevance:

Modern computer technology requires an understanding of both hardware and software, since the interaction between the two offers a framework for mastering the fundamentals of computing.

The purpose of this course is to cultivate an understanding of modern computing technology through an in-depth study of the interface between hardware and software.

In this course, you will study the history of modern computing technology before learning about modern computer architecture and a number of its essential features, including instruction sets, processor arithmetic and control, the Von Neumann architecture, pipelining, memory management, storage, and other input/output topics.

The course will conclude with a look at the recent switch from sequential processing to parallel processing by looking at the parallel computing models and their programming implications.

SECTION I

Basic concepts of Digital Electronics, Organization and Architecture, Structure & Function, Brief History of computers, Von Neumann Architecture, Integer Representation: Fixed point & Signed numbers. Integer Arithmetic: 2's Complement arithmetic, multiplication, Booth's Algorithm, Division Restoring Algorithm, Non Restoring algorithm, Floating point representation: IEEE Standards for Floating point representations.

8086 Microprocessor Architecture, Register Organization, Instruction types, Types of operands, Instruction formats, addressing modes and address translation. Near & FAR procedure, Instruction cycles. RISC Processors: RISC- Features, CISC Features, Comparison of RISC & CISC Superscalar Processors. Case study of Processor.

Fundamental Concepts: Single Bus CPU organization, Register transfers, Performing an arithmetic/ logic operations, fetching a word from memory, storing a word in memory, Execution of a complete instruction. Micro-operations, Hardwired Control, Example-Multiplier CU. Micro-programmed Control: Microinstructions, Microinstruction-sequencing: Sequencing techniques, Micro-program sequencing

SECTION II

Need, Hierarchical memory system, Characteristics, Size, Access time, Read Cycle time and address space. Main Memory Organization: ROM, RAM, EPROM, E 2 PROM, DRAM, Design examples on DRAM, SDRAM, DDR3, Cache memory Organization: Address mapping. Basic concepts: role of cache memory, Virtual Memory concept. Pipeline and its performance, Data hazards: operand forwarding, handling data hazards in software, side effects. Instruction hazards: unconditional branches, conditional branches and branch prediction.

Parallelism in Uniprocessor system, Evolution of parallel processors, Architectural Classification, Flynn's, Fengs, Handler's Classification, Multiprocessors architecture basics, Parallel Programming Models : Shared memory, Message passing, Performance considerations : Amdahl's law, performance indications.

Parallel computing architectures (multi-core CPUs, GPUs, traditional multi-processor system, Xeon-Phi, Jetson Kit, Kilocore processor), multiprocessor and multicomputer systems, interconnection networks, Modern GPU architecture (in brief), Performance comparison: Speedup, Gain time and scalability.

List of Practical (Any Six)

1. Study of 8086 Architecture and Execution of sample programs.
2. Write 8086 ALP to access marks of 5 subjects stored in array and find overall percentage and display grade according to it.
3. Write 8086 ALP to perform block transfer operation. (Don't use string operations) Data bytes in a block stored in one array transfer to another array. Use debugger to show execution of program.
4. Write 8086 ALP to find and count zeros, positive number and negative number from the array of signed number stored in memory and display magnitude of negative numbers.
5. Write 8086 ALP to convert 4-digit HEX number into equivalent 5-digit BCD number.
6. Write 8086 ALP to convert 5-digit BCD number into equivalent 4-digit HEX number.
7. Write 8086 ALP for following operations on the string entered by the user.
   a. String length
   b. Reverse of the String
   c. Palindrome
8. Write 8086 ALP for following operations on the string entered by the user (Use Extern Far Procedure).
   a. Concatenation of two strings
   b. Find number of words, lines.
   c. Find number of occurrences of substring in the given string.
9. Write 8086 ALP to initialize in graphics mode and display following object on screen.
10. Write 8086 ALP to encrypt and decrypt the given message.
11. Write 8086 ALP to perform following operations on file
    a. Open File
    b. Write data in the file.
    c. Delete data in the file.
    d. Close the file.

List of Course Projects:

1. Combinational and Sequential circuits
2. Memory Management
3. Graphics Mode
4. IOT based projects.
5. IoT based atmospheric CO2 administration.
6. IoT based flood risk predictor.
7. Simulate modern traffic control system.
8. Online Parallel Examination.

List of Course Seminar Topics:

1. Computer Architecture VS Computer Organization
2. Evolution of Computing Devices
3. Instructions types , formats and execution
4. Interrupts in Microprocessor
5. Trends in computer architecture
6. RISC Vs CISC architecture : A Case Study
7. ARM processor architecture
8. Latest Technology in Embedded systems
9. Multiplier Control Unit
10. Booth's Encoding Pattern for Fast Scalar Point Multiplication in ECC for Wireless Sensor Networks
11. Internet of Things (IoT) in 5G Wireless Communications
12. State of the art parallel processor design.
13. Memory management in mobile OS.
14. Evolution of processors.
15. Ultra SPARC Processor Architecture.

List of Course Group Discussion Topics:

1. GPU computing: CUDA
2. Memory System
3. Replacement Algorithms
4. Pipelining
5. Cache Coherance
6. Virtural Memory
7. Hazards in pipelining
8. Super Computer
9. Modern computer generations
10. Parallel computing models

List of Home Assignments:

Design:

1. Write the sequence of control steps required for the single bus organization for each of the following instructions:
   1. ADD the (immediate) number NUM to register R1
   2. ADD the contents of memory location NUM to register R1

   Assume that each instruction consists of two words. The first word specifies the operation and addressing mode, and second word contains the number NUM
2. Configure a 32 Mb DRAM chip. Consider cells to be organized in 8K X 4 array. Find out the number of address lines.
3. A set associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Analyze the format of main memory addresses with proper explanation.

4. A one pipeline system takes 50 ns to process a task. The same task can be processed in 6 segment pipeline with a clock cycle of 10 ns. Determine the speedup ratio of pipeline for 100 tasks. What is maximum speedup ratio?

Case Study:

1. Micro-programmed Control Unit and Hardwired Control Unit.
2. Pipeline Hazards
3. Flynn's architectural classification scheme.
4. Modern Processor units

Survey:

1. New memory technologies and their potential impact on **architecture**
2. Virtual Memory
3. Simulation of a superscalar processor and analyzing impact of design tradeoffs
4. Cache Consistency Models in Modern Microprocessors

Blog:

1. Super Computer
2. Intel Journey
3. New Arm Interconnect technologies
4. Distributed Systems and Parallel Computing

Assessment Scheme:

Mid Semester Examination - 10 Marks
Presentation - 15 Marks
Laboratory - 10 Marks
Course Project - 10 Marks
Home Assignment - 10 Marks
Group Discussion - 15 Marks
End Semester Examination - 10 Marks
Comprehensive Viva Voce - 20 Marks

Text Books:

1. William Stallings, "Computer Organization and Architecture: Designing for Performance", 7th Edition, Pearson Prentice Hall Publication, ISBN 81-7758-9 93-8.
2. C. Hamacher, V. Zvonko, S. Zaky, "Computer Organization", 5th Edition, Tata McGraw Hill Publication, ISBN 007-120411-3.
3. Kai Hwang, "Advanced Computer Architecture", Tata McGraw-Hill ISBN 0-07-113342-9
4. Douglas Hall, "Microprocessors and Interfacing", 2nd Edition, Tata McGraw Hill Publications, ISBN 0-07-025742-6.
5. Peter Abel, "Assembly Language Programming," 5th Edition, Pearson Education Publications, ISBN 10:013030655.

Reference Books:

1. *Hwang and Briggs,"Computer Architecture and Parallel Processing", Tata McGraw Hill Publication ISBN 13: 9780070315563.*

2. A. Tanenbaum, "Structured Computer Organization", Prentice Hall Publication, ISBN 81 –203 – 1553 – 7, 4th Edition.

MOOCs Links and additional reading material:

1. www.nptelvideos.in
2. https://www.udemy.com/
3. https://learn.saylor.org/
4. https://www.coursera.org/
5. https://swayam.gov.in/

Course Outcomes:

Upon completion of the course, post graduates will be able to –

1. Demonstrate computer architecture concepts related to design of modern processors, memories and I/Os. (2)
2. Illustrate the micro operations sequencing. (3)
3. Evaluate various alternatives in processor organization. (3)
4. Understand concepts related to memory & IO organization (2)
5. Adapt the knowledge based on Pipeline and its performance (3)
6. Design real world applications using processors. (4)

Future Courses Mapping:
Advance Computer Architecture, Advance Operating Systems

Job Mapping*:*
Application Developers, System programmer