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ID NO. :- 21EL095

Division :- 11

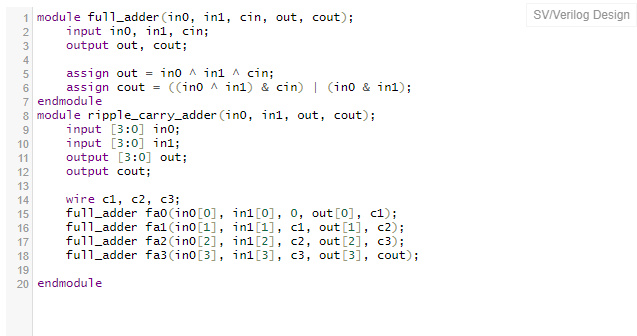
Subject:- Digital System Design

Branch :- Electronics

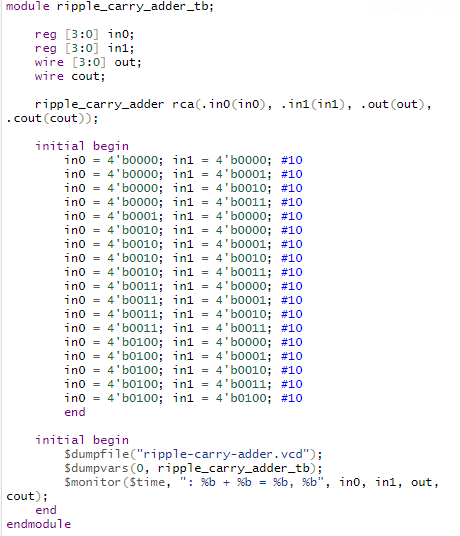
Assignment: - 2

Design 4-bit Ripple Carry Adder with the help of 1-bit adder

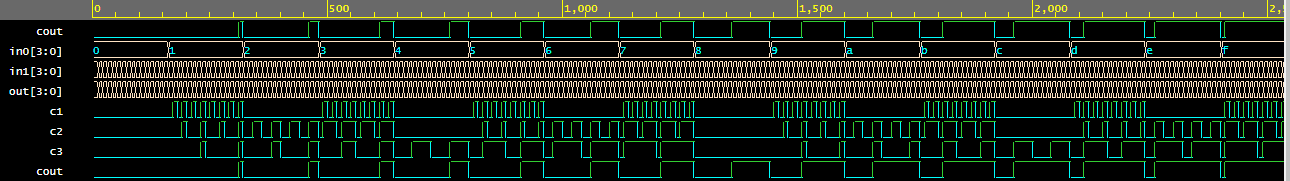
VERILOG CODE:-



TEST BENCH

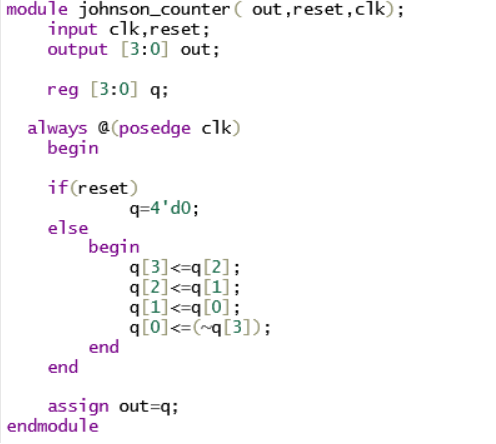


OUTPUT

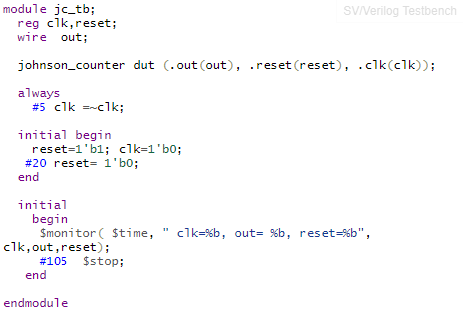


Design D-flipflop and reuse it to implement 4- bit Johnson Counter

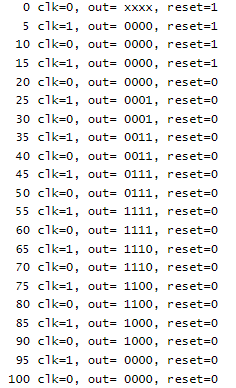
Verilog code



TEST BENCH

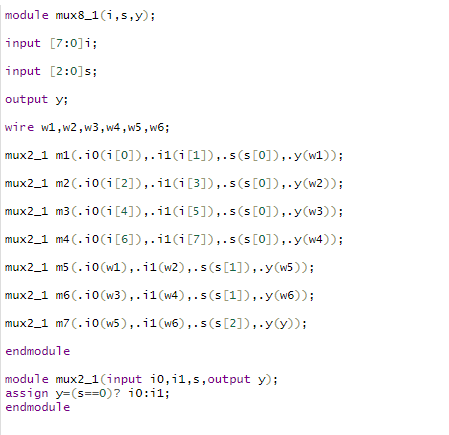


OUTPUT

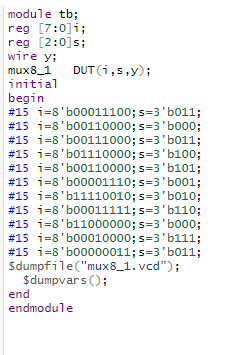


Reuse 2:1 Mux code to implement 8:1 Mux

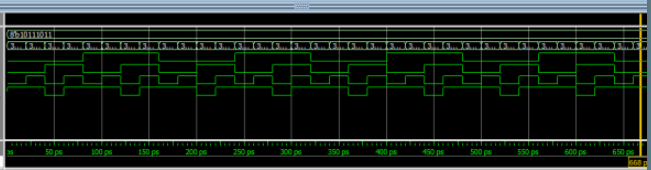
VERILOG CODE:-



TEST BENCH:-

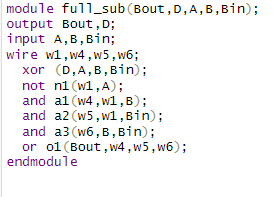


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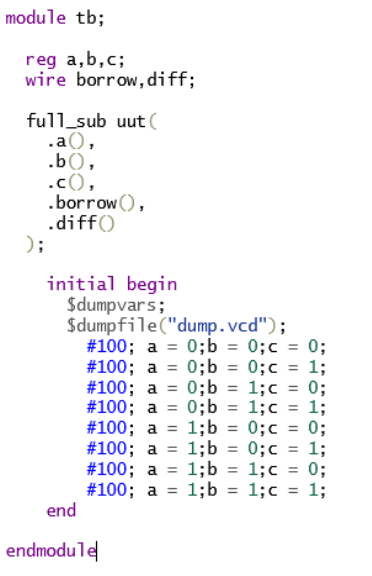


Design a Full Subtractor with Gate Level Modelling Style. (Use primitive gates)

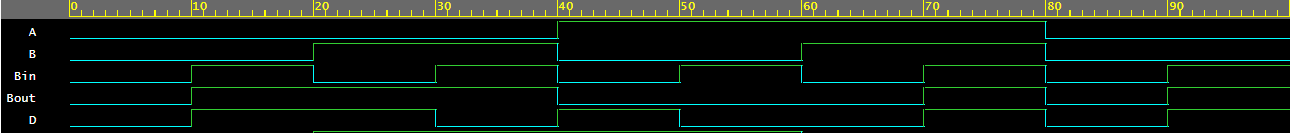
VERILOG CODE:-

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TEST BENCH:-

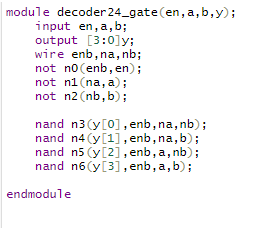


OUTPUT:-

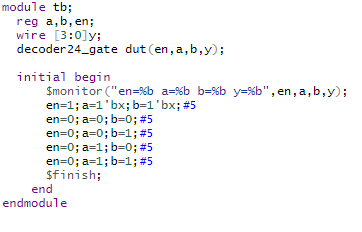


Design a 2X4 decoder using gate level modelling

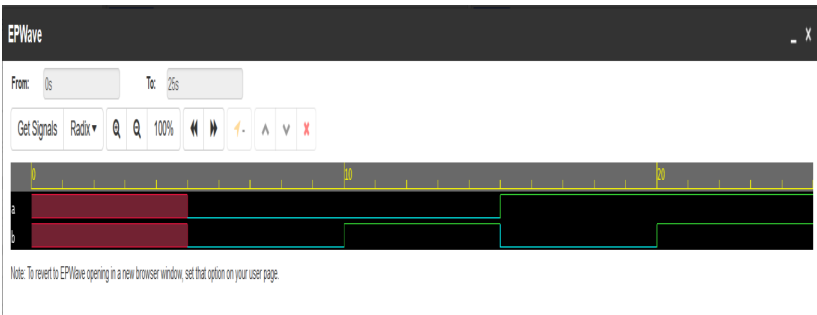
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TEST BENCH:-

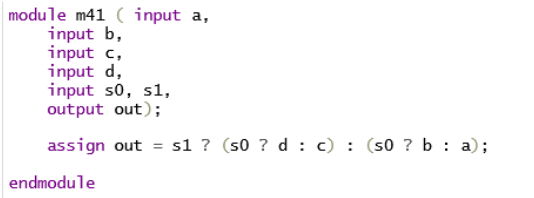


OUTPUT:-

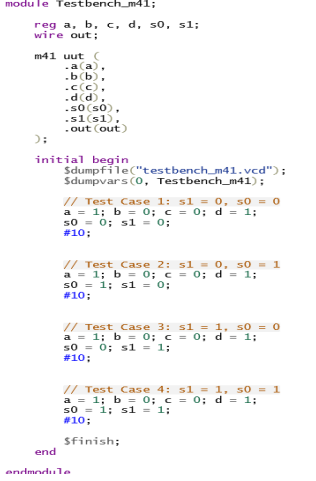


Design a 4x1 mux using operators. (Use data flow)

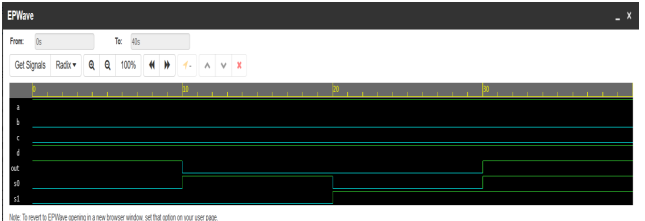
VERILOG CODE: -



TEST BENCH: -

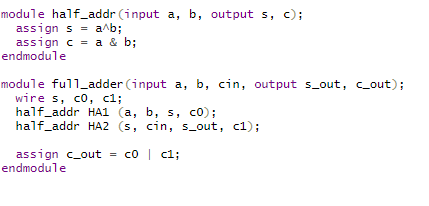


OUTPUT: -

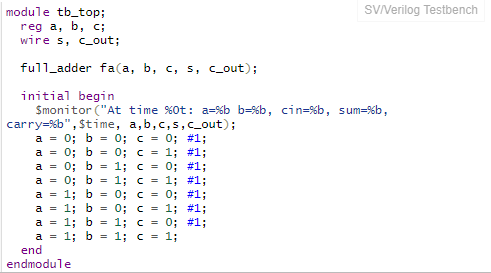


Design a Full adder using half adder.

VERILOG CODE:-



TEST BENCH: -



Output

