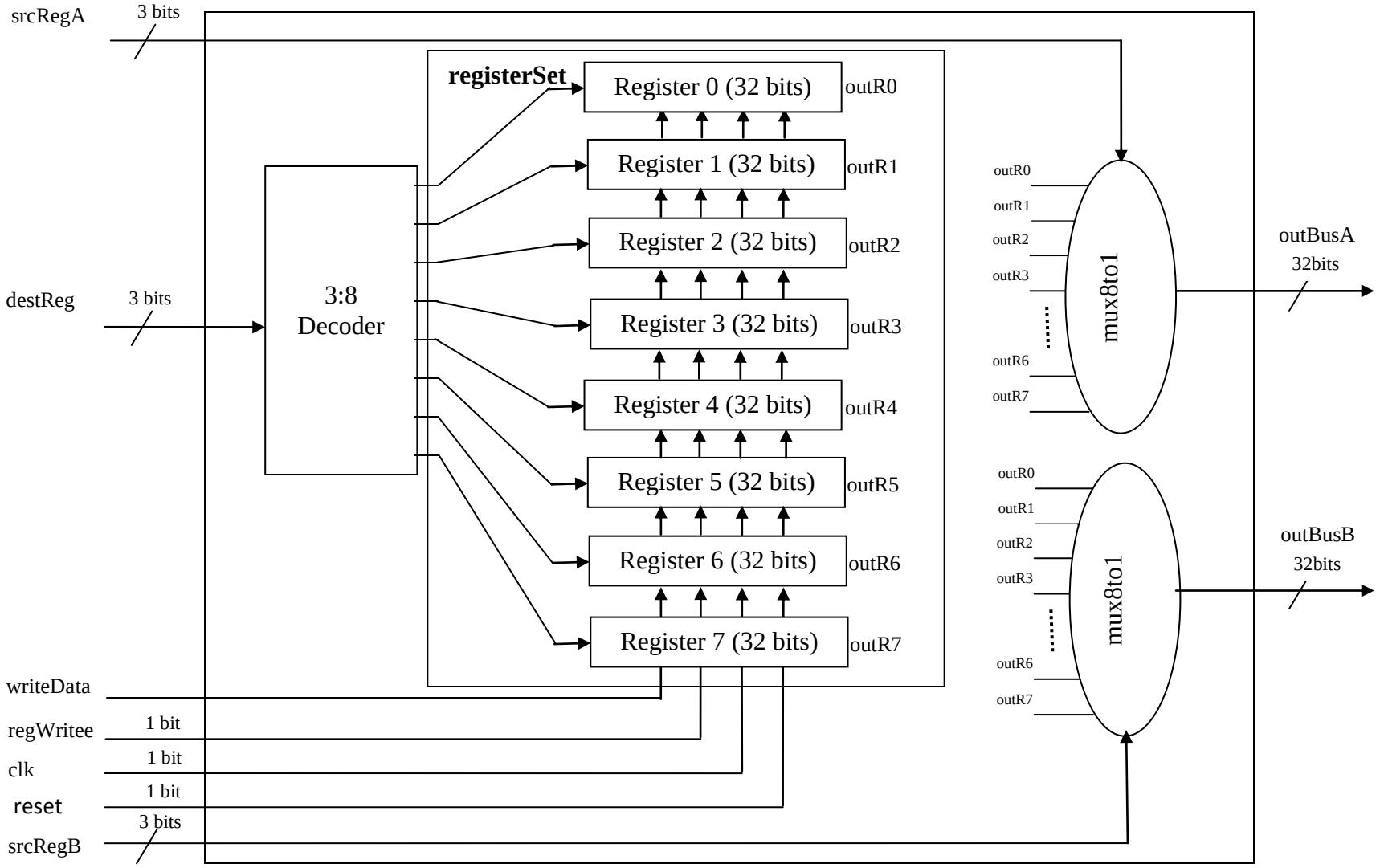
BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI K. K. BIRLA Goa Campus
First Semester 2014-2015
CS F342 Computer Organization and Architecture
Lab – 1, 14th August 2014

Design and implement the following using verilog HDL in **ModelSim software** with the following specifications.



Modules

1.module D_ff(input clk, input reset, input regWrite, input decOut1b , input d, output reg q);

```
always @ (negedge clk)
begin
if(reset==1)
        q=0;
else
        if(regWrite == 1 && decOut1b==1)
        begin
                q=d;
        end
end
```

endmodule

2.module register32bit(input clk, input reset, input regWrite, input decOut1b, input [31:0] writeData, output [31:0] outR);

3. module registerSet(input clk, input reset, input regWrite, input [7:0] decOut, input [31:0] writeData, output [31:0] outR0,outR1,outR2,outR3,outR4,outR5,outR6,outR7);

4. module decoder(input [2:0] destReg, output reg [7:0] decOut);

5. module mux8to1(input [31:0] outR0,outR1,outR2,outR3,outR4,outR5,outR6,outR7, input [2:0] Sel, output reg [31:0] outBus);

6. module registerFile(input clk, input reset, input regWrite, input [2:0] srcRegA, input [2:0] srcRegB, input [2:0] destReg, input [31:0] writeData, output [31:0] outBusA, output [31:0] outBusB);

7.module test_registerFile( );

```
    //inputs
    reg clk,reset,regWrite;
    reg [2:0] srcRegA,srcRegB,destReg;
    reg [31:0] writeData;
    //outputs
    wire [31:0] outBusA;
    wire [31:0] outBusB;
    registerFile uut(clk,reset,regWrite,srcRegA,srcRegB,destReg,writeData,outBusA,outBusB);

    always begin #5 clk=~clk; end

    initial
    begin clk=0; reset=1; srcRegA=5'd0; srcRegB=5'd0;
    #5 reset=0; regWrite=1; destReg=3'd0; writeData=32'd8;
    #10 destReg=3'd1; writeData=32'd7;
    #10 destReg=3'd2; writeData=32'd6;
    #10 destReg=3'd3; writeData=32'd5;
    #10 destReg=3'd4; writeData=32'd4;
    #10 destReg=3'd5; writeData=32'd3;
    #10 destReg=3'd6; writeData=32'd2;
    #10 destReg=3'd7; writeData=32'd1;
    #10 regWrite=0; srcRegA=5'd7; srcRegB=5'd6;
    #10 srcRegA=5'd5; srcRegB=5'd4;
    #10 srcRegA=5'd3; srcRegB=5'd2;
    #10 srcRegA=5'd1; srcRegB=5'd0;
    #10 $finish;
    end
```

endmodule