Accurate Power and Latency Analysis of a Through-Silicon Via(TSV)

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***Abstract*—A Through Silicon Via(TSV) interconnects vertically stacked layers of circuit elements in a 3D IC. This leads to reduced distance and increased communication bandwidth between any two circuit elements located on different layers of the chip compared to 2D NoCs. TSVs have different physical characteristics and associated latency and power consumption compared to horizontal chip interconnects. The need of the hour is to accurately estimate the power consumption and latency of TSVs separately from horizontal interconnects through simulation. Accurate power and latency models of TSVs enable architects and researchers to arrive at the optimal design space by performing quick trade-off studies. We propose an extension to the BookSim simulator that considers TSVs as a separate type of on-chip interconnect. The associated latency and dynamic power consumption is calculated based on delay and power models involving various physical parameters of the TSV. Upon applying these models in a 3D 4x4x4 mesh topology simulation, it is observed that the total average link power consumed is lower than a 2D mesh by 13% when the vertical links(containing TSVs) are treated separately from the horizontal links. Additionally, the average network latency in the 3D mesh topology is roughly 60-82% lower than the 2D case.**

***Index Terms*—dynamic power consumption, Through-Silicon Via (TSV), Network On Chip(NoC)**

I. Introduction

As Moore's Law continues to promise larger processing power in smaller packages, TSV technology has paved the way for manufacturing 3D NoCs, densely packing more circuit elements into a single chip die. This allows any two elements located on different planes of the IC to communicate effectively and efficiently through the shortest possible path determined by routing algorithms[1]. TSVs are inter-layer vertical chip interconnects with physical characteristics and microarchitecture parameters such as height, diameter, pitch, etc. TSVs thus have different latency and power consumption behaviours compared to intra-layer horizontal chip interconnects. Power-Performance trade-off studies are critical in arriving at the optimal design space of 3D TSVs.

Cycle-accurate simulators help in visualizing the effect of changing various physical parameters of the TSV on the given performance attributes. The BookSim[2] simulator has been the de facto option for simulating 2D NoC architectures as its user-friendly suite provides a large number features and comprehensive reports that aid researchers in narrowing down to an optimal design space. Support for detailed microarchitectural parameters of TSVs for 3D NoCs is yet to be incorporated into cycle accurate simulators such as BookSim. This is because in practice, the total average power consumed by the 3D NoC is much lesser than the results from simulators as TSVs consume much lesser power compared to a horizontal interconnect. While adding new functionality to the existing simulators to support 3D NoCs, it is also important to ensure that the models used for latency and power consumption estimation are accurate and simple to incorporate into the code base.

The main focus of our work is to make use of existing accurate latency and power estimation models for TSVs and incorporate them as extensions to BookSim in order to support 3D NoC topology simulation. By considering these accurate models in 3D NoC toplogy simulations, we begin to get a clearer picture on the power consumption and transmission latency within a network in real-world scenarios. We set out to calculate the delay and power associated with a TSV, aiming to improve the accuracy of existing cycle-accurate simulators.

The work discussed in this paper involves creating a modified version of the BookSim simulator. During a simulation, the number of times the vertical and horizontal links are used in the NoC is considered separately. An analytical delay model based on dimensional analysis computes the latency for a single TSV. TSV latency can be generalized to one clock cycle[3]. A simple power model is used to calculate the dynamic power consumption only for the vertical links containing TSVs. The effects of altering the physical parameters of a single TSV such as TSV height, TSV diameter and TSV pitch, bump height, inter-metal dielectric(IMD) layer height and oxide layer thickness on the power consumption and latency have also been discussed.

Our results indicate the total average power consumed in the 3D 4x4x4 mesh topology is lower by 13% when the vertical links(containing TSVs) are treated separately from the horizontal links. Additionally, the average network latency in the 3D mesh topology is roughly 60-82% lower than the 2D case. This modification will enable researchers and NoC architects perform more reliable cycle-accurate simulation.

This paper is structured as follows: Section II discusses the related work. Section III explains the electrical model of a TSV. Section IV describes the models used for power and

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delay estimation. Section V provides information about the experimental setup. Section VI demonstrates the our results and analysis. The paper concludes in Section VII.

II. Related Work

Kim et al.[4] explored various routing designs for inter-strata communication architectures using real-world traffic patterns in 3D NoCs and proposed their own novel partially-connected 3D crossbar structure. Agyeman et al.[5] developed a novel algorithm to generate hybrid 3D NoC architectures owing to the high amount of power consumed by 3D routers and additional area requirement. The vertical connections were minimized without sacrificing the overall NoC performance. Chen et al.[6] have discussed the effect of increasing number of cores in NoCs and how to reduce the memory access latencies for cores placed in various positions(centre, corner, edge) using packet prioritization.

Kapadia et al.[7] focused on 3D NoC Power Delivery Networks(PDNs) to minimize the NoC power as well as chip-cooling power and proposed a framework that intelligently maps computation and communication resources on a die, for a given workload. Hou et al.[8] describe in detail, a new 3D Torus NoC architecture with optimal latency, power consumption and bandwidth. They also discussed the design of a bidirectional router and its corresponding routing algorithm for this optimal architecture.

Kim et al.[9] proposed a scalable RLGC model(shown in Fig. 1) considering multiple physical parameters(Table I) of the TSV to determine the capacitance of a single via. This is necessary in order to derive the power consumed under a given operating frequency and voltage. Their work in [10] used a simple equation to calculate the power consumed which involves the TSV capacitance values from [9] and the Activity Factor, a measure of the amount of work done by the underlying chip interconnects. The model is based on the via-last process since parasitic capacitances from elements like C_{imd} have to be neglected in the via-first or via-middle configurations.

For estimating latency, Khalil et al.[11] made use of dimensional analysis to devise a light-weight model that uses only three TSV parameters, namely Length, Radius and Pitch. The safe limits for these parameters used while testing the above models were taken from [12] and [13].

III. Electrical Model of the TSV

Each TSV pair is made up of a signal and ground TSV(Fig. 1(a)). The TSV and bump provide a vertical interconnect through the silicon substrate, joining the stacked chips. When designing the I/O channel with TSVs in 3-D IC, the bump is an essential component that should be considered with the TSV. Therefore, modeling and analysis of a TSV with the bump is important for advanced 3-D IC design. The underfill is the separation between the TSV bumps. The Inter Metal Dielectric layer is the separation between the TSVs. The influence of these parasitic components increases as the operating frequency increases, and has to be considered in TSV modeling for high-speed I/O design that includes TSVs.[9]

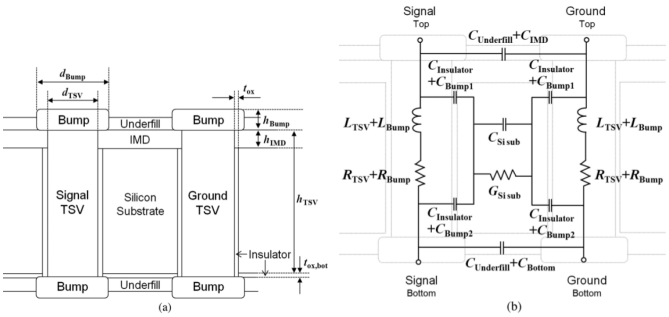


Fig. 1. (a) Structure of a signal TSV and a ground TSV with bumps with the via-last process and their structural parameters, and (b) the proposed scalable electrical model with labeled components. [9]

TABLE I
Important Physical Parameters Fig. 1 (a)

Parameter Name	Inference	Values[12]
h_{TSV}	TSV Height/Length	20–100 μm
d_{TSV}	TSV Diameter	20–80 μm
p_{TSV}	TSV Pitch	90–180 μm
h_{bump}	Bump Height	5–50 μm
t_{ox}	Oxide Layer Thickness	0.1–1.0 μm
t_{ox_bot}	Bottom Oxide Layer Thickness	1 μm
h_{imd}	Inter-metal dielectric Layer Height	5–30 μm
σ_{Cu}	Conductivity of Copper	5.96 * 10^7 S/m
ε_{Si}	Permittivity of Silicon	1.05315* 10^{-10} F/m
μ_o	Permeability in free space	1.25663706 * 10^{-6} H/m
d_{bump}	Bump Diameter	
ω	$2\pi f$	

From Fig. 1(a), a logical electrical model(Fig. 1(b)) was derived containing various values for capacitance(Table II).

L_{TSV}+L_{Bump} in series with R_{TSV}+R_{Bump} and in parallel with $C_{Insulator}$+C_{Bump2} and $C_{Insulator}$+C_{Bump1} are electrical equivalents of the Signal TSV along with the top and bottom bump. The same equivalence applies for Ground TSV. $C_{Underfill}$+C_{IMD} is the equivalent for the Underfill and Inter Metal Dielectric layers at the top of the TSV. $C_{Underfill}$+C_{Bottom} is the equivalent for the Underfill and Bottom Oxide layers at the bottom of the TSV. $C_{Si\ sub}$ and $G_{Si\ sub}$ are the capacitance and conductance of the silicon substrate respectively.

IV. TSV Latency and Power Models

A. Latency Model

Algorithm 1 shows the procedure from [11] in which TSV delay is estimated from Height/Length(l), Diameter(d) and Pitch/Separation(s). The errors in the propagation delay from the model from [11] are confined to l_o, which is the transition boundary.

TABLE II
ELECTRICAL MODEL PARAMETERS(FIG. 1(B))

Parameter Name	Inference
$C_{Underfill}$	Underfill capacitance
C_{Bump1}, C_{Bump2}	Bump capacitance
$C_{Insulator}$	Insulator capacitance
$C_{Si\ sub}$	Silicon substrate capacitance
C_{Bottom}	Bottom Oxide Layer capacitance
C_{imd}	Inter-metal dielectric Layer capacitance
R_{TSV}	TSV Resistance
R_{bump}	Bump Resistance
L_{TSV}	TSV Inductance
L_{bump}	Bump Inductance
$G_{Si\ sub}$	Silicon substrate conductance

Algorithm 1: TSV Delay Estimation

START
$r = d/2$
$l_o = \frac{\sigma_{Cu} * r^2 * \sqrt{(\mu_o/\varepsilon_{si})} * acosh(s/d)}{0.693 * (1 + 0.617 * (r/s))}$
if($l \geq lo$)
    $delay = \sqrt{(\mu_o/\varepsilon_{si})} * l * l/l_o$
else
    $delay = \sqrt{(\mu_o/\varepsilon_{si})} * l$
END

B. Dynamic Power Estimation Model

The electrical model from Fig. 1(b) was further condensed to Fig. 2, highlighting only the capacitance of important elements and configured as per Table III.

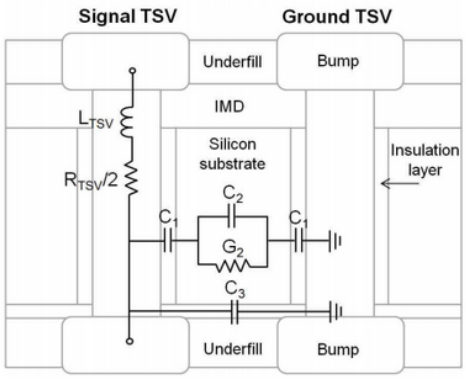


Fig. 2. Logical Layout of the TSV electrical model considered in the dynamic power model. [10]

Power consumption for each configuration was obtained using (1) where AF is the activity factor, C_{TSV} is the TSV capacitance calculated from the equation (2) and f and V are the operating frequency and voltage respectively[10].

$$Power_{TSV} = AF \,.\, C_{TSV} \,.\, V^2 \,.\, f \qquad (1)$$

$$C_{tsv} = C_3 + \frac{C_1 * C_2 * (1 + \sigma_{Cu}/(\varepsilon_{si} * \omega))}{C_1 + 2 * C_2 * (1 + \sigma_{Cu}/(\varepsilon_{si} * \omega))} \qquad (2)$$

TABLE III
REDUCED MODEL PARAMETERS(FIG. 2 (B))

Parameter Name	Inference
C_{b1}	C_{ins} + C_{Bump1}
C_{b2}	C_{ins} + C_{Bump2}
C_1	(C_{b1}*C_{b2})/(C_{b1}+C_{b2})
C_2	$C_{Si\ sub}$
C_3	$C_{Underfill}$ + C_{Bottom}

From Fig. 6(a) ,shorter TSVs consume lesser power due to the smaller TSV capacitance values. The TSV capacitances drop off significantly at larger lengths ($\geq 90\mu$m) due to the significant decrease in insulator and substrate capacitances. For a given pitch value, larger diameters cause higher insulator capacitance (C_{ins}) and bump capacitances (C_{Bump1} and C_{Bump2}). These result in higher power consumed for a larger diameter TSV. From Fig. 6(b), the combined effect of diameter and TSV capacitance influences the power consumed significantly for longer TSVs.

Smaller pitch values result in higher power consumption in TSVs. Decreasing the pitch values increases the capacitances of the Underfill, IMD, and the bottom oxide layer. These capacitances in turn increase the capacitance between the signal and the ground TSV, thereby increasing the total power consumed at lower pitch values. From Fig. 7(a), a larger reduction in power is seen at smaller pitch values ($\leq 120\mu$m). Pitch values above 130 μm do not affect the capacitance between the signal and the ground TSV significantly.

V. EXPERIMENTAL SETUP

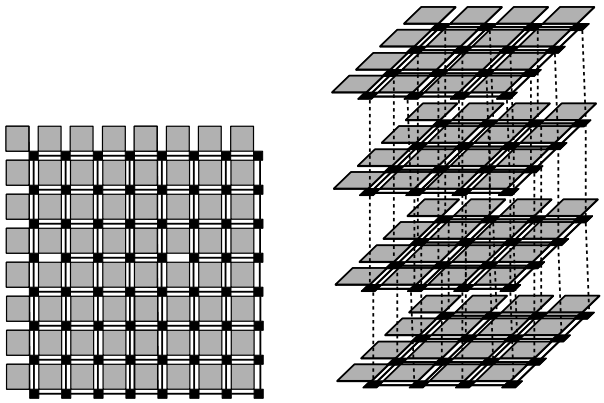
A parameter-based tool written in C/C++ using the equations from [9], [10] and [11] was used to find the latency and power consumption for varying values of parameters(from Table I) while keeping others constant generated using Python scripts. The power model was finally tested against a 3D 4x4x4 mesh topology under environmental constraints specified in Table IV. For the processor used in the mesh for the simulation we have considered the Sun SPARC chip which has a total area of 396mm^2 using 65nm fabrication technology. Scaled to 32nm technology, each core has an area of 3.4mm^2[14]. Dsent[15] was used for router area (32nm fabrication technology) and for latency comparison.

After brute-forcing all the valid combinations from the ranges of length, diameter and pitch given in [12] against the model, the ideal TSV has a length of 20μm, diameter of 20μm and pitch of 180μm, consuming only 4.2 μWatts of power anytime a bit is transmitted through it.

TABLE IV
SIMULATION ENVIRONMENT

Simulator	BookSim
Operating Frequency	2.5 GHz
Activity Factor	0.15
Packet Injection Rates(flits/cycle)	0.002–0.2
Traffic Pattern	Uniform
Clock Cycles(*CCycle*)	100000
Topology Simulated	3D 4x4x4 Mesh
TSVs per Vertical Link(*TSVL*)	128
Power Consumed per TSV(*PCT*)	4.2 μW

Using the simulation framework(shown in Fig. 4), the extended version of Booksim containing implementations of the accurate latency and power models described in the previous section is used to simulate a 4x4x4 3D Mesh architecture(Fig. 3(b)). The uniform traffic pattern was used and average network latency and link power were noted and compared against simulation results from a standard 2D Mesh NoC architecture(Fig. 3(a)).



(a) (b)

Fig. 3. 64 core NoC architecture (a) 2D 8x8 Mesh and (b)3D 4x4x4 Mesh Topology.

To evaluate the effectiveness of the power model, a simulation of uniform traffic patterns with varying packet injection rates was run over a simple 3D 4x4x4 mesh topology using the BookSim simulator, with a few changes to the underlying source code. A counter was added to monitor the number of times a vertical link was used to transmit data and stores it as *VLink*. Each simulation for a given packet injection rate was run for 100000 clock cycles(denoted by *CCycle*). From the log files summarizing each simulation, (3) was used to calculate the average TSV power. The result was added to the total average power consumption.

$$Average\_Power_{\text{TSV}} = \frac{VLink * TSVL * PCT}{CCycle} \quad (3)$$

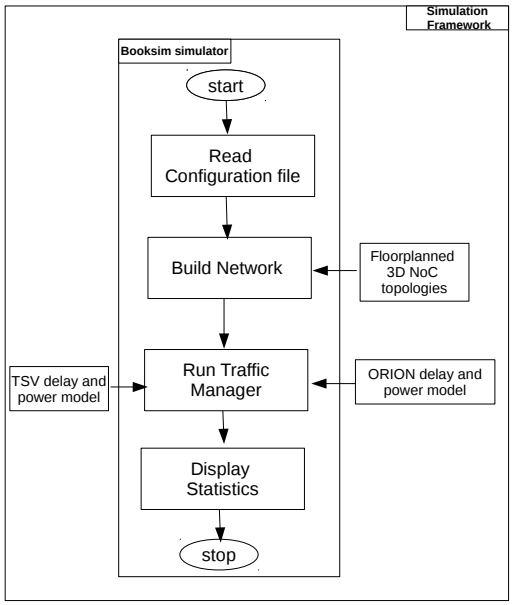


Fig. 4. Workflow of the extended version of BookSim

VI. RESULTS AND ANALYSIS

A. TSV Delay Analysis

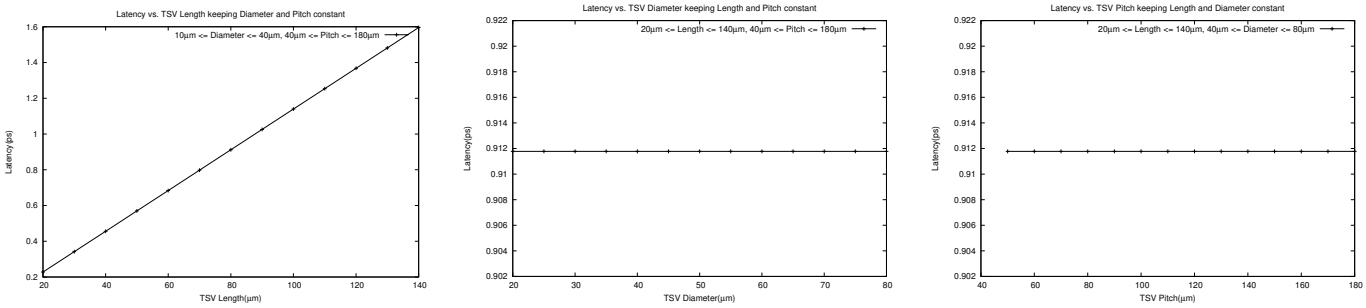
From Fig. 5 it is clear that the length of the TSV is the major contributing factor to the latency for different fixed values of TSV Diameter and Pitch. Varying the Pitch and Diameter however, does not affect the latency which confirms the logical intuition that sending a bit across a line is simply the propagation delay along the line which is solely dependent on the its length. The TSV latency can be generalized to one clock cycle and a lower TSV length implies a lower latency.

B. TSV Power Analysis

It can be observed that ideally, an energy efficient TSV should be constructed such that it has a low length so that less energy is spent transmitting a bit across, a low diameter since lesser power is required to maintain the current through a smaller cylinder and a high pitch which reduces the effective coupling capacitance from neighbouring TSVs.

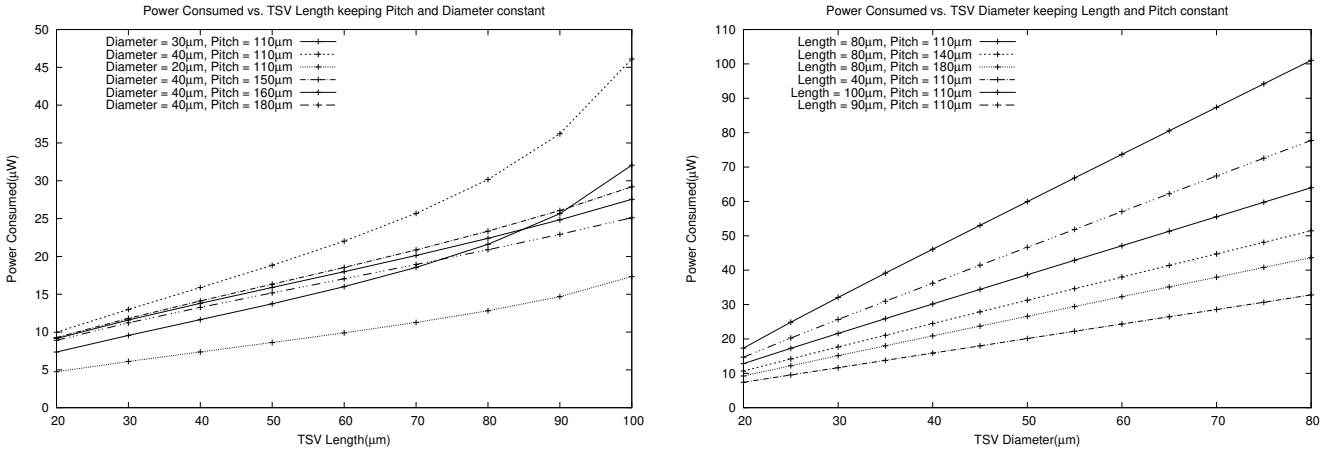
The effect of varying other TSV parameters such as the Bump Height(Fig. 7(b)) and IMD Layer Height(Fig. 8(b)) and Oxide Layer Thickness($\mathbf{t_{ox}}$ in Fig. 1) was also investigated keeping TSV Length, Diameter and Pitch constant(Fig. 8(b)). While one of the three parameters was varied, the other two were set to the default of 1 μm.

Bump Height is a negligible component in power consumption since the Underfill capacitiance does not greatly affect the overall TSV capacitance. Insulator capacitance however, has a negative dependence on the IMD Layer Height, resulting in a linear decrease . A higher oxide layer thickness also



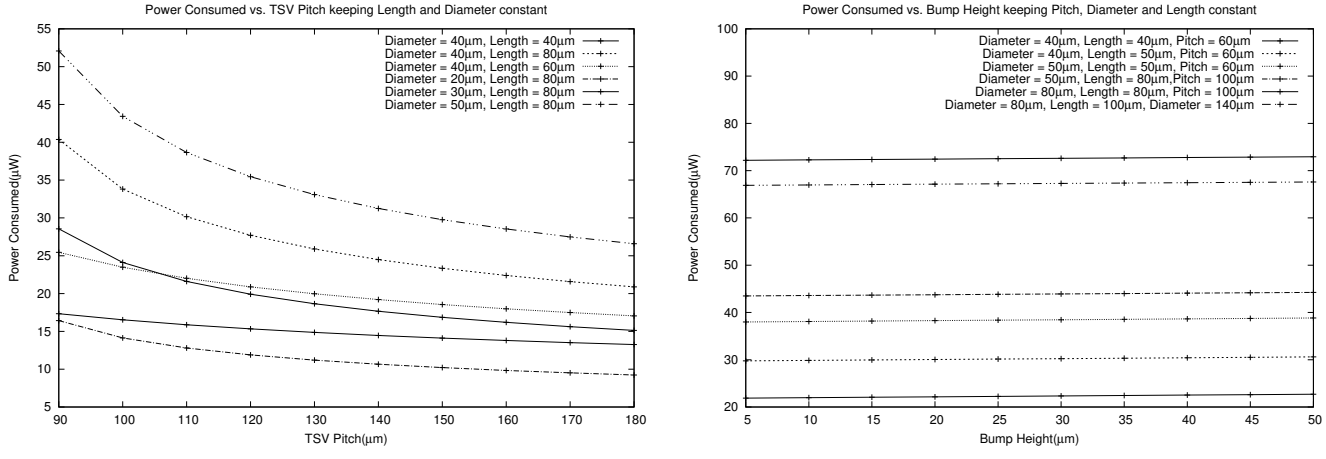
(a) (b) (c)

Fig. 5. Effect of varying TSV (a)length, (b)diameter and (c)pitch on latency for a single via, at operating frequency=2.5 GHz and voltage=1.1 V



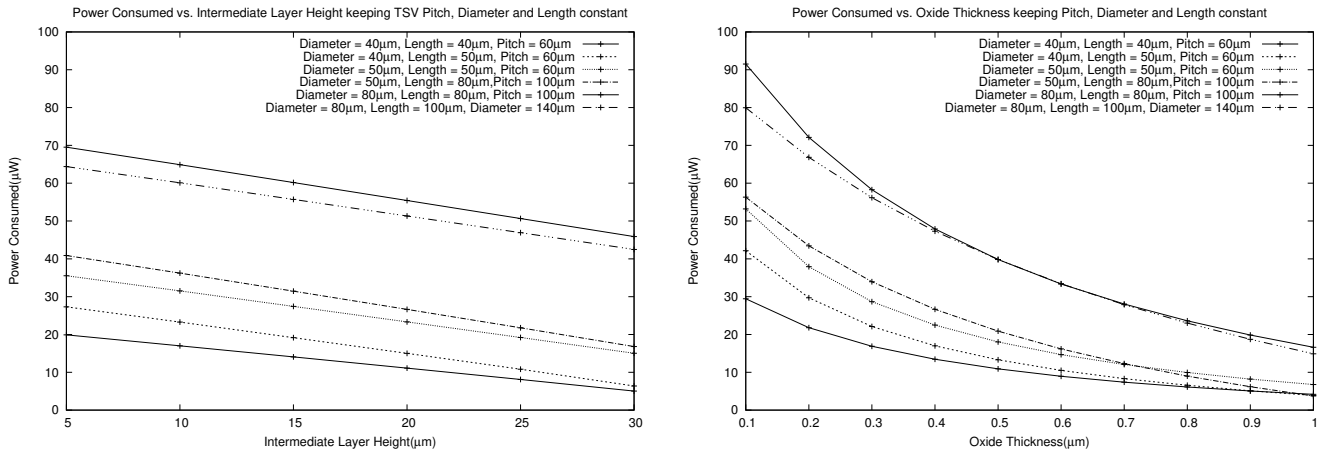
(a) (b)

Fig. 6. Effect of varying TSV (a)length, and (b)diameter on Power Consumption for a single TSV, at operating frequency=2.5 GHz and voltage=1.1 V with activity factor(AF) = 0.15



(a) (b)

Fig. 7. Effect of varying (a)TSV pitch (b)Bump Height on Power Consumption for a single TSV, at operating frequency=2.5 GHz and voltage=1.1 V with activity factor(AF) = 0.15



(a) (b)

Fig. 8. Effect of varying (a)IMD Layer Height and (b)Oxide Layer Thickness on Power Consumption for a single TSV, at operating frequency=2.5 GHz and voltage=1.1 V with activity factor(AF) = 0.15

contributes to lower power drawn by the TSV due to the its logarithmic relationship with insulator capacitance.

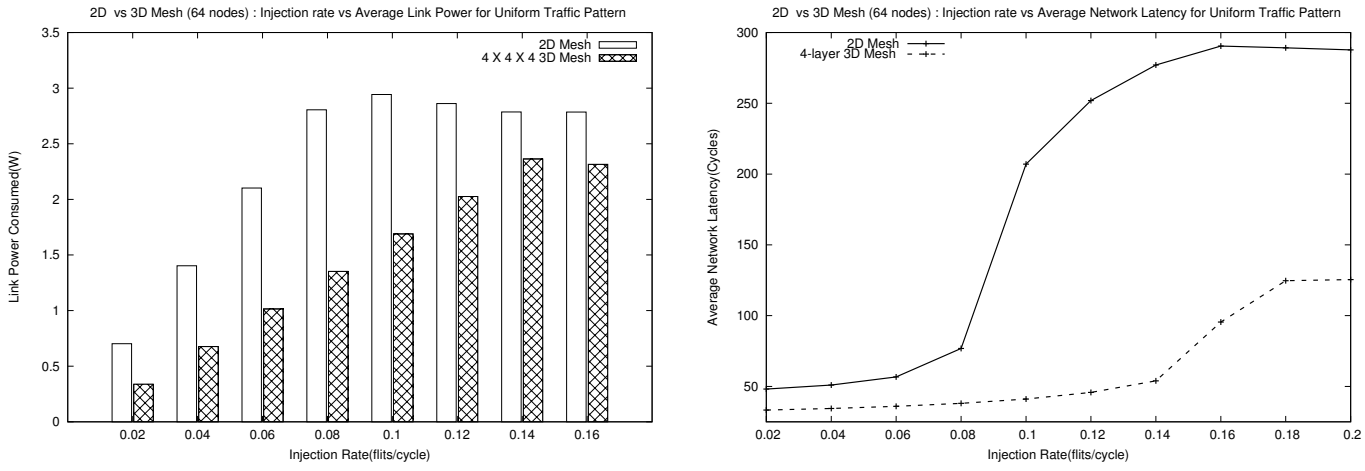
C. Power Analysis of the 3D Mesh Topology

The ideal TSV configuration discussed in Section V was used in the evaluation of power consumption in a 3D 4x4x4 mesh topology. Each vertical link is basically a 128-bit channel. So each link can be logically treated as 128 TSVs transmitting one bit of data each. Fig. 9(a) shows how the Total Average Power increases with increasing packet injection rates.

Since more packets are present in the system and transmitting from one processing element to another takes longer and hence, more power is drawn. The results show that considering TSVs separately gives a more accurate estimation(lower by 13% than unmodified BookSim) of the power drawn by the 3D NoC architecture. This is because TSVs consume lesser power than a standard horizontal link. When scaled to a network containing a large number of TSVs, the reduction in power consumption becomes apparent and the gap becomes larger as more packets are injected through the network.

D. Network Latency Analysis

Fig. 9(b) indicate that Average Packet Latency increases at a much faster rate in 2D networks as compared to 3D networks. This happens because TSVs take much lesser time to send the same amount of data as a horizontal link. These differences are based on horizontal link latency values taken from Orion[16] and the vertical TSV latency derived from the model described in Section IV A. It can be observed from Table V that the latency in the 3D mesh is lower than that of the 2D case by 30-80%.



(a) (b)

Fig. 9. (a)Average total Power Consumption while considering TSVs separately from horizontal interconnects and (b)Average Packet Latency at varying injection rates in 2D and 3D networks, at operating frequency=2.5 GHz and voltage=1.1 V with activity factor(AF) = 0.15

TABLE V
NETWORK LATENCY(NO. OF CLOCK CYCLES) IN 2D AND 3D NETWORKS USING UNIFORM TRAFFIC PATTERNS

Packet Injection rate(flits/cycle)	2D	3D
0.02	48.1253	33.3303
0.04	50.9528	34.4178
0.06	56.7397	35.9283
0.08	76.8547	38.0294
0.08	76.8547	38.0294
0.1	207.035	41.0715
0.12	251.966	45.741
0.14	277.088	53.953
0.16	290.439	95.4649
0.18	289.196	124.675
0.2	287.708	125.492

VII. CONCLUSION AND FUTURE WORK

In this work, the effect of varying multiple TSV parameters on power and performance metrics was investigated. The current work provides better insights on the optimal design 3D TSV design space.

The cycle-accurate BookSim On-Chip network simulator was extended to include the delay and power models of 3D TSVs. We evaluated the latency and power consumed by a 4x4x4 3D Mesh on the extended BookSim version. The results show that the power consumed while transmitting over a 128-bit channel when treating TSVs separately is lower by 13% than the results aggregated by BookSim that assumes equal delays and power consumption for horizontal and vertical links. Also, the average packet latency in the 3D mesh is lower than that of the 2D case by 60-82%.

We plan to use the detailed parameterized 3D TSV models to perform power and performance trade-off studies on other 3D NoC architectures. We are now working on extending these models by including the thermal effects of TSVs in the 3D ICs.

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APPENDIX
ESSENTIAL EQUATIONS FOR CALCULATING POWER CONSUMPTION IN A THROUGH-SILICON VIA

$$C_{\text{ins}} = \pi.\varepsilon_{\text{ins}}.\frac{h_{\text{tsv}}-h_{\text{imd}}}{log(1+(2.t_{\text{ox}}/d_{\text{TSV}}))}$$

$$C_{\text{Bump1}} = \varepsilon_{\text{imd}}.\pi.\frac{(\frac{d_{\text{bump}}}{2})^2-(\frac{d_{\text{TSV}}}{2}+t_{\text{ox}})^2}{h_{\text{imd}}}$$

$$C_{\text{Bump2}} = \varepsilon_{\text{tox}}.\pi.\frac{(\frac{d_{\text{bump}}}{2})^2-(\frac{d_{\text{TSV}}}{2}+t_{\text{ox\_bot}})^2}{t_{\text{ox\_bot}}}$$

$$C_{\text{Underfill}} = \frac{\pi.\varepsilon_{\text{Underfill}}.h_{\text{bump}}}{acosh(\frac{p_{\text{tsv}}}{d_{\text{bump}}})}$$

$$C_{\text{imd}} = \frac{\pi.\varepsilon_{\text{imd}}.h_{\text{imd}}}{acosh(\frac{p_{\text{tsv}}}{d_{\text{tsv}}})}$$

$$C_{\text{Bottom}} = \frac{\pi.\varepsilon_{\text{ox\_bot}}.t_{\text{ox\_bot}}}{acosh(\frac{p_{\text{tsv}}}{d_{\text{tsv}}})}$$

$$G_{\text{Si sub}} = \pi.\sigma_{\text{Si}}.\frac{(h_{\text{TSV}}-h_{\text{imd}})}{acosh(\frac{p_{\text{TSV}}}{d_{\text{TSV}}})}$$

$$C_{\text{Si sub}} = (\frac{\varepsilon_{\text{Si}}}{\sigma_{\text{Si}}}).G_{\text{Si sub}}$$