Simulation Modelling Practice and Theory 96 (2019) 101929

Contents lists available at ScienceDirect

Simulation Modelling Practice and Theory

journal homepage: www.elsevier.com/locate/simpat

Extending BookSim2.0 and HotSpot6.0 for power, performance and thermal evaluation of 3D NoC architectures

Bheemappa Halavar*, Ujjwal Pasupulety, Basavaraj Talawar

Systems, Parallelization and Architecture Research Lab (SPARK-Lab), National Institute of Technology Karnataka Surathkal, Mangalore, 575025, Karnataka

ARTICLE INFO

Keywords:
3D network-on-chip (3D NoC)
BookSim2.0
HotSpot
Through-silicon via (TSV) power
TSV delay modeling
Design space exploration
Energy Delay Product

ABSTRACT

With the increase in number and complexity of cores and components in Chip-Multiprocessors (CMP) and Systems-on-Chip (SoCs), a highly structured and efficient on-chip communication network is required to achieve high-performance and scalability. Network-on-Chip (NoC) has emerged as a reliable communication framework in CMPs and SoCs. Many 2-D NoC architectures have been proposed for efficient on-chip communication. Cycle accurate simulators model the functionality and behaviour of NoCs by considering micro-architectural parameters of the underlying components to estimate performance, power and energy characteristics. Employing NoCs in three-dimensional integrated circuits (3D-ICs) can further improve performance, energy efficiency, and scalability characteristics of 3D SoCs and CMPs. Minimal error estimation of energy and performance of NoC components is crucial in architecture trade-off studies. Accurate modeling of re:Horizontal and vertical links by considering micro-architectural and physical characteristics reduces the error in power and performance estimation of 3D NoCs. Additionally, mapping the temperature distribution in a 3D NoC reduces estimation error.

This paper presents the 3D NoC modelling capabilities extended in two existing state-of-the-art simulators, viz., the 2D NoC Simulator - BookSim2.0 and the thermal behaviour simulator - HotSpot6.0. With the extended 3D NoC modules, the simulators can be used for power, performance and thermal measurements through micro-architectural and physical parameters. The major extensions incorporated in BookSim2.0 are: Through Silicon Via power and performance models, 3D topology construction modules, 3D Mesh topology construction using variable *X, Y, Z* radix, tailored routing modules for 3D NoCs. The major extensions incorporated in HotSpot6.0 are: parameterized 2D router floorplan, 3D router floorplan including Through Silicon Vias (TSVs), power and thermal distribution models of 2D and 3D routers.

Using the extended 3D modules, performance (average network latency), and energy efficiency metrics (Energy-Delay Product) of variants of 3D Mesh and 3D Butterfly Fat Tree topologies have been evaluated using synthetic traffic patterns. Results show that the 4-layer 3D Mesh is 2.2 × better than 2-layer 3D Mesh and 4.5 × better than 3D BFT variants in terms of network latency. 3D Mesh variants have the lowest Energy Delay Product (EDP) compared to 3D BFT variants as there is an 80% reduction in link lengths and up to 3 × more TSVs. Another observation is that the EDP of the 4-layer 3D BFT (with transpose traffic) is 1.5 × the EDP of the 4-layer 3D Mesh (with transpose traffic). Further optimizations towards a tailored 3D BFT for transpose traffic could reduce this EDP gap with the 4-layer 3D Mesh. From the 3D NoC heat

* Corresponding author.
E-mail addresses: cs14f06.bheem@nitk.edu.in (B. Halavar), 15it150.ujjwal@nitk.edu.in (U. Pasupulety), basavaraj@nitk.edu.in (B. Talawar).

https://doi.org/10.1016/j.simpat.2019.101929
Received 27 November 2018; Received in revised form 9 April 2019; Accepted 8 May 2019
Available online 09 May 2019
1569-190X/

maps, it was found that the edge routers in the floorplan of the tested 3D Mesh and 3D BFT topologies have the least ambient temperature.

1. Introduction

The interconnection network affects the performance of SoCs and Chip Multiprocessors significantly. High performance SoCs cannot rely on the traditional bus based communication infrastructure due to high power consumption and performance bottlenecks introduced by buses [1]. NoCs have emerged as the reliable, high-performance, energy efficient communication framework in SoCs and CMPs [2]. The building blocks of an NoC are, (a) a crossbar based hardware component to switch incoming data to target output ports called the Router, and (b) data and control transfer medium called links [3]. NoC routers connect processing elements (PEs) and memory elements in a well-defined arrangement called the topology. Accurate power and performance NoC simulators have been indispensable tools for early exploration studies in the design cycle of NoCs. These simulators measure latency, power, energy, energy efficiency, and power-performance metrics that aid a quantitative, well-informed comparison of multiple NoC design points.

Existing simulators have explored various architectural and micro-architectural design parameters at routers level such as router pipeline depth, arbitration techniques, number and size of virtual channels, number and size input/output buffers, bufferless implementations, and switching techniques. At the network level, simulators allow restructuring of the NoC topology, network partitions, node concentrations, redesigning and evaluation of routing algorithms, flow control mechanisms, deadlock detection and avoidance strategies, adaptive and fault tolerance mechanisms. At the link level, the simulators enable designers to evaluate wire width, wire delays, interfaces, deployment of express physical links and serialization strategies [4].

Today, 3-Dimensional Integrated Design (3D-ICs) SoCs serve emerging applications that demand tailored accelerators for high performance and improved energy efficiency [5]. The number of components placed on a standard SoC die has been on the rise over recent years [6]. 3D ICs place components in vertically stacked Silicon layers in a single package. The component redistribution in 3D ICs enables higher performance at competitive energy budgets by allowing greater integration capabilities while lowering the overall wire area, providing greater communication bandwidth, high flexibility, throughput and lower overall communication latencies [7,8].

Typically the 3D ICs are used for Stacking Memory, placing Memory on Processor, Logic on Logic and Heterogeneous Integration [9]. Collection of DRAM dies are stacked with a logic controller at the bottom layer. High Bandwidth Memory (HBM) [10] and Hybrid Memory Cube (HMC) [11] are examples of 3D IC architectures for increased memory bandwidth, power and scalability. Through Silicon Vias (TSVs) provide a communication link for dies in the vertical direction to achieve 3D integration. TSVs are made up of copper or tungsten. TSVs are used for signal communication and power delivery. There are two mechanism for TSV fabrication i.e via-first and via-last [12,13]. TSVs in 3D ICs enable building 3-Dimensional communication infrastructure called the 3D NoCs. Accurate simulation of 3D NoCs requires incorporating power and performance models of TSVs in existing 2D NoC simulators. The state-of-the-art NoC simulators [14–16], while having complete support for 2D NoC architectures and peak power traffic generator [17], do not support configurable, parameterized design and implementation of 3D NoCs. The configuration parameters of current 2D NoC simulators do not allow such link lengths with varying delays to be included in delay calculations. Incorporating delay and power models of TSVs and the inclusion of varying delays in horizontal links improve the accuracy of power and performance measurements of 3D NoC simulators.

The thermal effect in 3D NoCs has become a major concern because it increases total power generated per area, thermal gradient across layers, if cooling is not adequately provided [18]. State of the art 3D IC simulators [19,20] incorporate better thermal models for analysing the thermal effect, but support for thermal analysis for 3D NoC architectures is lacking.

The goal of this work is to extend the NoC simulators to analyze the 3D NoC topologies for accurate power and performance. Our work incorporates vertical interconnect models (TSV delay and power models) into the BookSim2.0 simulator for the evaluation of 3D NoC Mesh and BFT topology variants for uniform and transpose traffic patterns. We have considered accurate wire length by drawing the floorplans of the NoCs. 2D and 3D variants of Mesh and BFT topologies are considered for experimental analysis. The link delay models from ORION3.0 [21] and micro architectural details of TSVs are used in the experiments. Power of the NoC components and accurate link delay with the optimal (number, size) repeaters are calculated using ORION3.0 and TSVs power models.

1.1. Contributions of this work

The BookSim2.0 cycle accurate simulator has a wide range of design space options and is validated against RTL implementation. We extend BookSim2.0 and HotSpot6.0 for evaluating power, performance and thermal behaviour of 3D NoC architectures.

This paper presents an extension to BookSim2.0 and Hotpot simulators to support floorplan-based 3D topologies and TSV power and delay measurements. The extensions enable designers to evaluate the power, performance and thermal effects of 3D NoC architectures. We present a detailed evaluation of 3D NoC Mesh and BFT topologies for power, performance using uniform and transpose traffic patterns. Additionally, using modified floorplans, the thermal profiling on two variants of 3D Mesh and 3D BFT were obtained by using the newly extended HotSpot extension. The main contributions of this work are:

- State-of-the-art TSV power and delay models were incorporated into BookSim2.0 and HotSpot6.0 to enable analysis of power and performance of 3D NoC architectures.

- Implemented a Variable radix Mesh NoC topology generation mechanism in BookSim (uses unequal values for *X, Y* and *Z*). For example, 64 nodes NoCs can be simulated as `4 × 4 × 4` or `4 × 8 × 2` or `8 × 8 × 1` networks.
- Extended HotSpot6.0 for thermal evaluation of 3D NoC architectures by (a) adding configurable router-TSVs elements into the core layer floorplan and (b) augmenting router and TSV power and thermal models.

2. Network-on-chips

Network-on-Chips (NoC) have emerged as a highly structured and efficient on-chip reliable communication framework in CMPs and SoCs to achieve high-performance and scalability.

NoC interconnects the Processing elements (PEs) with the routers and links in a scheme called topology. The basic building blocks of interconnection networks are a topology, routing, flow control, and router. Routing defines how packets have to route from source to destination without the congestion. Flow control helps to control resources such as buffers and bandwidth during traffic flow. Fig. 1 depicts 4 × 4 2D Mesh NoC topology. The PEs generate and consume data and routers are responsible for forwarding data between the PEs. A router is composed of the set of input and output ports, buffers to store the incoming flits, switching matrix connecting the input port to output port and a designated local port to connect to its local PE [22]. The generic microarchitecture of the router shown in Fig. 2.

The data from PEs are divided into packets. The packets are again subdivided into flow control units called flits. Flits are the units of packets on which flow control policies are applied in an NoC. Flits transfer through the RC, VA, SA, ST and LT stages in the router pipeline. The output channel is identified for the head flit in Route Computation (RC) stage. The virtual-channel (VA) allocates the VC for the head flit. Switch allocation (SA) finds the output physical channel and transfers data on output physical channel by switch traversal (ST). Link Traversal (LT). The router pipeline has been extended using techniques such as bypassing [23] to improve NoC performance [24]

2.1. Performance evaluation of 2D and 3D NoCs

The evaluation methodology to compare the performance and characteristics of 2D NoC architectures such as SPIN, Torus, Folded torus, Octagon, BFT has been discussed in [3]. Balfour et al. [25] and Psathakis et al. [4] made comprehensive studies on the internal elements of a router in order to optimize the Energy-Throughput Ratio of NoC architectures. Most of the state-of-the-art studies discuss the performance and area optimisation by considering details of the micro architectural elements. As there is an increase in the cores, the 2D plane has communication overhead due to interconnect length and the area overhead [26]. 3D IC technologies can be adopted to NoC to avoid long interconnect as it stacks multiple dies on a single chip. 3D NoC is the result of NoC and 3D IC technologies to support scaling of cores [27].

2.2. 3D network on chips

Feero et al. [28] have extensively evaluated and analyzed the throughput, latency, and energy dissipation performance in a variety of 3D NoC architectures. Grot et al. [29] also made efforts in understanding how network topologies (such as CMesh) scale with regard to cost, performance, and energy considering the advantages and limitations afforded on a die. The thermal effect of TSVs on these architectures is yet to be investigated. The work by Prabhat et al. [30] explored the Concentrated mesh (CMesh) 3D NoC as a low-cost alternative to the naive 3D Mesh. It efficiently shares on-chip network resources such as buffers and wire bandwidth. This architecture has been considered as a part of our analysis to verify whether there is an improvement in power consumption and thermal behaviour.

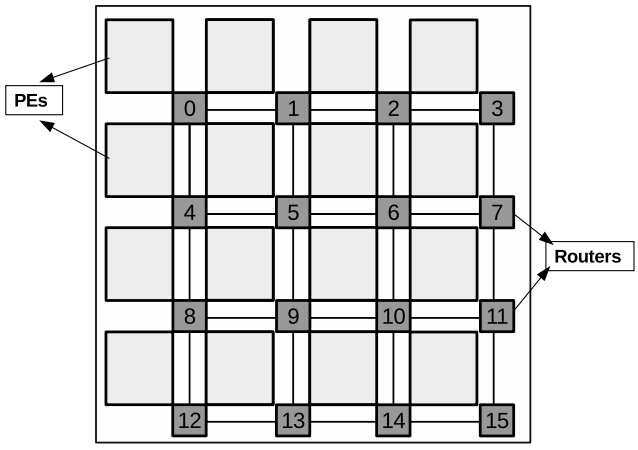

Fig. 1. 4 × 4 NoC Mesh topology. Each PE connects to on router. One router connects to North, East, South and West neighbours using links.

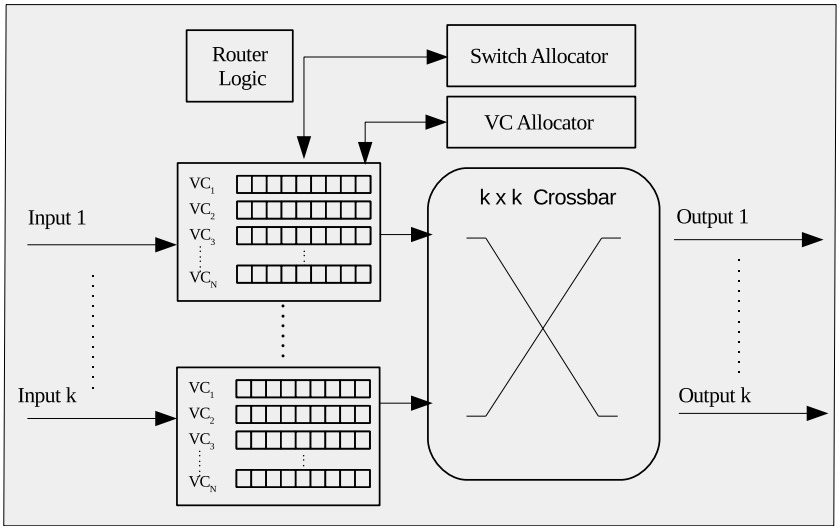

Fig. 2. Generic Kinput, Koutput router microarchitecture. Each input port has n Virtual Channels. Output port for data is chosen by the Router Logic. Switching mechanism is implemented by SA and VC- Allocator block [3].

In [31], proposed 3D-HiCIT (Hierarchical Crossbar-based Interconnection Topology) NoC whose scalability and performance is compared with other hierarchical topologies. 3D-HiCIT reduces the average latency up to 50% and 45% compared to the 3D-BFT and 3D-SPIN respectively.

In [32], to address the power and performance issue in 3D NoC Bus Hybrid architecture, the authors have proposed an ultra-optimized hybridization scheme call LastZ allowing optimized inter-layer communication. Area, power, and performance improvements of 10% compared to 3D NoC-Bus Hybrid Mesh architecture.

Based on 3D NoC partitioning, two different variants are generated namely 3D Stacked Mesh NoC and 3D Stacked Hexagonal NoC. The performance of these two NoC topology is analyzed by comparing them with the Stacked 2D Mesh and 3D Mesh NoC. Due to the significance of the wire delay effect of 3D NoC architectures, using partitioning shows better performance than 3D Mesh NoC [33]. Most of the state of art 3D NoC topologies are evaluated with in house simulators. None of the work address considering the TSV models as a base to the evaluation of 3D NoC topologies to get accurate performance. The next section discusses the state-of-the-art about the different NoC simulators.

3. NoC Simulators

Jiang et al. [14] presented BookSim2.0, a cycle-accurate simulator for NoCs. BookSim2.0 offers a large set of configurable NoC parameters such as topology, routing algorithm, flow control, traffic and injection rate. BookSim2.0 results are validated against the RTL implementation of the NoC router for accuracy. NIRGAM [34] is a modular SystemC based simulator supporting for 2D mesh and

Table 1
Comparison of state of art simulators and the modified simulators.

Tools	Design space exploration								Results			
	General NoC design features					3D NoC design space features				Latency	Power	Area
	2D topology	Network	Router components	Buffer space	Link analysis	3D topology	TSVs	Floorplan model	Thermal design	Latency behaviour	Power	Area
Acces Noxim [35]	Yes	Yes	Yes		Yes	Yes	No	No	No	Yes	Yes	No
Orion [21]	No	No	Yes	Yes	Yes	No	No	No	No	No	Yes	Yes
Nirgam [34]	Yes	yes	Yes	Yes	No	No	Yes	Yes	Yes	No	Yes	Yes
Dsent [37]	No	No	Yes	Yes	Yes	No	No	No	No	Yes	Yes	
Garnet [15]	Yes	Yes	Yes	Yes	No	No	No	No	No	Yes	Yes	No
WormSim [36]	Yes	Yes	Yes	Yes	No	No	No	No	No	No	Yes	No
NoCTweak [16]	Yes	yes	Yes	Yes	No	No	No	No	No	Yes	Yes	No
BookSim2.0 [14]	Yes	Yes	Yes	Yes	No	Yes	No	No	No	Yes	yes	No

torus NoC architectures. Access Noxim [35] is another open source SystemC based, configurable, cycle-accurate NoC simulator which allows analysing the performance and power conventional wires. It also simulates the power performance and thermal of 3D NoC Mesh topology. GARNET [15] is an NoC simulator incorporated in the GEM5 full system simulator. GARNET models micro architectural detail of the router and buffers. Worm_sim [36] is cycle accurate simulator for evaluating performance and communication energy of 2D NoC architecture. NoCTweak [16] is a highly parametrizable NoC simulator for early exploration of performance and energy efficiency NoCs. The simulator has been developed in SystemC, which allows a wide range of configurations to be applied on the NoC platform under simulation. ORION2.0 [21] includes power and area model to estimate the accurate power and area of interconnection network routers accurately. These results can be used to get effective NoC design space exploration in the early phases. DSENT [37] is an area and power model tool which also considers same microarchitectural models from ORION3.0 and it is used for rapid design space exploration of the electrical and opto-electrical network.

The NoC simulators can be compared based on their coverage, configuration parameters and metrics measured. Most on-chip simulators consider a static wire length or constant delay during communications. However, the length and the delay of NoCs link vary according to the floorplan of the NoC. Table 1 compares the design space approaches of the state-of-art simulators with the modified simulator (modified BookSim2.0).

BookSim2.0 contains detailed models of all network elements with router microarchitecture. BookSim2.0 is widely used NoC simulators for its flexibility and accuracy. However, BookSim2.0 does not supports variable configuration of the link delays for irregular topologies, BookSim2.0 also lacks support for TSV delays based 3D NoC simulation. Hence we consider the BookSim2.0 for extension for 3D NoC architecture.

3.1. BookSim2.0 NoC simulator

BookSim2.0 is a flexible and a detailed cycle accurate simulator designed for NoCs. BookSim2.0 is a parametrized simulator where the internal organization of routers, including the buffers, crossbar, allocators are input to observe the behaviour of desired NoC topology. The simulator offers a large degree of network customization and numerous network component designs. BookSim2.0 provides detailed modelling of networks and routers. BookSim2.0 has been a standard for NoC simulation since its release. It provides a large degree of flexibility and can be used for evaluation of novel network designs [14].

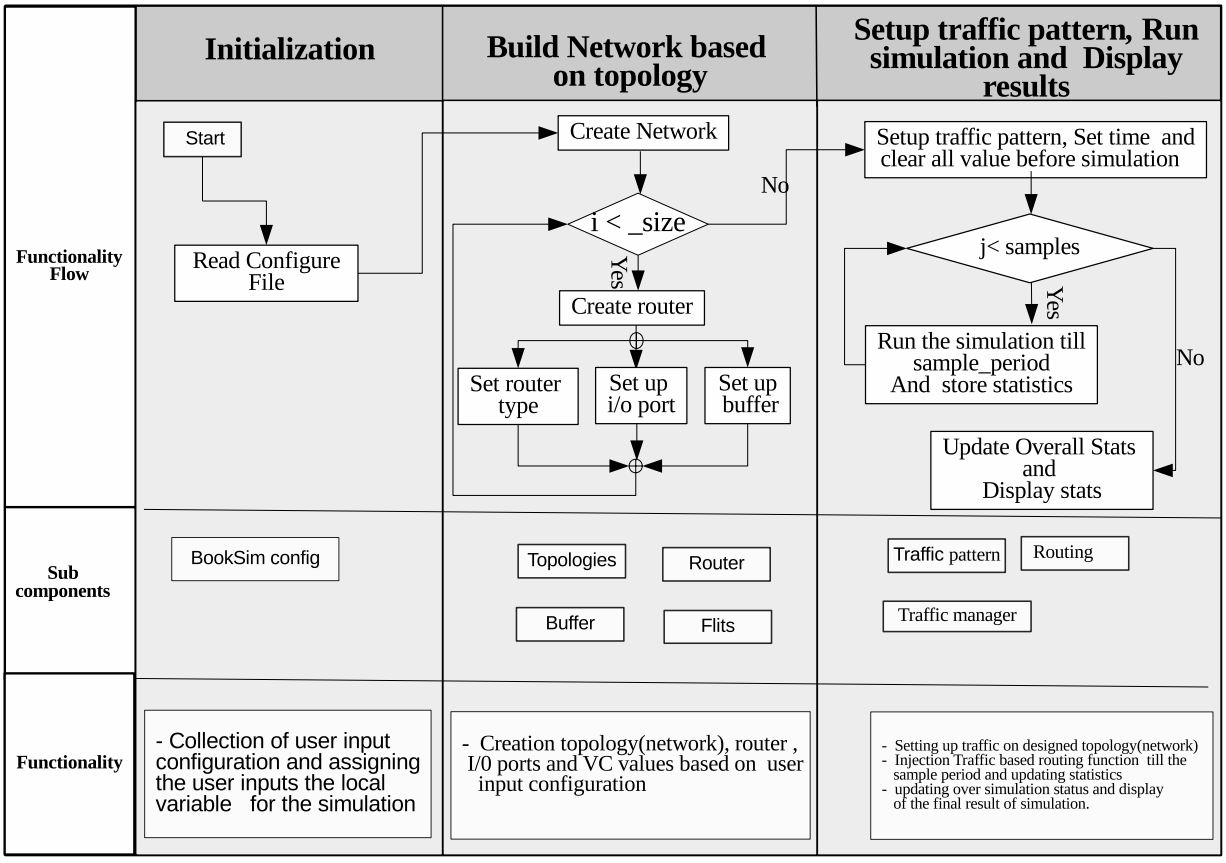

Fig. 3. The overall simulation flow between Modules during the simulation in BookSim2.0.

Fig. 3 depicts the simulation flow and the models involved in each stage. There are three stages in the simulation of a network topology in BookSim2.0, 1. initialization, 2.building network (*network*), and 3. setup traffic and simulation (*trafficmanager*). In the initialization stage, the user configuration is read and assigned to individual simulator parameters, clearing all the previous statistics. The network is built by instantiating and interconnecting routers and channels in a topology defining how these modules are interconnected. All communication between routers occurs through `send` and `receive` functions. The `trafficmanager` module is responsible for the flow of flits over the network module from source to destination. Based on the supplied configuration parameters such as traffic pattern, packet size, injection rate, etc., the packets are injected into the network and latency measurements are taken. `trafficmanager` collects appropriate statistics, and terminates the simulation based on the user input simulation time.

The `router` module in BookSim2.0 is an input-queued virtual channel, canonical four-stage router pipeline for packet header flits. Pipeline delays are configurable. The NoC traffic can be injected using (a) synthetic traffic modules (b) real-time work load traffic. Arbitrary delays can be assigned to each pipeline stage, and the entire router can be configured to mimic the behaviour of a single cycle router. Multiple subnetworks with different traffic classes to be transported on separate physical networks can be simulated. NoC traffic can be fed using synthetic traffic models or by interfacing with a full-system simulator or by replaying traffic traces. Table 2 depicts the list of input parameter for network, router and simulation with description of each parameter in BookSim2.0.

The BookSim2.0 simulator supports Mesh, Cmesh, Torus and Tree based 2D NoC topologies. We extend the capabilities of BookSim2.0 by (a) incorporating TSV delay models (b) support of creating custom wire 3D lengths in standard topologies (c) 3D Mesh topology with variable radix at each dimensions. This extension enables designers to simulate a variable radix 3D Mesh NoC in BookSim2.0. The TSV models incorporated in BookSim2.0 are presented in the Section 5.2.

3.2. Thermal simulation of 3D ICs

Sridhar et al. [19] developed a new simulator for the compact modelling of liquid cooled 3D-ICs. Kinoshita et al. [38] used ADVENTURECluster, a large-scale parallel computing simulator based on Finite Element Modelling to study the thermal elevation in stacked 3D chips and TSV structure stress in 3D System in Packages based on CAD models. Tain et al. [39] developed a simulation model using Flotherm and equivalent thermal conductivity correlations the measure the performance of doubly stacked 3D IC structures assembled in Quad Flat Packages. Fourmigue et al. [40] proposed a novel, Finite Difference method based algorithm for efficiently computing transient temperatures in liquid-cooled 3D ICs with high accuracy. Lu et al. [41] arrived at simple empirical formulas to model heat generated in TSVs using classical equations on heat conduction. The state of art work and [19] used HotSpot [42] base models and hence we extended the HotSpot6.0 for 3D NoC architecture.

3.3. HotSpot6.0 temperature modelling tool

HotSpot6.0 is a widely used model for studying thermal behaviour at the architecture level [42]. Within a thermal package, HotSpot6.0 considers microarchitecture block details as an equivalent circuit of thermal resistances and capacitances. The sample chip floorplans that have been provided in HotSpot6.0 are based on the Alpha Ev6 processor architecture. The sample 3D test case that is provided in the unmodified version of HotSpot6.0 mentions the dimensions of TSV used and the number of TSVs that make up one logical TSV unit. Currently, it does not consider the router as a significant element in the floorplan of the processor. Fig. 4 shows the overall simulation flow of HotSpot tool. This work extends HotSpot6.0 to simulate the 2D and 3D NoC architecture by adding router-TSVs elements based on the floorplan details.

Table 2
Configuration parameters in BookSim2.0.

Input parameter	Description
Network	
topology	Name of the topology (Mesh, CMesh)
k	Topology radix
n	Network dimension
c	Concentration (No. of PEs per router)
Router options	
router	Router type (input queue)
in_ports	Number of input ports in router
out_ports	Number of output ports in router
num_vcs	Total number of Virtual Channel per port
vc_buf_size	Buffer size per Virtual Channel (VC)
routing_function	The name of the routing function (XY,DOR)
Simulation parameters	
traffic patterns	Type of traffic in network (uniform, transpose, bit-compliment, tornado)
packet_size	Size of packets in Flits
sim_type	Latency and throughput simulation type
warmup_periods	Number of samples periods to warm-up the simulation
sample_period	Total Number of measurements cycles
sim_count	Number of simulations to perform

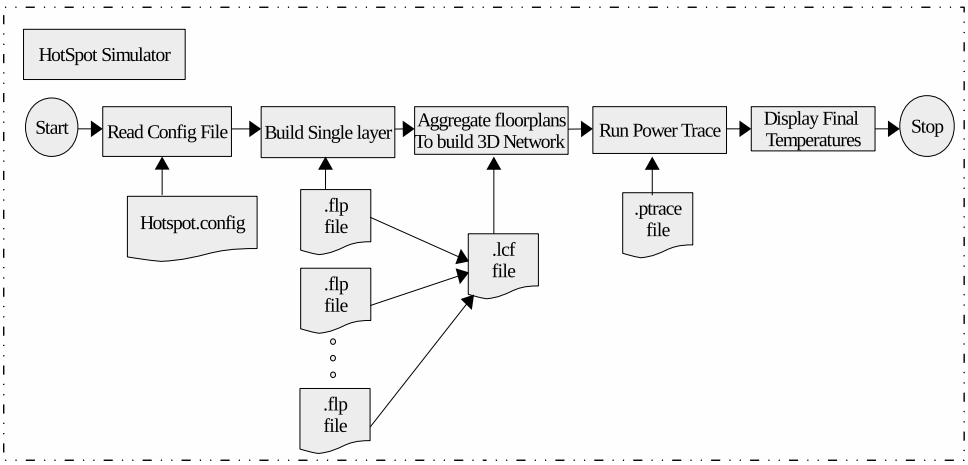

Fig. 4. HotSpot6.0 thermal simulation flow chart for thermal analysis.

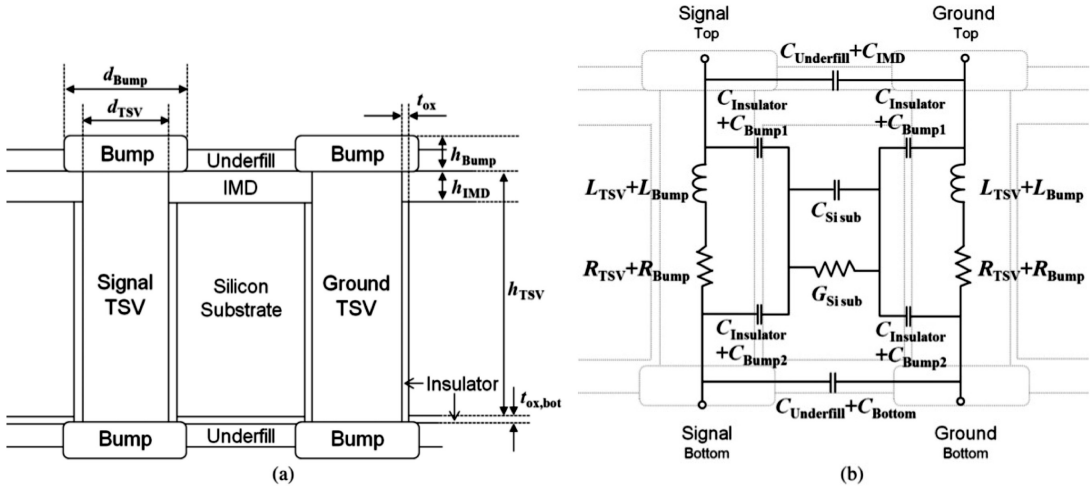

Fig. 5. (a) Structure of a signal TSV and a ground TSV with bumps with the via-last process and their structural parameters, and (b) the proposed scalable electrical model with labelled components [50].

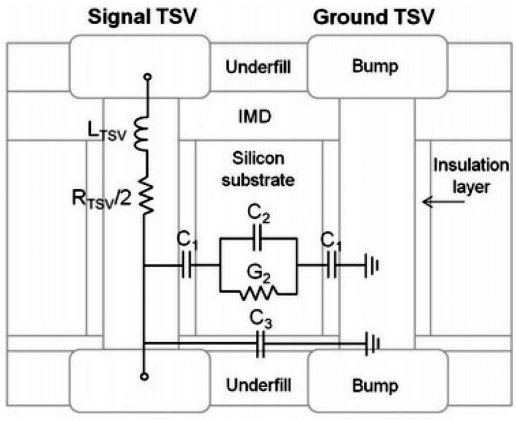

Fig. 6. Logical layout of the TSV electrical model considered in the dynamic power model. [13].

4. TSV delay and power models

4.1. TSV delay models

Weerasekara et al. [43] modelled TSVs in a compact manner by deriving reduced electrical circuit models for isolated and bundled structures. Their model took into account the coupling capacitance, resistance and inductance between the vias and their effect on the overall delay. However, the numerical data furnished only provided values for self and coupling capacitance of a 3 × 3 TSV bundle. You et al. [44] characterized TSV using an approximate ring oscillator model where the Driver resistance and TSV capacitance are the main contributors to the propagation delay. Ahmed et al. [45] recently proposed delay aware floorplanning which considers the coupling capacitance between adjacent TSVs (C_{TT}) and between the horizontal wire and TSV (C_{TW}).

For power, Jueping et al. [46] proposed a simple model to estimate TSV capacitance using few microarchitectural parameters and approximation techniques. Bamberg and Garcia-Ortiz [47] described a regression method for energy estimation based on the probability of bits passing through a 3 × 3 submicrometric TSV array.

Kim and Lim [48] modelled the RC parasitics of a TSV as a 3D interconnect along with buffers which add a non-trivial area overhead. However, their model does not consider physical parameters of the TSV such as its length, diameter and separation from other TSVs. Also the delay of the buffer element is equal to 70 ps, which is very high to be acceptable in a 3D NoC. Khalil et al. [49] made use of dimensional analysis to create a light-weight, high fidelity model that takes three parameters, namely TSV length, radius and pitch. We chose to incorporate Khalil's model due to its simplicity and agreement with simulations using electromagnetic field solvers and the lossy transmission line circuit model.

4.2. TSVs power model

Kim et al. [50] proposed an RLGC model considering multiple physical parameters of the via to determine the capacitance of a single TSV, which is necessary in order to derive the power it consumes under a given operating frequency and voltage. Their work was extended in [13] by devising a equation to calculate the power consumed using the TSV values from previous work and have also considered the Activity Factor which is a measure of the amount of work done by the underlying chip interconnects. This model considers more microarchitectural details, hence we consider it for accurate estimation of dynamic power of TSVs as vertical interconnects in 3D NoCs. Fig. 5(a) shows the each pair of TSV is made up of a signal and ground TSV. The TSV and bump provide a vertical interconnect through the silicon substrate i.e joining the stacked chips. The under fill is the separation between the TSV bumps. The Inter Metal Dielectric layer is the separation between TSVs. The influence of these parasitic components increases as the operating frequency increases.

5. 3D NoC modelling in BookSim2.0 and HotSpot

5.1. Variable radix at X, Y, Z in Mesh topology

BookSim2.0 can construct and simulate a k-array n-cube Mesh, where is k is the radix (number of elements in each dimensions) and n is the number of dimensions. The radix is fixed for all dimensions. For example, `8 × 8` Mesh topology is `8-array, 2-cube` 2D Mesh topology has total number of routers $(k^n) = 64$. An `8 × 8` Mesh can be arranged into other configurations, for eg. `4 × 4 × 4` and `8 × 4 × 2` as a variable radix at each dimension. Creating such topologies requires support for creating custom number of PEsS in the *X, Y,* and *Z* dimensions. Additionally the routing algorithm has to be modified to support variable radix topologies. Variable radix Mesh has been added to the network module. The *ZXY* routing has been implemented in the routing module `Z` as a new parameter is added. Configuration file is modified to receive *X, Y, Z* values. 3D NoC can be simulated using by supplying $n = 3$ (three dimension) in the configuration file. 2D NoCs are simulated with $n = 2$ (two dimension) and `Z=1`. Table 3 shows the list of new parameters and values. To evaluate variable radix mesh topology, `varmesh` to be used as topology name during simulation.

5.2. TSV based delay model and power module in BookSim2.0

Using Khalil's [49] model, we generated an ideal TSV configuration by combining these models by considering safe limits for each parameter to avoid the manufacturer complexity during the fabrication process. The safe limits (Table 4) are taken from [43] and [51].

An analytical model of the propagation delay for TSVs is shown in Algorithm 1. TSV delay is estimated from Height/Length (*l*), Diameter (*d*) and Pitch/ Separation (*s*) and brute-forcing these parameters within the safe limits, We considered that the least power

Table 3
Variable radix Mesh topology details.

Changes made	Description
Parameters	*X, Y, Z*
Topology name	`varmesh`
Route Function	MeshZXY

Table 4
Important physical parameters for TSVs [49] and safe limits values for each parameter. All the parameter are from the Electrical TSV model shown in Fig. 5(a).

Parameter name	Inference	Values [43,51]
d_{TSV}	TSV–Diameter	[20,...,80] μm
p_{TSV}	TSV–Pitch,	[40,...,180] μm
h_{bump}	Bump Height	[5,...,50] μm
d_{bump}	Bump Diameter	[5,...,30] μm
t_{ox}	Oxide Layer Thickness	[0.1,...,1.0] μm
t_{ox_bot}	Bottom Oxide Layer Thickness	1 μm
h_{imd}	Inter-metal dielectric Layer Height	[20,...,100] μm
σ_{Cu}	Conductivity of Copper	5.96×10^{7} S/m
ε_{Si}	Permittivity of Silicon	1.05315×10^{-10} F/m
μ_o	Permeability in free space	$1.25663706 \times 10^{-6}$ H/m
ω	$2\pi f$	

Input: Length (l), Diameter (d_{TSV}) and Pitch/ Separation (s) of TSV
Output: TSV delay
START
r = $d_{tsv}/2$
$l_o = \frac{\sigma_{Cu} * r_2 * \sqrt{(\mu_o/\varepsilon_{si})} * acosh(s/d_{tsv})}{0.693 * (1+0.617 * (r/s))}$
if($l \geq l_o$)
  $delay = \sqrt{(\mu_o/\varepsilon_{si})} * l * l/l_o$
else
  $delay = \sqrt{(\mu_o/\varepsilon_{si})} * l$
END

Algorithm 1. TSV delay estimation.

configuration for this work. The TSV configuration, TSV length 20 μm, diameter 20 μm and pitch 60 μm. These are the default TSV values for the simulator.

The overall power consumption of the NoC can be calculated as sum of the power consumption of link and routers. Power consumption is given by Eq. (1), where P_t is total power, P_r is router power, P_l wire power and P_{tsv} is TSV power consumption.

$$P_t = P_r + P_l + P_{tsv} \quad (1)$$

The router (P_r) and link (P_l) power is calculated dynamical from ORION3.0 [21] power models. Power (P_{tsv}) consumption for each configuration was obtained using Eq. (2) where AF is the activity factor, C_{TSV} is the TSV capacitance calculated from the equation (3) [13].

$$P_{TSV} = AF * C_{TSV} * V^2 * F \quad (1)$$

$$C_{TSV} = C_3 + \frac{C_1 * C_2 * (1 + \sigma_{Cu}/(\varepsilon_{si} * \omega))}{C_1 + 2 * C_2 * (1 + \sigma_{Cu}/(\varepsilon_{si} * \omega))} \quad (2)$$

The electrical model from Fig. 6 shows the highlighting the capacitance of TSVs elements. Table 5 shows the representation of capacitance of each of the TSV elements. C_1 is the insulator capacitance of a TSV, silicon-substrate capacitance is C_2 and C_3 denotes the combined capacitance of the bottom and under fill sections of the TSV.

Table 5
Reduced model parameters (Fig. 6(b)).

Parameter name	Inference
C_{b1}	$C_{ins} + C_{Bump1}$
C_{b2}	$C_{ins} + C_{Bump2}$
C_1	$(C_{b1} * C_{b2}) / (C_{b1} + C_{b2})$
C_2	C_{Sisub}
C_3	$C_{Underfill} + C_{Bottom}$

5.3. TSV-router in HotSpot for 3D NoC architecture

The Alpha Ev6 processor architecture (Fig. 7(a)) is the base configuration provided by HotSpot6.0. It is yet to include support for an element responsible for routing. A router-TSV element of standard dimensions was incorporated into the Ev6 floorplan.

The position of the router in the floorplan of the chip affects the heat distribution across its neighbours. The Data cache and Integer Registers are the primary regions where the temperature is high due to their relatively higher power consumption in each time step.

The router is responsible for pushing packets across the network, an ideal placement would be a region where most of the data reside. Two separate configurations were considered under the 3D Mesh architecture: i) Router at the bottom-right corner (Naive 3D Mesh), next to the Data cache (Fig. 7(b)) and ii) Router shifted to the center (Thermal Aware Mesh architecture), between the Instruction and Data cache (Fig. 7(c)). The data cache tends to be one of the hottest parts of the core. This high temperature from a neighboring element may affect the long-term performance of the router and, effectively the chip as a whole. On the other hand, shifting the router away from the data cache reduces the interfacial contact between the two elements. The effect of thermal conduction from the hotter data cache is lowered. Router shifted away from Data cache Fig. 7(b) considered as Thermal-Aware Mesh architecture.

The Route-TSV based floorplans for 3D NoC Mesh and BFT topologies are shown in Fig. 7(c) and (d). The router is placed in between the Instruction ad Data cache (Fig. 7(c)) to keep it equidistant from both as thermal aware design. For the BFT topology, one router is shared by 4 leaf PEs as shown in Fig. 13 and Fig. 7(d) presents the layout. HotSpot6.0 was extended to provide support for the two mentioned 3D NoC architectures (Mesh and BFT) to analyze the thermal effects.

Router-TSV elements were added to the floorplans in HotSpot. Adding this router element results in the final picture not being a perfect closed figure (rectangle or square). For this, the filler elements were added as dead space (Fig. 7(b) and (c)).

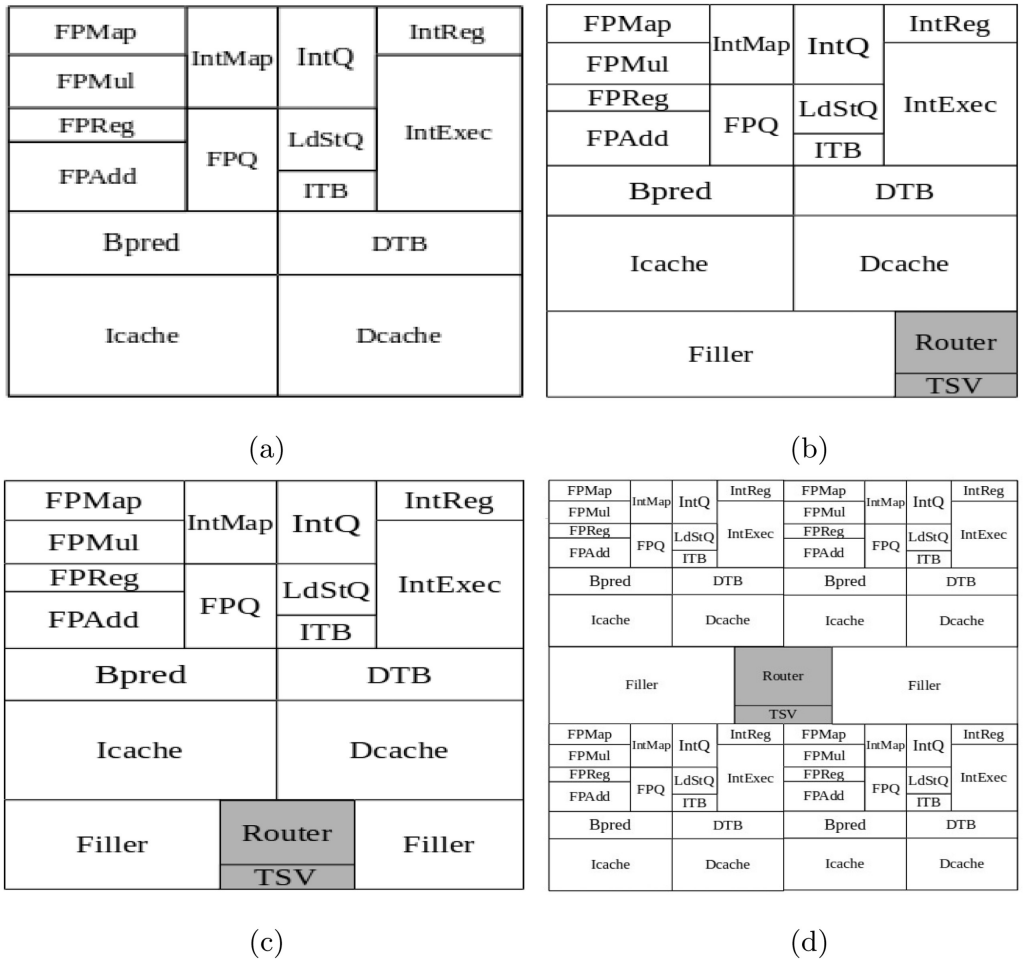

Fig. 7. Logical representations of (a) Default Alpha Ev6 processor layout in HotSpot6.0. (b) Modified layout with router next to the Data cache (Mesh topology). (c) Modified layout with router shifted away from the Data cache (Thermal Aware Mesh architecture). (d) One router shared between 4 cores (not to scale) for BFT architecture.

The process of generating floorplan and power trace files for both 3D Mesh and 3D BFT NoC architectures was automated using scripts which take a small number of parameters (Fig. 8). Power trace files contain the power consumed by every element in the NoC floorplan at each time step. In our experiments, power values for 100 time steps were generated from the existing power trace files in HotSpot6.0 based on the SPEC CPU2000 Benchmark [52]. Corresponding components on all cores consume the same power in each time step. All the layers are arranged in the layer configuration file.

The 3D NoC power models were added to both BookSim2.0 and HotSpot6.0 simulators. Fig. 9 shows the overall modified framework which was used for analysis of the power, performance and thermal behaviour of the 3D NoC architecture with accurate interconnect delay and power models.

6. Analysis of 3D NoC topology variants

The extended version of BookSim2.0 has been used to evaluate 2-layer and 4-layer 3D Mesh and BFT topology variants. In this section details of simulating and analysing the topologies presented.

6.1. General procedure to add new topologies

New topologies are added into BookSim2.0 through these steps:

- Create the topology and store the file `topo.cpp and topo.hpp` at network directory and add the topology name in `network.cpp` file to use the topology in configuration file during the simulation.
- New routing methods can be added in `routefunc.cpp` file with route function name as `topology_rout_name` and add `rout_name` in the beginning of the file to select in configuration file during the topology simulation
- The traffic and flow of simulation can be tracked through `trafficmanger.cpp` to make necessary changes.

Table 6 depicts the new list of files, function and parameters added to the simulator for 3D Mesh and BFT NoC architectures.

6.2. Mesh topology

The floorplan consists of a system with a tiled Chip Multiprocessor consisting of 64 Sun-SPARC cores [53] and area of core

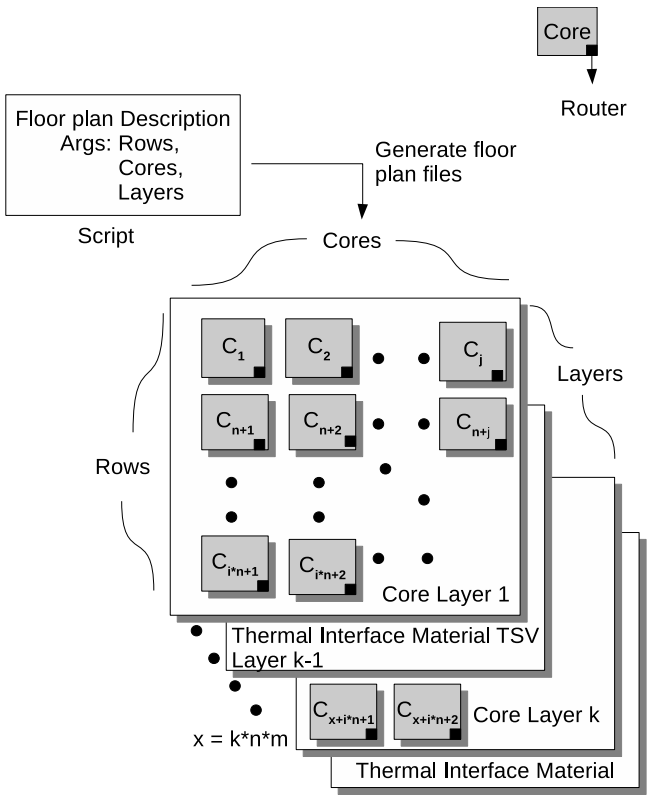

Fig. 8. The automated floorplans generation in HotSpot for 3D NoC architecture.

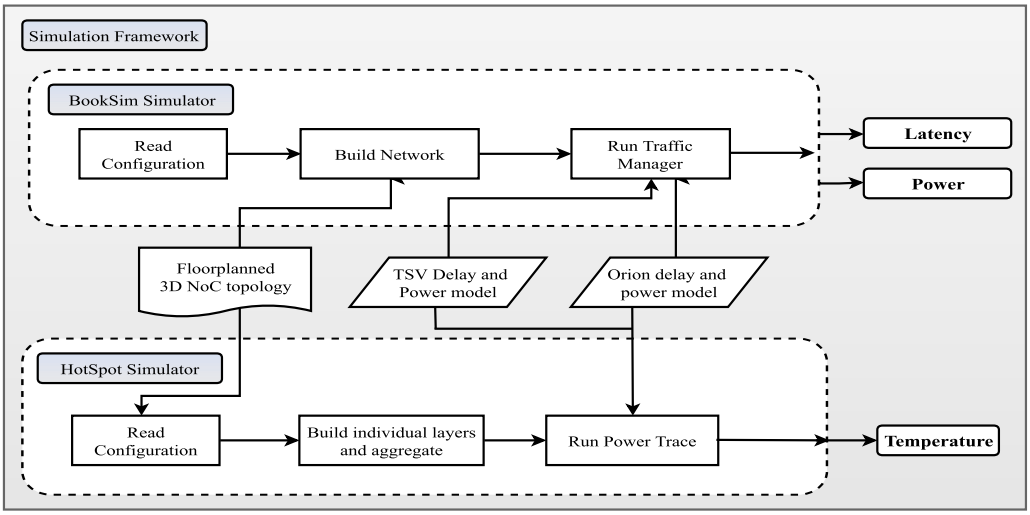

Fig. 9. The over all modified simulation framework for power, performance, thermal behaviour of 3D NoC architecture.

Table 6
The detail of modification to BookSim2.0 for 3D NoC topology.

Input parameter	Description
List Files added/modified	
TSV.hpp, TSV.cpp	Detailed TSV power and Delay model which checks the valid TSV configuration
varmesh.hpp and varmesh.cpp	Mesh topology with variable radix at *X, Y, Z* dimensions
flbft.hpp and flbft.cpp	To evaluate 2D BFT topology
bft2l.hpp and bft2l.cpp	To evaluate 2-layer 3D BFT topology
bft4l.hpp and bft4l.cpp	To evaluate 4-layer 3D BFT topology
New functions	
valid_tsv (h,r,p)	checks the TSV configuration is within safe-limits.
get_lpTSV ()	returns low power TSV configuration within safe-limits
get_least _area_TSV	returns TSV configuration which has lowest area
_xLeftNode (node, dim)	returns the left node in *X* dimension
_xRightNode (node, dim)	returns the left node in *X* dimension
_yLeftNode (node, dim)	returns the left node in *Y* dimension
_yRightNode (node, dim)	returns the right node in *Y* dimension
_zLeftNode (node, dim)	returns the left node in *Z* dimension
_zRightNode (node, dim)	returns the right node in *Z* dimension
link_trace ()	returns the details of links utilization (horizontal and vertical) in topologies
New parameters	
TSV Type	Type of TSV (Currently its signal and ground TSV)
TSV Diameter	Diameter of TSV ((μm))
TSV Pitch	Distance between two TSV (μm)
TSV Height	Height of TSV (μm)
_x	Radix at *X* dimension (No. of router in *X* dimension)
_y	Radix at *Y* dimension (No. of router in *Y* dimension)
_z	Radix at *Z* dimension (No. of router in *Z* dimension)
HL1-HL4	Four different horizontal link latencies
VL1,VL2	Two different vertical link latencies

Table 7
Parameters used in designing the floorplan.

Clock frequency (GHz)	PEs area (mm^2)	4-port router area (mm^2)	5-port router area (mm^2)	6-port router area (mm^2)	7-port router area (mm^2)	Channel size (bit)	TSV delay (Clock cycle)
2.5	3.4	0.47098	0.598509	0.729954	0.865314	64	1

3.4 mm^2. Router area is estimated from ORION3.0 [21]. The values of the micro-architectural parameters used are shown in Table 7.

Fig. 10 shows the floorplan of a `8 × 8` 2D Mesh network consisting of 64 routers. This configuration is simulated in BookSim2.0 simulator by considering accurate wire delay (`HL1 = 4`) for the horizontal length of 1.8 mm.

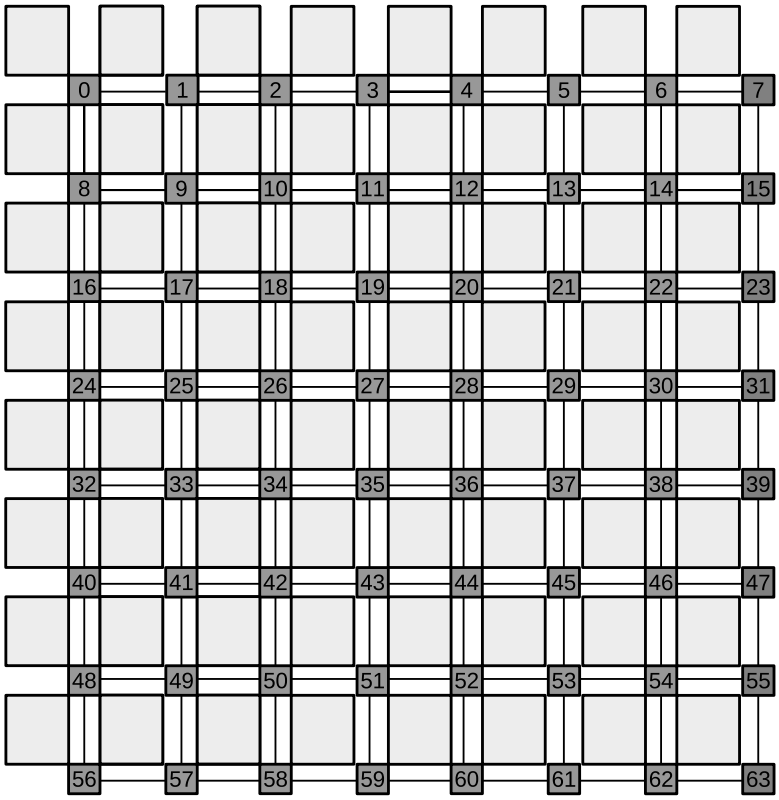

Fig. 10. 8 × 8 2D Mesh with 4 PEs.

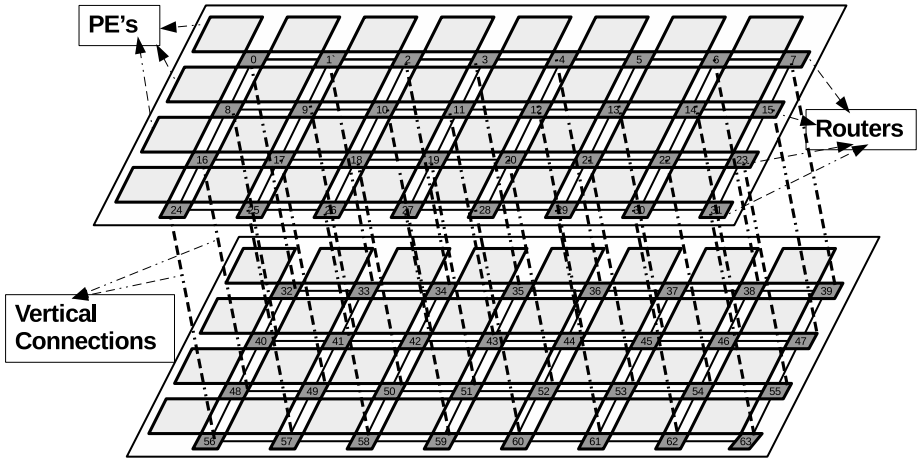

Fig. 11. Floorplan of 8 × 4 × 2 3D Mesh with two stacked layers connected using TSVs.

`8 × 4 × 2` (Fig. 11) and `4 × 4 × 4` (Fig. 12) are the two 3D Mesh variants used as case studies for the proposed BookSim2.0 3D extensions. Table 8 shows details about changes made for 2-layer and 4-layer 3D Mesh topology. Horizontal and vertical delays, `HL1 and VL1` are recorded in the configuration file before simulation. Based on the floorplan the link delay are `HL1 = 4 and VL1 = 1`. `mesh2l` and `mesh4l` are the names of the topologies in the configuration file to be used during the simulation.

The ZXY routing in Algorithm 2 is implemented in routfunction.cpp for 2D and 3D Mesh topologies. ZXY routes flit intra layer and then inter layer based on the destination coordinates.

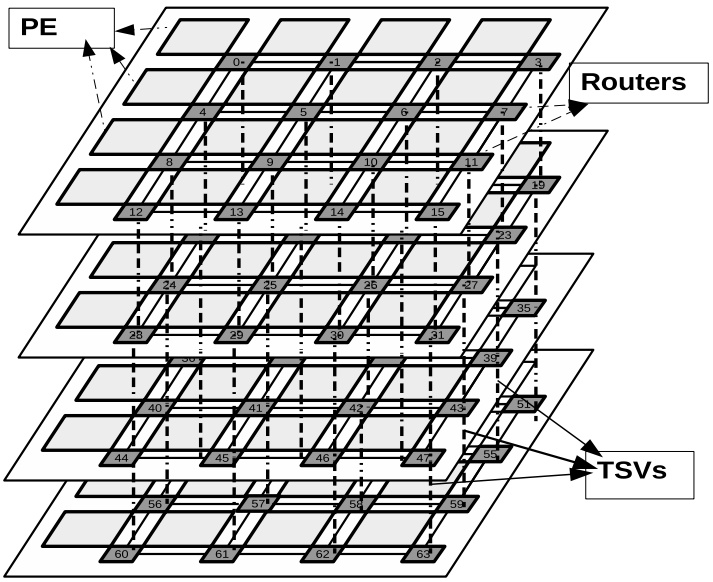

Fig. 12. Floorplan of 4 × 4 × 4 3D Mesh with four stacked layers connected using TSVs.

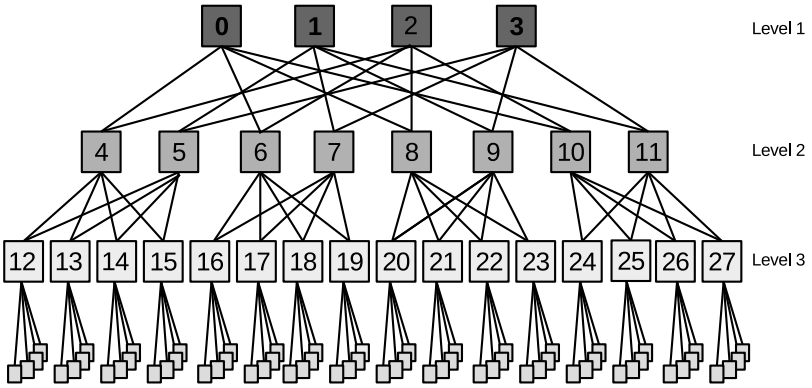

Fig. 13. 64 node BFT topology with three levels. Level 1 is of 4 router, level 2 of 8 routers, level 3 of 16 routers. The leaves are the PEs which are connected to level-3 routers and 4 PE's per router.

Table 8
2-layer and 4-layer 3D Mesh topology details.

Changes made	Description
New parameters	`HL1 and VL1` (Link delays as horizontal (HL) and vertical (VL))
Topology name	`mesh21` (8 × 4 × 2), `mesh21` (4 × 4 × 4)
Route Function	MeshZXY

6.3. 3D BFT topology

In the Butterfly Fat Tree (BFT) topology, PEs are placed at the leaves and routers placed at the top and intermediate levels as shown in Fig. 13. A pair of coordinates is used to label each node, (*L, P*) where L denotes a nodes level and P denotes its position within that level. The PEs have addresses ranging from 0 to ($N - 1$) and BFT has different non-uniform links in each level [54].

Fig. 14(a) shows 2D floorplan of BFT topology. Micro-architectural parameters used for our experiments is shown in Table 7.

From the floorplan, there are five different links lengths. Table 9 shows the details about the changes added to the simulator to simulate a functional 3D BFT topology.

`2-layer 3D BFT`: Starting from the 2D BFT floorplan, level 2 routers are moved towards level 1 to reduce overall link length. Fig. 15 shows the 2-layer 3D BFT which is extended from a 2D BFT. The 2-layer 3D BFT has two stacked layers connected through vertical TSVs. The overall link length is reduced upto 50% in 3D BFT compared to its 2D counterpart. Table 9 shows the details about the changes added to simulator for 2-layer 3D BFT topology.

Input: Current node and *dest* node
Output: Output port from current node to *dest*
if *cur!=dest* **then**
  if *cur and dest are at different plane (Layer)* **then**
    Find_output port in *Z* direction (left or right)
  end
  else if *cur and dest are at same offset of X dimension and are at different Y dimension* **then**
    Find_output port in *Y* direction (left or right)
  end
  else
    Find output port in *X* direction (left or right)
  end
end

Algorithm 2. Routing algorithm for both 2D and 3D (XY and ZXY).

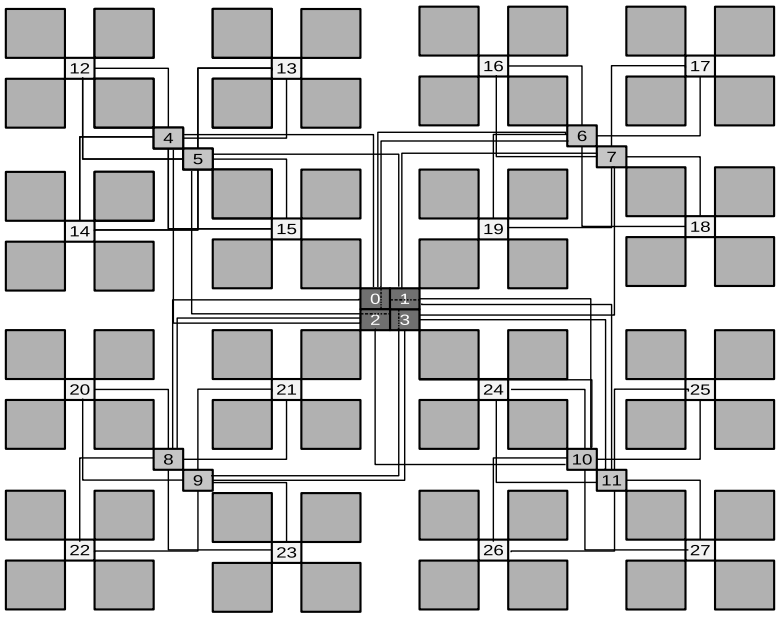

Fig. 14. Floorplan of 2D Mesh with 64 PEs and each PEs are connected routers for inter PEs communication.

Table 9
Floorplan based 2D BFT and 3D BFT variants topology details.

Changes made	2D BFT	2-layer 3D BFT	4-layer 3D BFT
New parameters	HL1-HL4	HL1-HL3	VL1 HL1-HL3, VL1, VL2
Topology name	`flbft`	`bft2l`	`bft4l`
Route function		Nearest Common Ancestor (NCA)	

`4-layer 3D BFT`: Fig. 16 shows a 2-layer 3D BFT modified to 4-layer 3D BFT topology with each layer consisting of 16 PEs. Level 1 routers are placed in between layers to reduce the length of TSVs. Fig. 16(c1) shows the vertical connection between the routers from level 1 to level 2. Table 9 shows the details about the changes added to the simulator for 4-layer 3D BFT topology.

6.3.1. Random and round robin output based deflection routing

Nearest Common Ancestor (NCA) (in Algorithm 3) is implemented in routfunction.cpp for 2D and 3D BFT variants. NCA identifies the minimum and maximum reachable destination at each router and then forwards packets to an appropriate output port of the router.

In BFT topology, there are two upward paths per level, per source and destination pair (from Node 0 to 32, Fig. 17) with an equal number of hops in each path. Hence this allows alternative paths to be chosen to avoid congestion and obtain improved on chip

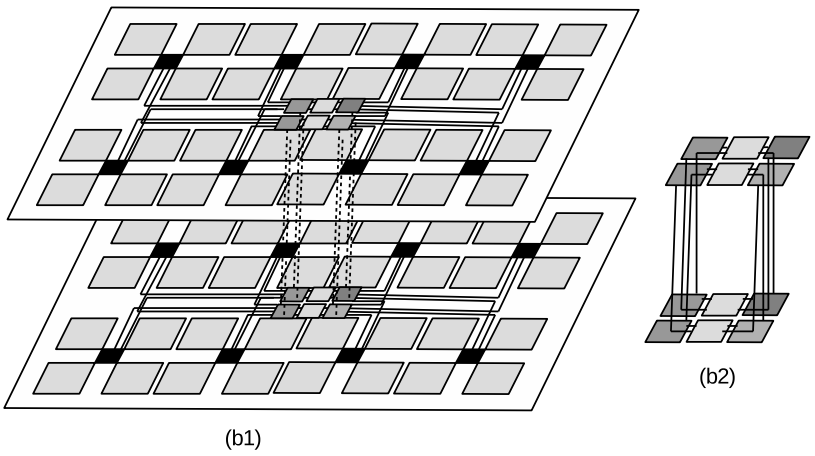

Fig. 15. (b1) 8 × 4 × 2 3D Mesh with two stacked layers connected using TSVs. (b2) Inter-layer connections.

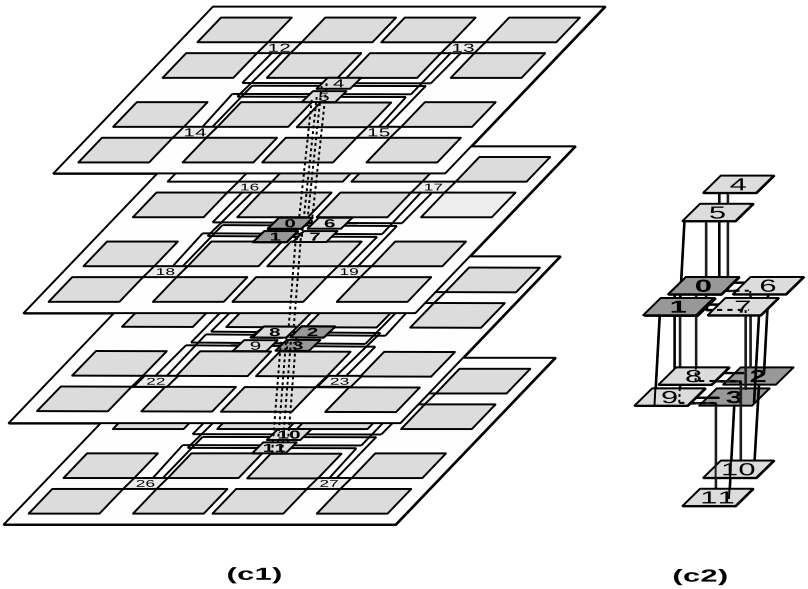

Fig. 16. (c1) 4 × 4 × 4 3D Mesh with four stacked layers connected using TSVs. (c2) Inter-layer connections.

communication. We analyse Random Output Deflection (ROD) and Round Robin Output Deflection (RROD) path selection mechanism in the NCA algorithm (Algorithms 3 and 4).

The ROD routing selection one of two output ports at each level arbitrarily per packet. Fig. 18 depicts the scenario for node 0 to 32 and 3 to 35. ROD routing algorithm presented in Algorithm 4. It can be observed that during random output deflection, there might be chances of selecting the same output port for two different packets which might lead to congestion and increases the communication latency.

RROD select output port in round-robin manner (Fig. 19) while routing packets (Algorithms 3 and 4). Fig. 19 shows a selection of alternative port while routing packets. The RROD Output Deflection shown in Algorithm 4. Our experiments shows that RROD lead to less congestion, better communication latency compared to ROD.

6.4. Link delay analysis of both Mesh and BFT

Link lengths are extracted from the floorplan of the topologies and RC delay models from ORION3.0 [21] are used for estimating the horizontal link delay (ns). The number of cycles per link is calculated for the 2.5 GHz frequency with a voltage of 1.1 V(32 nm Technology). Table 10 shows the details of link length, delay (Clock cycle) and horizontal link counts of both 2D and 3D variants of Mesh, BFT topologies based on the floorplan. The Delay column in Table 10 shows the delays in clock cycles (cc) of respective wire lengths.

```
Input: cur node, flow and dest node
Output: output_port from cur node to dest
if cur!=dest then
    Find the cur node level (nl) and Position of node (rp) in the level ;
    if nl ==zero then
        output_port = dest/16
    end
    else if nl==1 then
        Find Lowest (min) node and maximum (max) node which can reach from cur;
        if dest is in beween max and min then
            out_port= (dest/4)%4;
        end
        else
            out_port=getoutport (flow);
        end
    end
    else
        Find Lowest (min) node and maximum (max) node which can reach from cur;
        if dest is in beween max and min then
            out_port= (dest%4);
        end
        else
            out_port = getoutport(flow);
        end
    end
end
```

Algorithm 3. NCA Routing algorithm for both 2D and 3D BFT.

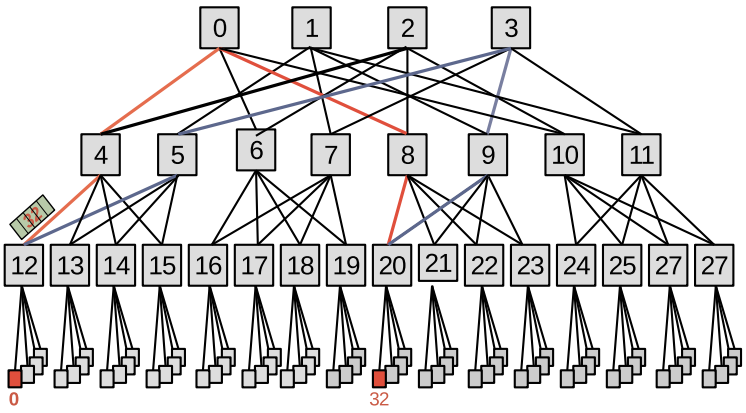

Fig. 17. 2D BFT topology with two path flows from **node 0** to **node 32**.

The Vertical link counts of both Mesh and BFT variants are evaluated and Table 11 shows the vertical links delay (cc), number of vertical connections and number of TSVs count of both BFT and Mesh variants.

Table 12 depicts the total number of resources such as network, number of routers, link details of the 2D and 3D Mesh and BFT variants. From Table 12, the 4-layer 3D Mesh has a reduction in horizontal links from 112 to 96 and there are 48 extra VL compared 2D NoC mesh topology.

7. Experimental setup

The BookSim2.0 simulator was extended to support 3D NoCs by adding (a) TSV delay and power modules, (b) Orion power and delay modules for horizontal links. The HotSpot6.0 thermal analysis tool was extended to support by, (a) adding TSV area and power model, and (b) Router area and Power model. Fig. 9 shows the overall modified simulation framework for power, performance and

Input: Output flow (*flow*)(ROD or RROD)
Output: *output_port*
Function `getoutport(`*flow*`)`**:**

```
/* Random Output Deflection (ROD)                                    */
if flow==ROD then
    out_port=rand ()%2+4;
end
/* Round-Robin Output Deflection (RROD)                              */
else
    if RB==1 then
        out_port=4; RB=0;
    end
    else
        out_port=5; RB=1;
    end
end
return out_port ;
```

Algorithm 4. ROD and RROD routing function in NCA for 2D and 3D BFT topology.

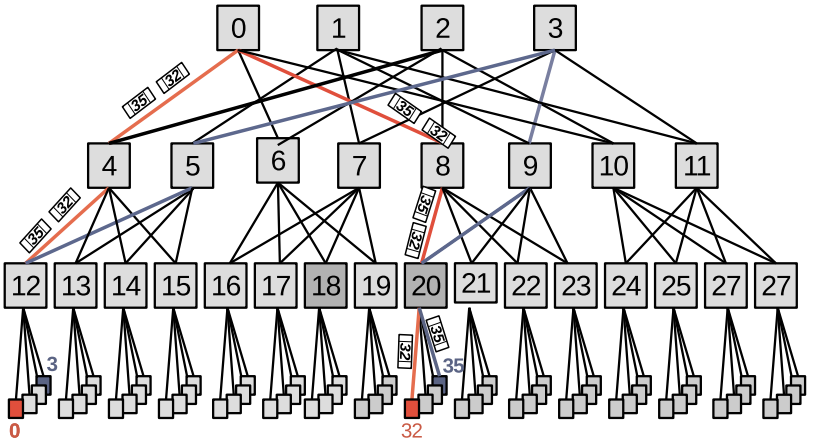

Fig. 18. ROD routing for from **node 0** to **node 32** and **node 3** to **node 35** for 2D BFT topology.

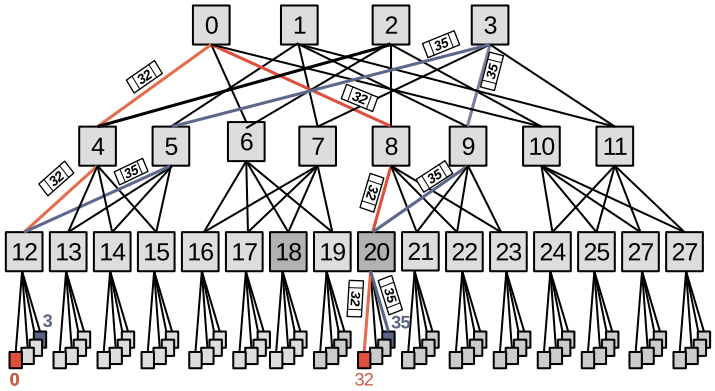

Fig. 19. RROD - from **node 0** to **node 32** and **node 3** to **node 35** for 2D BFT topology.

Table 10
Horizontal link (HL) length and delay (cc) details of 2D and 3D variants of Mesh, BFT. These delays are considered for the simulation.

Topology	Wire (mm)	Delay (clock cycle)	HL (wire) count
2D Mesh	1.844	4	112
2-layer 3D Mesh	1.844	4	108
4-layer 3D Mesh	1.844	4	96
2D BFT	8.825	73	8
	8.342	73	8
	7.859	64	8
	4.654	23	8
	4.171	19	16
2-layer 3D BFT	8.342	73	8
	7.859	64	8
	4.654	23	8
	4.171	19	8
4-layer 3D BFT	4.654	23	14
	4.171	19	14
	Less than 1mm	1	12

Table 11
Vertical Link details of 3D variants of Mesh, BFT each link has 64 TSVs.

	2-layer 3D Mesh	4-layer 3D Mesh	2-layer 3D BFT	4-layer 3D BFT
VL count	32	48	16	8
Number of TSVs	4096	6144	2048	1024
Delay (Clock cycle)	1	1	1	1

Table 12
Total resources in the 2D and 3D variants of Mesh and BFT considered in this work. Network size is 64 PEs. Links are horizontal (HL) and vertical (VL). VC is the number of virtual channels and D is buffer depth per V.

NoC Topology	Network (x/k,y/n,z)			Router (In,Out,VC,D)				Link counts HL,VL	
	X	*Y*	*Z*	No. router	In/Out	VC	D	HL	VL
2-D Mesh	8	8	1	64	5/5	8	7	112	0
2-layer 3D Mesh	8	4	2	64	6/6	8	6	108	32
4-layer 3D Mesh	4	4	4	64	6/6, 7/7	8	6	48	0
2-D BFT	4	3	1	28	4/4, 8/8	8	16	96	48
2-layer 3D BFT	4	3	2	28	4/4, 8/8	8	16	32	16
4-layer 3D BFT	4	3	4	28	4/4, 8/8	8	16	40	8

Table 13
NoC BookSim2.0 parameter for 2D and 3D Mesh and BFT variants.

Input configuration	Input values
Topology	mesh, mesh2l, mesh4l, bft2d, bft2l, bft4l
Size	k = 4, 8 and n = 2, 3
Number of VCs, VC buffer size	8, 12
Routing	xy, xyz, nca, nca_RROD, nca_ROD
Packet size	5
Traffic pattern	Uniform, Transpose
Injection rate	0.02 to 0.20
Sample period	10,000 (cycles)
Simulation count	10

Table 14
Thermal evaluation simulation environment.

Environment variable	Specification
Simulator	HotSpot6.0
Operating frequency	2.5 GHz
Activity factor	0.15
Clock Cycles (cc)	100,000
Topology Simulated	2D, 2-layer and 4-layer 3D Mesh and 3D BFT variants
TSVs per Vertical Link (*TSVL*)	64
Power consumed per TSV (*PCT*)	4.2 μW

thermal behaviour of 3D NoC architectures. In all four 3D variants of Mesh and BFT topologies are implemented in BookSim2.0 as mesh2l, mesh4l, bft2l, bft4l. Link delays are provided as horizontal delay (HL), vertical delay (VL) and TSVs (Height, diameter and pitch) details.

The link delays are configurable and can be varied based on floorplans of the NoCs. By default, HL and VL is 1 clock cycle. Table 13 shows experimental set up in BookSim2.0 simulator. All temperatures are in degree Kelvin (K) and the HotSpot6.0 simulations were run in the environment specified in Table 14.

8. Results

8.1. Average network latency

Average network latency obtained from BookSim2.0 using default link latencies and from floorplan based link latencies are plotted in Fig. 20(a) and (b) for 2D mesh and 2D BFT respectively. Using floorplan based link lengths and corresponding delays in simulation, an increase in average network latency from 19% to 43% is observed. To observe the accurate performance of the NoC architecture, floorplan and accurate delay estimation plays a signification role. An increase in average network latency up to 1.45 × is observed in Mesh and up to 8 × in BFT topology using floorplan derived, accurate link delays in the simulation. BFT topology link length 2.5 × greater than the Mesh, resulting in a larger increase in the average network latency.

8.1.1. Evaluation of ROD and RROD routing (NCA) in BFT topology

Fig. 21 depicts the comparison of latencies of 2-layer 3D BFT topology for random and round robin output deflection routing for uniform and transpose traffic pattern.

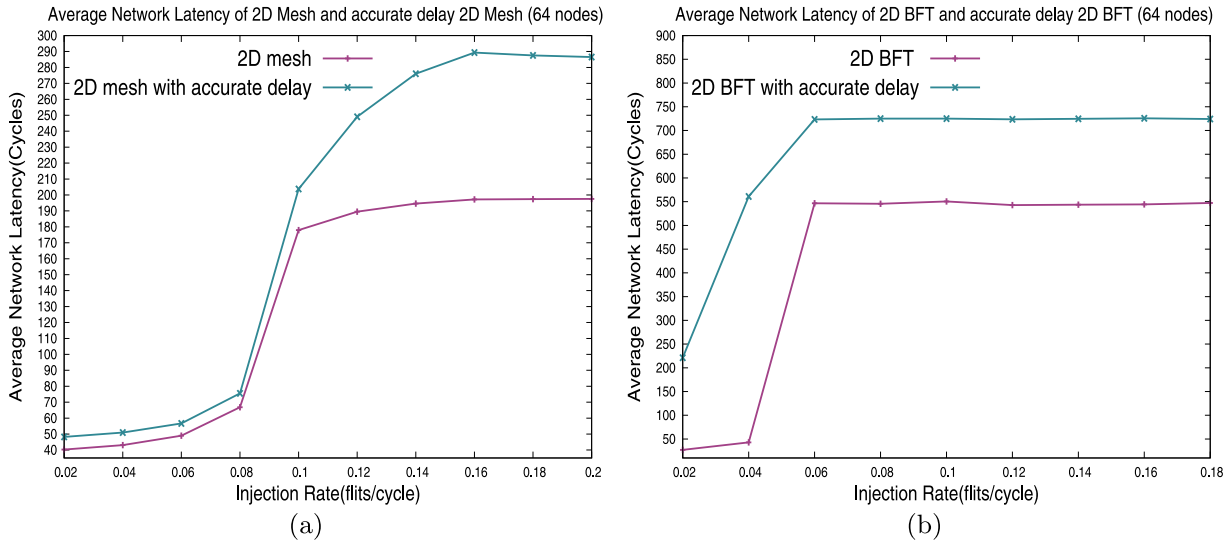

Fig. 20. Average network latency comparison with accurate link delay modelling. (a) 2D Mesh(default link delay) and 2D Mesh with accurate link delay and (b) 2D BFT (default link delay) and 2D BFT with accurate link delay.

In Fig. 21, there is 10–13% increase in the overall network latency for RROD compared to ROD. With RROD, the flow of flits balanced between links which lead to transfer of more flits compared to ROD. RROD routing is selected as the best output path selection for the BFT topology variants compared to ROD routing. Further evaluation, RROD used as output path in 2D and 3D BFT NoC variants.

8.2. Performance evaluation of 3D Mesh and BFT

In Fig. 22, the average network latency comparison of both 2D and 3D variants Mesh and BFT with uniform and transpose traffic patterns is shown. Results are shown for VC = 8 and buffer-depth (D) = 12.

8.2.1. Mesh topology

The Mesh topology shows improved performance on the uniform traffic pattern compared to the transpose traffic pattern for all variants. In Fig. 22(a), the 4-layer 3D Mesh with uniform traffic shows up to 2.3 × improvement over 2D Mesh uniform and up-to 2 × improvement over 2-layer 3D Mesh. The 2-layer 3D Mesh with uniform traffic shows up-to 1.11 × improvement over 2D Mesh for uniform traffic pattern.

The 4-layer 3D Mesh with transpose traffic shows up-to 3 × improvement over 2D Mesh transpose and up-to 3.1 × improvement over 2-layer 3D Mesh transpose. The 2-layer 3D Mesh with transpose traffic shows up-to 1.1 × improvement over 2D Mesh for

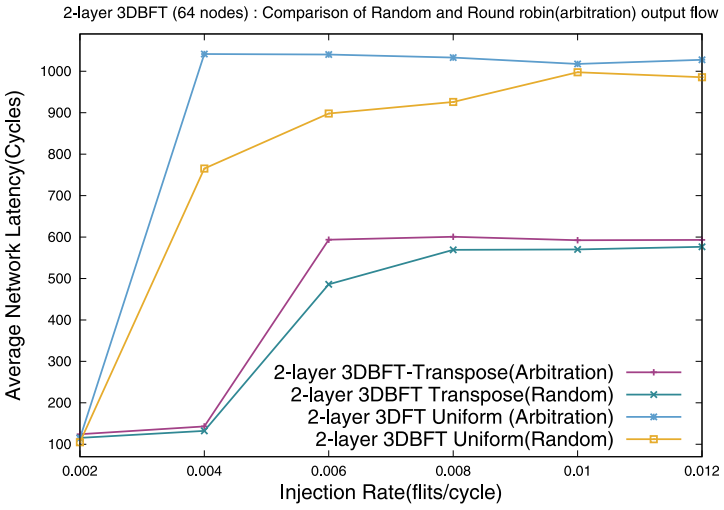

Fig. 21. Average network latency comparison for 2-layer 3D BFT for RROD and ROD routing.

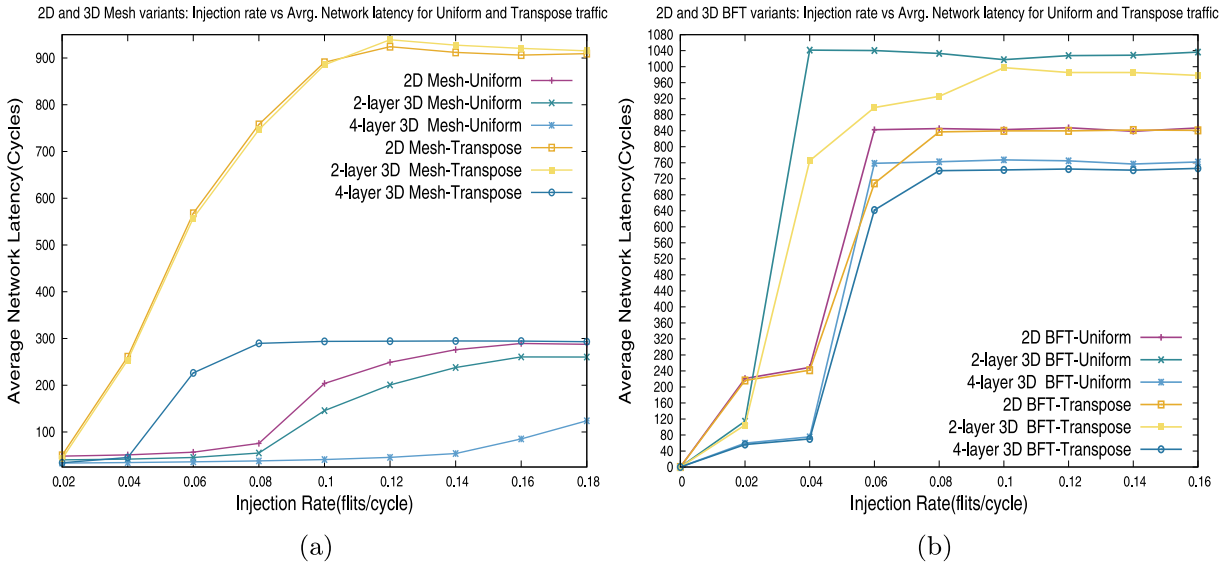

Fig. 22. Average network latency comparison between uniform and transpose traffic pattern for 2D and 3D variants of (a) Mesh topology and (b) BFT topology.

transpose traffic pattern. The improved performance in 3D Mesh is due to the replacement of horizontal wires with the TSVs (wire delay is 4 × greater than the TSV delay) and additional vertical connection (Table 10).

The 4-layer 3D Mesh with uniform traffic shows up-to 2.3 × improvement over 4-layer 3D Mesh transpose traffic pattern. The 2-layer 3D Mesh with uniform traffic shows up-to 3.4 × improvement over 2-layer 3D Mesh transpose traffic pattern. The uniform distribution of the packets in uniform traffic results in lower contention in the links compared to the transpose traffic pattern.

8.2.2. BFT topology

The BFT topology shows improved performance on transpose traffic pattern compared to uniform traffic pattern for all variants. In Fig. 22(b), the 4-layer 3D BFT with uniform traffic shows up-to 1.2 × improvement over 2D BFT uniform and up to 1.3 × improvement over 2-layer 3D BFT uniform.

The 4-layer 3D BFT with transpose traffic shows up-to 1.2 × improvement over 2D BFT transpose and up-to 1.3 × improvement over 2-layer 3D BFT transpose. In the 3D BFT topology, average delays of wire delay are 21 × than the TSV delay as shown in Table 10, and eight horizontal wire links are converted to TSV links.

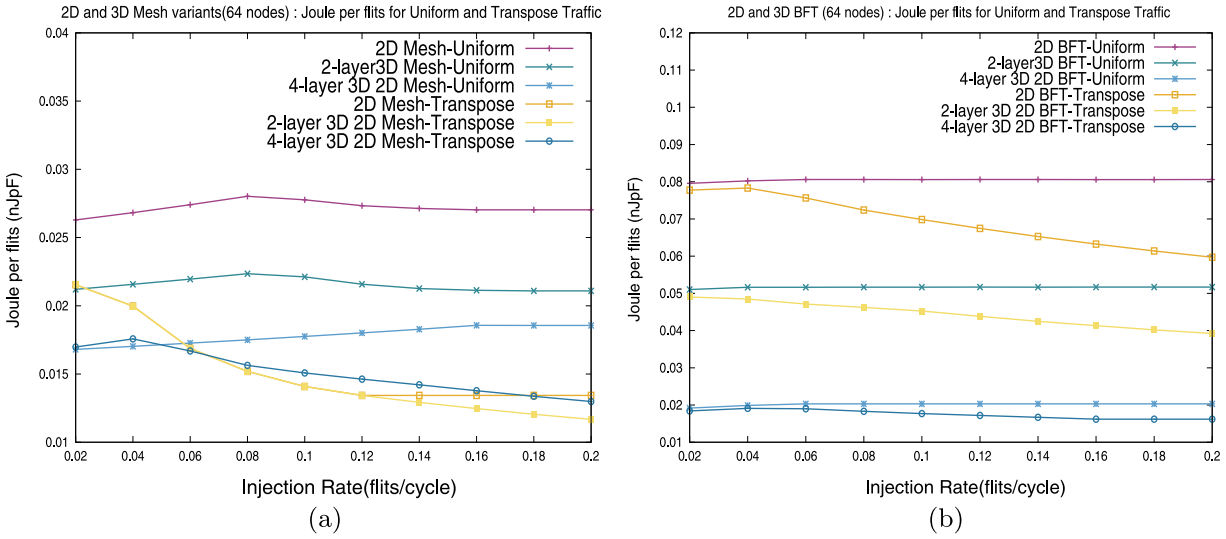

Fig. 23. (a) Average EPF for 2D and 3D Mesh topology variants. (b) Average EPF for 2D and 3D BFT topology variants.

The 4-layer 3D BFT with transpose traffic shows up-to 1.1 × improvement over 4-layer 3D BFT uniform traffic pattern. The 2-layer 3D BFT with transpose traffic shows up-to 1.2 × improvement over 2-layer 3D BFT uniform traffic pattern. The transpose traffic results in better localised traffic compared to the uniform traffic pattern.

8.3. Average energy per flit (EPF)

The Fig. 23(a) and (b) depicts the average energy consumption per flit of 2D and 3D variants of Mesh and BFT topologies.

Fig. 23(a) depicts the EPF of 2D and 3D Mesh topology variants for both uniform and transpose traffic. The 4-layer Mesh topology has average 15% reduction of EPF compared to 2-layer 3D Mesh and 35% reduction in 2D Mesh for both uniform and transpose traffic. The 2D and 3D Mesh variants with a uniform has a 10% reduction of EPF compared to transpose traffic.

Fig. 23(b) shows the EPF of 2D and 3D BFT topology variants for both uniform and transpose traffic. The 4-layer BFT topology has average 40% reduction of EPF compared to 2-layer 3D BFT and 75% reduction in 2D BFT for both uniform and transpose traffic. The 2D and 3D BFT variants with transpose traffic has a 15% reduction of EPF compared to uniform traffic.

8.4. Energy Delay Product (EDP)

Fig. 24 shows the EDP of 2D and 3D variants of Mesh and BFT topology for uniform and transpose traffic patterns. The EDP is the product of average network latency and average Energy per flit.

Fig. 24(a) depicts EDP of all variants for uniform traffic pattern. The 4-layer 3D Mesh has lowest EDP, 2-layer 3D Mesh is second lowest EDP compared to other variants. Fig. 24(b) shows the EDP of all variants for transpose traffic pattern. The 4-layer 3D Mesh has the lowest EDP, and 2-layer 3D Mesh is second the lowest EDP compared to other variants.

3D Mesh variants have the lowest EDP compared to 3D BFT variants as there is 80% reduction link lengths and up to 3 × larger TSVs in 3D Mesh. We also observe that the 4-layer 3D BFT transpose has nearest EDP (1.5 ×) compared to 4-layer 3D Mesh transpose and by optimising 4-layer 3D BFT design we can achieve a lower EDP than 4-layer 3D Mesh. The 2D BFT has the largest EDP because of delay of links, and the horizontal links are up to 2.5 × larger compared to other variants as discussed link delay analysis.

8.5. Thermal behaviour

8.5.1. Mesh topology

Fig. 25(a), (b), (c) and (d) shows the thermal behaviour of 2D, 2-layer, 4-layer 3D and comparison of 2D and 3D variants () Mesh topology respectively. The temperature variation in the 2D Mesh topology follows the pattern of high temperature at middle router compared to corner routers, i.e, 8 × 8 Mesh topology two routers and last router at every *X* radix shows the drop in temperature up to 7 ˚C compared to centre routers. 2-layer 3D Mesh shows the also follows the pattern of corner router with low temperature. The layer 1 routers (router 0 to 31) shows an average of 8 ˚C more than the layer 0 routers (router 32 to 64). Within each layer the corner routers show less temperature compared to centre routers.

Similarly, the 4-layer 3D Mesh also follows the pattern of corner router with low temperature and the layers which are near to heat sink have a lower temperature. The layer 4 routers (router 0 to 15) shows average 20 ˚C more than the layer 0 routers (router 48

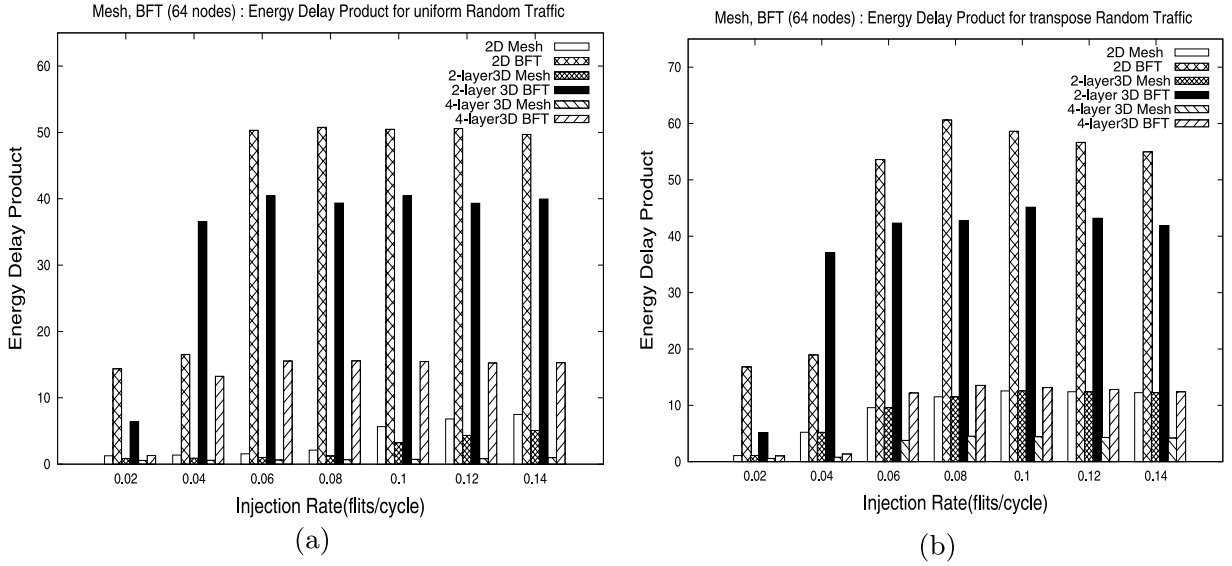

Fig. 24. EDP of 2D and 3D Mesh and BFT topology for (a) uniform traffic pattern (b) transpose traffic pattern.

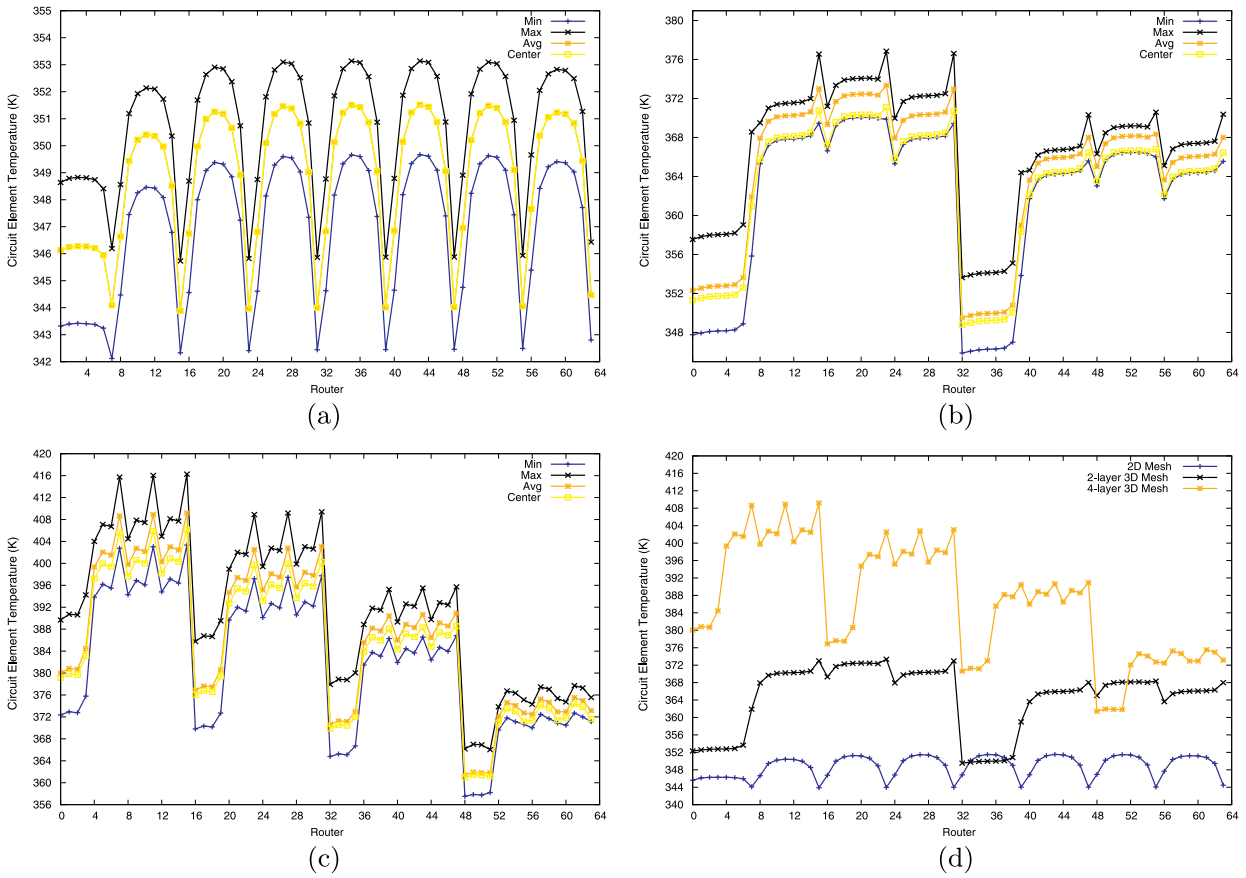

Fig. 25. Thermal behaviour of (a) 2D mesh topology (b) 2-layer 3D Mesh topology (c) 4-layer Mesh topology. (d) Average thermal behaviour comparison of 2D and 3D Mesh variants.

to 63). Within each layer, the corner routers show less temperature compared to centre routers. The layers which are away from sink have higher temperature. The good packaging will help in controlling the thermal affect on the NoC architecture.

8.5.2. BFT topology

Fig. 26(a), (b), (c) and (d) shows the thermal behaviour of 2D, 2-layer, 4-layer 3D and comparison of 2D and 3D BFT variants respectively. The temperature variation in the 2D BFT topology follows different pattern compared to the Mesh topology. It is because of the routers organization in BFT. The pattern is, routers which connects to core have high temperature and it is because the routers are concentrated (C = 4). The Level Zero routers have low temperature compared to higher levels in BFT topology.

The 2-layer 3D BFT also follows the pattern of 2D BFT topology lower level router with low temperature. The layer 1 routers show an average of 5 ˚C more than the layer 0 routers. Similarly, the 4-layer 3D BFT also follows the pattern of corner router with low temperature and the layer which are near to heat sink with lower temperature. The layers which are away from sink have a higher temperature and the good packaging will help in controlling the thermal effect on the NoC architecture.

A general observation in all of the evaluated architectures is that the outer cores show lower temperature values than those located at the centre. This is because heat dissipation is better at the edge of the floorplan, but the elements in the middle of the die are surrounded from all sides. The only way heat can sink is through the Thermal Interface Material below. Hence the elements at the centre get hotter than the boundary elements over the duration of the simulation. It is evident that the routers in the naive setup register higher maximum and minimum temperatures as compared to the proposed thermally aware floorplan.

8.5.3. Router power analysis

The Power dissipation of routers is observed under uniform traffic pattern for 2D BFT and 2D Mesh topologies at 0.01 injection rate. The runtime power trace generated from the BookSim2.0 simulator is fed to the HotSpot6.0 to generate the heat dissipation of the NoC architecture. Router's power (mW) utilisation are generated from 1000 cc to 10,000 cc with an interval of 2000 cc for Mesh topology (64-router) and BFT topology (28-routers).

Table 15 shows the average of the router powers at each level of the BFT topology. From Table 15, it is observed that the level-1 routers have higher power usage, level 2 has the least power and level-0 medium power usage. Considering nodes 0–3 as sources, the

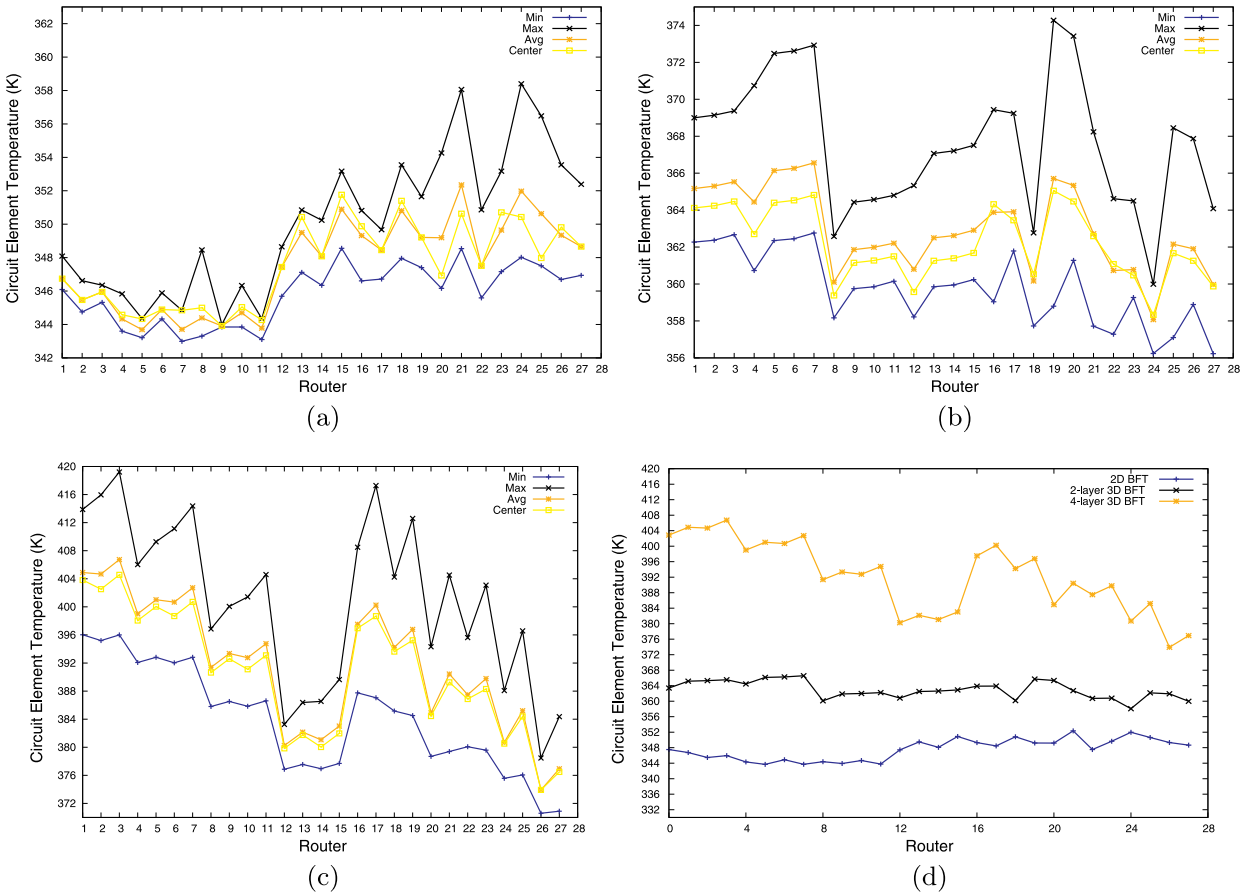

Fig. 26. Thermal behaviour of (a) 2D BFT topology (b) 2-layer 3D BFT topology (c) 4-layer 3D BFT topology. (d) Average thermal behaviour comparison of 2D and 3D Mesh variants.

Table 15
Average of router's power of each level of 2D BFT topology with interval of 2000cc.

	Average power (mW)		
	Level 0 (R0 to R3)	Level 1 (R4 to R11)	Level 2 (R12 to R27)
2000	30.6977	31.6374	30.1445
4000	29.1810	29.9401	29.1623
6000	28.6611	29.3543	28.8281
8000	28.4031	29.0668	28.6686
10,000	28.2285	28.8741	28.5811

Table 16
Average of router's power utilisation of peripheral routers (each side) and middle routers of Mesh topology.

	Left column	Top row	Right column	Bottom row	Middle routers
2000	10.2467725	10.1711225	10.2551875	10.3467875	10.4728
4000	9.91973375	9.90385875	9.94620125	9.96809875	10.0679
6000	9.82164625	9.81374	9.82349875	9.8513875	9.9296
8000	9.768175	9.76879	9.77123	9.78861125	9.8547
10,000	9.745785	9.7327425	9.73685625	9.75603625	9.8098

level-1 routers transfer packets from 4 to 63 (up to 90%). The level-0 routers transfer packets from 32 to 63 (up to 50%). Level 2 routers transfer packets for 0–3 (only 10%).

Table 16 depicts the average power utilisation of peripheral routers on each (left, top, right, bottom) side and middle routers of Mesh topology.

The evolution of overall power consumed by the routers throughout the simulation was observed. The overall thermal dissipation is identical for all routers in each time interval. The thermal dissipation of the routers is influenced by the adjoining PE temperature. The power and temperature of the PEs overshadow the small variation in router power and thermal behaviour. Further, the router power values indicate that the traffic is uniformly distributed in the Mesh (unlike the BFT).

9. Conclusion

This paper presents the 3D NoC modelling capabilities extended in two existing state-of-the-art simulators, viz., the 2D NoC Simulator - BookSim2.0 and the thermal behaviour simulator - HotSpot6.0. With the extended 3D NoC modules, the simulators can be used for power, performance and thermal measurements through micro-architectural and physical parameters. The presented simulator can be used to observe the Power, Performance and Thermal behaviour of behaviours of 3D NoC architecture. The TSV based power and delay model is incorporated into BookSim2.0 to estimate accurate power and performance of 3D NoC architectures. The support of irregular (Variable radix at each dimension (*X, Y, Z*)) 3D Mesh and BFT topology variants with ZXY routing and nearest common ancestor respectively. The HotSpot6.0 simulator is extended support for the inclusion of a router-TSV circuit element as a part of the 3D NoC floorplan for thermal behaviour.

Using the extended 3D modules, performance (average network latency), and energy efficiency metrics (Energy-Delay Product) of variants of 3D Mesh and 3D Butterfly Fat Tree topologies have been evaluated using synthetic traffic patterns. Results of our experiments show that the average network latency of a 4-layer 3D Mesh is 25–54% lesser than its 2D counterpart for injection rates of up to 0.18 for uniform traffic pattern. 4-layer 3D Mesh has on-chip communication performance up to 4.5 × than 4-layer 3D BFT. The Mesh performs better than BFT topology due to its topology structure i.e. links, router input ports, buffers are larger in the 2D and 3D Mesh compared to 2D and 3D BFT. 3D Mesh variants have the lowest EDP compared to 3D BFT variants as there is 80% reduction link lengths and up to 3 larger TSVs in 3D Mesh. We also observe that the 4-layer 3D BFT transpose has nearest EDP (1.5 ×) compared to 4-layer 3D Mesh transpose and by optimising 4-layer 3D BFT design we can achieve the lower EDP than 4-layer 3D Mesh. The thermal behaviour of the 4-layer Mesh and BFT topologies show that the corner routers have lower temperatures. In both, the layer closer to the heat sink are cooler by 20 ˚C compared to the other layers.

References

[1] L. Benini, G.D. Micheli, Networks on chips: a new SoC paradigm, Computer 35 (1) (2002) 70–78.
[2] W. Dally, B. Towles, Principles and Practices of Interconnection Networks, Morgan Kaufmann, San Francisco, 2004.
[3] P.P. Pande, C. Grecu, M. Jones, A. Ivanov, R. Saleh, Performance evaluation and design trade-offs for network-on-chip interconnect architectures, IEEE Trans. Comput. 54 (8) (2005) 1025–1040.
[4] A. Psathakis, V. Papaefstathiou, N. Chrysos, F. Chaix, E. Vasilakis, D. Pnevmatikatos, M. Katevenis, A systematic evaluation of emerging mesh-like CMP NoCs, 2015 ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS), (2015), pp. 159–170.
[5] A.B. Ahmed, A.B. Abdallah, K. Kuroda, Architecture and design of efficient 3D network-on-chip (3D NoC) for custom multicore SoC, 2010 International Conference on Broadband, Wireless Computing, Communication and Applications, (2010), pp. 67–73.
[6] J.U. Knickerbocker, P.S. Andry, B. Dang, R.R. Horton, M.J. Interrante, C.S. Patel, R.J. Polastre, K. Sakuma, R. Sirdeshmukh, E.J. Sprogis, S.M. Sri-Jayantha, A.M. Stephens, A.W. Topol, C.K. Tsang, B.C. Webb, S.L. Wright, Three-dimensional silicon integration, IBM J. Res. Dev. 52 (6) (2008) 553–569.
[7] Y. Xie, G.H. Loh, B. Black, K. Bernstein, Design space exploration for 3D architectures, J. Emerg. Technol. Comput. Syst. 2 (2) (2006) 65–103.
[8] A.M. Ralimani, P. Liljeberg, J. Plosila, H. Tenhunen, BBVC-3D-NoC: an efficient 3D NoC architecture using bidirectional bisynchronous vertical channels, Proc. - IEEE Annu. Symp. VLSI, ISVLSI 2010, (2010), pp. 452–453.
[9] V. Kumar, A. Naeemi, An overview of 3D integrated circuits, 2017 IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization for RF, Microwave, and Terahertz Applications (NEMO), (2017), pp. 311–313.
[10] D.U. Lee, K.W. Kim, K.W. Kim, H. Kim, J.Y. Kim, Y.J. Park, J.H. Kim, D.S. Kim, H.B. Park, J.W. Shin, J.H. Cho, K.H. Kwon, M.J. Kim, J. Lee, K.W. Park, B. Chung, S. Hong, 25.2 A 1.2V 8Gb 8-channel 128Gb/s high-bandwidth memory (HBM) stacked DRAM with effective microbump I/O test methods using 29nm process and TSV, 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), (2014), pp. 432–433.
[11] J. Jeddeloh, B. Keeth, Hybrid memory cube new dram architecture increases density and performance, 2012 Symposium on VLSI Technology (VLSIT), (2012), pp. 87–88.
[12] Y. Xie, C. Bao, C. Serafy, T. Lu, A. Srivastava, M. Tehranipoor, Security and vulnerability implications of 3D ICS, IEEE Trans. Multi-Scale Comput. Syst. 2 (2) (2016) 108–122.
[13] J.K. et al., I/o power estimation and analysis of high-speed channels in through-silicon via (TSV)-based 3D IC, 19th Topical Meeting on Electrical Performance of Electronic Packaging and Systems, (2010), pp. 41–44.
[14] N. Jiang, D.U. Becker, G. Michelogiannakis, J. Balfour, B. Towles, D.E. Shaw, J.-H. Kim, W.J. Dally, A detailed and flexible cycle-accurate network-on-chip simulator, Performance Analysis of Systems and Software (ISPASS), 2013 IEEE International Symposium on, IEEE, 2013, pp. 86–96.
[15] N. Agarwal, T. Krishna, L. Peh, N.K. Jha, GARNET: a detailed on-chip network model inside a full-system simulator, IEEE International Symposium on Performance Analysis of Systems and Software, ISPASS 2009, April 26–28, 2009, Boston, Massachusetts, USA, Proceedings, (2009), pp. 33–42.
[16] A.T. Tran, B. Baas, NoCTweak: A Highly Parameterizable Simulator for Early Exploration of Performance and Energy of Networks On-Chip, Technical Report ECE-VCL-2012-2, VLSI Computation Lab, ECE Department, University of California, Davis, 2012.
[17] I. Seitanidis, C. Nicopoulos, G. Dimitrakopoulos, Automatic generation of peak-power traffic for networks-on-chip, IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. 38 (1) (2019) 96–108.
[18] S. Swarup, S.X. Tan, Z. Liu, Thermal characterization of TSV based 3D stacked ICS, 2012 IEEE 21st Conference on Electrical Performance of Electronic Packaging and Systems, (2012), pp. 335–338.
[19] A. Sridhar, A. Vincenzi, D. Atienza, T. Brunschwiler, 3D-ICE: a compact thermal model for early-stage design of liquid-cooled ICS, IEEE Trans. Comput. 63 (10) (2014) 2576–2589.
[20] W. Huang, K. Skadron, S. Gurumurthi, R.J. Ribando, M.R. Stan, Differentiating the roles of IR measurement and simulation for power and temperature-aware design, 2009 IEEE International Symposium on Performance Analysis of Systems and Software, (2009), pp. 1–10.
[21] A.B. Kahng, B. Li, L.-S. Peh, K. Samadi, Orion 2.0: a fast and accurate NoC power and area model for early-stage design space exploration, Proceedings of the Conference on Design, Automation and Test in Europe, European Design and Automation Association, 2009, pp. 423–428.
[22] W.J. Dally, B. Towles, Route packets, not wires: on-chip interconnection networks, Design Automation Conference, 2001. Proceedings, IEEE, 2001, pp. 684–689.
[23] A. Psarras, I. Seitanidis, C. Nicopoulos, G. Dimitrakopoulos, Shortpath: a network-on-chip router with fine-grained pipeline bypassing, IEEE Trans. Comput. 65 (10) (2016) 3136–3147.

[24] G. Dimitrakopoulos, A. Psarras, I. Seitanidis, Microarchitecture of Network-on-chip Routers, 1025 Springer, 2015.
[25] J.D. Balfour, W.J. Dally, Design tradeoffs for tiled CMP on-chip networks, Proceedings of the 20th Annual International Conference on Supercomputing, ICS 2006, Cairns, Queensland, Australia, June 28–July 01, 2006, (2006), pp. 187–198.
[26] V.F. Pavlidis, E.G. Friedman, 3-D topologies for networks-on-chip, IEEE Trans. Very Large Scale Integr. Syst. 15 (10) (2007) 1081–1090.
[27] Y. Qian, Z. Lu, W. Dou, From 2D to 3D NoCs: a case study on worst-case communication performance, Proceedings of the 2009 International Conference on Computer-Aided Design, ICCAD '09, ACM, New York, NY, USA, 2009, pp. 555–562.
[28] B.S. Feero, P.P. Pande, Networks-on-chip in a three-dimensional environment: a performance evaluation, IEEE Trans. Comput. 58 (1) (2009) 32–45.
[29] B. Grot, J. Hestness, S.W. Keckler, O. Mutlu, Express cube topologies for on-chip interconnects, 2009 IEEE 15th International Symposium on High Performance Computer Architecture, (2009), pp. 163–174.
[30] P. Kumar, Y. Pan, J. Kim, G. Memik, A. Choudhary, Exploring concentration and channel slicing in on-chip network router, 2009 3rd ACM/IEEE International Symposium on Networks-on-Chip, (2009), pp. 276–285.
[31] M. Debora, P. Max, K. Marcio, C. Luigi, S. Altamiro, Performance evaluation of hierarchical NoC topologies for stacked 3D ICs, Proc. - IEEE Int. Symp. Circuits Syst. 2015-July, (2015), pp. 1961–1964.
[32] A.M. Rahmani, P. Liljeberg, J. Plosila, H. Tenhunen, Lastz: An ultra optimized 3D networks-on-chip architecture, 2011 14th Euromicro Conference on Digital System Design, (2011), pp. 173–180.
[33] M.H. Jabbar, D. Houzet, O. Hammami, Impact of 3D IC on NoC topologies: a wire delay consideration, 2013 Euromicro Conference on Digital System Design, (2013), pp. 68–72.
[34] L. Jain, B. Al-Hashimi, M. Gaur, V. Laxmi, A. Narayanan, Nirgam: a simulator for NoC interconnect routing and application modeling, Design, Automation and Test in Europe Conference, (2007), pp. 16–20.
[35] V. Catania, A. Mineo, S. Monteleone, M. Palesi, D. Patti, Cycle-accurate network on chip simulation with noxim, ACM Trans. Model. Comput. Simul. 27 (1) (2016) 4:1–4:25.
[36] U.Y. Ogras, R. Marculescu, "it's a small world after all": NoC performance optimization via long-range link insertion, IEEE Trans. Very Large Scale Integr. Syst. 14 (7) (2006) 693–706.
[37] C. Sun, C.H.O. Chen, G. Kurian, L. Wei, J. Miller, A. Agarwal, L.S. Peh, V. Stojanovic, DSENT - a tool connecting emerging photonics with electronics for opto-electronic networks-on-chip modeling, 2012 IEEE/ACM Sixth International Symposium on Networks-on-Chip, (2012), pp. 201–210.
[38] T. Kinoshita, T. Kawakami, T. Sugiura, K. Matsumoto, S. Kohara, Y. Orii, Thermal stress simulation for 3D sip with TSV structure under unsteady thermal loads, ASME 2015 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems collocated with the ASME 2015 13th International Conference on Nanochannels, Microchannels, and Minichannels, American Society of Mechanical Engineers, 2015. V002T02A020–V002T02A020
[39] R.-M. Tain, M.-J. Dai, Y.-L. Chao, S.-L. Li, H.-C. Chien, S.-T. Wu, W. Li, W.-C. Lo, Thermal performance of 3D IC package with embedded TSVs, Trans. Jpn. Inst. Electron. Packag. 5 (1) (2012) 75–84.
[40] A. Fourmigue, G. Beltrame, G. Nicolescu, Efficient transient thermal simulation of 3D ICS with liquid-cooling and through silicon vias, 2014 Design, Automation Test in Europe Conference Exhibition (DATE), (2014), pp. 1–6.
[41] B. Lu, L. Hou, J. Fu, J. Wang, Simplified empirical formula on TSV thermal analysis for 3D IC EDA, 2014 12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), (2014), pp. 1–3.
[42] K. Skadron, M.R. Stan, W. Huang, S. Velusamy, K. Sankaranarayanan, D. Tarjan, Temperature-aware microarchitecture, 30th Annual International Symposium on Computer Architecture, 2003. Proceedings. (2003), pp. 2–13.
[43] R. Weerasekera, M. Grange, D. Pamunuwa, H. Tenhunen, L. Zheng, Compact modelling of through-silicon vias (TSVs) in three-dimensional (3-D) integrated circuits, 2009 IEEE International Conference on 3D System Integration, (2009), pp. 1–8.
[44] J. You, S. Huang, Y. Lin, M. Tsai, D. Kwai, Y. Chou, C. Wu, In-situ method for TSV delay testing and characterization using input sensitivity analysis, IEEE Trans. Very Large Scale Integr. Syst. 21 (3) (2013) 443–453.
[45] M.A. Ahmed, S. Mohapatra, M. Chrzanowska-Jeske, TSV- and delay-aware 3D-IC floorplanning, Analog Integr. Circuits Signal Process. 87 (2) (2016) 235–248.
[46] C. Jueping, J. Peng, Y. Lei, H. Yue, L. Zan, Through-silicon via (TSV) capacitance modeling for 3D NoC energy consumption estimation, 2010 10th IEEE International Conference on Solid-State and Integrated Circuit Technology, (2010), pp. 815–817.
[47] L. Bamberg, A. Garcia-Ortiz, High-level energy estimation for submicrometric TSV arrays, IEEE Trans. Very Large Scale Integr. Syst. 25 (10) (2017) 2856–2866.
[48] D.H. Kim, S.K. Lim, Through-silicon-via-aware delay and power prediction model for buffered interconnects in 3D ICS, Proceedings of the 12th ACM/IEEE International Workshop on System Level Interconnect Prediction, SLIP '10, ACM, New York, NY, USA, 2010, pp. 25–32.
[49] D. Khalil, Y. Ismail, M. Khellah, T. Karnik, V. De, Analytical model for the propagation delay of through silicon vias, 9th International Symposium on Quality Electronic Design (ISQED 2008), (2008), pp. 553–556.
[50] J. Kim, J.S. Pak, J. Cho, E. Song, J. Cho, H. Kim, T. Song, J. Lee, H. Lee, K. Park, S. Yang, M.S. Suh, K.Y. Byun, J. Kim, High-frequency scalable electrical model and analysis of a through silicon via (TSV), IEEE Trans. Compon. Packag. Manuf. Technol. 1 (2) (2011) 181–195.
[51] M. Lee, J.S. Pak, J. Kim, Electrical Design of Through Silicon Via, Springer Publishing Company, Incorporated, 2014.
[52] J.L. Henning, SPEC CPU2000: measuring cpu performance in the new millennium, Computer 33 (7) (2000) 28–35.
[53] T.C. Xu, P. Liljeberg, H. Tenhunen, Euro-Par 2011: Parallel Processing Workshops: CCPI, CGWS, HeteroPar, HiBB, HPCVirt, HPPC, HPSS, MDGS, ProPer, Resilience, UCHPC, VHPC, Bordeaux, France, August 29–September 2, 2011, Revised Selected Papers, Part I, Springer Berlin Heidelberg, Berlin, Heidelberg, pp. 281–291.
[54] C. Grecu, P.P. Pande, A. Ivanov, R. Saleh, A scalable communication-centric SoC interconnect architecture, International Symposium on Signals, Circuits and Systems. Proc., SCS 2003. (Cat. No.03EX720), (2004), pp. 343–348.