OP3DBFT: A Power and Performance Optimal 3D BFT NoC Architecture

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Abstract. Network on Chips (NoC) have emerged as a reliable communication framework in CMPs and SoCs. Many 2-D NoC architectures have been proposed for efficient on-chip communication. The use of 3D IC technology in NoC promises to improve communication latency and power. Most of the 3D ICs use Through-silicon via (TSVs) as vertical interconnect. In this paper, we explore the design space of 2-layer 3D Butterfly Fat Tree (BFT) variants. Floorplan driven wire and TSV lengths are used to obtained power and performance optimal 3D NoC architectures. We analysed the performance of the output flow control using random and round robin output based deflection routing for 3D BFT variants. TSV based power and delay models were extended to a cycle accurate simulator to estimate accurate power and performance of 3D NoC architecture. We propose a new OP3DBFT (Optimal Power and Performance 3DBFT) architecture with round-robin deflection routing (RROD) as power and performance optimal 2-layer 3D NoC architecture. OP3DBFT has symmetric link lengths and 75% of TSVs count reduced compared to the regular 2-layer 3D BFT topology. Results of our experiments show that the performance improved up to 1.39× and 1.3× in OP3DBFT with fewer TSV counts compared to the regular 2-layer 3D BFT for uniform and transpose traffic respectively. The OP3DBFT NoC architecture EDP (Energy delay product) was lower by 40% for uniform traffic and 48% for transpose traffic.

Keywords: 3-D integration · Network-on-chip (NoC) · Through-silicon via (TSV) · Interconnect · 3D Butterfly Fat Tree · 3D topology

1 Introduction

Network on chip is used as on-chip communication paradigm in Chip-Multiprocessors (CMPs) and System-on-chips (SoCs) to address the scalability and performance than the conventional on-chip communication fabric [2]. Processing elements (PEs) exchange information using packet routing network instead of conventional wires [3]. Use of 3D IC technology in NoC improves the power, heterogeneity and the overall communication time. 3D NoCs have lesser

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link lengths compared to 2D resulting in improved communication latency [8,13]. 3D NoCs interconnect these layers using direct vertical interconnects Through Silicon Vias (TSVs) [11].

Mesh topology is symmetric and has uniform link length hence its commonly used topology. Generally the decision of choosing topology relay on the performance and cost [12]. In tree-based topology, Butterfly Fat Tree (BFT) has lower resources with varying link lengths compared to the Mesh. In BFT topology, leaves are the processing elements, and nodes at intermediate levels are router [6]. The links lengths are non-uniform BFT topology and it depends on PEs physical dimensions. For accurate design trade-off studies, link delay based on physical dimensions are necessary and the performance of NoC topology depends on link latency.

Three-dimensional integrated circuits (3D ICs) are emerging as a promising technology for Systems-on-Chip (SoCs). As compared to 2D designs, 3D ICs have improved performance. 3D ICs uses Through Silicon Vias (TSVs) to connect the stacked layers. 3D IC technology (TSVs) are used in NoCs interconnect as direct vertical interconnects [11]. Use of TSVs in 3D NoC had lesser wire length and increased on-chip communication compared to 2D NoC [13]. TSV have relatively low yield and which restrict the number of TSV on a chip.

In 3D, links are divided into horizontal and vertical links again the delay of vertical links depends on the type of vertical connection. Most of the simulators consist of fixed delay component and supports only 2D NoC topology. There is a need of early-stage accurate performance evaluation 3D NoC simulators considering accurate delay and accurate physical dimensions. BFT topology has lower resource compared to Mesh topology hence BFT topology is considered for the experiments.

In this work, we evaluate and analyze the 2-layer 3D BFT variants for power and performance by extension of the simulator with the support of 3D variants of the BFT. The main focus of this paper is the detailed comparative evaluation of 3D-NoC architectures to get power and performance optimal 2-layer 3D NoC architecture. We evaluated the conventional 2-layer 3D BFT and Modified 2-layer 3D BFT (OP3DBFT) for different flow control (RROD and ROD) mechanism. The power and Performance of 3D BFT variants have been evaluated for uniform and transpose traffic patterns with accurate vertical and horizontal link latency details.

1.1 Contributions of This Work

1. Accurate power and performance evaluation and analysis of 2-layer 3D BFT based on floorplan with TSV as a vertical connection in the third dimension.
2. 3D BFT topologies variants are evaluated with Random output deflection (ROD) and Round Robin output deflection (RROD) routing.
3. OP3DBFT with RROD routing proposed as novel 3D NoC topology for Power and Performance optimal 2-layer 3D BFT NoC architecture.

2 Related Work

In [1], discussed the details of a new 3D BFT NoC design with table based uniform routing. The proposed new BFT NoC compared with torus, butterfly, mesh, and flattened butterfly topologies. In Feero et al. [5], Latency, energy dissipation, and wire area overhead of 3D NoC architectures are compared with 2D NoC architectures. With small area overhead, Mesh-based architectures have significant performance gain. Latency characteristics better for 3D Mesh over the 2D Mesh and area overhead in tree-based NoCs with an increase in energy dissipation.

In [4], proposed Hierarchical Crossbar-based Interconnection Topology (3D-HiCIT) network-on-chip (NoC. The scalability and performance of proposed topology are compared with hierarchical topologies. 3D-HiCIT allows reducing the average latency up to 50% when compared to the 3D-BFT and 45% when compared to 3D-SPIN. In [14], proposes a 3D NoC Bus Hybrid ultra-optimized inter-layer communication architecture. There is a significant area, power, and performance improvements under uniform, a hotspot of 10% compared to regular 3D NoC-Bus Hybrid Mesh architecture.

In [16], 3D partitioning and floorplanning are employed to overcome the limitation of long global wire in 3D Clos NoC (CNOC). The 3D CNOC topology supports scalability with an upper bound on power consumption.

On-chip simulators consider a constant delay on the communications and most of the state of art studies have not considered exact floorplan based approach. The link lengths depend on the floorplan of the NoC. The accurate performance of topology is observed only by considering the physical dimensions of elements. Hence we evaluated our 2-layer 3D BFT and newly modified 2-layer BFT topologies based on the floorplan. For evaluation of 3D NoC architecture, BookSim [7] cycle-accurate simulator used for evaluation 3D BFT NoC architecture and link delay models from ORION [9] are considered. ORION and TSVs power models are used to get power details of NoC architecture.

3 Power and Performance Optimal 2-layer 3D BFT Topology

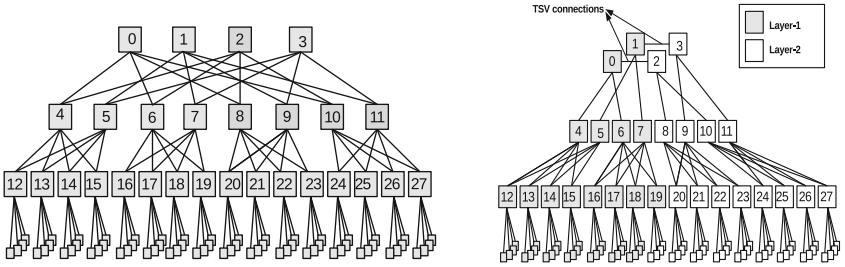
3.1 3D BFT Topology

The BFT topology is shown in Fig. 1(a) and the PEs are connected to the lowest level, and routers are placed in intermediate levels. Table 1 shows the floorplan and micro-architectural parameters details and 64 Sun-SPARC cores area are taken from [15] and router area are from the ORION area models. The degree of routers is four and six in BFT and Fig. 1(a) shows floorplan of 2D BFT topology. Micro-architectural parameters from Table 1 are used for floorplan.

There are five different links lengths are obtained from floorplan and Table 3 depicts the link lengths and their respective delay. 2D BFT topology is converted to 2-layer 3D BFT. The routers are arranged while going from 2D to 3D. 2-layer

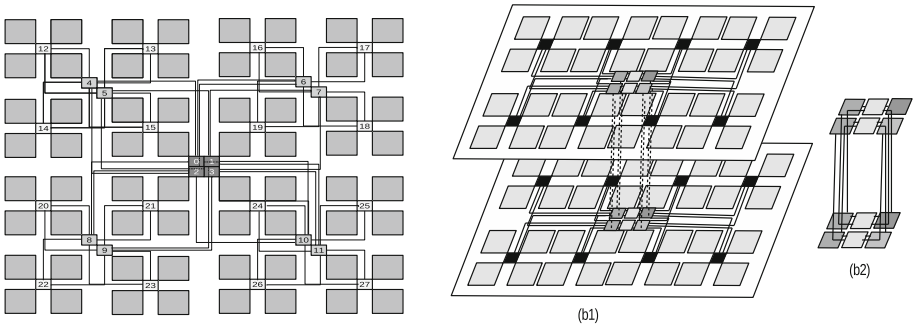
Table 1. Parameters used in the design of the floorplan [15]

Parameter	PEs area	Router area				Channel size
		3-port	5-port	6-port	7-port	
Value	3.4 mm^2	0.69 mm^2	1.25 mm^2	1.57 mm^2	1.91 mm^2	128 bit



(a) (b)

Fig. 1. (a) BFT topology and (b) OP3DBFT topology



(a) (b)

Fig. 2. (a) 2D BFT topology and (b) (b1) $8 \times 4 \times 2$ 3D BFT with two stacked layers connected using TSVs. (b2) Inter-layer connections

3D BFT shown in Fig. 2(b) with TSVs as vertical interconnect between layers. The inter-layer connection between routers are shown Fig. 2 and there eight inter-layer connection, and each connection is of 128bit TSVs.

Figure 1(b) shows modified BFT topology where each layer consist of 32 PE's each. Level 1 router has a degree of three, one link is TSV, and is connected to the next odd router in level 0, and two more links are connected to a level 1 router. Figure 3(a) shows 2D Floorplan BFT topology. Figure 3(b) shows the 2-layer 3D Floorplan and two links lengths obtained from floorplan. There are six links reduced compared to Fig. 1(a) and all these six links are vertical interconnects. Hence the Modified 2-layer 3D BFT has fewer resources compared to 2-layer 3D BFT, and we referred it as Optimal Power Performance BFT (OP3DBFT) 3D

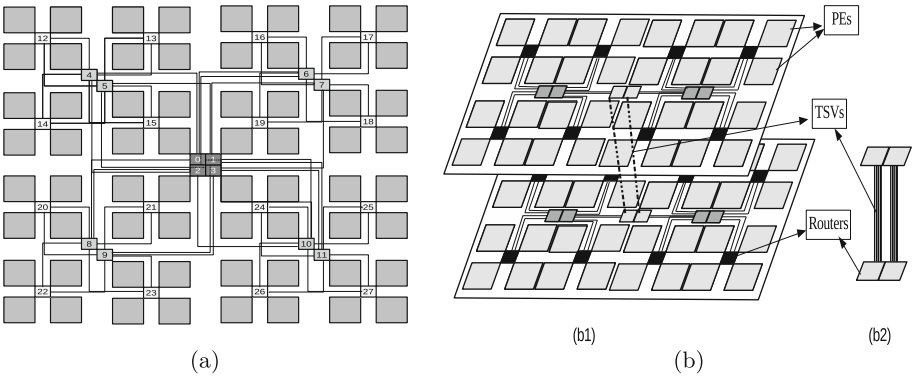


Fig. 3. (a) Proposed OP3DBFT (2-layer Optimal Power and Performance 3D BFT NoC) NoC architecture floorplan and (b) 2-layer 3D OP3DBFT topology variants.

Table 2. Total number of resources used for 2D and 3D variants topology

NoC topology	Network (x/k, y/n, z)			Router (In, Out, VC)				Link counts (HL, VL)	
	X	Y	Z	No. Router	In/Out	VC	D	HL	VL
2-layer 3D BFT	4	3	2	28	4/4, 8/8	8	16	40	8
OP3DBFT	4	3	2	28	4/4, 8/8	8	16	40	2

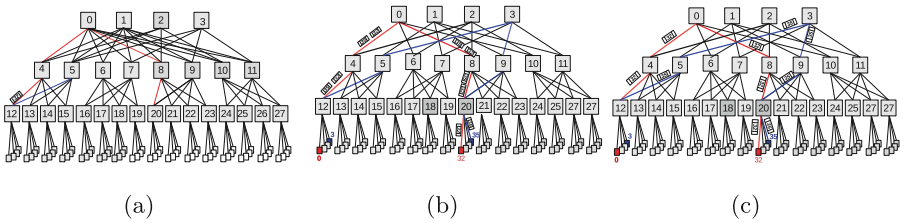
NoC architecture. The total number of resources used shown in Table 2. The OP3DBFT is 2-layer3D BFT with 80% lower TSV connection compared regular 2-layer 3D BFT.

3.2 Random and Round Robin Output Based Deflection Routing in BFT Topology

The BFT topology has two upward path flow (in level 3 and level 2) of flits to the destination with the same number of hops in both paths. There are two paths to reach from **node 0** to **node 32** and vice-versa as shown in Fig. 4(a). Hence we can apply flow control mechanism to avoid congestion and to get improved on-chip communication performance. This flow control can be handled in two ways, one is Random (ROD), and other is Round Robin (RROD) path section for output flow control.

Random Output Deflection (ROD) Routing: The ROD routing is a selection of random output port while sending packets. The Fig. 4(b) depicts the scenario of a random selection of the output port and The ROD routing shown in algorithm 1. Packets are generated from **node 0 to node 32** and **node 3 to node 35** are followed same path because of the ROD routing. Its also observed

that during random output deflection, there might be chances of selecting the same output port for two different packets which are leads to congestion and increases the communication latency.



(a) (b) (c)

Fig. 4. 2D BFT topology (a) Two paths are available from **node 0** to **node 32** (b) ROD routing for from **node 0** to **node 32** and **node 3** to **node 35** (c) RROD - from **node 0** to **node 32** and **node 3** to **node 35**

The Round Robin Output Deflection (RROD) Routing: The Round Robin (RROD) output based deflection routing is a selection of output port in round-robin fashion while sending packets. Figure 4(c) shows a selection of alternative port while routing packets. The RROD Output Deflection shown in algorithm 1. Packets are generated from **node 0 to node 32** and **node 3 to node 35** are followed alternative path because of the RROD routing. Its also observed that during RROD, the alternative output port is selected which is leads to less congestion and decreases the communication latency compared to random output deflection routing (Fig. 4).

3.3 Link Delay Estimation

The delay of wire is calculated using RC delay models of ORION for 2.5 GHz frequency. To get accurate 3D NoC power and performance the valid TSV configuration Khalil et al. [10] model is used. The model takes TSV length, TSV radius, and TSV pitch as input parameters. The safe limits are used overcome manufacturer difficulty in the fabrication. Based on safe limits, The ideal TSV configuration is generated by using this model. Based on generated different configuration the lowest TSV power parameter are considered for evaluation. The TSV configuration is, TSV length of 20 µm, a diameter of 20 µm and pitch of 60 µm and these are implicit TSV values for the simulator.

The delay of the TSV smaller than operating frequency delay hence the delay is considered as one clock cycle. Table 3 showed the delays details about the horizontal and vertical link analysis of both 2-layer 3D and modified 2-layer 3D BFT based on the floorplan. Each vertical link contains 128 TSVs (128-bit channel) Last two columns of the Table 3 shows the count and delay of the TSVs.

In 2-layer 3D BFT, total 8 links count is reduced to half compared to 2D BFT and OP3DBFT 2-layer 3D BFT has a reduction in 6 links compared to regular 2-layer 3D BFT topology.

```
Input: cur node, Flow and dest node
Output: output port from cur node to dest
if cur!=dest then
    . . . else if nl==2 then
        Find Lowest(min) node and maximum(max) node which can reach
         from cur;
        if dest is in beween max and min then
            out_port=(dest%4);
        end
        else
            #Random Output Deflection (ROD)
            if Flow==ROD then
                out_port=rand()%2+4;
            end
            #Round-Robin Output Deflection (RROD)
            else
                if RB==1 then
                    out_port=4; RB=0;
                end
                else
                    out_port=5; RB=1;
                end
            end
        end
    end
end
```

Algorithm 1. Random and Round Robin output based deflection routing algorithm for OP3DBFT NoC architecture.

4 Experimental Setup

The cycle-accurate on-chip network simulator [7] is modified to support 2-layer 3D NoC BFT variants with accurate delay. Horizontal wire delays and TSV delays were modeled as described in the Sect. 3.3. The BFT variants as shown in Figs. 2 and 3 are implemented in the simulator. For routing, nearest common ancestor algorithm used for 64 nodes with ROD and RROD. Table 4 shows experiment setup configuration parameters for 3D BFT variants

5 Results and Discussion

5.1 Average Network Latency

Figure 5 depicts the comparison of latencies of OP3DBFT for Random and Round robin output deflection routing for uniform and transpose traffic pattern. OP3DBFT with Round Robin deflection routing has a reduction in the average network latency up to 3% compared to OP3DBFT with Round throughout the simulation for both traffic pattern. RROD routing is selected as the best output

Table 3. Link length and delay details of BFT topology variants.

Topology	Wire (mm)	Delay (clock cycle)	HL (wire) count	VL count	Number of TSVs	Delays (Clock Cycle)
2-layer 3D BFT	8.176	68	8			
	7.776	63	8			
	4.088	18	8	8	1024	1
	3.688	14	8			
	1 mm	1	8			
OP3DBFT 2-layer 3D BFT	4.088	14	24			
	3.688	16	16	2	256	1

Table 4. Experimental setup

Simulator	BookSim
Topology	2-layer 3D BFT & Modified 2-layer 3D BFT (OP3DBFT)
Network Size	64 Nodes
Switches	28
Traffic	Uniform Random, Transpose
Number of VCs	8
VC buffer size	16
Simulation time	10^5 cycles

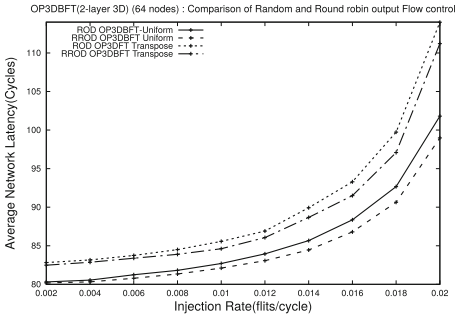
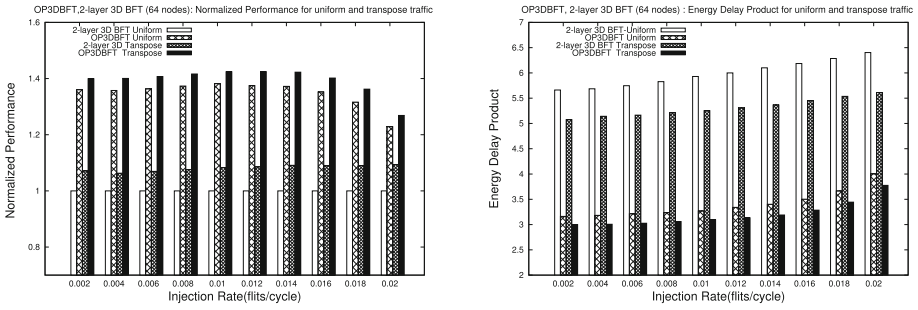


Fig. 5. Average network latency comparison for OP3DBFT for RROD and ROD routing.

flow control for the tree based topologies compared to ROD routing. Hence for further evaluation 2-layer and modified 2-layer 3D BFT are based on the RROD routing.

5.2 Performance Analysis

The Fig. 6(a) depicts the 2-layer 3D BFT and modified BFT (OP3DBFT) performance for uniform and transpose traffic pattern with considering the round robin deflection flow control. The OP3DBFT shows 1.39× and 1.3× performance improvement compared to 2-layer 3D BFT uniform and transpose traffic respectively. OP3DBFT has improved performance because there is a reduction of up to 75% of TSV count, i.e., six links are reduced compared regular 2-layer 3D BFT as shown in Table 2.



(a) The Normalized performance (b) Energy Delay Product

Fig. 6. Comparison of regular 2-layer 3D BFT and OP3DBFT for uniform and transpose traffic (a) Normalized performance and (b) EDP

5.3 Power Performance Trade-Off

We evaluate the power performance trade-off of 3D BFT variants using Energy Delay Product (EDP) over various injection rate. The Fig. 6(b) shows the EDP of OP3DBFT and regular 2-layer 3D BFT variants for uniform and transpose traffic pattern. The OP3DBFT shows 40% and 48% reduction in EDP compared 2-layer 3D BFT for uniform and transpose traffic pattern respectively.

6 Conclusion

This work proposes a 2-layer Optimal Power and Performance 3D BFT NoC (OP3DBFT) with Round Robin Output deflection (RROD) routing. Floorplan based wire lengths and link latencies were considered to get more accurate latency values. Results of our experiments show that the OP3DBFT with Round Robin deflection (RROD) routing reduces the average network latency up to 3% compared to OP3DBFT with Random deflection (ROD) routing for both uniform and transpose traffic. RROD routing is better for the BFT based topologies compared to random selection RROD due to equal traffic distribution among links. The OP3DBFT architecture with RROD routing shows a 1.39× and 1.3× performance improvement compared to the regular 2-layer 3D BFT for uniform

and transpose traffic respectively. OP3DBFT has improved performance because of the modified structure and usage of 75% lesser TSVs. OP3DBFT shows a 40% and 48% reduction in EDP compared 2-layer 3D BFT for uniform and transposed respectively. This work considers the floorplan based accurate wire and TSVs delays in 3D variants BFT NoCs. Further, this study can be expanded to understand the thermal behavior TSVs on OP3DBFT to develop a thermally aware routing algorithm.

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