# Bheemappa Halavar

Dept. of CSE – National Institute of Technology Karnataka, Surathkal, India -575025

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PhD student in Computer Science and Engineering with more than 4 years of Research experience in High Performance Computing (Network on Chip and Computer Architecture). Passionate about technology, with strong technical and interpersonal skills for working in a team and successfully completing challenging tasks.

#### **Education**

## Academic Qualifications.....

National Institute of Technology Karnataka , Surathkal

**NITK Surathkal** 

- Ph.D in Computer Science and Engineering (Computer Architecture), Dec-2014 Aug-2019(Expected)
  - Visvesvaraya Technological University

VTU Belgaum

 $^{\circ}$  M.Tech in Computer Network Engineering, First Class with CGPA 7.75%

2011–2013

Visvesvaraya Technological University

VTU Belgavi

B.E in Information Science and Engineering, First Class with Distinction with 71%

2009-2013

# **Previous Employment**

#### Research Scholar

National Institute of Technology Karnataka, Karnataka

Dept. of Computer Science and Engineering
(High Performance Computing- Network on Chips)

Dec 2014–Till Date

**Assistant Professor**Secab Institute of Engineering and Technology

Bijapur, Karnataka Aug 2013-December 2014

**Subjects handled** 1. Web Programming, Computer Networking, Wireless networks, C# and .Net and socket programming.

# **Projects**

Online Share Trading System -B.E

A web based interface for uses to bid, buy and sell shares. The broker performs the transaction process even if orders are not matched. The broker sends message to seller and buyer through his/her mobile connected to PC's or laptops when transaction been done. Demand for company shares increases.

**Tools and Programming languages:** NetBeans 6.9, Wamp Server, MySql Turbo Manager, jdk1.Java Server Page (JSP), HTML, JavaScript.

 Cognitive Characterization Of Learner Behaviour Based On Brain Lateralization and Other Parameters -M.Tech

This project attempts at developing a system that classifies the learner into Cognitive categories based on assessing the learner based on brain lateralization and other parametric tests.

Tools and Programming languages:: NetBeans 6.9, Wamp Server, MySql Turbo Manager,

jdk1.Java Server Page (JSP), HTML, JavaScript.

Power and Performance optimal 3D NoC architecture (Ongoing) -Ph.D

The goal of the project is quantitative analysis of 3D NoC architecture and Design of power optimal 3D NoC architectures. NoCs on 3D ICs technology provides an opportunity to better the on chip communication delay, energy and area parameters compared to the 2D-NoCs. We are extending the existing simulators to support 3D-NoC topologies. Design space exploration of 3D-NoC is being driven by considering physical characteristics of vertical connections like Through Silicon Vias (TSVs). The exploration is aided using power, performance and cost metrics such as area, throughput, avg. flit latency, Energy per bit transferred, and EDP.

**Tools and Programming languages:**: NetBeans, BookSim, ORION ,HotSpot, Gem5, Vivado High Level Synthesis, Dsent, Pyhton, C++, JavaScript. Xilix Vivado.

#### **Technical and Personal skills**

- **Programming Languages:** Proficient in C,Python,C++,HTML,PHP,
- Industry Software Skills: MySQL, Servelt, Jsp, Jquery ,python.
- General Business Skills: Have experience in agile methodology. Good presentation skills, Works well
  in a team.

## **Publications**

#### **Journals**

- 1. B. Halavar, U.Pasupulety and B. Talawar, Extending BookSim and HotSpot for Power, Performance and Thermal evaluation of 3D NoC Architectures, Simulation Modelling Practice and Theory, Elsevier.
- 2. B. Halavar and B. Talawar, *Power and Performance Analysis of TSV based 3D Network on Chip Architectures*, Journal of Circuits, Systems, and Computers, World Scientific [communicated].

#### Conference

- 1. B. Halavar and B. Talawar, *Accurate Performance Analysis of 3D Mesh Network on Chip Architectures*, 2018 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT), March-2018.
- B. Halavar and B. Talawar, Floorplan Based Performance Evaluation of 3D Variants of Mesh and BFT Networks-on-Chip, International Conference on Signal Processing and Communication (SPCOM), July-2018.
- 3. B. Halavar and B. Talawar, *OP3DBFT: A Power and Performance Optimal 3D BFT NoC Architecture*, 18th International Conference on Intelligent Systems Design and Applications(ISDA).India, Dec-2018.
- 4. U.Pasupulety, B. Halavar and B. Talawar, *Accurate Power and Latency Analysis of a Through-Silicon Via(TSV)*, 7th International Conference on Advances in Computing, Communications and Informatics (ICACCI), Sep-2018.
- 5. U.Pasupulety, B. Halavar and B. Talawar, *Thermal Aware Design for Through-Silicon Via (TSV)* based 3D Network-on-Chip (NoC) Architectures, 8th Int'l Symp. on Embedded computing & system Design(ISED), Dec-2018,

### Reference

- Dr. Basavaraj Talawar, Assistant Professor, Department of CSE, NITK Surathkal. Email: bt.cse.nitk@gmail.com,
- o Dr. Manu Basavaraj, Assistant Professor, Department of CSE, NITK Surathkal.

Email: manub@nitk.ac.in@gmail.com,

# **Personal Details**

Name: : BHEEMAPPA H HALAVAR

Father name :: HANUMANTAPPA HALAVAR

**Date of Birth ::** 30-09-1989

**Gender :**: Male

Nationality :: Indian

Permanent Address:: BHEEMAPPA H HALAVAR S/o H.B.Halavar Mirjakar buiding, Tabib Land,

near CBT, HUBLI - 580020. KARNATAKA PH:9986581954.

Languages Known:: Kannada, Hindi, and English.

Hobbies:: Listening music, Playing cricket, Watching news, Reading books, Reading magazines.