Power and Performance Analysis of Through Silicon Via based 3D Network-on-Chip Architectures

Bheemappa Halavar, Basavaraj Talawar

{*cs14f06.bheem,basavaraj*}*@nitk.edu.in*
SPARK Lab, Computer Science and Engineering, National Institute of Technology Karnataka, India

Abstract

Emerging 3D ICs employ 3D NoCs for improved power, performance and scalability. NoC simulators use micro-architectural parameters to estimate the power and performance of NoCs. We explore the design space of 3D Mesh and Butterfly Fat tree(BFT) NoC architectures using floorplan driven wire lengths and link delay estimation. The delay and power models are extended using Through Silicon Via(TSV) power, and delay models. Serialisation is employed to reduce the area cost of TSVs. Buffer space is equalised for a fair comparison between the topologies. Performance, Flits per Joules(FpJ) and Energy Delay Product(EDP) of six 2D and 3D variants(2-layer, 4-layer) of Mesh and BFT topologies are analysed by injecting synthetic traffic patterns. 3D-4L Mesh exhibit better performance, energy efficiency (up to 4.5×), and EDP (up to 98%) compared to other variants. This is due to shorter overall horizontal link lengths and greater number(3×) of TSVs compared to the other variants.

Keywords:
Network-on-chip (NoC) 3D NoC Topologies, Through-silicon via (TSV), Design space exploration, performance analysis, Energy Delay Product.

1. Introduction

Massive integration of processing and memory elements in System-on-chips (SoCs) and Chip-Multiprocessors (CMPs) demand a power-performance efficient and calable communication fabric - the Network on chip(NoCs). In NoCs,

the processing elements (PEs) exchange data via an optimally designed packet routing network. The flow control units in NoC are called as flits which are smaller units of packets. The flits are routed through a set of routers and links to reach the destination from a source node. Based on the bandwidth requirements of an application, the routers are connected in well-defined topology [1].

Three-dimensional integrated circuits (3D ICs) is an emerging technology for high performance and low power VLSI solutions. 3D ICs distribute logic and memory in stacked layers. NoCs interconnect these layers using direct vertical interconnects called Through Silicon Vias (TSVs) [2]. NoCs exploit 3D IC technology as a way to improve power, heterogeneity, and area, which also has an effect on improving on the overall communication time. In comparison with 2D NoC, the 3D NOC have shorter link length which results in the reduction of latency and power. The overall reduction of wire length is the factor of the square root of the number of layers in 3D NoC[3].

The amount of time employed during the NoC design period can be reduced by using cycle accurate simulators as an early power and performance estimation tool. Existing simulators explore various architectural and microarchitectural design parameters at the router level such as router pipeline depth, arbitration techniques, number and size of virtual channels, number and size of input/output buffers, routing and switching techniques. Simulators have been extended to explore new designs such as network partitions, node concentrations, express physical links, and asymmetric buffer reorganization and so on [4].

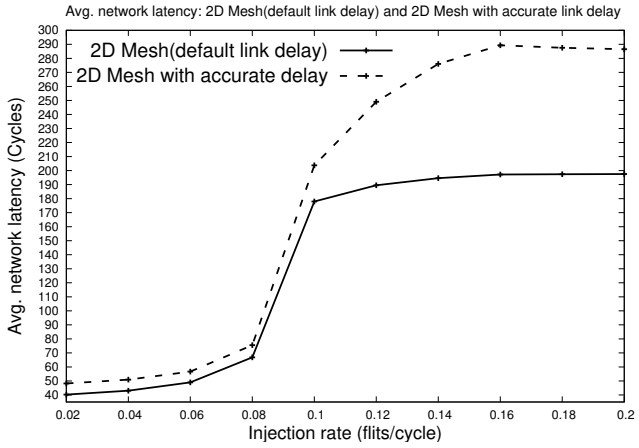
Link latency plays a significant role in overall performance of NoC. Our experiments on a 64 node 2D Mesh with uniform random traffic at the injection rate of 0.1 with default constant link latency show that, 15-20% of flit traversal time is spent in the links of the NoC. However, the wire lengths estimated using floorplans of the topology have non-identical lengths. The wire delays depend on the R,C values of the wire, which are in turn dependent on the length of the links (Section 4). Accurate modeling of link delay is necessary in early stage design trade-off studies.

The link lengths on the chip depend on the area of the component. In order

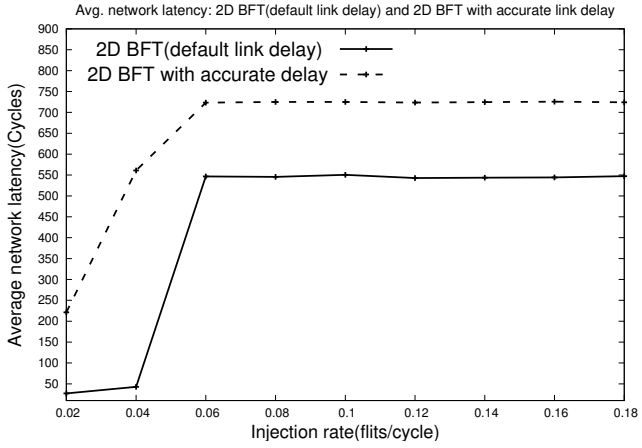
to estimate the exact length of the link, it is essential to consider the physical dimension of the components. Variable link lengths which have variable delays are a function of the PE area and the topology of the NoC. The interconnect length, operating frequency, and voltage must be considered to estimate the exact link delay. The topology selection process is a significant NoC design decision as it influences key NoC attributes. The decision on the topology is relies on the application bandwidth requirements, chip power and performance constraints, area budget and resources available. Mesh topology is symmetric and has short wire lengths between routers. Thus, it is most commonly used topology in NoC due to its symmetric nature. Butterfly Fat Tree (BFT) is another topology which has less number of routers compared to the Mesh topology. The earlier work[5] takes into account the state-of-the-art latency values of TSVs[6] to evaluate 3D Mesh variants performance. The importance of considering floorplan details is shown in Figure 1. Average network latency of floorplan-based link latency and default link latency(BookSim) of 2D Mesh and BFT topologies is shown in Figure 1. An increase in latency by 1.45× and 8× for 2D Mesh and 2D BFT topologies has been observed employing the floorplan link latency compared to the default link latency[5].

Estimation of wire lengths based on floorplan and consideration of latencies during simulation will improve the accuracy in the evaluation of NoC performance.

In this work, we present a detailed microarchitectural design space exploration of 2D and 3D variants(2-layer and 4-layer) of the Mesh and BFT topologies. We evaluate and analyse the topologies for power, performance and cost trade-offs by extending the 2D simulator[7] support for 3D variants of the Mesh and BFT topologies. The design space parameters explored at the input/output ports are the virtual channels(V) and the depth of the buffer (D). The main objective of this paper is to evaluate 3D-NoC architectures comparatively with their 2D counterparts in order to quantitatively determine the power and performance benefits. We evaluate the conventional 2D Mesh with 2-layer 3D (3D-2L) Mesh, 4-layer 3D (3D-4L) Mesh, 2D BFT, 3D-2L BFT and 3D-4L BFT. In the



(a)



(b)

Figure 1: Network Latency comparison of (a) 2D Mesh(constant link delay) and 2D Mesh (flooplan based delay) and (b) 2D BFT(constant link delay) and 2D BFT (flooplan based link delay).

presence of uniform and transpose traffic patterns, the performance of both 2D and 3D variants of Mesh and BFT NoC topologies were characterized using cycle accurate simulation by considering accurate wire delay estimated from ORION [8] and TSV delay models. Wire lengths were derived from floorplans and TSV parameters from recent literature. Buffer space has been equalized for

a fair comparison between topologies and the 2D and 3D variants. 3D-4L Mesh with uniform traffic shows the performance improvement of 2× to 2.3× better than other 2D, 3D Mesh variants for uniform and transpose traffic patterns. 3D-4L BFT with transpose traffic shows an improvement in performance of up to 1.1× to 1.3× over other 2D and 3D BFT variants for uniform and transpose traffic patterns. After buffer space equalisation, the 3D-4L Mesh has improved performance up to 5× to 12× better than the all other variants with uniform and transpose traffic pattern for injection rate up to 0.16. The Flits per joule for 3D-4L Mesh topology is up to 4.5× compared to all other the variants with uniform and transpose traffic pattern. As we move towards 3D from 2D in BFT, data transferred per Joule(measured as flits per Joule) increased up to 1.5× in 3D-2L and up to 3.9× flits per joule in 3D-4L BFT compared to 2D BFT topology. The EDP is lower(80% to 98%) for 3D-4L Mesh compared to all other variants.

2. Related Work

2.1. Design Space Exploration

2.1.1. 2D NoC

The evaluation methodology for comparing 2D Octagon, Torus, SPIN, Folded torus, BFT NoC architectures have been discussed by Pande et al. [9]. For a high degree of connectivity, high throughput and low latency were observed. SPIN and Octagon show greater average dissipation of energy at saturation compared to other NoC architectures. The switches were designed to maintain low latency and significant throughput by considering four virtual channels. Grot et. al.[1] proposed MECS topology where routers are highly concentrated and connected via express physical links. Concentration is used for designing the scalable networks which lead to increases router complexity. 4-way concentration is used and which leads to a 4x reduction in the PEs count with higher router complexity. MECS has more energy consumption than the homogeneously partitioned MECS.

Designers have explored the architectural design space to optimize both performance and energy-efficiency. Architectural choices for NoCs include partitioning using multiple sub-networks, concentration and express physical links. The design options such as multiple physical (P) networks, concentration core(C), express channel(X), flit width(W) or virtual channel(V) has been introduced, and all combinations of this option were evaluated by means of the energy throughput ratio (ETR)[4]. Virtual channels (VCs) have been proposed as solution to the head-of-line blocking problem. VCs regulate flow control and are assigned to each I/O port of the router. Using VC flow control, performance is improved in available channel bandwidth. Advantages of replicating physical networks over using VCs are investigated in [10]. Replication is achieved by using multiple parallel physical networks (multi-planes) with smaller channels with separate traffic classes. Chen et. al. [11] compare the effectiveness of physical and virtual express Mesh topologies with large node counts, under constraints of bisection bandwidth. Virtual channels are a better solution for NoCs in case of high resource availability and performance needs. Physical express topologies provide higher throughputs and are more robust across traffic patterns.

2.1.2. 3D NoC

Feero et. al [12] discuss 3D topologies derived from Mesh and Tree topologies. Throughput, latency, energy dissipation, and wiring area overhead of 3D NoC architectures are compared with 2D NoC architectures. The Mesh-based architectures have significant performance gains with a small area overhead. 3D tree-based NoCs have significant gain in energy dissipation and area overhead. 3D Mesh-based NoCs have superior latency characteristics over the 2D versions. Accurate link delay plays a significant role in the overall performance of NoC. This paper does not examine accurate link delays (horizontal and vertical) for assessment. Butterfly Fat-Tree (BFT) is introduced as an overall interconnect architecture, where IPs reside at the leaves of the tree and switches at its vertices. In [13], A new 3D NoC design with an efficient table based routing derived from BFT topology. The new BFT design is compared with Mesh. The

accurate wire delays are not considered in the simulation. A 3D-HiCIT (Hierarchical Crossbar Interconnection Topology) topology is proposed as a high performance and scalable 3D NoC architecture. In comparison to 3D-BFT and 3D-SPIN, 3D-HiCIT has a reduction of latency of 50% and 45% respectively[14].

Josphet et.al[15] have focused on the buffer distribution in heterogeneous 3D-SoCs.Buffers in router architecture are reorganised among dies in the 3D Mesh to save area and power. Buffer reorganisation helped save 8.3% of area and 5.4% of power with a small performance decline. Wire delays influence the performance of the NoCs significantly. Optimal floor planning and partitioning can help to reduce the effect of wire delays through reduced wire lengths. Energy efficiency and resiliency of Near Field Inductive Coupling of links are exploited for a 3D NoC design as commination backbone. Low latency is achieved in collective communication for 3D NoC by employing an efficient router bypass[16].

2.2. NoC Simulation Frameworks

Jiang et. al [7] have presented BookSim, a cycle-accurate simulator for performance evaluation of NoC architectures. BookSim has a wide range of configurable NoC parameters. ORION [8] and DSENT [17] incorporate the power and area model for electrical and optoelectrical interconnection network power and area estimation. In [18], a SystemC based cycle-accurate NoC simulator(NOXIM) presented for performance and power evaluation of wired NoC architectures. Cycle-accurate simulators consider the length or delay of communication to be constant. However, the length of links in NoCs varies based on the NoC floorplan. In this work, experimental analysis of 2D and 3D variants of Mesh and BFT topologies are conducted based on floorplan. Correct length and number of links (horizontal and vertical) are determined in each topology using floorplan. For the evaluation of NoC architecture, BookSim2.0 simulator has been considered. The ORION link delay model, power models and microarchitectural details of TSVs are used in the experiments to calculate accurate NoC component power and link delay (optimal number, repeater size). The cycle accurate link delays were updated in BookSim, and routing models were

also modified to model the behaviour of the 3D variants. The NoC simulators can be compared based on their coverage, configuration parameters and metrics measured. Most on-chip simulators consider a static wire length or constant delay during communications. However, the length and the delay of NoCs link vary according to the floorplan of the NoC. Table 1 compares the design space approaches of the state-of-art simulators with the modified simulator(modified BookSim2.0).

3. Floorplan of the Mesh and BFT NoC Topologies

3.1. Through Silicon Via Link Delay Model

Through silicon via (TSV) is a vertical electrical link (via) through the silicon wafer. TSV provides high bandwidth, low latency compared to wires at the edges. Figure 2(a) shows a pair of signal and ground TSV. The stacked chips are connected through a vertical TSV and bump interconnection. The TSV bumps are separated by underfill. Inter Metal Dielectric(IMD) layers separate TSVs. Kim et al.[21] derived an RLGC model in which multiple physical parameters are used to estimate the single TSV capacitance. For the derivation of TSV power consumption, the TSV capacitances are used. Also, a power consumption equation using the TSV value has been developed in [21].

Khalil et al. [22] derived a compact latency model from a TSV dimension analysis. The input parameters are the TSV dimensions such as TSV's length, radius and pitch. To Generate TSVs delay, power and valid TSV configuration, we have created an ideal TSV configuration by looking at safe limits for each parameter to avoid manufacturer complexity during a production process. Each parameter safe limits are considered from [23] and [24]).

3.2. Data serialization over TSVs

Data serialization is used to reduce the area footprint of the TSVs with a little power overhead. NoC interconnects channel size is 64 bit. Serial TSVs have been proposed as an effective solution to keep overall TSV count small.

Table 1: Summary of Comparison of Different NoC Simulators from the Literature

Tools	Design Space Exploration									Results		
	General NoC design Features					3D NoC Design Space Features						
	2D topology	Network	Router	Buffer	Link	3D	TSVs	Floorplan		Latency	Power	Area
Acces Noxim [19]	✓	✓	✓		✓	✓	✗	✗		✓	✓	✗
Orion [8]	✗	✗	✓	✓	✓	✗	✗	✗		✗	✓	✓
Nirgam [20]	✓	✓	✓	✓	✗	✗	✓	✓		✗	✓	✓
Dsent [17]	✗	✗	✓	✓	✓	✗	✗	✗		✓	✓	
BookSim2.0 [7]	✓	✓	✓	✓	✗	✓	✗	✗		✓	✓	✗
Extended BookSim2.0(3D NoC)	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓

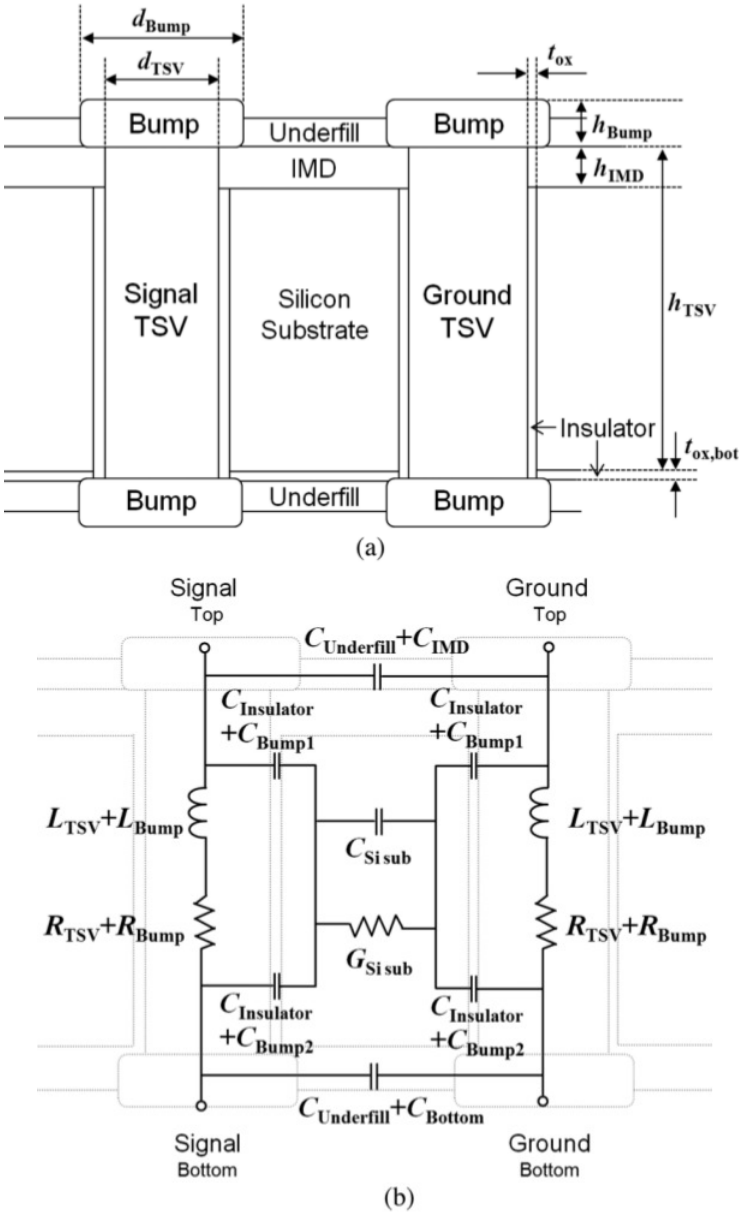


Figure 2: (a) Signal TSV and ground TSV structural parameters (b) Electrical model. [21]

Using serial TSVs in 3D ICs Vertical link leads to a reduction in the area of TSVs with little reasonable overhead[25]. The area footprint of 64-bit TSVs connection will impact on the overall area of the chip. Hence, we consider the

2:1 data serialization where the footprint area is decreased to half. Table 2 shows the parallel and serial case with the TSVs design parameters and TSV count. A serializer-deserializer module is considered to send the vertical communication in stream.

An analytical model of the propagation delay of the TSV is shown in Algorithm 1 and TSV delay depends on the Height/Length(l), Diameter(d) and Pitch/Separation(s). The Safe limits values of each parameter are considered to generated set of TSVs configuration, and the 20μm is the height, the diameter of 20μm and pitch of 40μm yield lowest TSV power. The lowest yield TSVs conflagration has a higher pitch, and the area of TSVs is directly proportional to the pitch size. Hence, we considered the area power product metric. The TSV configuration which has lowest power consumption is considered for evaluation of the 3D variants of Mesh and BFT NoC architecture. The Height of 20μm, the diameter of 20μm and pitch of 40μm has the lowest PAP, and this TSV configuration is used for the 1:2 data serialization. The details are shown in Table 2. The delay of the TSV is 50ps which is much smaller than 0.4ns (2.5GHz). Thus, the delay of TSV is represented as one clock cycle throughout the paper.

Two state-of-the-art 2D NoC topologies are considered to evaluate proposed serialised TSVs model. A topology with the larger TSVs count, i.e., 3D Mesh

Algorithm 1: TSV Delay Estimation

START
$r = d/2$
$l_{\mathrm{o}} = \frac{\sigma_{\mathrm{Cu}} * r^2 * \sqrt{(\mu_{\mathrm{o}}/\varepsilon_{\mathrm{si}})} * acosh(s/d)}{0.693 * (1 + 0.617 * (r/s))}$
if($l \geq lo$)
    $delay = \sqrt{(\mu_{\mathrm{o}}/\varepsilon_{\mathrm{si}})} * l * l/l_{\mathrm{o}}$
else
    $delay = \sqrt{(\mu_{\mathrm{o}}/\varepsilon_{\mathrm{si}})} * l$
END

Table 2: Parallel and serial case with the TSVs design parameters and TSV count per channel

	1:1 TSVs	2:1 serialisation TSVs
TSVs count	64	32
KOZ (μm)	5	5
TSV array (μm) (TSV+KOZ)	270 x 640	135 x 640

topology and 3D BFT topology with reduced vertical connection compared to 3D Mesh are considered. 2-layer 3D (3D-2L) and 4-layer 3D (3D-4L) variants of Mesh and BFT topologies are evaluated to observe the performance by employing the vertical connection(TSVs).

3.3. 3D Mesh Topology

Mesh is a direct network topology that allows PEs to be integrated into a regular structure, where every router except those at the edges are connected to neighbouring routers.

Sun-SPARC 64 Core Chip Multiprocessor is considered for floorplan . Each PE area is of 3.4mm^2. The 3D Mesh topology consists of 5-port and 6-port routers.The router area is estimated from the ORION2.0 [8] area model and the area of each router is shown in Table 3. All the micro-architectural parameters used are shown in Table 3. Two 3D NoC topologies have been designed to analyse the performance of going vertical from 8×8 2D Mesh topology (64 nodes). The floor plan of two 3D NoC designs ($8 \times 4 \times 2$ and $4 \times 4 \times 4$) is shown in 3 and 4 respectively.

3D Mesh 2-layer (3D-2L Mesh) consists of 32 routers per layer routers, while 3D mesh 4-layer ((3D-4L Mesh)) has 16 routers per layer.

The ZXY routing algorithm is used for the 3D Mesh topology. The ZXY algorithm, first routes the packets to layer (Z) of the destination node and then performs the XY routing destination (Z) layer.

Table 3: Floorplan parameter details

Clock Frequency		2.5GHz
PEs area		3.4mm^2
Router area	4-port	0.47098mm^2
	5-port	0.598509mm^2
	6-port	0.729954mm^2
	7-port	0.865314mm^2
Channel size		64(bit)

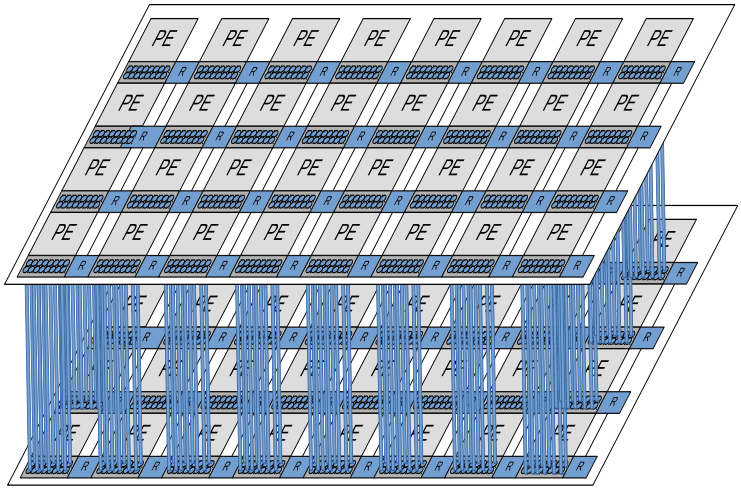


Figure 3: Floorplan of two layer 3D Mesh($8 \times 4 \times 2$) and each vertical connection consists of 32 bit TSVs.

3.4. BFT topology

The Figure 5 depicts Butterfly Fat Tree (BFT) topology. The BFT topology connects 64 nodes using 28 routers. Routers(0-27) are the top and intermediate nodes. The PEs(64) are the leaves. Non-uniform links are present in each level of BFT topology[13].

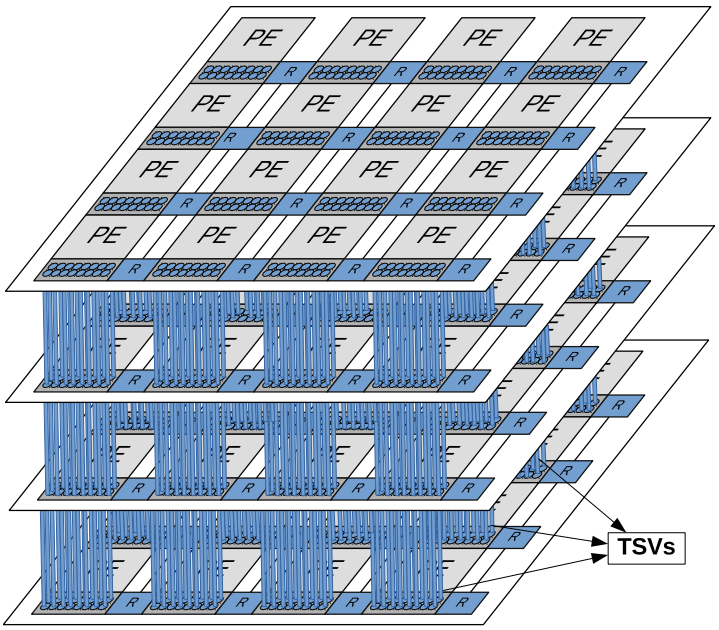


Figure 4: Floorplan of four layer 3D Mesh($4 \times 4 \times 4$) and each vertical connection consists of 32 bit TSVs.

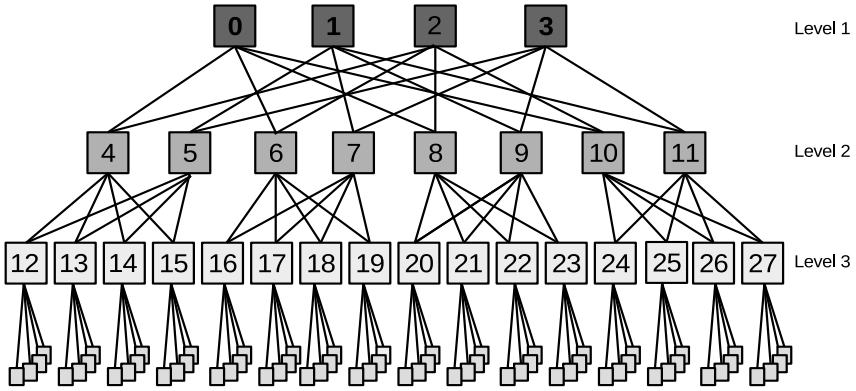


Figure 5: 64 node BFT topology with three levels. Level 1 contains four 4-port routers, level 2 has eight 6-port routers, and level 3 has sixteen 6-port routers. Four PEs are connected per router(leaves).

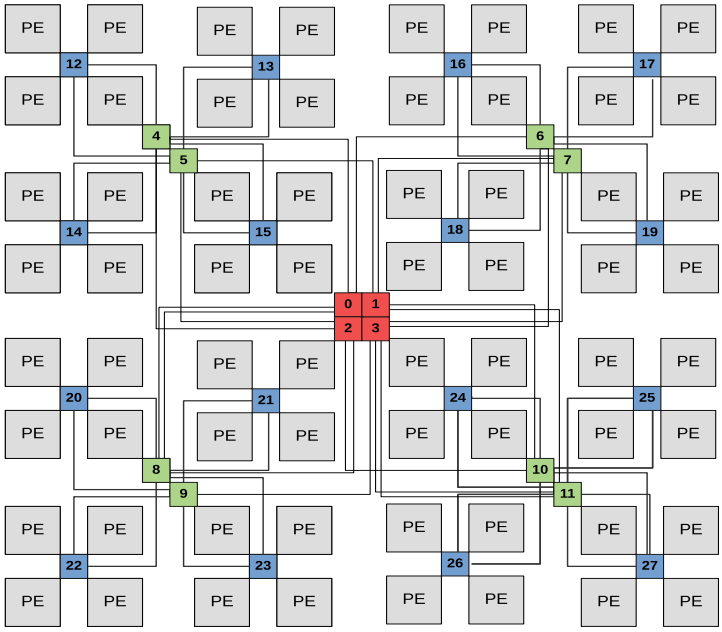


Figure 6: Floorplan of 2D topology BFT. 0-3 top level routers from level 1 and 4 to 11 router are from level 2 and 12-27 routers are from level 3. There are 5 different length of links are obtained from floorplan details shown in Table 4.

2D BFT topology shown in Figure 5 consist 64 PEs and 28 routers. Except for the top level routers(which have 4-ports), all routers contain six ports. In the 6-port router, one port is connected to each of four child nodes and remaining two ports connected to parent nodes.

Figure 6 shows the floorplan of 2D BFT topology. Microarchitectural parameters used for our experiments are shown in Table 3. Table 4 represents the length of the link with delays (in clocks cycles).

3.4.1. 2-layer 3D BFT (3D-2L BFT)

The 3D-2L BFT shown in Figure 7 extended from a 2D BFT. 3D-2L BFT is connected by vertical TSV with two layers. The 3D-2L flooplan based link length, delay(cc) of wire details are shown in Table 4. The level 2 routers are rearranged to reduce the length of links. In Figure 7, 8 links from level 1 to

level 2 are converted as TSV because of moving from 2D to 3D.

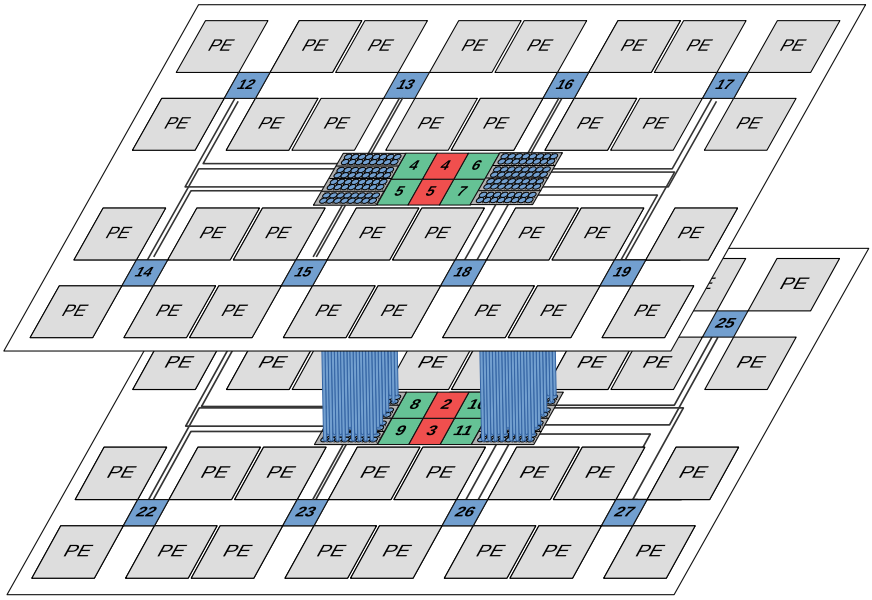


Figure 7: Floorplan of 3D-2L BFT topology with each layer of 32 PEs. Vertical connection of routers between level 1 and leve 2 of BFT topology.

3.4.2. 4-layer 3D BFT (3D-4L BFT)

Figure 8(a) shows floorplan of 3D-4L BFT(16 PEs at each layer) which is modified from 3D-2L BFT topology. In 3D-4L BFT Link lengths are decreased compared to 3D-2L.

Nearest Common Ancestor (NCA) routing algorithm is employed in 2D and 3D BFT variants. The algorithm identifies the nearest common ancestor between source and destination. At each router, it finds the minimum and maximum reachable nodes and then based on reachability packets are routed to appropriate ports.

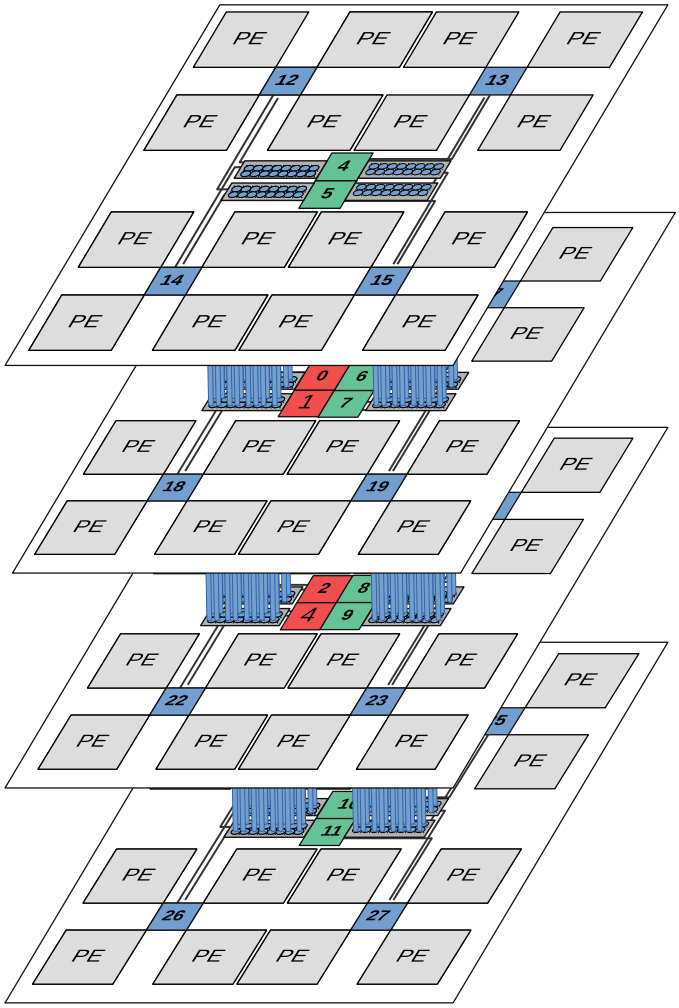


Figure 8: Floorplan of 3D-4L(16 PEs per layer) BFT topology.

4. Link Delay and Buffer Space Analysis

4.1. Horizontal and Vertical Link Delay Estimation

Table 4 shows the wire lengths, delays(cc), counts and powers of the horizontal links(HL) of Mesh and BFT (2D, 3D variants). The delays(in ns) are extracted using RC delay models from ORION [8]. Further delay(ns) are converted to clock cycles for the 2.5 GHz operating frequency. Mesh topology has

uniform horizontal link lengths in all the variants(2D, 3D-2L, 3D-4L). Floorplans of the BFT topology indicate that the horizontal link lengths depend on the level, router placement, and the PE size. When we move from 2D to 3D in BFT, links connecting from level 1 to level 2 (Figure 5) are reduced up to 40-80% compared to 2D BFT.

Table 4: Mesh and BFT (2D, 3D variants) horizontal link length and delay details based on the floorplan.

Topology	Length of Wire (mm)	Delay of wire (clock cycle)	Horizontal link count
2D Mesh	1.844	4	112
3D-2L Mesh	1.844	4	108
3D-4L Mesh	1.844	4	96
2D BFT	8.825	73	8
	8.342	73	8
	7.859	64	8
	4.654	23	8
	4.171	19	16
3D-2L BFT	8.342	73	8
	7.859	64	8
	4.654	23	8
	4.171	19	8
3D-4L BFT	4.654	23	14
	4.171	19	14
	1μm	1	12

Table 5 shows the number of vertical connections and number of TSVs for each topology. Each vertical link contains 32 TSVs.

Table 5: Vertical Link count and number of TSVs of Mesh and BFT (2D, 3D variants).

	Mesh			BFT		
	2D	3D-2L	3D-4L	2D	3D-2L	3D-4L
VL count	0	32	48	0	16	8
number of TSVs	0	1024	1536	0	512	256

4.2. Buffer Space Analysis

Buffers in the router I/O ports are expensive resources as they consume as much as 30% of the router area. Buffers improve the overall throughput of the NoC. Total buffer space (B) utilisation of topology is presented in Equation 1. Total buffer space depends on the number of routers, input/output ports, virtual channels per port, buffer depth per virtual channels.

$$B = \sum_{i=1}^{n} (R_i * P_i) * V * D \qquad (1)$$

where, R_i is the total number of routers in i^{th} class, P_i is the total number of ports in router R_i. Routers having identical P_i belong to the same class. n is the total classes of router. V is the number of VC per port, Buffer depth per virtual channel is D. B is the overall topology buffer space.

The total buffer spaces used in Mesh and BFT (2D, 3D variants) topologies for the various virtual channel and buffer depth are presented in table 6. The first two columns are VC parameters, while the other columns show the amount of buffer space used in the Mesh and BFT (2D, 3D variants). Table 6's last two rows represent the number of routers and the number of ports (Rn, Pn) per router. There are two router classes (6 and 7 port) in 3D-4L Mesh, one class has 32 routers with six ports and the other has 32 routers with seven ports. For a router with 8 VCs per ports and 12 buffers per VC the total buffer space is 39936 flits. The total buffer space depends on R_i , P_i, V and D. Therefore, each topology's buffer space is different. In 3D-4L Mesh, the buffer space has increased by 9% and 30% for 6-port and 7-port routers (additional

Table 6: Buffer Space utilization of 2D and 3D Mesh and BFT variants.

		Total Buffer Space (flits)					
Buffer parameters		Mesh Topology			BFT Topology		
No. of Virtual channel(V)	No. of Buffer depth(D)	2D	3D-2L	3D-4L	2D BFT	3D-2L	3D-4L
4	4	5120	6144	6656	2368	2368	2368
	8	10240	12288	13312	4736	4736	4736
	12	15360	18432	19968	7104	7104	7104
6	4	7680	9216	9984	3552	3552	3552
	8	15360	18432	19968	7104	7104	7104
	12	23040	27648	29952	10656	10656	10656
8	4	10240	12288	13312	4736	4736	4736
	8	20480	24576	26624	9472	9472	9472
	12	30720	36864	39936	14208	14208	14208
(R_i,P_i)		(64,5)	(64,6)	(32,6) (32,7)	(4,4) (22,6)	(4,4) (22,6)	(4,4) (22,6)

TSV ports) respectively. 2D and 3D BFT variants have the same buffer space as no additional ports were required.

4.3. Buffer Space Equalisation (BSE)

From Table 6, it can be seen that, the buffer space varies between topologies. For a fair performance comparison between the topologies, the buffer space has been equalised. The number of VCs and buffer depth are modified to equalise the buffer space. Equation 2 represents the BSE and C_1, C_2 are the equalisation factors (positive or negative).

$$B_E = \sum_{i=1}^{n} (R_i * P_i) * (V + C_1) * (D + C_2) \tag{2}$$

2D Mesh NoC is considered as the baseline buffer space. Table 7 shows approximately($\pm$10%) equalised buffer space for all the topologies to the 2D Mesh buffer space. For 3D-2L Mesh, the buffer space changed from 36864 to 32256 after BSE because of the change in V from 8 to 7. The error in equalisation varied from 5% in case of D=4 and 12% in case of D=12 and 8% decrease in buffer space. For 3D-4L Mesh, the buffer space changed from 39936 to 32032 after BSE because of the change in V from 8 to 7 and the buffer space decreased 20% after BSE. In BFT topology, the buffer space changed from 14208 to 30720 after BSE because of the change in V from 8 to 12 for BFT variants and 2$\times$ buffer space increased.

4.4. The Resources Utilisation

The cost of interconnection networks depends on the area, number routers, links lengths and wiring complexity.The resource used for BSE topology variants is shown in Table 8. The horizontal links in the 3D-4L Mesh are reduced from 112 to 96, and 48 additional VL are provided compared to 2 D Mesh. There are 16 additional 3D-4L VL connections compared to 3D-2L Mesh.

5. Experimental Setup

Figure 9 shows the simulation framework used to evaluate the Mesh and BFT topology variants. The BookSim simulator was modified to simulate 3D

Table 7: Mesh and BFT (2D, 3D variants) buffer Space Equalisation for varying virtual channel and buffer depth

Mesh Topology									BFT Topology						
2D			2 Layer			4 Layer			2D			3D-2L		3D-4L	
V	D	Buffer space	V	D	Buffer space	V	D	Buffer space	V	D	Buffer space	D	Buffer space	D	Buffer space
	4	5120		3	4608		3	4992		6	5760	6	5760	6	5760
4	8	10240	4	7	10752	4	7	11648	6	11	10560	11	10560	11	10560
	12	15360		10	15360		10	16640		16	15360	16	15360	16	15360
	4	7680		4	7680		4	8320		6	7680	6	7680	6	7680
6	8	15360	5	8	15360	5	8	16640	8	12	15360	12	15360	12	15360
	12	23040		12	23040		12	24960		18	23040	18	23040	18	23040
	4	10240		4	10752		4	11648		5	9600	5	9600	5	9600
8	8	20480	7	8	21504	7	8	23296	12	11	21120	11	21120	11	21120
	12	30720		12	32256		11	32032		16	30720	16	30720	16	30720

Table 8: Resource used for Mesh and BFT (2D, 3D variants) topologies.

		Mesh Topology			BFT Topology		
		2D	3D-2L	3D-4L	2D	3D-2L	3D-4L
Network	X	8	8	4	4	4	4
	Y	8	4	4	3	3	3
	Z	1	2	4	1	2	4
Router	Size	64			28		
	In/out	5/5	6/6	6/6,7/7	4/4,8/8	4/4, 8/8	4/4, 8/8
Link Count	HL	112	108	96	48	40	36
	VL	0	32	48	-	8	12

Mesh and BFT topologies with configurable dimensions. Floorplan module takes topology, PEs size and router area to generate link length. These parameters are passed to link delay and power module. The delay of horizontal and vertical links is calculated using a link delay module. The horizontal link (T_{D_H}) delay is calculated using ORION, and vertical link delay(T_{D_TSV}) is calculated from TSV delay module. The delay of individual links is passed to the simulator to create topology(build network).

Power module takes the link length and router details to calculate the accurate power details. The vertical links power(T_{D_TSV}) is calculated using the TSV power module and the router (P_r) and horizontal links power(P_{D_H}) are calculated using ORION.

The mesh and BFT (two layers and four layers 3D) topology variants with TSV delay and TSV power modules are implemented BookSim2.0. The TSV power and delay module is a parameter based program using the equations from [21], [21] and [22]. XY and ZXY routing are used for 2D and 3D Mesh respectively. Nearest common ancestor algorithm implemented for the both 2D and 3D BFT.

Delays are estimated based on the link lengths derived from the floorplans

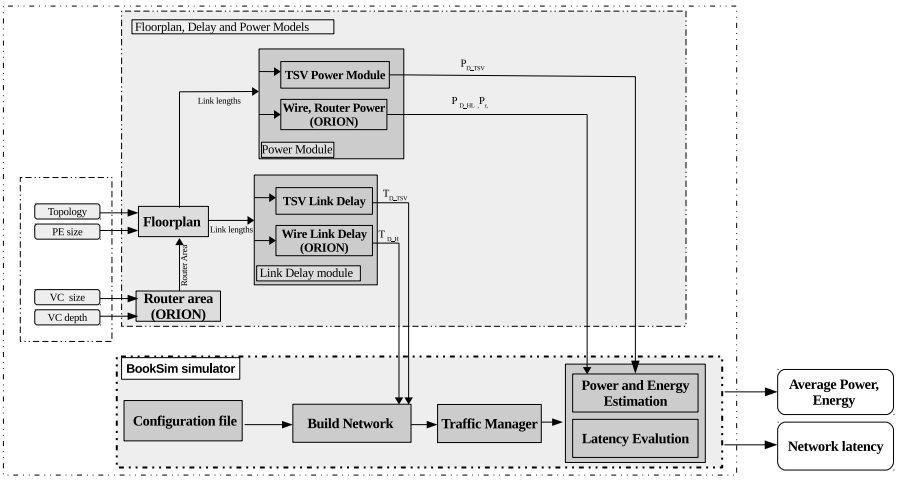


Figure 9: Simulation framework for evaluating power and performance. BookSim was extended with 3D TSV delay, power and link delay modules.

(Figures 3, 4,6, 7 and 8). The channel size is 64 bit. Table 9 describe the simulation configuration parameters of Mesh and BFT (2D, 3D variants) topologies.

6. Results and Discussion

6.1. BSE based Mesh and BFT Topology

Mesh and BFT topologies (2D, 3D variants) are evaluated based on equalised buffer space for fair comparison. The buffer space in all topology variants is equalised within 10% to keep resource cost similar and the Table 7 shows equalised buffer space. Figure 10 and 11 show the average network latency of 3D-2L and 3D-4l Mesh and BFT for both uniform and transpose traffic. The results are based on the equalised buffer space for V=8 and D=12.

Figure 10 (a) and (b) depict the average network latency of 3D-2L and 3D-4L Mesh with BSE and without BSE. There are 8% variation in network latency till 0.8 injection rate and reduces up to 10 to 12% after. From Figure 10 (b), There is up to 5% variation in network latency till 0.16 injection rate and reduces up to 12% after. Figure 10 (c) and (d) depicts average network latency of 3D-2L

Table 9: BookSim simulation configurations of Mesh and BFT (2D, 3D variants) topologies.

Simulation Parameter	Range of values
Topology	Mesh topology (2D & 3D-2L & 3D-4L) & BFT topology (2D & 3D-2L & 3D-4L)
Size of network	64 Nodes
Number of Switches	28 - 64
Traffic patterns	Uniform, Transpose and Bit-reversal
Number of Virtual channels	4, 6, 8
VC-buffers size	4, 8, 12
Total time (Simulation)	10^5 cycles

and 3D-4L Mesh for transpose traffic pattern. A 30 % reduction in the average network latency for 3D-2L Mesh and up to 15% reduction in the average network latency for 3D-4L Mesh after BSE.

Employing buffer equalisation, the buffer space of the 3D-2L and 3-layer 3D Mesh variants decreased up to 15% for each V and D as shown in the Table 7, 3D Mesh variants show a small variation in the network latency till the saturation point.

In the BFT variants, buffer space increases up to 2× in both variants after BSE as shown in Table 7. Figure 11 depict the comparison of average network latency for uniform and transpose traffic patterns of BFT variants.

Figure 11 (a), (b) and (c) depict average network latency of 2D, 3D-2L, 3D-4L BFT for uniform traffic pattern. Figure 11 (a) the average network latency is reduced up 60% till 0.04 injection rate. This is observed due to increased buffer space for 2D BFT compared to without BSE. After 0.04 injection rate the network latency has increased up 20% due to transferring more data flits compared to without BSE based topology and in 2D BFT with BSE saturation

is increased to 0.04 from 0.002. Figure 11 (b) the average network latency is reduced up 10% till 0.02 injection rate. After 0.04 injection rate, the network latency has increased up 45% due to transferring more data flits compared to without BSE based topology. Figure 11 (c) the average network latency is reduced up 53% till 0.04 injection rate. After 0.04 injection rate, the network latency has increased up 55% due to transferring more data flits compared to without BSE based topology.

The transpose traffic (Figure 11(d),11(e),11 (f)) pattern has up to 2× saturation point and a 10% reduction in average network latency compared to uniform traffic in all variants of BFT topology. The network latency has reduced in BFT till saturation point.

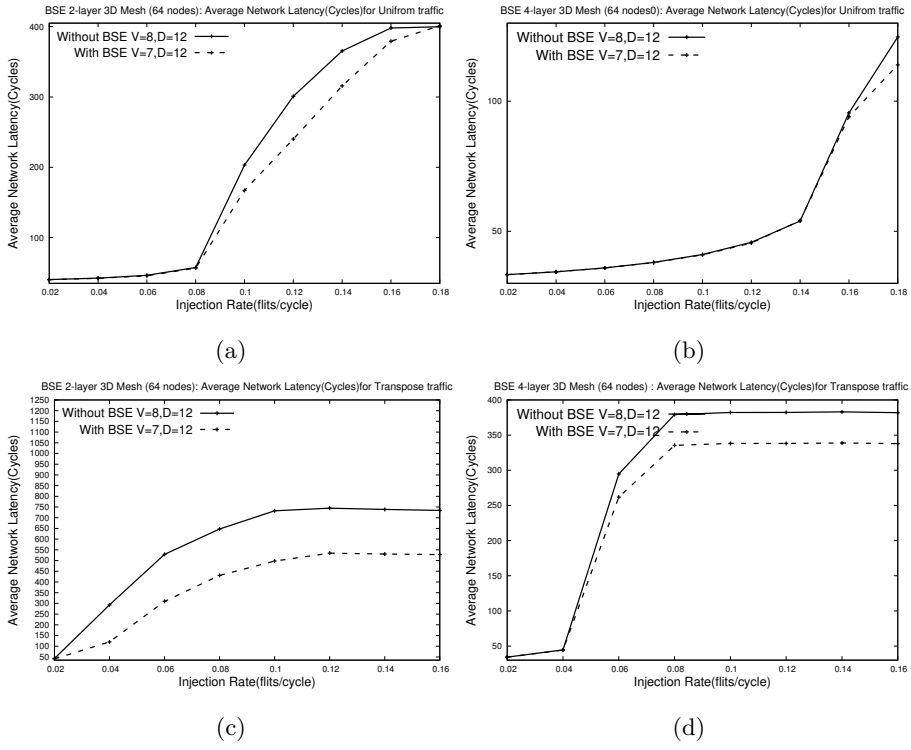


Figure 10: Average network latency comparison after BSE (varying VC and D) (a) 3D-2L Mesh uniform traffic (b) 3D-4L Mesh uniform traffic (c) 2D Mesh transpose (d) 3D-2L Mesh transpose traffic(f) 3D-4L Mesh transpose traffic

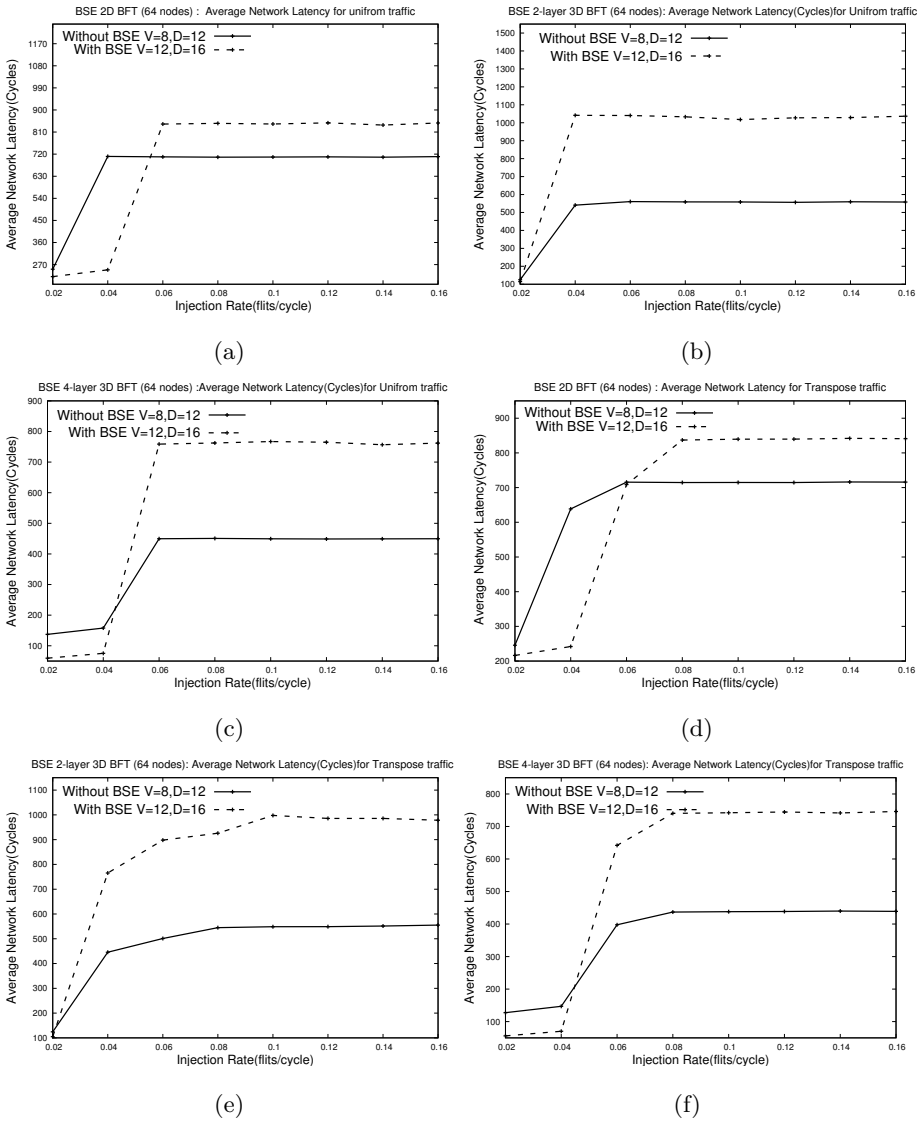


Figure 11: Average network latency comparison after BSE (varying VC and D) (a) 2D BFT uniform traffic (b) 3D-2L BFT uniform traffic (c) 3D-4L BFT uniform traffic (d) 2D BFT transpose (e) 3D-2L BFT transpose traffic(f) 3D-4L BFT transpose traffic

6.2. BFT vs Mesh Topology

The normalised performance of Mesh and BFT are depicted in Figure 12 for uniform and transpose traffic patterns. The performance is normalised to 2D

BFT topology.

Figure 12 (a) shows the performance normalization of all variants for uniform traffic pattern. The 3D-4L Mesh performance is up to 5× compared to 2D Mesh, up to 4× compared to 3D-2L Mesh, 12× compared to 2D BFT. 14× to 3D-2L BFT and 12× compared to 3D-4L BFT. Link length in Mesh is up to 80% shorter compared to BFT topology, and vertical links have a reduction in delay up to 75%. Hence the 3D-4L Mesh outperforms all other variants.

The 3D-2L and 3D-4L BFT have 40% and 2.6× improvement in normalised performance till 0.02 injection rate and after that, 3D-2L and 3-layer 3D BFT losses 19% and 21% normalised performance compared to 2D BFT. The 3D BFT variants lose performance because of while going from 2D to 3D the level 2 to level 3 links length has increased to 2× compared to 2D BFT, and as injection rate increases there is more contention in the network.

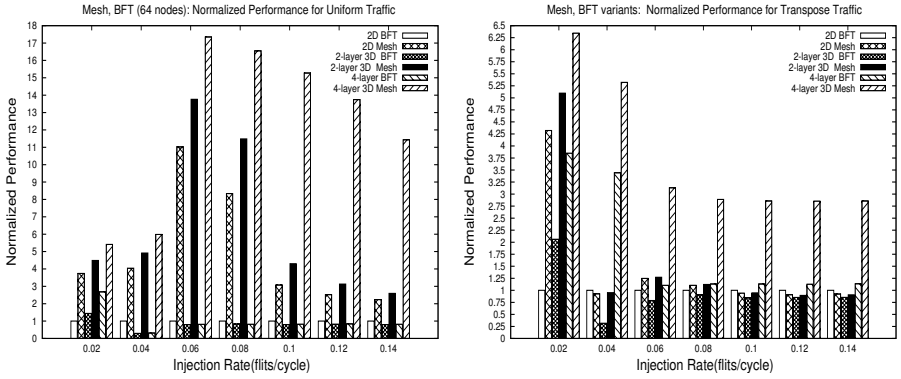


Figure 12: Normalized performance between 2D Mesh and 3D Mesh and BFT variants for (a) Uniform traffic (b) Transpose traffic.

Figure 12 (b) shows the performance normalization of all variants for transpose traffic pattern. 3D-4L Mesh performance best over all. 3D-4L Mesh has normalized performance 1.4× to 3.4× compared to 2D Mesh, 1.2× to 3.1× compared to 3D-2L Mesh, 4.5× compared to 2D BFT. 3.4× to 3D-2L BFT and 2.5× compared to 3D-4L BFT.

The 3D-2L and 3D-4L BFT have 2× and 3.8× improvement in normalised

performance till 0.02 injection rate, and after that, 3D-2L BFT loses average 6% normalised performance compared to 2D BFT. The 3D BFT variants lose performance because of the level 2 to level 3 links lengths has increased by 2× compared to 2D BFT.

The 3D-4L Mesh has 5× normalized performance compared to 3D-4L BFT. Hence, 3D-4L Mesh has least average network latency compared to other Mesh, BFT variants. There are 36 additional routers and 2× additional links in Mesh compared to BFT which leads to distribute traffic over the network, i.e. reduced waiting time at the buffers.

It is observed that there is a drop in maximum normalised performance from 17 to 6.25 in Figure 12 (a) and (b), Mesh topology performs better in uniform compared to transpose due to the better distribution of traffic in the network. In BFT, the transpose traffic pattern has 1.5× improvement normalised performance than the uniform traffic pattern as BFT is suited for localised traffic rather than uniformly distributed traffic.

6.3. Flit Energy Analysis

Total Power consumption is calculated as the sum of the powers of links and routers. The formula for power consumption is given by Equation 3. P_t is the total power, P_r, P_l, P_{tsv} are powers of the routers, links and TSVs respectively.

$$P_t = P_r + P_l + P_{tsv} \tag{3}$$

$$P_{\mathrm{TSV}} = AF \,.\, C_{\mathrm{TSV}} \,.\, V^2 \,.\, f \tag{4}$$

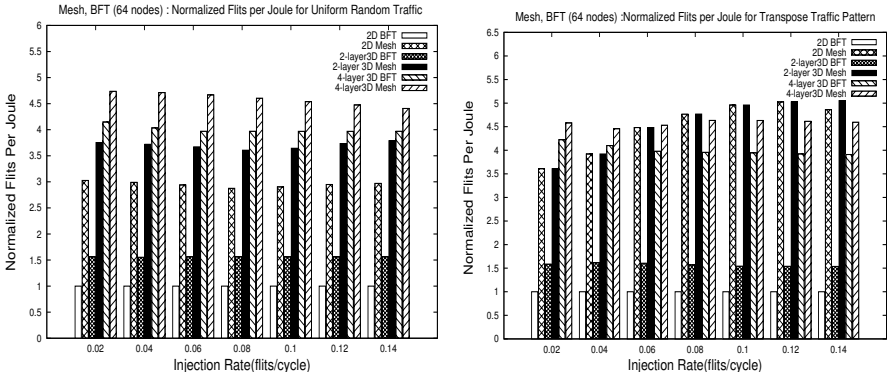
P_{tsv} was obtained using Equation 4, where AF is the activity factor, TSV capacitance is C_{TSV}. V is voltage and f is the operating frequency[21].

Equation 5 shows the calculation of C_{TSV}. In Equation 5, ϵ is the silicon substrate permittivity, and conductivity of the silicon substrate, σ. From Figure 2 (b), sum of insulator and bump2 capacitance is C_1, C_2 is the silicon substrate capacitance and C_3 is the under-fill capacitance.

$$C_{\mathrm{tsv}} = C_3 + \frac{C_1 * C_2 * (1 + \sigma_{\mathrm{Cu}}/(\varepsilon_{\mathrm{si}} * \omega))}{C_1 + 2 * C_2 * (1 + \sigma_{\mathrm{Cu}}/(\varepsilon_{\mathrm{si}} * \omega))} \qquad (5)$$

Flits per Joules (FpJ) is calculated using Equation 6, $\mathrm{F_t}$ is the total number flits delivered throughout the simulation and T is the total simulation in the cycle. Figure 13 (a) and (b) shows the average Flits per Joules of 2D and 3D Mesh and BFT variants for uniform and transpose traffic patterns respectively.

$$FpJ = \frac{F_{\mathrm{t}}}{(P_{\mathrm{t}} * T)} \qquad (6)$$



(a) (b)

Figure 13: Mesh and BFT (2D, 3D variants) topologies normalized Flits per Joules for (a) Uniform traffic (b) Transpose traffic.

Figure 13 (a) plots the normalised Flits per joule of all variants for uniform traffic pattern. The 3D-4L Mesh topology delivers up to 1.5× Flits per joule compared to 2D Mesh and 1.2× more than 3D-2L Mesh. The 3D-4L Mesh topology has up to 4.5× Flits per joule compared to 2D BFT, 3.2× than 3D-2L BFT and 1.15× than 3D-4L BFT.

In Figure 13 (b) plots the normalised Flits per joule of all variants for transpose traffic pattern. The 3D-4L Mesh topology has up to 1.15× Flits per joule compared to 2D Mesh and 1.1× than 3D-2L Mesh. The 3D-4L Mesh topology

has up to 4.5× Flits per joule compared to 2D BFT, 2.9× than 3D-2L BFT and 1.1× than 3D-4L BFT.

The BFT topology has a lower flits per joule compared to Mesh topology because of the longer link lengths in the BFT. BFT has up to 3× longer horizontal links than the Mesh topology. As we move towards 3D from 2D, flits per joule increased up to 1.5× in 3D-2L and up to 3.9× flits per joule in 3D-4L BFT compared to 2D BFT topology. A Higher flits per joule in 3D variants is seen as eight horizontal links in 3D-2L and 12 horizontal links in 3D-4L are converted to TSVs.

6.4. Energy Delay Product (EDP)

Figure 14 (a) and (b) depict the Mesh and BFT variants(2D, 3D-2L and 3D-4L) EDP comparison for uniform and transpose traffic respectively. EDP compared for 0.02 injection rate as minimum and 0.1 maximum injection rate. It is observed that 3D-4L Mesh has lowest EDP compared to 3D-2L Mesh, 2D Mesh, 2D BFT, 3D-2L BFT and 3D-4L BFT for both traffic pattern. In

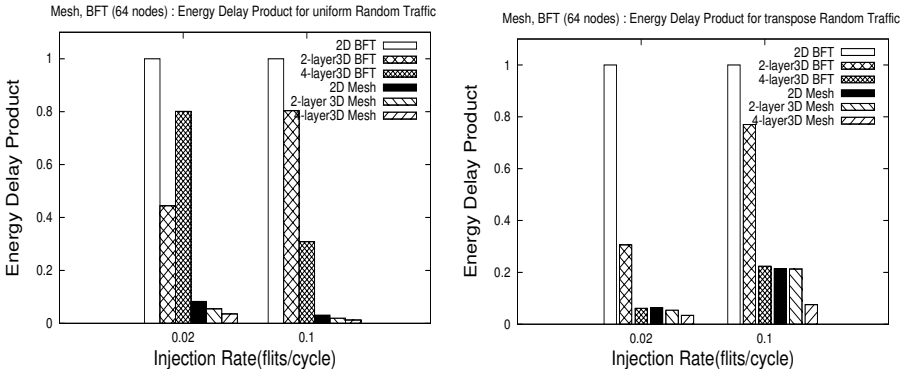


Figure 14: Normalized EDP of Mesh and BFT (2D, 3D variants) for (a) Uniform traffic (b) Transpose traffic

comparison with 3D BFT variants, the 3D Mesh variants have the lowest EDP since the link lengths for 3D meshing decreased by 80 %, and the TSV count increased up-to 3×.

7. CONCLUSION

The microarchitectural design space of 2D and 3D Mesh and BFT topologies have been explored. The conventional 2D Mesh with 3D-2L Mesh, 3D-4L Mesh, 2D BFT, 3D-2L BFT and 3D-4L BFT topologies are evaluated for performance and energy trade-offs. All variants were analysed after buffer equalization for a fair evaluation. Horizontal link delay and power were estimated through microarchitectural models from ORION. TSV delay models were used for delay calculation of vertical links. The lengths of horizontal links and TSVs were estimated using the floorplans. Analysis of topologies were carried out using uniform random traffic and transpose traffic.

3D-4L Mesh with uniform traffic exhibits a performance improvement of up to 2.3× compared to other Mesh variants. 3D-4L BFT with transpose traffic shows an improvement in performance up to 1.3× over all other BFT variants. BFT with transpose traffic pattern has a 1.5× improvement in performance compared to uniform traffic pattern showing that BFT is suitable for localised traffic rather than uniformly distributed traffic. The improved performance in 3D-4L Mesh and BFT is due to the replacement of horizontal wires with the TSVs. The wire delay is 4× greater than the TSV delay. After buffer space equalisation, the 3D-4L Mesh has improved performance of 5× - 12× against all the other variants. The 3D Mesh performance is improved compared to the BFT as vertical links reduce the delay up to 75% compared to the horizontal links. Hence the 3D-4L Mesh outperforms all other variants. 3D-4L Mesh has up to 4.5× Flits per Joule, and up to 80% lesser Energy Delay Product compared to other variants. The EDP is reduced, and FpJ is increased in 3D-4L Mesh because of the 80% shorter link lengths and 3× larger TSVs in Mesh compared to BFT topology.

References

[1] B. Grot, J. Hestness, S. W. Keckler, O. Mutlu, Express cube topologies for on-chip interconnects, in: High Performance Computer Architecture, 2009.

HPCA 2009. IEEE 15th Int. Symp. on, IEEE, 2009, pp. 163–174.

[2] D. H. Kim, K. Athikulwongse, S. K. Lim, A study of through-silicon-via impact on the 3d stacked ic layout, in: Proc. of the 2009 International Conference on Computer-Aided Design, ACM, 2009, pp. 674–680.

[3] V. F. Pavlidis, E. G. Friedman, 3d topologies for networks-on-chip, IEEE Trans. Very Large Scale Integr. Syst. 15 (10) (2007) 1081–1090.

[4] A. Psathakis, V. Papaefstathiou, N. Chrysos, F. Chaix, E. Vasilakis, D. Pnevmatikatos, M. Katevenis, A systematic evaluation of emerging mesh-like CMP NoCs, in: Architectures for Networking and Communications Systems (ANCS), 2015 ACM/IEEE Symp. on, IEEE, 2015, pp. 159–170.

[5] B. Halavar, U. Pasupulety, B. Talawar, Extending booksim2.0 and hotspot6.0 for power, performance and thermal evaluation of 3d noc architectures, Simulation Modelling Practice and Theory (2019) 101929.

[6] P. M. Yaghini, A. Eghbal, S. S. Yazdi, N. Bagherzadeh, M. M. Green, Capacitive and inductive tsv-to-tsv resilient approaches for 3d ics, IEEE Transactions on Computers 65 (3) (2016) 693–705.

[7] N. Jiang, D. U. Becker, G. Michelogiannakis, J. Balfour, B. Towles, D. E. Shaw, J.-H. Kim, W. J. Dally, A detailed and flexible cycle-accurate network-on-chip simulator, in: Performance Analysis of Systems and Software (ISPASS), 2013 IEEE International Symposium on, IEEE, 2013, pp. 86–96.

[8] A. B. Kahng, B. Li, L.-S. Peh, K. Samadi, Orion 2.0: a fast and accurate noc power and area model for early-stage design space exploration, in: Proc. of the conference on Design, Automation and Test in Europe, European Design and Automation Association, 2009, pp. 423–428.

[9] P. P. Pande, C. Grecu, M. Jones, A. Ivanov, R. Saleh, Performance evaluation and design trade-offs for network-on-chip interconnect architectures, IEEE Transactions on Computers 54 (8) (2005) 1025–1040.

[10] E. Carara, F. Moraes, N. Calazans, Router architecture for high-performance nocs, in: Proceedings of the 20th Annual Conference on Integrated Circuits and Systems Design, SBCCI '07, ACM, New York, NY, USA, 2007, pp. 111–116.

[11] C. H. O. Chen, N. Agarwal, T. Krishna, K.-H. Koo, L.-S. Peh, K. C. Saraswat, Physical vs. virtual express topologies with low-swing links for future many-core nocs, in: Proceedings of the 2010 Fourth ACM/IEEE Int. Symp. on Networks-on-Chip, NOCS '10, IEEE Computer Society, Washington, DC, USA, 2010, pp. 173–180.

[12] B. S. Feero, P. P. Pande, Networks-on-chip in a three-dimensional environment: A performance evaluation, Computers, IEEE Transactions on 58 (1) (2009) 32–45.

[13] C. Grecu, P. P. Pande, A. Ivanov, R. Saleh, A scalable communication-centric soc interconnect architecture, in: International Symposium on Signals, Circuits and Systems. Proc., SCS 2003. (Cat. No.03EX720), 2004, pp. 343–348.

[14] M. Debora, P. Max, K. Marcio, C. Luigi, S. Altamiro, Performance evaluation of hierarchical NoC topologies for stacked 3D ICs, Proc. - IEEE Int. Symp. Circuits Syst. 2015-July (2015) 1961–1964.

[15] J. M. Joseph, C. Blochwitz, A. Garcia-Ortiz, T. Pionteck, Area and power savings via asymmetric organization of buffers in 3d-nocs for heterogeneous 3d-socs, Microprocessors and Microsystems 48 (2017) 36 – 47, extended papers from the 2015 Nordic Circuits and Systems Conference.

[16] B. K. Joardar, K. Duraisamy, P. P. Pande, High performance collective communication-aware 3d network-on-chip architectures, in: 2018 Design,

Automation Test in Europe Conference Exhibition (DATE), 2018, pp. 1351–1356.

[17] C. Sun, C. H. O. Chen, G. Kurian, L. Wei, J. Miller, A. Agarwal, L. S. Peh, V. Stojanovic, Dsent - a tool connecting emerging photonics with electronics for opto-electronic networks-on-chip modeling, in: 2012 IEEE/ACM Sixth International Symposium on Networks-on-Chip, 2012, pp. 201–210.

[18] K. Swaminathan, D. Thakyal, S. G. Nambiar, G. Lakshminarayanan, S.-B. Ko, Enhanced noxim simulator for performance evaluation of network on chip topologies, in: Engineering and Computational Sciences (RAECS), 2014 Recent Advances in, 2014, pp. 1–5.

[19] V. Catania, A. Mineo, S. Monteleone, M. Palesi, D. Patti, Cycle-accurate network on chip simulation with noxim, ACM Trans. Model. Comput. Simul. 27 (1) (2016) 4:1–4:25.

[20] L. Jain, B. Al-Hashimi, M. Gaur, V. Laxmi, A. Narayanan, Nirgam: a simulator for noc interconnect routing and application modeling, in: Design, Automation and Test in Europe Conference, 2007, pp. 16–20.

[21] J. Kim, J. Cho, J. S. Pak, T. Song, J. Kim, H. Lee, J. Lee, K. Park, I/o power estimation and analysis of high-speed channels in through-silicon via (tsv)-based 3d ic, in: 19th Topical Meeting on Electrical Performance of Electronic Packaging and Systems, 2010, pp. 41–44.

[22] D. Khalil, Y. Ismail, M. Khellah, T. Karnik, V. De, Analytical model for the propagation delay of through silicon vias, in: 9th International Symposium on Quality Electronic Design (isqed 2008), 2008, pp. 553–556.

[23] R. Weerasekera, M. Grange, D. Pamunuwa, H. Tenhunen, L. R. Zheng, Compact modelling of through-silicon vias (tsvs) in three-dimensional (3-d) integrated circuits, in: 2009 IEEE International Conference on 3D System Integration, 2009, pp. 1–8.

[24] M. Lee, J. S. Pak, J. Kim, Electrical Design of Through Silicon Via, Springer Publishing Company, Incorporated, 2014.

[25] G. Beanato, A. Cevrero, G. D. Micheli, Y. Leblebici, Impact of data serialization over tsvs on routing congestion in 3d-stacked multi-core processors, Microelectronics Journal 51 (2016) 38 – 45.

Authors

Bheemappa Halavar is currently Ph.D student(Research Scholar) in Computer Science and Engineering (CSE) Department at National Institute of Technology Karnataka (NITK), Surathkal, India. He received M.Tech. degree in Department PG studies from Visvesvaraya Technological University, Belagavi Karnataka in 2013. His research interests include in Network-on-Chips and High performance computing.

Basavaraj Talawar heads the the SPARK (Systems, Parallelization and Architecture Research at NITK) at the CSE department at NITK, Surathkal, India. He has a PhD from the Indian Institute of Science, Bangalore. His research interests are in Network-on-Chips, Simulation Acceleration and Parallelization. He is a recipient of the Visvesvaraya Young Research Fellowship from the Govt. of India and a faculty award from IBM. His research is supported through grants from the DST, IBM, and Intel.