

## **CSc 256 Chapter 9 Assignment**

PDF or MSWord .docx files due on iLearn Monday 12/12/2016, 5pm  
(no late submissions; 6% of your grade)

This is an individual project. Work on your own. All submissions *must* be typed. Submit via the iLearn submission link. [Both Word docx and pdf versions of this document available at iLearn.]

### **Problem 1:**

Suppose we have a 8KB direct-mapped data cache with 4-byte blocks.

a) Show how a 32-bit memory address is divided into tag, index and offset. Show clearly how many bits are in each field. (10 points)

ANS:

b) How many total bits are there in this cache? (15 points)

ANS:

c) Consider this address trace:

0x404c4958  
0x404c46d8  
0x404c4944  
0x404c86d8  
0x40544944  
0x404c4958  
0x404c86d8  
0x404c4970

For this cache, for each address in the above trace, show the tag, index and offset in binary. Indicate whether each reference is a hit or a miss. What is the miss rate? (20 points)

ANS:

address	tag	index	offset	Hit/miss
0x404c4958				
0x404c46d8				
0x404c4944				
0x404c86d8				
0x40544944				
0x404c4958				
0x404c86d8				
0x404c4970				

miss rate =

**Problem 2:**

Suppose we have a 8KB direct-mapped data cache with 64-byte blocks.

a) Show how a 32-bit memory address is divided into tag, index and offset. Show clearly how many bits are in each field. (10 points)

ANS:

b) How many total bits are there in this cache? (15 points)

ANS:

c) For this cache, for each address in the trace in Problem 1c, show the tag, index and offset in binary. Indicate whether each reference is a hit or a miss. What is the miss rate? (15 points)

ANS:

address	tag	index	offset	Hit/miss
0x404c4958				
0x404c46d8				
0x404c4944				
0x404c86d8				
0x40544944				
0x404c4958				
0x404c86d8				
0x404c4970				

miss rate =

**Problem 3 (15 points):**

We are comparing the two caches in Problem 1 and Problem 2. Suppose the cache in Problem 1 has a hit time of 1 cycle; the one in Problem 2 has a hit time of 2 cycles. The miss penalty for both is 50 cycles. Calculate the total time taken (in cycles) for all accesses, for each cache.

ANS: