

Bheemappa Halavar

Assistant Professor

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EDUCATION

- **National Institute of Technology Karnataka** Karnataka, India
Ph.D in Computer Science and Engineering (Computer Architecture) 2015 -2020
- **Visvesvaraya Technological University** Karnataka, India
M.Tech in Computer Network Engineering; CGPA 7.75 First Class 2011-2013
- **Visvesvaraya Technological University** Karnataka, India
B.Tech in Information Science and Engineering; 71% First Class with Distinction 2007-2011

SKILLS SUMMARY

- **Languages:** C, C++, PHP, HTML, SQL, Python, Java, C++, Unix scripting
- **Tools:** Cloud Deployment, Linux Administration, Matlab,

EXPERIENCE

- **Dept. of Computer Science and Engineering** MSRIT, Karnataka
Assistant Professor Sept.2019 -
- **Dept. of Computer Science and Engineering** NITK, Karnataka
Research Scholar Jan 2015 - Sep 2019
 - **Teaching Assistantship:** Courses: Computer architecture, Computer Organisation, Parallel Programming (2014-2019).
- **Secab Institute of Engineering and Technology** Karnataka, India
Assistant Professor Aug 2013-Dec 2014
 - **Courses:** Web Programming, Computer Networking, Wireless networks, C# and .Net and socket programming

ACADEMIC PROJECTS

- **Online Share Trading System**
A web based interface for users to bid, buy and sell shares.
- **Cognitive Characterization Of Learner Behaviour Based On Brain Lateralization and Other Parameters**
This project attempts at developing a system that classifies the learner into Cognitive categories based on assessing the learner based on brain lateralization and other parametric tests.
- **Power and Performance optimal 3D NoC architecture (Ongoing).**
The goal of the project is quantitative analysis of 3D NoC architecture and Design of power optimal 3D NoC architectures. NoCs on 3D ICs technology provides an opportunity to better the on chip communication delay, energy and area parameters compared to the 2D-NoCs. We are extending the existing simulators to support 3D-NoC topologies. Design space exploration of 3D-NoC is being driven by considering physical characteristics of vertical connections like Through Silicon Vias (TSVs). The exploration is aided using power, performance and cost metrics such as area, throughput, avg. flit latency, Energy per bit transferred, and EDP.

JOURNALS

1. B. Halavar and B. Talawar, *Power and Performance Analysis of 3D Network on Chip Architectures*", Computers & Electrical Engineering - Journal - Elsevier [Accepted].
2. B. Halavar , U.Pasupulety and B. Talawar, *Extending BookSim and HotSpot for Power, Performance and Thermal evaluation of 3D NoC Architectures*, Simulation Modelling Practice and Theory, Elsevier.
3. B. Halvar, B Talawar, "A Power and Performance Optimal 3D BFT NoC Architecture" -IET Computers & Digital Techniques [Communicated].

CONFERENCE

1. B. Halavar and B. Talawar, *Accurate Performance Analysis of 3D Mesh Network on Chip Architectures*, 2018 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT), March-2018.
2. B. Halavar and B. Talawar, *Floorplan Based Performance Evaluation of 3D Variants of Mesh and BFT Networks-on-Chip*, International Conference on Signal Processing and Communication (SPCOM), July-2018.
3. B. Halavar and B. Talawar, *OP3DBFT: A Power and Performance Optimal 3D BFT NoC Architecture*, 18th International Conference on Intelligent Systems Design and Applications(ISDA).India, Dec-2018.
4. U.Pasupulety, B. Halavar and B. Talawar, *Accurate Power and Latency Analysis of a Through-Silicon Via(TSV)*, 7th International Conference on Advances in Computing, Communications and Informatics (ICACCI), Sep-2018.
5. U.Pasupulety, B. Halavar and B. Talawar, *Thermal Aware Design for Through-Silicon Via (TSV) based 3D Network-on-Chip (NoC) Architectures*, 8th Int'l Symp. on Embedded computing & system Design(ISED), Dec-2018,

PERSONAL DETAILS

- Name : BHEEMAPPA HALAVAR
- DOB : 30/09/1989.
- Fathers Name :HANUMANTHAPPA HALAVAR.
- Mothers Name : SHANTADEVI HALAVAR.
- Languages : English, Kannada,Hindi.