ASIAN COLLEGE OF HIGHER STUDIES

ACHS

COLLEGE OF IT AND COMPUTER SCIENCE

LAB REPORT COVER PAGE

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Initial Submission Date: .....

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Course Name: Microprocessor

Course Code: CSC167

Semester: 2nd

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Evaluator's Comment:

Evaluator's Signature: .....

LAB 4:- Familiarization with ADD, ADI, SUB, SUI, RLC, RRC, RAR, CMA Instructions

Objectives:

-> To demonstrate the basic understanding of arithmetic group instructions, logical group instructions and logical rotate instructions
-> To add or subtract the contents of register/ mememory to the contents of the accumulator.
-> To complement the contents of the accumulator.
-> To rotate the accumulator data left or right.

Introduction:-

Arithmetic group Instructions:-
The 8085 microprocessor perform various arithmetic operations such as addition, subtraction, increment and decrement. The arithmetic operation add and subtract are performed in relation to the contents of accumulator. Arithmetic group Instructions modify all the flags according to the data conditions of the result and also place the result in the accumulator.

The arithmetic group instructions include ADD, ADI, SUB, SUI etc

a. ADD:-

-> It is 1 byte add instruction which adds the contents of register/memory to the contents of the accumulator and stores the result in accumulator.
Eg:- Add B; A ← A+B

b. ADI 8 bit data :-

-> It is 2 byte add immediate instruction which adds the 8 bit data with the contents of accumulator and stores result in accumulator.

E.g. ADI 9BH ; A ← A+9BH

c. SUB R/M

-> It is 1 byte subtract instruction which subtracts the contents of specified register/m with the contents of accumulator and stores the result in accumulator.

E.g, SUB D ; A ← A-D

d. SUI 8 bit data

-> It is 2 byte subtract immediate instruction which subtracts the 8 bit data from the contents of accumulator stores result in accumulator.

E.g ; SUI D3H ;

logical Group Instructions :-

Microprocessor can perform all the logic functions of the hardwired logic through its instruction set. The 8085 instruction set include such logic functions as AND, OR, XOR and NOT.

The instructions implicitly assume that the accumulator is one of the operands. All instructions reset(clear) carry flag except for complement whereve flag remain unchanged. They modify Z, P and S flags according to the data conditions of the result. They also place result in the accumulator. They donot affect the contents of the operand register. some instructions are ANA, ANI, CMA etc

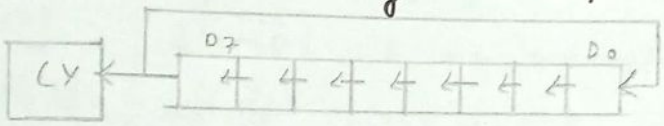
CMA (complement accumulator) :-

→ It is 1 byte instruction which complements the contents of the accumulator. It doesn't affect flag.

Logical Rotate instructions :-

a) RLC : Rotate accumulator left

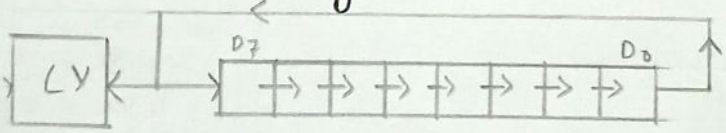
Here, each bit is shifted to the adjacent left position. Bit D_7 becomes D_0. The carry flag is modified according to D_7



$CY = D_7$, $D_7 = D_6$, $D_6 = D_5$, ... , $D_1 = D_0$, $D_0 = D_7$

b) RRC : rotate accumulator right

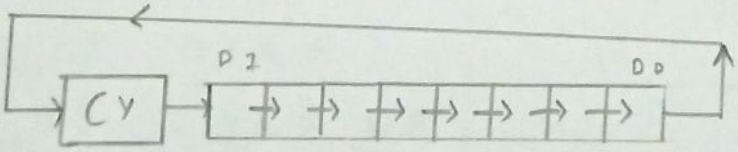
Here, each bit is shifted right to the adjacent position. Bit D_0 becomes D_7. The carry flag is modified according to D_0.



$CY = D_0$, $D_7 = D_0$, ..., $D_0 = D_1$

c) RAR : Rotate accumulator right through carry

Here, each bit is shifted right to the adjacent position. Bit D_0 becomes the carry bit and the carry bit is shifted into D_7.



$CY = D_0$, $D_0 = D_1$, ... , $D_7 = CY$

WAP to add number from 1 to 5 and finally add the sum with 03H.

Instruction	Description
MVI A,00H	loads data 00H to accumulator i.e A ← 00H
MVI B,05H	loads data 05H to specified HL pair address i.e [HL] ← 05H
UP: ADD B	adds the data of B register with accumulator and store result in accumulator. i.e A ← A+B
DCR B	decrease the data of register B by 1 i.e B = B - 1
JNZ UP	Jumps if no zero (if Z=0)
ADI 03H	adds immediate with accumulator i.e A = A+3
STA 2200H	stores the contents of accumulator to 2200H
HLT	

Memory view:

	0	1	2 ...
220	12	00	00
:			

Registers

A/PSW	0x 12 16
BC	0x 00 05
DE	0x 00 00
HL	0x 00 00
SP	0x FF FF
PC	0x 08 0F

Assembler output	
3E 00	MVI A,00H
06 05	MVI B,05H
80	UP~~LOOP~~: ADD B
05	DCR B
C2 04 08	JNZ UP
C6 03	ADI 03H
32 00 22	STA 2200H
76	HLT

Flags

Z	☐
S	☐
P	☑
C	☐
AC	☑

Program to illustrate the use of RLC, RRC

Instruction	Description
MVI A, 07 H	loads data 07H to the specified accumulator 07 = 0 0 0 0 0 1 1 1
RLC	shifts each bit to the adjacent left position CY = 0 0 0 0 0 1 1 1 0 = 0E H
MOV B, A	copies accumulator data to B register
RLC	CY = 0 0 0 0 1 1 1 0 0 = 1C H
RLC	CY = 0 0 0 1 1 1 0 0 0 = 38 H
ADD B	adds the data of B register with accumulator and store result in accumulator A = 38 + 0E i.e 0 1 0 0 0 1 1 0 = 46 H
RRC	shifts each bit right to the adjacent position CY = 0 0 0 1 0 0 0 1 1 = 23 H
HLT	

Assembler	output
3E 07	MVI A, 07H
07	RLC
47	MOV B, A
07	RLC
07	RLC
80	ADD B
0F	RRC
76	HLT

Registers

A/PSW	0x 23 12
BC	0x 0E 00
DE	0x 00 00
HL	0x 0000
SP	0x FFFF
PC	0x 0809

Flags

Z	☐
S	☐
P	☐
C	☐
AC	☑

ADD two number 33H and 78H and complement of accumulator result

Instruction	Description
MVI B, 33H	loads data 33H to the specified B register
ADI 78H	adds imeediate data 78H with accumulator
CMA	complements the contents of the accumulator
STA 2200H	stores the contents of accumulator in 2200H address
HLT	

output

memory view :-

	0	1	2	...
220	87			
221				
⋮				

Assembler output	
06 33	MVI B, 33H
C6 78	ADI 78H
2F	CMA
32 00 22	STA 2200H
76	HLT

Flags

Z	☐
S	☐
P	☑
C	☐
AC	☐

Registers

A / PSW	0x 87 06
BC	0x 33 00
DE	0x 00 00
HL	0x 00 00
SP	0x FF FF
PC	0x 08 08

Find the output of following program

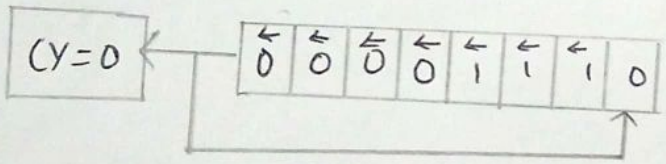
MVI A, 07 H	86 07
RLC	07
MOV B, A	47
RAR	1f
RLC	07
SUB B	90
RAR	1F
HLT	76

Here,

Accumulator is loaded with immediate data 07H

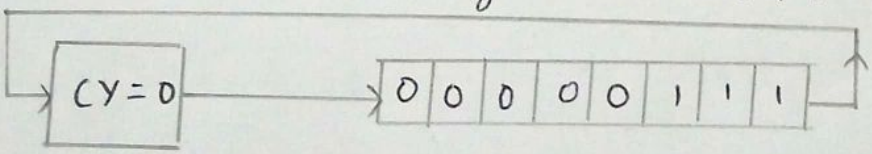
RLC: Rotate left accumulator where $D_7 = D_6$, $D_6 = D_5$, $D_0 = D_7$, carry $= D_7$.

07H = 00000111



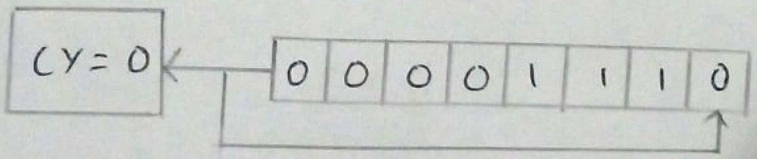
Here, 0E H i.e 00001110 is stored in register B.

RAR Rotate accumulator right through carry where, D_0 = carry and carry bit shift into D_7.



After RAR instructions, accumulator is loaded with 00000111 H data.

RLC



so,
again the data is 07H loaded in accumulator which is later subtracted to register B i.e 07H resulting 0H as final result.

Registers:

A/PSW	00	56
BC	0E	00
SP	FF	FF
PC	08	09

Flags:

Z	S	P	C	AC
✓		✓		✓