Homework 6

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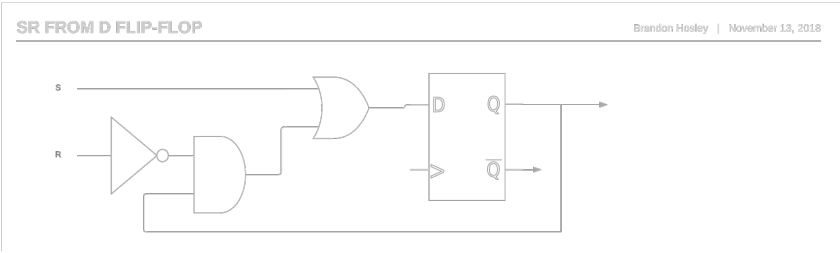
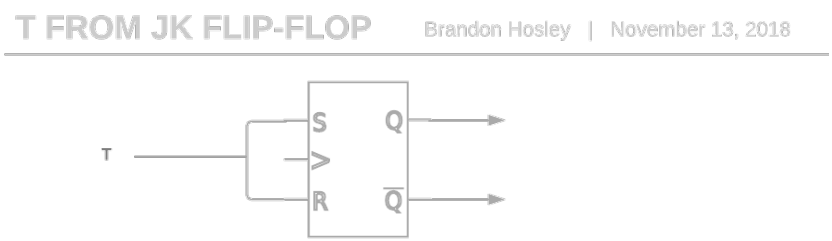
Problem 1

Draw the Design Table, the K-maps and the circuit for:

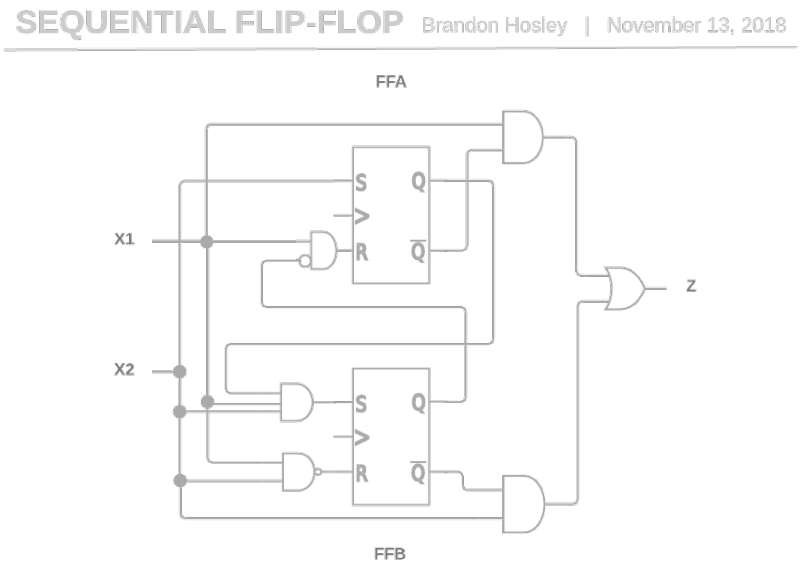
a. *Construct an SR flip-flop from a D flip-flop*



b. *Construct a T flip-flop from a JK flip-flop*



Problem 2



A(t)	B(t)	$X_1(t)$	$X_2(t)$	Z(t)	JA(t)	KA(t)	JB(t)	KB(t)	A($t+1$)	B($t+1$)
0	0	0	0	0	0	0	0	1	0	0
0	0	0	1	1	1	0	0	1	1	0
0	0	1	0	1	0	1	0	1	0	0
0	0	1	1	1	1	1	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	0	1	0	1	0	0	1	1	0
0	1	1	0	1	0	0	0	1	0	0
0	1	1	1	1	1	0	0	0	1	1
1	0	0	0	0	0	0	0	1	1	0
1	0	0	1	1	1	0	0	1	1	0
1	0	1	0	0	0	1	0	1	0	0
1	0	1	1	1	1	1	1	0	0	1
1	1	0	0	0	0	0	0	1	1	0
1	1	0	1	0	1	0	0	1	1	0
1	1	1	0	0	0	0	0	1	1	0
1	1	1	1	0	1	0	1	0	1	1

Problem 3

Textbook page 593, #16 (d) Show the Truth Table, the K-maps (There will be two – one for each Flip-Flop) and then finally draw the circuit.

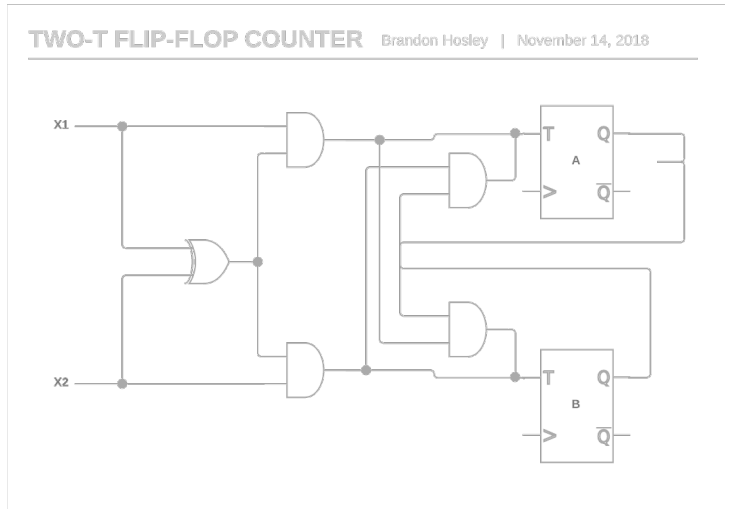
A(t)	B(t)	X_1	X_2	A($t+1$)	B($t+1$)
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	1
0	0	1	1	0	0
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	1	1
1	1	0	1	0	0
1	1	1	0	1	0
1	1	1	1	1	1

A($t+1$)

A \ B, X_1X_2	00	01	11	10
0	0	1	x	1
1	0	1	x	1
1	1	0	x	0
0	1	0	x	0

B($t+1$)

A \ B, X_1X_2	00	01	11	10
0	0	1	x	1
1	1	0	x	0
1	1	0	x	0
0	1	0	x	1



Problem 4

A sequential circuit has three state registers (or flip-flops) and 3 inputs

(a) How many states does it have?

$2^3 = 8$ Possible Flip-Flop states;

(b) How many transitions from each state does it have?

$2^3 = 8$ Possible switch states;

(c) How many total transitions does it have?

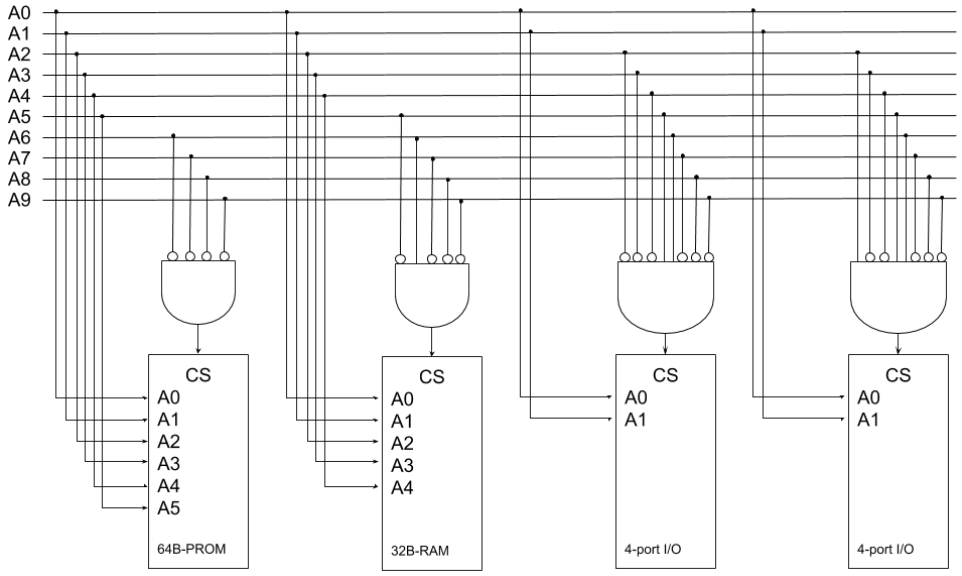
$8 \times 8 = 64$

Number of Switch States $\times$ Number of Flip-Flop States.

Problem 5

Textbook page 594, #21(a)

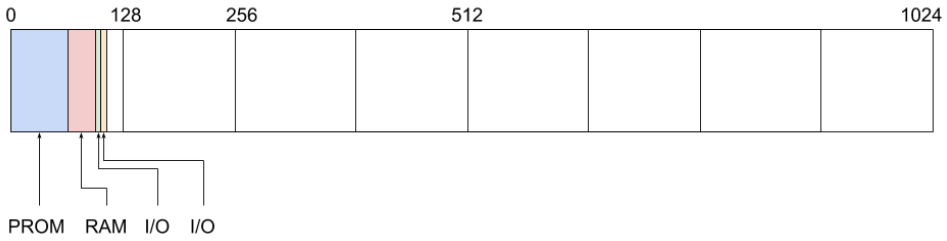
(a) Draw the Full Address decoding – Similar to Fig 11.48 .



(b) Include a table similar to Fig 11.47 .

Device	64 x 8 PROM	32 x 8 RAM	4-Port I/O	4-Port I/O
Minimum Address	00 0000 0000	00 0100 0000	00 0110 0000	00 0110 0100
Maximum Address	00 0011 1111	00 0101 1111	00 0110 0011	00 0110 0111
General Address	00 00xx xxxx	00 010x xxxx	00 0110 00xx	00 0110 01xx

(c) Draw a Memory Map like in Fig 11.50 and show which addresses each chip is enabled .



(d) Can you add additional chips on this bus? Explain .

Yes, this bus has plenty of seating left. This chipset arrangement would be able to fit into an 7-bit addressed bus, this 10-bit has 8-times the capacity currently used. 920 addresses remain available.

References

Warford, J. (2009). *Computer systems* (4th ed.). Jones and Bartlett.