**CDAC Feb 2015**

**LAB 4**

Q4. 16 x 16 Bidirectional Memory

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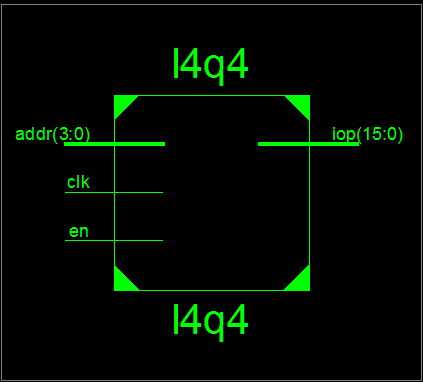
**16 x 16 Bidirectional Memory**

# Design Approach:

A Ram memory is non-volatile which is used to store the data using the d flip-flops .The outputs of the each d flip-flop is concatenated and passed as a single input to the multiplexer and depending on the read address the output is read.

* We design bidirectional 16 x16 memory by using behavioural modelling.
* Here we design the 16 x16 Ram memory using the component of tri state buffer .
* First check for the clk if clk is 1 then we will check for enable pin otherwise it maintain the previous data
* If enable is high then it write the data .

**Block Diagram:**

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**Fig 1:- Block Diagram**

**Source Code:**

module l4q4 (inout [15:0] iop,input clk,en,input [3:0] addr);

reg [15:0] mem [15:0];

reg [15:0] temp ;

bufif0 u0 [15:0] (iop,temp,en);

always @ (posedge clk)

begin

if(en==1)

mem[addr]<=iop;

else

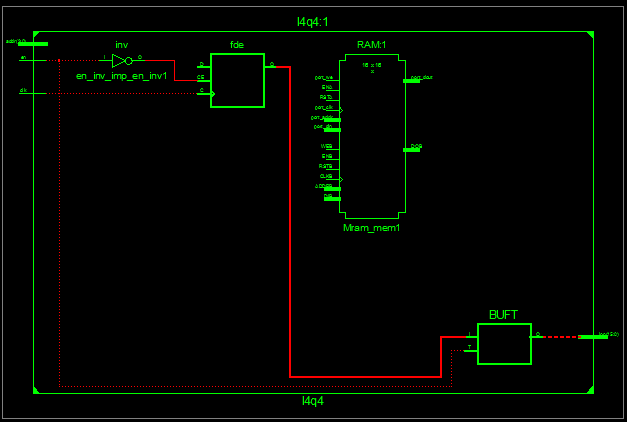
temp<=mem[addr];

end

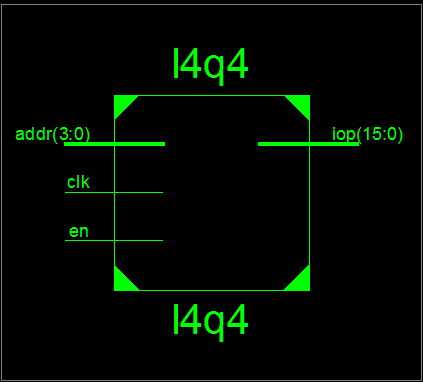
endmodule

**Synthesis:**

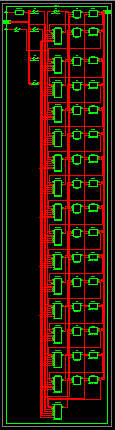
1. RTL Schematic



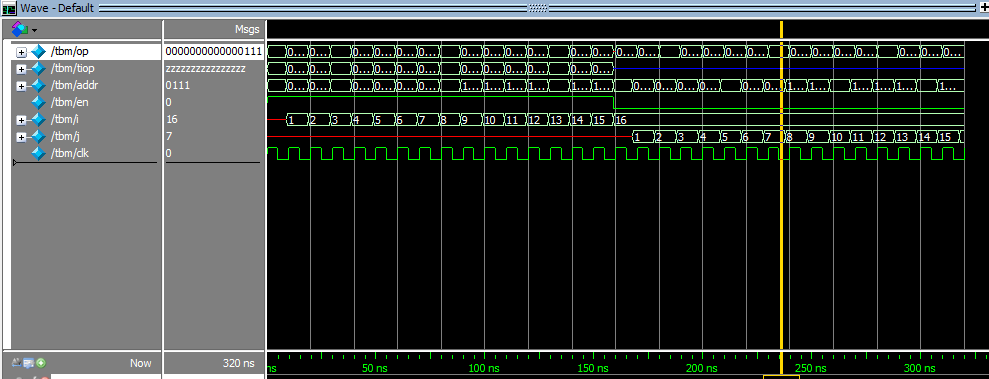
1. Block Diagram

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1. Tech Schematic



1. Simulation Waveform Result

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**Error:**

None

**Verified by:**

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