**CDAC Feb 2015**

Arithmetic Logical Unit

Name: Bhrigu Bhargava

**ALU**

# Design Approach:

The arithmetic logical unit performs various mathematical functions. This can be utilized to perform different gate based functions. We designed this using package designing and inside the package called multiple functions and performed various functionality under respective functions. When the functions were called then their respective functionality was performed.

**Source Code:**

module alu(c,borrow,carry,equal,less,more,a,b,alu\_control);

output reg[7:0]c=0;

output reg borrow=0,carry=0,equal=0,less=0,more=0;

input [7:0]a,b;

input [2:0]alu\_control;

always @ (\*)

begin

case(alu\_control)

3'd0 : begin

{carry,c} =(a + b); //Addition//

$display ("IN ADDITION a=%b b=%b alu\_control=%d carry=%b, c=%b",a,b,alu\_control,carry,c);

end

3'd1 : begin

{borrow,c} =(a - b); //Subtraction//

$display ("IN SUBTRACTION a=%b b=%b alu\_control=%d borrow=%b c=%b",a,b,alu\_control,borrow,c);

end

3'd2 : begin

c = a ^ b; //XOR operation//

$display ("IN XOR a=%b b=%b alu\_control=%d c=%b",a,b,alu\_control,c);

end

3'd3 : begin

c = a & b; //AND operation//

$display ("IN AND a=%b b=%b alu\_control=%d c=%b",a,b,alu\_control,c);

end

3'd4 : begin

c = ~(a | b); //NOR operation//

$display ("IN NOR a=%b b=%b alu\_control=%d c=%b",a,b,alu\_control,c);

end

3'd5 : begin

c = ~(a & b); //NAND operation//

$display ("IN NAND a=%b b=%b alu\_control=%d c=%b",a,b,alu\_control,c);

end

3'd6 : begin//Comparison operation//

if(a>b)

begin

more=1'b1;

end

else if(b>a)

begin

less=1'b1;

end

else

begin

equal=1'b1;

end

$display ("IN COMP a=%b b=%b alu\_control=%d more=%b less=%b equal=%b ",a,b,alu\_control,more,less,equal);

end

default: begin

c=1'b0;

equal=0;

less=0;

more=0;

carry=0;

borrow=0;

$display("Invalid ALU signal");

$display("Invalid Selection alu\_control=%d", alu\_control);

end

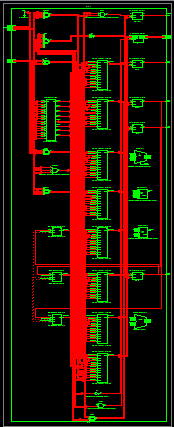
endcase

end

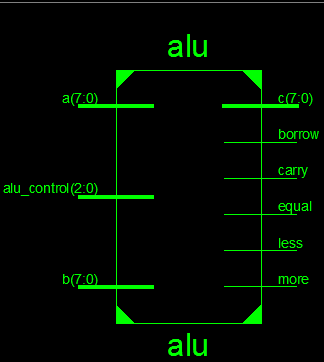
endmodule

**Synthesis:**

1. RTL Schematic



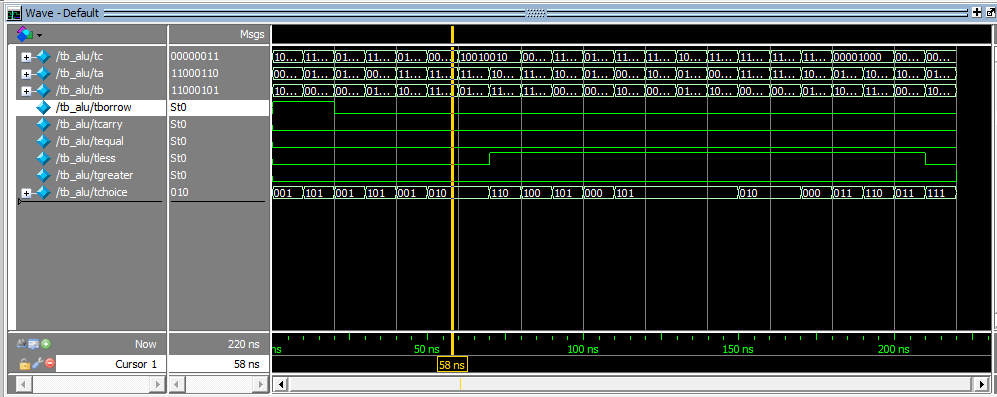
1. Block Diagram

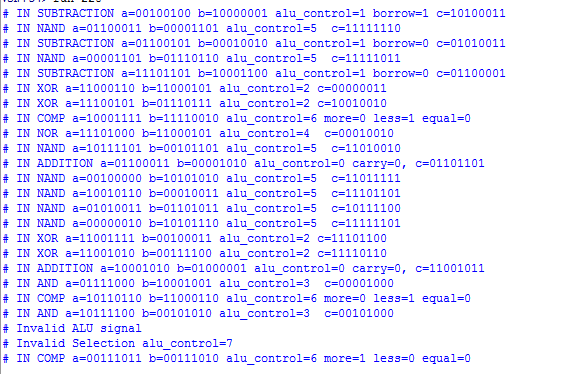
****

1. Tech Schematic



1. Simulation Waveform Result

****

****

**Error:**

Incorrect declaration of xor,nand,nor,or,and gates.

Soln: Resolved issue by completion of it by using transcript for depicting result.

**Verified by:**

Dharamvir Chundawat (150240133007)