**CDAC Feb 2015**

**LAB 7**

Q2. Asynchronous RAM (CY6264)

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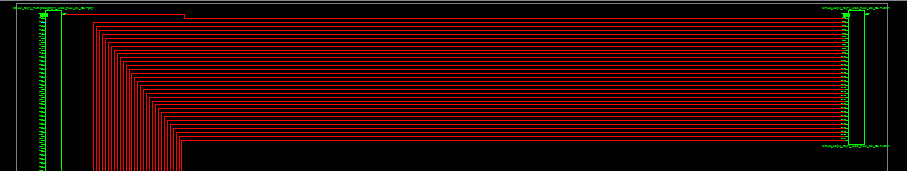
**Asynchronous RAM (CY6264)**

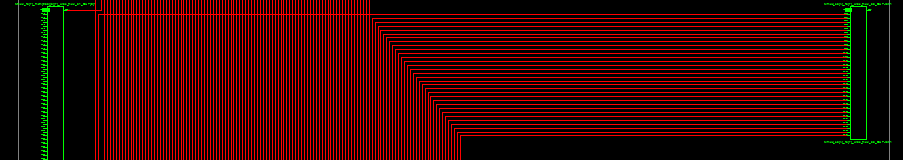
# Design Approach:

# Asynchronous RAM is a form of RAM that does not have clock signal. The truth table of Asynchronous RAM is provided in the PDF. This type of memory has 256 rows, 32 columns and each location has ability capable of storing 8 bit. This type of memory is 256X32X8 i.e. 8KX8 RAM. Row address is of 8-bit & column address is of 5 bit. This also portrays bidirectional port, so we can implement ternary operator to include the buffers. As it is asynchronous memory, we got latches in its RTL

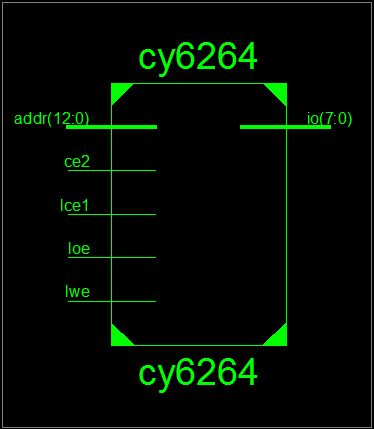
**Synthesis:**

1. RTL Schematic

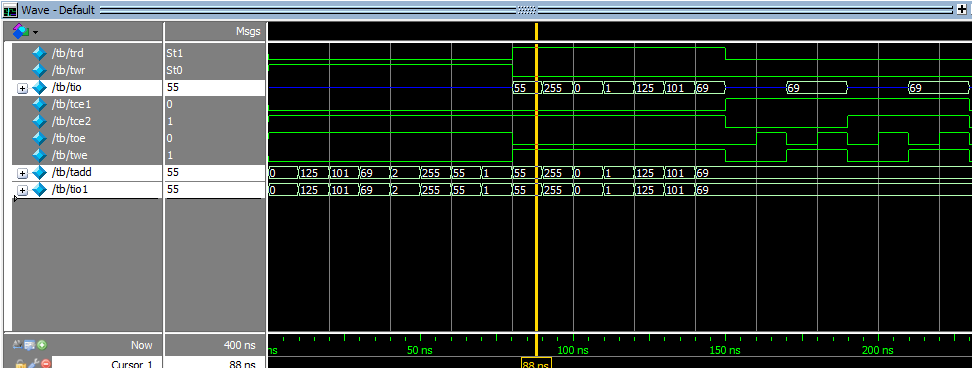


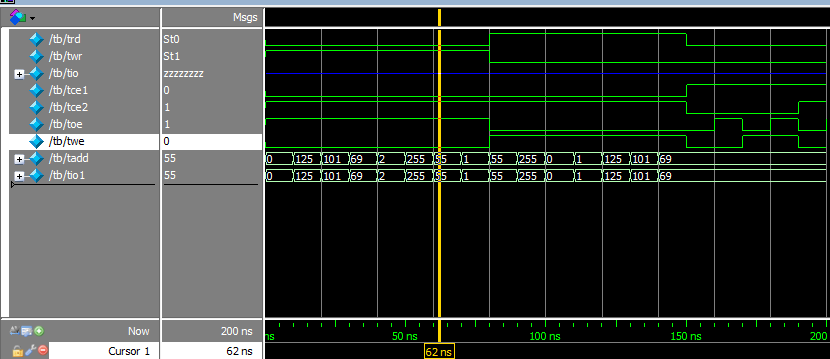


1. Block Diagram

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1. Simulation Waveform Result





**Error:**

Incorrect usage of case statement. Removed the typo of colon.

**Verified by:**

Dharamveer Babusen Chundawat (150240133007)