# TechSHILP
## VHDL

**INSTRUCTIONS:**

- A team may consist of maximum 2 members.
- The vhdl code should be compiled in Active HDL 7.1 or Active HDL 4.2SE
- There are 6 problems, each of different level and different points.
- It is not necessary that a team may submit all 6 problems. Any no. of problems solved can be submitted.
- The solutions should be sent in text files (.txt format) at **techshilp@techsrijan.com** with **vhdl in the subject** latest by **1100 hrs on 15th October 2011.** Along with the solutions a team is also required to send its team name, name, branch, year, contact number and email-id of both the participants.
- The short-listed teams for the final round will be informed through phone and email.
- **Use of packages unsigned.all and arith.all is strictly prohibited**.
- For any query, contact the event coordinator.

**1.** Design 8*1 multiplexer using two 4*1 multiplexers and one 2*1 multiplexer. [100 points]
The code should be in **structural modeling**.

**2.** Design a **universal shift register**(4 bit) in VHDL which performs the following four functions: [200 points]
i) Parallel loading
ii)Left shift
iii)Right Shift
iv)No operation

**3.** Write a VHDL code to compute parity (even) of a 16-bit number. [300 points]
The result is a 1-bit value that is assigned to the output after three positive edges of the clock.

**4.** Define two functions with the same name CONVERT. **First function converts a 2-digit octalnumber to an integer and the second function converts a 3-digit octal no. to an integer.** Both the functions should be defined in a single package. Additional points will be awarded if the first function is used in the definition of second function.
[400 points]

**5.** Write a VHDL code for **digital clock**. Your count will start from 00:00:00 to 23:59:59.There will be **an input square wave signal on whose rising edge there will be an increment of 1 count in the clock output**. All increments which will be done should be in binary. No conversion from binary to decimal or decimal to binary is allowed in the code.
Hint: Use one register for each digit of the clock. [500 points]

**6.** Design a Counter which follows the Fibonacci series pattern, till the $n^{th}$ term. The counter should work efficiently for all **$5 \leq n \leq 10$.** Additional points would be awarded for use of asynchronous counter.

[600 points]