

**ECE 571**

**Final Project Proposals**

**DDR4 Memory Controller Interface**

**by**

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## **Abstract**

This is a project proposal for a Final Project in ECE 571 – Introduction to System Verilog. It is proposed that a DDR4 memory system simulation be developed and tested using System Verilog constructs. The project will involve the development of a System Verilog Interface for DDR4 operations between the Memory Controller and the DIMMs (in this case a simulated memory block). The Memory controller will take ACTIVATE, READ, and WRITE requests for the processor and perform the appropriate operations by using the DDR4 Interface. The testbench will play the role of the memory management unit to verify that operations are performed according to JEDEC standards for the DDR4 memory system.

## 2. Overview

The DDR4 memory system will consist of a host memory management unit (commonly used on a PC for translating virtual address to physical addresses) as the test bench that will communicate to a memory controller to request operations ACTIVATE, READ, or WRITE. The memory controller then perform the appropriate operations by using the DDR4 interface to the memory block.

### DDR4 Interface Operations

- Reset
- Power Down
- Read
- Write
- Others

### Host → DDR4 Interface Signals

- Clock frequency
- Reset
- Power down
- Read request
- Write request
- Address
- Write data
- Refresh request
- Read Length
- Write Length

### DDR4 Interface → Host Signals

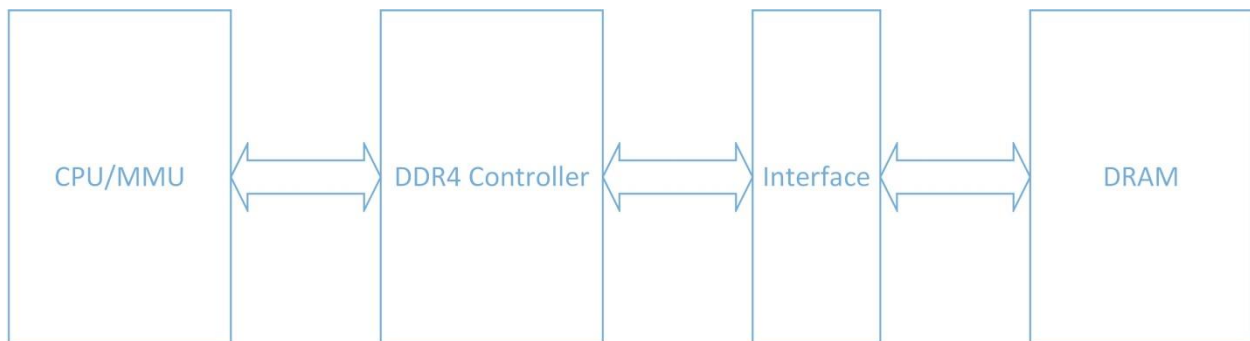
- Device Ready
- Read Data
- Write active
- Read active
- Refresh active

### DDR4 Interface → DDR4 Memory Block Signals

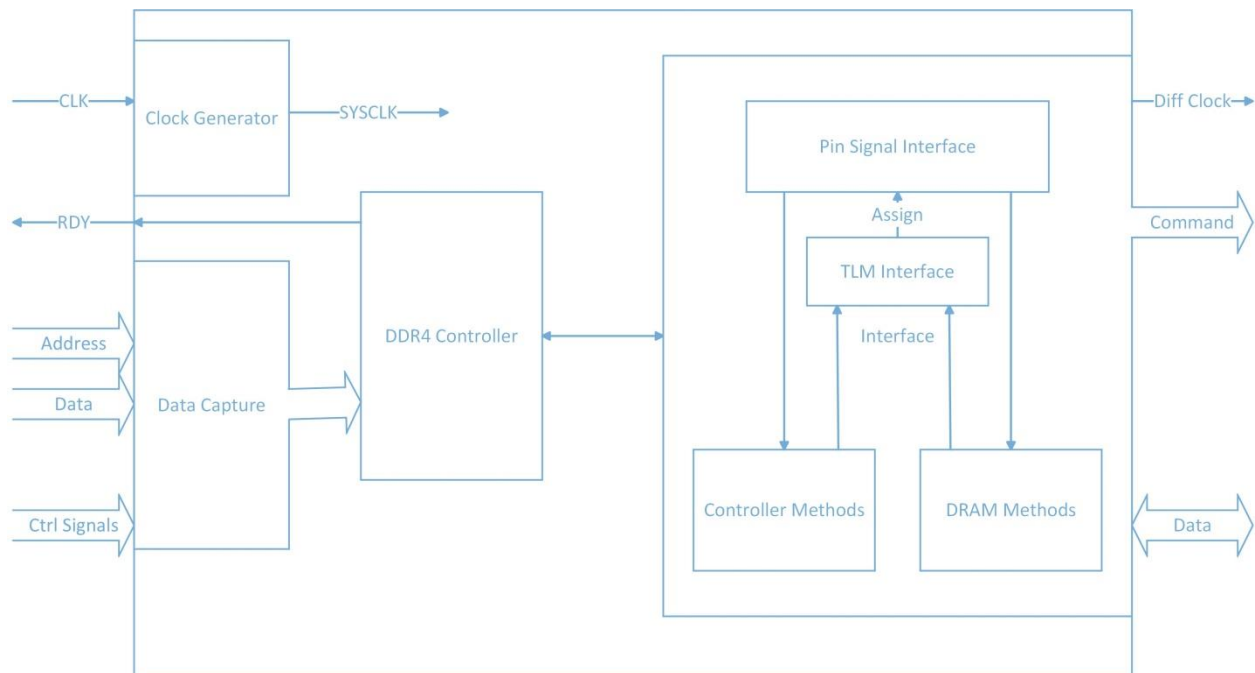
- Differential Clocks
- Reset
- Clock Enable
- Chip Select
- On Die Termination (should be disabled for this project))
- Activation Command Input.
- Command Inputs
- Input Data Mask and Data Bus Inversion
- Bank Address
- Bank Group Address
- Addresses Input
- I/O Data Bus

- Data Strobe Signals
- Terminal Data Strobe
- PAR (
- Auto pre-charge
- Burst Chop

### Level 0 Block Diagram of System



### Level 1 Block Diagram of Controller and Interface



### 3. Proposal Items

**The DDR4 Interface contains the following items in design:**

- The DDR4 Interface must be developed in SystemVerilog
- The DDR4 Interface should be designed to instantiate for 2,4,6,8, and 16GB DDR4 Memory.
- The DDR4 Interface must provide the differential clock to Memory block based on the frequency from the host.
- The DDR4 Interface must perform the Power-Up initialization Sequence
- The DDR4 Interface must perform Reset Initialization Sequence
- The DDR4 Interface must perform write to DDR4 Memory according to device's timing and protocol.
- The DDR4 Interface must perform read command to DDR4 Memory according to device's time and protocol
- The DDR4 Interface must operate in all Burst Length Modes (Fix Burst Length 8 bit, Block-Chop 4 bits, or on the Fly)
- The DDR4 Interface should generate Read/Write commands in both Pre-Charge Modes (Auto and Off)
- The DDR4 Interface must initiate the Power-down Mode
- The DDR4 Interface must initiate the Self-Refresh Mode or Controlled-Refresh
- The DDR4 Interface must deselect (de-activate) the device.
- The DDR4 Interface may perform data, address, strobe pins calibration
- The DDR4 Interface may perform write with CRC mode
- The DDR4 Interface may perform read with Address –Parity Mode
- The DDR4 Interface may perform various delays for CAS Latency, Write Recovery, Read-to-PreCharge
- The DDR4 Interface may perform n-die termination and output impedance pins,
- The DDR4 Interface may perform Temperature Controlled Refresh Mode for simplicity.
- The DDR4 Interface may be synthesized, translate, mapping, PAR, BitGen for either Xilinx or Altera
- Additional features may be considered during detailed requirements capture.

**The DDR4 Verification (e.g . Test Bench) shall have the following:**

- The DDR4 Interface design must perform Function Simulation on QuestaSim version 10.3a (either on Window or Linux)
- The simulation test bench must be created to verify correct functionality of the design as a Directed Test.
- The Test Bench should use stimulus files. The stimulus file is a text file (ASCII) that contains memory addresses, data, commands, and timing to the DDR4 Interface ( DUT)

- The Test Bench must have a module (or modules) to read and translate stimulus file (or files) into signal transaction to DUT.
- The Test Bench must have a module (or modules) to monitor all the signal transaction on DUT outputs.
- The log report must be generated during simulation to capture all the outputs from DUT as well as expected output from the Test Bench module to verify to correct functionality of DUT.
- The Stimulus file (or files) must contain all completed test cases to demonstrate the correct functionality of DUT.
- The DDR4 Verification may perform Post-Synthesis Timing Simulation
- As the Mentor Graphics Veloce only has 1GB of memory it is not possible to an exhaustive test of all possible addresses that can be used by the DDR4 system. Even with this constraint it is still possible to verify and validate the system by choosing both specific and random memory locations within the available memory space.

#### **4. Member Responsibility**

- Each member in the group must understand the SystemVerilog design and DDR4 Memory Device to contribute into requirements capture, RTL Coding on design and Test Bench,
- Code review.
- For academic purposes, each member must participate in all phases of the project.
- Each member must be responsible not only for his work but also for provide code reviews, collaboration, and advice to other members for the success of the project.
- Each member must have their own work completed on time. In case there is a problem or issue, each member shall notify other members in advance to avoid delay of the project integration and ultimate fail of project.
- Each member should be responsible for one part of the design and different part of the verification. The assignment provides the independence between design and verification to guarantee the success of the project.

#### **5. Artifacts**

- Block diagrams for both Design and Test Bench must be generated
- Detailed Design Requirements must be generated for DDR4 Design. The requirements are created and reviewed by all team members. The requirements must be correct, achievable, and verifiable. The requirements must be captured in spreadsheet or word document.
- Design files (modules) in SystemVerilog.
- TestBench files (modules) in SystemVerilog
- Stimulus files.
- Run files(e.g do files)
- Log reports files.
- Spreadsheets (or word document) to keep track schedule assignments, problems, code review input between team members.

## 6. Milestones

- Jul 8<sup>th</sup> – Jul 15<sup>th</sup> : Study DDR4 Memory Device.  
Capture details requirements.  
Defines Block Diagrams  
Project Assignments  
Create a workspace for the project.
- Jul 15<sup>th</sup> - Jul 29<sup>th</sup>: RTL Code for Design  
Code Reviews for other team member  
Define test bench requirements.  
Integration design
- Jul 29<sup>th</sup> – Aug 5<sup>th</sup> : Test Bench, Stimulus, Integration, Review, Presentation

## 7. Member Contact Information

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