DDR2, DDR3, and DDR4 SDRAM Board Design Guidelines

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The following topics provide guidelines for improving the signal integrity of your system and for successfully implementing a DDR2, DDR3, or DDR4 SDRAM interface on your system.

The following areas are discussed:

- comparison of various types of termination schemes, and their effects on the signal quality on the receiver
- proper drive strength setting on the FPGA to optimize the signal integrity at the receiver
- effects of different loading types, such as components versus DIMM configuration, on signal quality

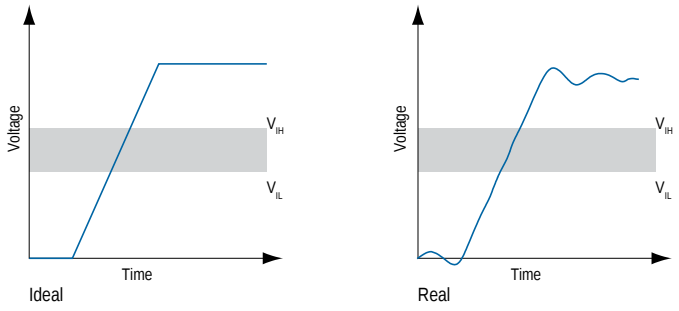
It is important to understand the trade-offs between different types of termination schemes, the effects of output drive strengths, and different loading types, so that you can swiftly navigate through the multiple combinations and choose the best possible settings for your designs.

The following key factors affect signal quality at the receiver:

- Leveling and dynamic ODT
- Proper use of termination
- Output driver drive strength setting
- Loading at the receiver
- Layout guidelines

As memory interface performance increases, board designers must pay closer attention to the quality of the signal seen at the receiver because poorly transmitted signals can dramatically reduce the overall data-valid margin at the receiver. The following figure shows the differences between an ideal and real signal seen by the receiver.

Figure 4-1: Ideal and Real Signal at the Receiver



Leveling and Dynamic ODT

DDR3 and DDR4 SDRAM DIMMs, as specified by JEDEC, always use a fly-by topology for the address, command, and clock signals.

Altera recommends that for full DDR3 or DDR4 SDRAM compatibility when using discrete DDR3 or DDR4 SDRAM components, you should mimic the JEDEC DDR3 or DDR4 fly-by topology on your custom printed circuit boards (PCB).

Note: Arria® II, Arria V, and Cyclone® V devices do not support DDR3 SDRAM with read or write leveling, so these devices do not support standard DDR3 SDRAM DIMMs or DDR3 SDRAM components using the standard DDR3 SDRAM fly-by address, command, and clock layout topology.

Table 4-1: Device Family Topology Support

Device	I/O Support
Arria II	Non-leveling
Arria V GX, Arria V GT	Non-leveling
Arria V GZ	Leveling
Cyclone V GX, Cyclone V GT	Non-leveling
Stratix III	Leveling
Stratix IV	Leveling
Stratix V	Leveling
Arria 10	Leveling

Related Information

www.JEDEC.org

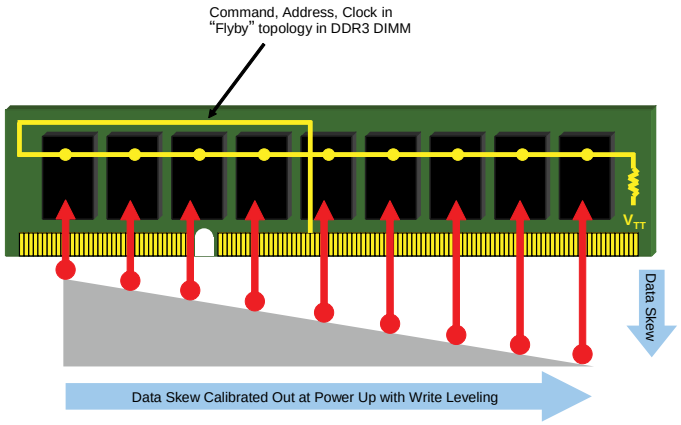
Read and Write Leveling

A major difference between DDR2 and DDR3 SDRAM is the use of leveling. To improve signal integrity and support higher frequency operations, the JEDEC committee defined a fly-by termination scheme used with clocks, and command and address bus signals.

Note: This section describes read and write leveling in terms of a comparison between DDR3 and DDR2. Leveling in DDR4 is fundamentally similar to DDR3. Refer to the DDR4 JEDEC specifications for more information.

Fly-by topology reduces simultaneous switching noise (SSN) by deliberately causing flight-time skew between the data and strobes at every DRAM as the clock, address, and command signals traverse the DIMM, as shown in the following figure.

Figure 4-2: DDR3 DIMM Fly-By Topology Requiring Write Leveling



The flight-time skew caused by the fly-by topology led the JEDEC committee to introduce the write leveling feature on the DDR3 SDRAMs. Controllers must compensate for this skew by adjusting the timing per byte lane.

During a write, DQS groups launch at separate times to coincide with a clock arriving at components on the DIMM, and must meet the timing parameter between the memory clock and DQS defined as tDQSS of ± 0.25 tCK.

During the read operation, the memory controller must compensate for the delays introduced by the fly-by topology. The Stratix® III, Stratix IV, and Stratix V FPGAs have alignment and synchronization registers built in the I/O element to properly capture the data.

In DDR2 SDRAM, there are only two drive strength settings, full or reduced, which correspond to the output impedance of 18-ohm and 40-ohm, respectively. These output drive strength settings are static settings and are not calibrated; consequently, the output impedance varies as the voltage and temperature drifts.

The DDR3 SDRAM uses a programmable impedance output buffer. There are two drive strength settings, 34-ohm and 40-ohm . The 40-ohm drive strength setting is currently a reserved specification defined by JEDEC, but available on the DDR3 SDRAM, as offered by some memory vendors. Refer to the data sheet of the respective memory vendors for more information about the output impedance setting. You select the drive strength settings by programming the memory mode register defined by mode register 1 (MR1). To calibrate output driver impedance, an external precision resistor, RZQ, connects the ZQ pin and VSSQ. The value of this resistor must be 240-ohm ± 1%.

If you are using a DDR3 SDRAM DIMM, RZQ is soldered on the DIMM so you do not need to layout your board to account for it. Output impedance is set during initialization. To calibrate output driver impedance after power-up, the DDR3 SDRAM needs a calibration command that is part of the initialization and reset procedure and is updated periodically when the controller issues a calibration command.

In addition to calibrated output impedance, the DDR3 SDRAM also supports calibrated parallel ODT through the same external precision resistor, RZQ, which is possible by using a merged output driver structure in the DDR3 SDRAM, which also helps to improve pin capacitance in the DQ and DQS pins. The ODT values supported in DDR3 SDRAM are 20-ohm , 30-ohm , 40-ohm , 60-ohm , and 120-ohm , assuming that RZQ is 240-ohm.

In DDR3 SDRAM, there are two commands related to the calibration of the output driver impedance and ODT. The controller often uses the first calibration command, ZQ CALIBRATION LONG (ZQCL), at initial power-up or when the DDR3 SDRAM is in a reset condition. This command calibrates the output driver impedance and ODT to the initial temperature and voltage condition, and compensates for any process

variation due to manufacturing. If the controller issues the ZQCL command at initialization or reset, it takes 512 memory clock cycles to complete; otherwise, it requires 256 memory clock cycles to complete. The controller uses the second calibration command, ZQ CALIBRATION SHORT (ZQCS) during regular operation to track any variation in temperature or voltage. The ZQCS command takes 64 memory clock cycles to complete. Use the ZQCL command any time there is more impedance error than can be corrected with a ZQCS command.

For more information about using ZQ Calibration in DDR3 SDRAM, refer to the application note by Micron, *TN-41-02 DDR3 ZQ Calibration*.

Related Information

www.JEDEC.org

Dynamic ODT

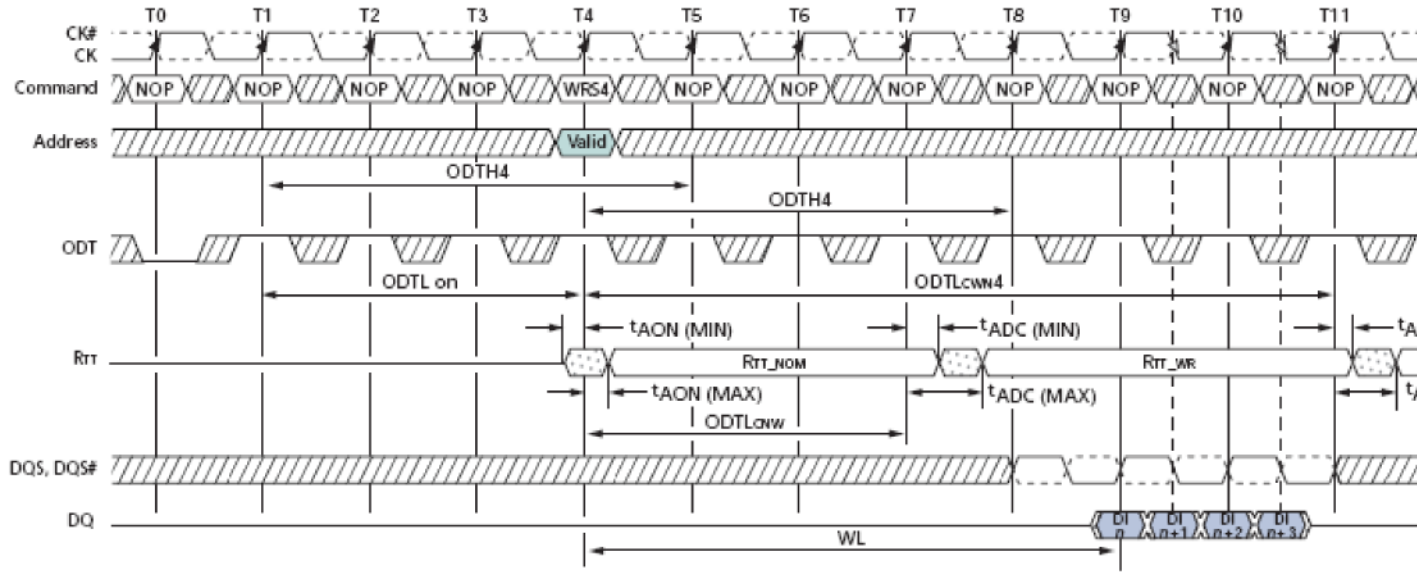
Dynamic ODT is a feature in DDR3 SDRAM that is not available in DDR2 SDRAM. Dynamic ODT can change the ODT setting without issuing a mode register set (MRS) command.

Note: This topic highlights the dynamic ODT feature in DDR3. To learn about dynamic ODT in DDR4, refer to the JEDEC DDR4 specifications.

When you enable dynamic ODT, and there is no write operation, the DDR3 SDRAM terminates to a termination setting of `RTT_NORM`; when there is a write operation, the DDR3 SDRAM terminates to a setting of `RTT_WR`. You can preset the values of `RTT_NORM` and `RTT_WR` by programming the mode registers, MR1 and MR2.

The following figure shows the behavior of ODT when you enable dynamic ODT.

Figure 4-3: Dynamic ODT: Behavior with ODT Asserted Before and After the Write



In the two-DIMM DDR3 SDRAM configuration, dynamic ODT helps reduce the jitter at the module being accessed, and minimizes reflections from any secondary modules.

For more information about using the dynamic ODT on DDR3 SDRAM, refer to the application note by Micron, *TN-41-04 DDR3 Dynamic On-Die Termination*.

Related Information

www.JEDEC.org

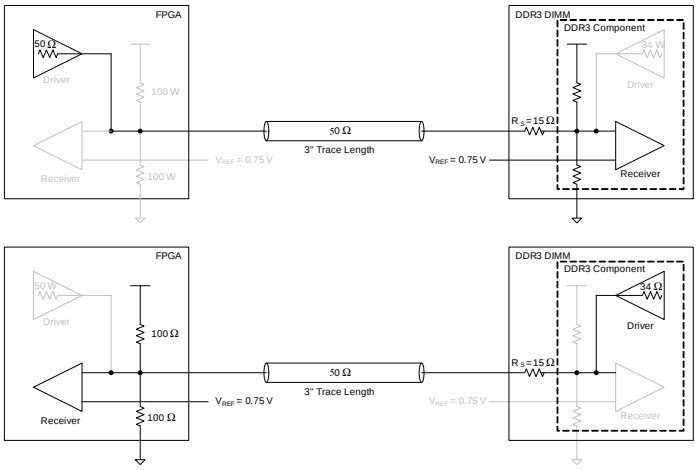
Dynamic OCT in Stratix III and Stratix IV Devices

Stratix III and Stratix IV devices support on-off dynamic series and parallel termination for a bidirectional I/O in all I/O banks. Dynamic OCT is a new feature in Stratix III and Stratix IV FPGA devices.

You enable dynamic parallel termination only when the bidirectional I/O acts as a receiver and disable it when the bidirectional I/O acts as a driver. Similarly, you enable dynamic series termination only when the bidirectional I/O acts as a driver and is disable it when the bidirectional I/O acts as a receiver. The default setting for dynamic OCT is series termination, to save power when the interface is idle—no active reads or writes.

Note: The dynamic control operation of the OCT is separate to the output enable signal for the buffer. UniPHY IP can enable parallel OCT only during read cycles, saving power when the interface is idle.

Figure 4-4: Dynamic OCT Between Stratix III and Stratix IV FPGA Devices



Dynamic OCT is useful for terminating any high-performance bidirectional path because signal integrity is optimized depending on the direction of the data. In addition, dynamic OCT also eliminates the need for external termination resistors when used with memory devices that support ODT (such as DDR3 SDRAM), thus reducing cost and easing board layout.

However, dynamic OCT in Stratix III and Stratix IV FPGA devices is different from dynamic ODT in DDR3 SDRAM mentioned in previous sections and these features should not be assumed to be identical.

For detailed information about the dynamic OCT feature in the Stratix III FPGA, refer to the *Stratix III Device I/O Features* chapter in volume 1 of the *Stratix III Device Handbook*.

For detailed information about the dynamic OCT feature in the Stratix IV FPGA, refer to the *I/O Features in Stratix IV Devices* chapter in volume 1 of the *Stratix IV Device Handbook*.

Related Information

- **Stratix III Device I/O Features**

- **I/O Features in Stratix IV Devices**

Dynamic OCT in Stratix V Devices

Stratix V devices also support the dynamic OCT feature and provide more flexibility. Stratix V OCT calibration uses one RZQ pin that exists in every OCT block.

You can use any one of the following as a reference resistor on the RZQ pin to implement different OCT values:

- 240-ohm reference resistor—to implement RS OCT of 34-ohm, 40-ohm, 48-ohm, 60-ohm, and 80-ohm; and RT OCT resistance of 20-ohm, 30-ohm, 40-ohm, and 120-ohm
- 100-ohm reference resistor—to implement RS OCT of 25-ohm and 50-ohm; and RT OCT resistance of 50-ohm

For detailed information about the dynamic OCT feature in the Stratix V FPGA, refer to the *I/O Features in Stratix V Devices* chapter in volume 1 of the *Stratix V Device Handbook*.

Related Information

I/O Features in Stratix V Devices

Board Termination for DDR2 SDRAM

DDR2 adheres to the JEDEC standard of governing Stub-Series Terminated Logic (SSTL), JESD8-15a, which includes four different termination schemes.

Two commonly used termination schemes of SSTL are:

- Single parallel terminated output load with or without series resistors (Class I, as stated in JESD8-15a)
- Double parallel terminated output load with or without series resistors (Class II, as stated in JESD8-15a)

Depending on the type of signals you choose, you can use either termination scheme. Also, depending on your design's FPGA and SDRAM memory devices, you may choose external or internal termination schemes.

To reduce system cost and simplify printed circuit board layout, you may choose not to have any parallel termination on the transmission line, and use point-to-point connections between the memory interface and the memory. In this case, you may take advantage of internal termination schemes such as on-chip termination (OCT) on the FPGA side and on-die termination (ODT) on the SDRAM side when it is offered on your chosen device.

Related Information

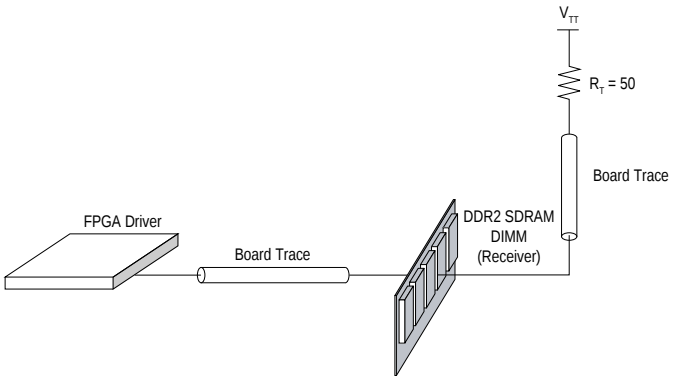
Board Termination for DDR3 SDRAM on page 4-13

External Parallel Termination

If you use external termination, you must study the locations of the termination resistors to determine which topology works best for your design.

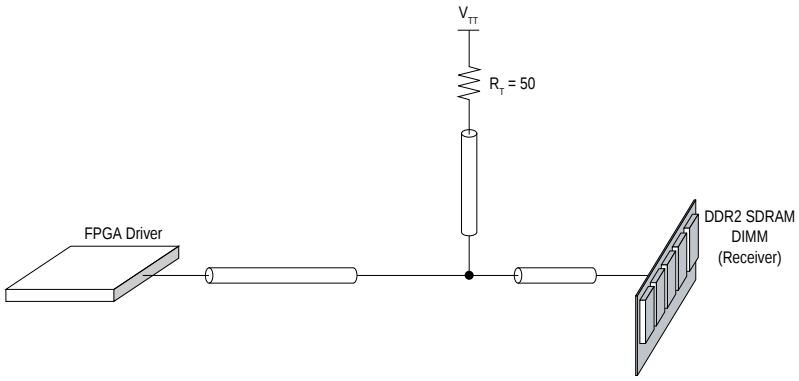
The following two figures illustrate the most common termination topologies: fly-by topology and non-fly-by topology, respectively.

Figure 4-5: Fly-By Placement of a Parallel Resistor



With fly-by topology, you place the parallel termination resistor after the receiver. This termination placement resolves the undesirable unterminated stub found in the non-fly-by topology. However, using this topology can be costly and complicate routing.

Figure 4-6: Non-Fly-By Placement of a Parallel Resistor



With non-fly-by topology, the parallel termination resistor is placed between the driver and receiver (closest to the receiver). This termination placement is easier for board layout, but results in a short stub, which causes an unterminated transmission line between the terminating resistor and the receiver. The unterminated transmission line results in ringing and reflection at the receiver.

If you do not use external termination, DDR2 offers ODT and Altera FPGAs have varying levels of OCT support. You should explore using ODT and OCT to decrease the board power consumption and reduce the required board space.

On-Chip Termination

OCT technology is offered on Arria II GX, Arria II GZ, Arria V, Cyclone V, Stratix III, Stratix IV, and Stratix V devices.

The following table summarizes the extent of OCT support for each device. This table provides information about SSTL-18 standards because SSTL-18 is the supported standard for DDR2 memory interface by Altera FPGAs.

On-chip series (RS) termination is supported only on output and bidirectional buffers. The value of RS with calibration is calibrated against a 25-ohm resistor for class II and 50-ohm resistor for class I connected to

RUP and RDN pins and adjusted to ± 1% of 25-ohm or 50-ohm . On-chip parallel (RT) termination is supported only on inputs and bidirectional buffers. The value of RT is calibrated against 100-ohm connected to the RUP and RDN pins. Calibration occurs at the end of device configuration. Dynamic OCT is supported only on bidirectional I/O buffers.

Table 4-2: On-Chip Termination Schemes

Termination Scheme	SSTL-18	FPGA Device					
		Arria II GX	Arria II GZ	Arria V	Cyclone V	Stratix III and Stratix IV	Stratix V *(1)*
		Column and Row I/O	Column and Row I/O	Column and Row I/O	Column and Row I/O	Column and Row I/O	Column I/O
On-Chip Series Termination without Calibration	Class I	50	50	50	50	50	50
	Class II	25	25	25	25	25	25
On-Chip Series Termination with Calibration	Class I	50	50	50	50	50	50
	Class II	25	25	25	25	25	25
On-Chip Parallel Termination with Calibration	Class I and Class II	—	50	50	50	50	50

Note to Table:

1. Row I/O is not available for external memory interfaces in Stratix V devices.

Recommended Termination Schemes

The following table provides the recommended termination schemes for major DDR2 memory interface signals.

Signals include data (DQ), data strobe (DQS/DQSn), data mask (DM), clocks (`mem_clk`/`mem_clk_n`), and address and command signals.

When interfacing with multiple DDR2 SDRAM components where the address, command, and memory clock pins are connected to more than one load, follow these steps:

1. Simulate the system to get the new slew-rate for these signals.
2. Use the derated tIS and tIH specifications from the DDR2 SDRAM data sheet based on the simulation results.
3. If timing deration causes your interface to fail timing requirements, consider signal duplication of these signals to lower their loading, and hence improve timing.

Note: Altera uses Class I and Class II termination in this table to refer to drive strength, and not physical termination.

Note: You must simulate your design for your system to ensure correct operation.

Table 4-3: Termination Recommendations *(1)*

Device Family	Signal Type	SSTL 18 IO Standard *(2) (3) (4) (5) (6)*	FPGA-End Discrete Termination	Memory-End Termination 1 (Rank/DIMM)	Memory I/O Standard
Arria II GX					
DDR2 component	DQ	Class I R50 CAL	50-ohm Parallel to VTT discrete	ODT75 *(7)*	HALF *(8)*
	DQS DIFF *(13)*	DIFF Class R50 CAL	50-ohm Parallel to VTT discrete	ODT75 *(7)*	HALF *(8)*
	DQS SE *(12)*	Class I R50 CAL	50-ohm Parallel to VTT discrete	ODT75 *(7)*	HALF *(8)*
	DM	Class I R50 CAL	N/A	ODT75 *(7)*	N/A
	Address and command	Class I MAX	N/A	56-ohm parallel to VTT discrete	N/A
	Clock	DIFF Class I R50 CAL	N/A	×1 = 100-ohm differential *(10)* ×2 = 200-ohm differential *(11)*	N/A

Device Family	Signal Type	SSTL 18 IO Standard (2) (3) (4) (5) (6)	FPGA-End Discrete Termination	Memory-End Termination 1 (Rank/DIMM)	Memory I/O Standard
DDR2 DIMM	DQ	Class I R50 CAL	50-ohm Parallel to VTT discrete	ODT75 (7)	FULL (9)
	DQS DIFF (13)	DIFF Class I R50 CAL	50-ohm Parallel to VTT discrete	ODT75 (7)	FULL (9)
	DQS SE (12)	Class I R50 CAL	50-ohm Parallel to VTT discrete	ODT75 (7)	FULL (9)
	DM	Class I R50 CAL	N/A	ODT75 (7)	N/A
	Address and command	Class I MAX	N/A	56-ohm parallel to VTT discrete	N/A
	Clock	DIFF Class I R50 CAL	N/A	N/A = on DIMM	N/A
Arria V and Cyclone V					
DDR2 component	DQ	Class I R50/ P50 DYN CAL	N/A	ODT75 (7)	HALF (8)
	DQS DIFF (13)	DIFF Class I R50/P50 DYN CAL	N/A	ODT75 (7)	HALF (8)
	DQS SE (12)	Class I R50/ P50 DYN CAL	N/A	ODT75 (7)	HALF (8)
	DM	Class I R50 CAL	N/A	ODT75 (7)	N/A
	Address and command	Class I MAX	N/A	56-ohm parallel to VTT discrete	N/A
	Clock	DIFF Class I R50 NO CAL	N/A	×1 = 100-ohm differential (10) ×2 = 200-ohm differential (11)	N/A

Device Family	Signal Type	SSTL 18 IO Standard (2) (3) (4) (5) (6)	FPGA-End Discrete Termination	Memory-End Termination 1 (Rank/DIMM)	Memory I/O Standard
DDR2 DIMM	DQ	Class I R50/ P50 DYN CAL	N/A	ODT75 (7)	FULL (9)
	DQS DIFF (13)	DIFF Class I R50/P50 DYN CAL	N/A	ODT75 (7)	FULL (9)
	DQS SE (12)	Class I R50/ P50 DYN CAL	N/A	ODT75 (7)	FULL (9)
	DM	Class I R50 CAL	N/A	ODT75 (7)	N/A
	Address and command	Class I MAX	N/A	56-ohm parallel to VTT discrete	N/A
	Clock	DIFF Class I R50 NO CAL	N/A	N/A = on DIMM	N/A
Arria II GZ, Stratix III, Stratix IV, and Stratix V					
DDR2 component	DQ	Class I R50/ P50 DYN CAL	N/A	ODT75 (7)	HALF (8)
	DQS DIFF (13)	DIFF Class I R50/P50 DYN CAL	N/A	ODT75 (7)	HALF (8)
	DQS SE (12)	DIFF Class I R50/P50 DYN CAL	N/A	ODT75 (7)	HALF (8)
	DM	Class I R50 CAL	N/A	ODT75 (7)	N/A
	Address and command	Class I MAX	N/A	56-ohm Parallel to VTT discrete	N/A
	Clock	DIFF Class I R50 NO CAL	N/A	x1 = 100-ohm differential (10) x2 = 200-ohm differential (11)	N/A

Device Family	Signal Type	SSTL 18 IO Standard (2) (3) (4) (5) (6)	FPGA-End Discrete Termination	Memory-End Termination 1 (Rank/DIMM)	Memory I/O Standard
DDR2 DIMM	DQ	Class I R50/ P50 DYN CAL	N/A	ODT75 (7)	FULL (9)
	DQS DIFF (13)	DIFF Class I R50/P50 DYN CAL	N/A	ODT75 (7)	FULL (9)
	DQS SE (12)	Class I R50/ P50 DYN CAL	N/A	ODT75 (7)	FULL (9)
	DM	Class I R50 CAL	N/A	ODT75 (7)	N/A
	Address and command	Class I MAX	N/A	56-ohm Parallel to VTT discrete	N/A
	Clock	DIFF Class I R50 NO CAL	N/A	N/A = on DIMM	N/A

Notes to Table:

1. N/A is not available.
2. R is series resistor.
3. P is parallel resistor.
4. DYN is dynamic OCT.
5. NO CAL is OCT without calibration.
6. CAL is OCT with calibration.
7. ODT75 vs. ODT50 on the memory has the effect of opening the eye more, with a limited increase in overshoot/undershoot.
8. HALF is reduced drive strength.
9. FULL is full drive strength.
10. x1 is a single-device load.
11. x2 is two-device load. For example, you can feed two out of nine devices on a single rank DIMM with a single clock pair.
12. DQS SE is single-ended DQS.
13. DQS DIFF is differential DQS

Dynamic On-Chip Termination

Dynamic OCT is available in Arria V, Arria 10, Cyclone V, Stratix III, Stratix IV and Stratix V.

The dynamic OCT scheme enables series termination (RS) and parallel termination (RT) to be dynamically turned on and off during the data transfer. The series and parallel terminations are turned on or off depending on the read and write cycle of the interface. During the write cycle, the RS is turned on and the RT is turned off to match the line impedance. During the read cycle, the RS is turned off and the RT is turned on as the FPGA implements the far-end termination of the bus.

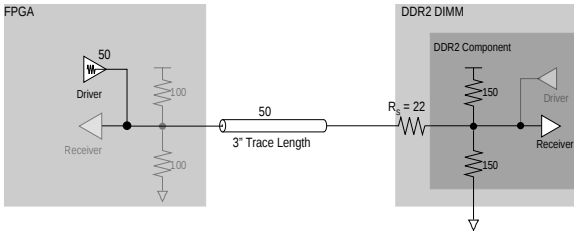
For more information about dynamic OCT, refer to the I/O features chapters in the devices handbook for your Altera device.

FPGA Writing to Memory

The benefit of using dynamic series OCT is that when driver is driving the transmission line, it "sees" a matched transmission line with no external resistor termination.

The following figure shows dynamic series OCT scheme when the FPGA is writing to the memory.

Figure 4-7: Dynamic Series OCT Scheme with ODT on the Memory



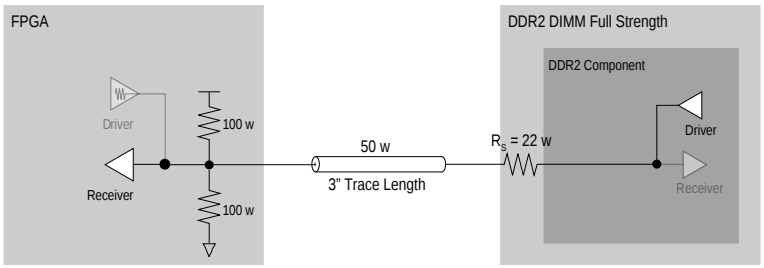
Refer to the memory vendors when determining the over- and undershoot. They typically specify a maximum limit on the input voltage to prevent reliability issues.

FPGA Reading from Memory

The following figure shows the dynamic parallel termination scheme when the FPGA is reading from memory.

When the DDR2 SDRAM DIMM is driving the transmission line, the ringing and reflection is minimal because the FPGA-side termination 50-ohm pull-up resistor is matched with the transmission line.

Figure 4-8: Dynamic Parallel OCT Scheme with Memory-Side Series Resistor



Board Termination for DDR3 SDRAM

DDR3 DIMMs have terminations on all unidirectional signals, such as memory clocks, and addresses and commands; thus eliminating the need for them on the FPGA PCB. In addition, using the ODT feature on the DDR3 SDRAM and the dynamic OCT feature of Stratix III, Stratix IV, and Stratix V FPGA devices completely eliminates any external termination resistors; thus simplifying the layout for the DDR3 SDRAM interface when compared to that of the DDR2 SDRAM interface.

The following topics describe the correct way to terminate a DDR3 SDRAM interface together with Stratix III, Stratix IV, and Stratix V FPGA devices.

Note: If you are using a DDR3 SDRAM without leveling interface, refer to the "Board Termination for DDR2 SDRAM".

Related Information

Board Termination for DDR2 SDRAM on page 4-6

Terminations for Single-Rank DDR3 SDRAM Unbuffered DIMM

The most common implementation of the DDR3 SDRAM interface is the unbuffered DIMM (UDIMM). You can find DDR3 SDRAM UDIMMs in many applications, especially in PC applications.

The following table lists the recommended termination and drive strength setting for UDIMM and Stratix III, Stratix IV, and Stratix V FPGA devices.

Note: These settings are just recommendations for you to get started. Simulate with real board and try different settings to get the best SI.

Table 4-4: Drive Strength and ODT Setting Recommendations for Single-Rank UDIMM

Signal Type	SSTL 15 I/O Standard (1)	FPGA End On-Board Termination (2)	Memory End Termination for Write	Memory Driver Strength for Read
DQ	Class I R50C/ G50C (3)	—	60-ohm ODT (4)	40-ohm (4)
DQS	Differential Class I R50C/G50C (3)	—	60-ohm ODT (4)	40-ohm (4)
DM	Class I R50C (3)	—	60-ohm ODT (4)	40-ohm (4)
Address and Command	Class I with maximum drive strength	—	39-ohm on-board termination to V_{DD} (5)	
CK/CK#	Differential Class I R50C	—	On-board (5) 2.2 pf compensation cap before the first component; 36-ohm termination to V_{DD} for each arm (72-ohm differential); add 0.1 uF just before V_{DD}.	

Notes to Table:

1. UniPHY IP automatically implements these settings.
2. Altera recommends that you use dynamic on-chip termination (OCT) for Stratix III and Stratix IV device families.
3. R50C is series with calibration for write, G50C is parallel 50 with calibration for read.
4. You can specify these settings in the parameter editor.
5. For DIMM, these settings are already implemented on the DIMM card; for component topology, Altera recommends that you mimic termination scheme on the DIMM card on your board.

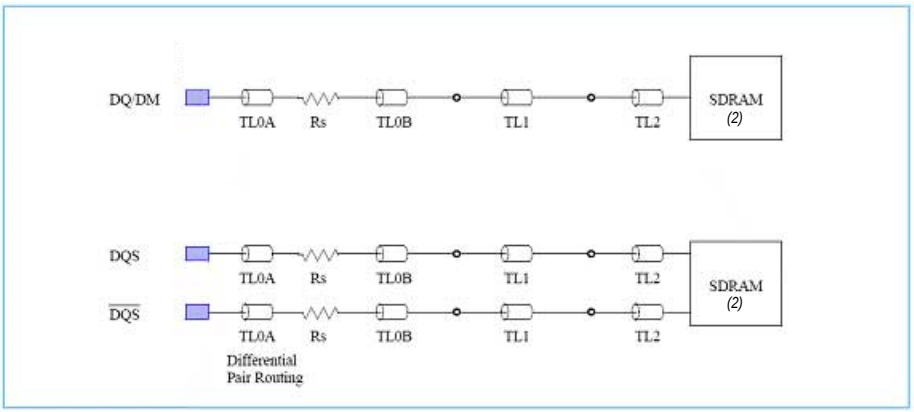
You can implement a DDR3 SDRAM UDIMM interface in several permutations, such as single DIMM or multiple DIMMs, using either single-ranked or dual-ranked UDIMMs. In addition to the UDIMM's form factor, these termination recommendations are also valid for small-outline (SO) DIMMs and MicroDIMMs.

DQS, DQ, and DM for DDR3 SDRAM UDIMM

On a single-ranked DIMM, DQS, and DQ signals are point-to-point signals.

The following figure shows the net structure for differential DQS and DQ signals. There is an external 15-ohm stub resistor, RS, on each of the DQS and DQ signals soldered on the DIMM, which helps improve signal quality by dampening reflections from unused slots in a multi-DIMM configuration.

Figure 4-9: DQ and DQS Net Structure for 64-Bit DDR3 SDRAM UDIMM



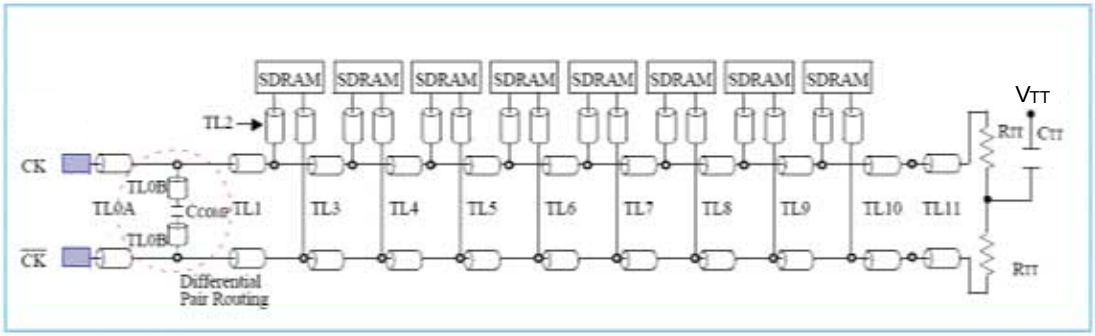
DDR3 SDRAM supports calibrated ODT with different ODT value settings. If you do not enable dynamic ODT, there are three possible ODT settings available for `RTT_NORM`: 40-ohm , 60-ohm , and 120-ohm . If you enable dynamic ODT, the number of possible ODT settings available for `RTT_NORM` increases from three to five with the addition of 20-ohm and 30-ohm. Trace impedance on the DIMM and the recommended ODT setting is 60-ohm.

Memory Clocks for DDR3 SDRAM UDIMM

For the DDR3 SDRAM UDIMM, you do not need to place any termination on your board because the memory clocks are already terminated on the DIMM.

The following figure shows the net structure for the memory clocks and the location of the termination resistors, RTT. The value of RTT is 36-ohm which results in an equivalent differential termination value of 72-ohm. The DDR3 SDRAM DIMM also has a compensation capacitor, CCOMP of 2.2 pF, placed between the differential memory clocks to improve signal quality. The recommended center-tap-terminated (C_{TT}) value is 0.1 uF just before V_{DD}.

Figure 4-10: Clock Net Structure for a 64-Bit DDR3 SDRAM UDIMM *(1)*



Notes to Figure:

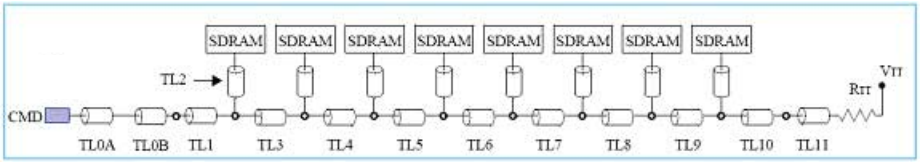
1. Source: *PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Unbuffered DIMM Design Specification*, July 2007, JEDEC Solid State Technology Association.
2. The recommeded C_{TT} value is 0.1 uF just before V_{DD}

Commands and Addresses for DDR3 SDRAM UDIMM

Similar to memory clock signals, you do not need to place any termination on your board because the command and address signals are also terminated on the DIMM.

The following figure shows the net structure for the command and address signals, and the location of the termination resistor, RTT, which has an RTT value of 39-ohm .

Figure 4-11: Command and Address Net Structure for a 64-Bit DDR3 SDRAM Unbuffered DIMM



In the above figure, note that the DDR3 SDRAM command and address signals are routed in a fly-by topology, resulting in the need for write-and-read leveling.

Terminations for Stratix III, Stratix IV, and Stratix V FPGAs

The following topics review the termination on the single-ranked single DDR3 SDRAM DIMM interface side and investigate the use of different termination features available in Stratix III, Stratix IV, and Stratix V FPGA devices to achieve optimum signal integrity for your DDR3 SDRAM interface.

DQS, DQ, and DM for Stratix III, Stratix IV, and Stratix V FPGA

Stratix III, Stratix IV, and Stratix V FPGAs support the dynamic OCT feature, which switches from series termination to parallel termination depending on the mode of the I/O buffer.

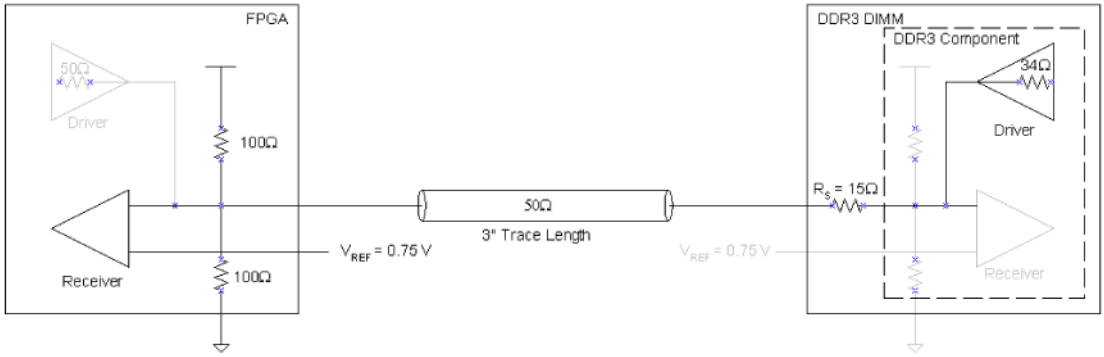
Because DQS and DQ are bidirectional signals, DQS and DQ can be both transmitters and receivers. “DQS, DQ, and DM for DDR3 SDRAM UDIMM” describes the signal quality of DQ, DQS, and DM when the Stratix III, Stratix IV, or Stratix V FPGA device is the transmitter with the I/O buffer set to a 50-ohm series termination.

This section details the condition when the Stratix III, Stratix IV, or Stratix V device is the receiver, the Stratix III, Stratix IV, and Stratix V I/O buffer is set to a 50-ohm parallel termination, and the memory is the transmitter. DM is a unidirectional signal, so the DDR3 SDRAM component is always the receiver.

For receiver termination recommendations and transmitter output drive strength settings, refer to “DQS, DQ, and DM for DDR3 SDRAM UDIMM” .

The following figure illustrates the DDR3 SDRAM interface when the Stratix III, Stratix IV, or Stratix V FPGA device is reading from the DDR3 SDRAM using a 50-ohm parallel OCT termination on the Stratix III, Stratix IV, or Stratix V FPGA device, and the DDR3 SDRAM driver output impedance is set to 34-ohm .

Figure 4-12: DDR3 SDRAM Component Driving the Stratix III, Stratix IV, and Stratix V FPGA Device with Parallel 50-ohm OCT Turned On



Use of the Stratix III, Stratix IV, or Stratix V parallel 50-ohm OCT feature matches receiver impedance with the transmission line characteristic impedance. This eliminates any reflection that causes ringing, and results in a clean eye diagram at the Stratix III, Stratix IV, or Stratix V FPGA.

Related Information

DQS, DQ, and DM for DDR3 SDRAM UDIMM on page 4-15

Memory Clocks for Stratix III, Stratix IV, and Stratix V FPGA

Memory clocks are unidirectional signals.

Refer to "Memory Clocks for DDR3 SDRAM UDIMM" for receiver termination recommendations and transmitter output drive strength settings.

Related Information

Memory Clocks for DDR3 SDRAM UDIMM on page 4-15

Commands and Addresses for Stratix III and Stratix IV FPGA

Commands and addresses are unidirectional signals.

Refer to "Commands and Addresses for DDR3 SDRAM UDIMM" for receiver termination recommendations and transmitter output drive strength settings.

Related Information

Commands and Addresses for DDR3 SDRAM UDIMM on page 4-16

Terminations for Multi-Rank DDR3 SDRAM Unbuffered DIMM

You can implement a DDR3 SDRAM UDIMM interface in several permutations, such as single DIMM or multiple DIMMs, using either single-ranked or dual-ranked UDIMMs. In addition to the UDIMM's form factor, these termination recommendations are also valid for small-outline (SO) DIMMs and MicroDIMMs.

The following table lists the different permutations of a two-slot DDR3 SDRAM interface and the recommended ODT settings on both the memory and controller when writing to memory.

Table 4-5: DDR3 SDRAM ODT Matrix for Writes *(1) (2)*

Slot 1	Slot 2	Write To	Controller OCT *(3)*	Slot 1		Slot 2	
				Rank 1	Rank 2	Rank 1	Rank 2
DR	DR	Slot 1	Series 50-ohm	120-ohm *(4)*	ODT off	ODT off	40-ohm *(4)*
		Slot 2	Series 50-ohm	ODT off	40-ohm *(4)*	120-ohm *(4)*	ODT off
SR	SR	Slot 1	Series 50-ohm	120-ohm *(4)*	Unpopulated	40-ohm *(4)*	Unpopulated
		Slot 2	Series 50-ohm	40-ohm *(4)*	Unpopulated	120-ohm *(4)*	Unpopulated
DR	Empty	Slot 1	Series 50-ohm	120-ohm *(4)*	ODT off	Unpopulated	Unpopulated
Empty	DR	Slot 2	Series 50-ohm	Unpopulated	Unpopulated	120-ohm *(4)*	ODT off
SR	Empty	Slot 1	Series 50-ohm	120-ohm *(4)*	Unpopulated	Unpopulated	Unpopulated
Empty	SR	Slot 2	Series 50-ohm	Unpopulated	Unpopulated	120-ohm *(4)*	Unpopulated

Notes to Table:

1. SR: single-ranked DIMM; DR: dual-ranked DIMM.
2. These recommendations are taken from the DDR3 ODT and Dynamic ODT session of the JEDEC DDR3 2007 Conference, Oct 3-4, San Jose, CA.
3. The controller in this case is the FPGA.
4. Dynamic ODT is required. For example, the ODT of Slot 2 is set to the lower ODT value of 40-ohms when the memory controller is writing to Slot 1, resulting in termination and thus minimizing any reflection from Slot 2. Without dynamic ODT, Slot 2 will not be terminated.

The following table lists the different permutations of a two-slot DDR3 SDRAM interface and the recommended ODT settings on both the memory and controller when reading from memory.

Table 4-6: DDR3 SDRAM ODT Matrix for Reads *(1) (2)*

Slot 1	Slot 2	Read From	Controller OCT *(3)*	Slot 1		Slot 2	
				Rank 1	Rank 2	Rank 1	Rank 2
DR	DR	Slot 1	Parallel 50-ohm	ODT off	ODT off	ODT off	40-ohm *(4)*
		Slot 2	Parallel 50-ohm	ODT off	40-ohm *(4)*	ODT off	ODT off

Slot 1	Slot 2	Read From	Controller OCT (3)	Slot 1		Slot 2	
				Rank 1	Rank 2	Rank 1	Rank 2
SR	SR	Slot 1	Parallel 50-ohm	ODT off	Unpopulated	40-ohm (4)	Unpopulated
		Slot 2	Parallel 50-ohm	40-ohm (4)	Unpopulated	ODT off	Unpopulated
DR	Empty	Slot 1	Parallel 50-ohm	ODT off	ODT off	Unpopulated	Unpopulated
Empty	DR	Slot 2	Parallel 50-ohm	Unpopulated	Unpopulated	ODT off	ODT off
SR	Empty	Slot 1	Parallel 50-ohm	ODT off	Unpopulated	Unpopulated	Unpopulated
Empty	SR	Slot 2	Parallel 50-ohm	Unpopulated	Unpopulated	ODT off	Unpopulated

Notes to Table:

1. SR: single-ranked DIMM; DR: dual-ranked DIMM.
2. These recommendations are taken from the DDR3 ODT and Dynamic ODT session of the JEDEC DDR3 2007 Conference, Oct 3-4, San Jose, CA.
3. The controller in this case is the FPGA. JEDEC typically recommends 60-ohms, but this value assumes that the typical motherboard trace impedance is 60-ohms and that the controller supports this termination. Altera recommends using a 50-ohm parallel OCT when reading from the memory.

Terminations for DDR3 SDRAM Registered DIMM

The difference between a registered DIMM (RDIMM) and a UDIMM is that the clock, address, and command pins of the RDIMM are registered or buffered on the DIMM before they are distributed to the memory devices. For a controller, each clock, address, or command signal has only one load, which is the register or buffer. In a UDIMM, each controller pin must drive a fly-by wire with multiple loads.

You do not need to terminate the clock, address, and command signals on your board because these signals are terminated at the register. However, because of the register, these signals become point-to-point signals and have improved signal integrity making the drive strength requirements of the FPGA driver pins more relaxed. Similar to the signals in a UDIMM, the DQS, DQ, and DM signals on a RDIMM are not registered. To terminate these signals, refer to "DQS, DQ, and DM for DDR3 SDRAM UDIMM".

Related Information

DQS, DQ, and DM for DDR3 SDRAM UDIMM on page 4-15

Terminations for DDR3 SDRAM Load-Reduced DIMM

RDIMM and LRDIMM differ in that DQ, DQS, and DM signals are registered or buffered in the LRDIMM. The LRDIMM buffer IC is a superset of the RDIMM buffer IC. The buffer IC isolates the memory interface signals from loading effects of the memory chip. Reduced electrical loading allows a system to operate at higher frequency and higher density.

Note: If you want to use your DIMM socket for UDIMM and RDIMM/LRDIMM, you must create the necessary redundant connections on the board from the FPGA to the DIMM socket. For example, the number of chip select signals required for a single-rank UDIMM is one, but for single-rank RDIMM the number of chip selects required is two. RDIMM and LRDIMM have parity signals associated with the address and command bus which UDIMM does not have. Consult the DIMM manufacturer's data sheet for detailed information about the necessary pin connections for various DIMM topologies.

Terminations for DDR3 SDRAM Components With Leveling

The following topics discusses terminations used to achieve optimum performance for designing the DDR3 SDRAM interface using discrete DDR3 SDRAM components.

In addition to using DDR3 SDRAM DIMM to implement your DDR3 SDRAM interface, you can also use DDR3 SDRAM components. However, for applications that have limited board real estate, using DDR3 SDRAM components reduces the need for a DIMM connector and places components closer, resulting in denser layouts.

DDR3 SDRAM Components With or Without Leveling

The DDR3 SDRAM UDIMM is laid out to the JEDEC specification. The JEDEC specification is available from either the JEDEC Organization website (www.JEDEC.org) or from the memory vendors. However, when you are designing the DDR3 SDRAM interface using discrete SDRAM components, you may desire a layout scheme that is different than the DIMM specification.

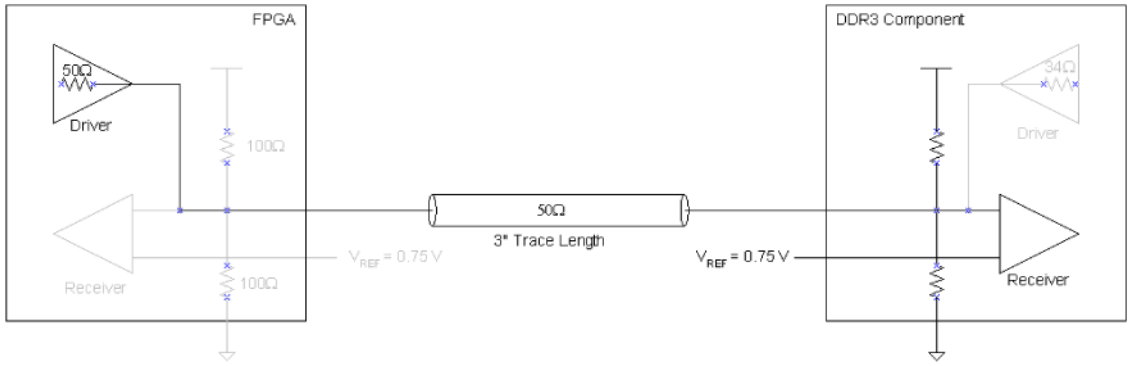
You have the following options:

- Mimic the standard DDR3 SDRAM DIMM, using a fly-by topology for the memory clocks, address, and command signals. This option needs read and write leveling, so you must use the UniPHY IP with leveling.
- Mimic a standard DDR2 SDRAM DIMM, using a balanced (symmetrical) tree-type topology for the memory clocks, address, and command signals. Using this topology results in unwanted stubs on the command, address, and clock, which degrades signal integrity and limits the performance of the DDR3 SDRAM interface.

DQS, DQ, and DM for DDR3 SDRAM Components

When you are laying out the DDR3 SDRAM interface using Stratix III, Stratix IV, or Stratix V devices, Altera recommends that you not include the 15-ohm stub series resistor that is on every DQS, DQ, and DM signal; unless your simulation shows that the absence of this resistor causes extra reflection. Although adding the 15-ohm stub series resistor may help to maintain constant impedance in some cases, it also slightly reduces signal swing at the receiver. It is unlikely that by removing this resistor the waveform shows a noticeable reflection, but it is your responsibility to prove by simulating your board trace. Therefore, Altera recommends the DQS, DQ, and DM topology shown in the following figure, when the Stratix III, Stratix IV, or Stratix V FPGA is writing to the DDR3 SDRAM.

Figure 4-13: Stratix III, Stratix IV, and Stratix V FPGA Writing to a DDR3 SDRAM Component



When you are using DDR3 SDRAM components, there are no DIMM connectors. This minimizes any impedance discontinuity, resulting in better signal integrity.

Memory Clocks for DDR3 SDRAM Components

When you use DDR3 SDRAM components, you must account for the compensation capacitor and differential termination resistor between the differential memory clocks of the DIMM.

To simplify your design, use the terminations outlined in the JEDEC specification for DDR3 SDRAM UDIMM as your guide and perform simulation to ensure that the DDR3 SDRAM UDIMM terminations provide you with optimum signal quality.

In addition to choosing the value of the differential termination, you must consider the trace length of the memory clocks. Altera's DDR3 UniPHY IP currently supports a flight-time skew of no more than 0.69 tCK in between the first and last memory component. If you use Altera's DDR3 UniPHY IP to create your DDR3 SDRAM interface, ensure that the flight-time skew of your memory clocks is not more than 0.69 tCK. UniPHY IP also requires that the total skew combination of the clock fly-by skew and DQS skew is less than 1 clock cycle.

Refer to "Layout Guidelines for DDR3 SDRAM Interface" for more information about layout guidelines for DDR3 SDRAM components.

Command and Address Signals for DDR3 SDRAM

You must properly terminate your command and address signals when you are using DDR3 SDRAM components. Choose your termination resistor value depending on your board stackup and layout requirements.

As with memory clocks, you must consider the trace delays of the command and address signals so that they match the flight-time skew of the memory clocks.

Related Information

- **Layout Guidelines for DDR3 and DDR4 SDRAM Interfaces** on page 4-32
- **www.JEDEC.org**

Stratix III, Stratix IV, and Stratix V FPGAs

Stratix III, Stratix IV, or Stratix V FPGA termination settings for DIMM also apply to DDR3 SDRAM component interfaces.

Drive Strength

Altera's FPGA products offer numerous drive strength settings, allowing you to optimize your board designs to achieve the best signal quality. The most commonly used drive strength settings are 8 mA and 16 mA, as recommended by JEDEC for Class I and Class II termination schemes.

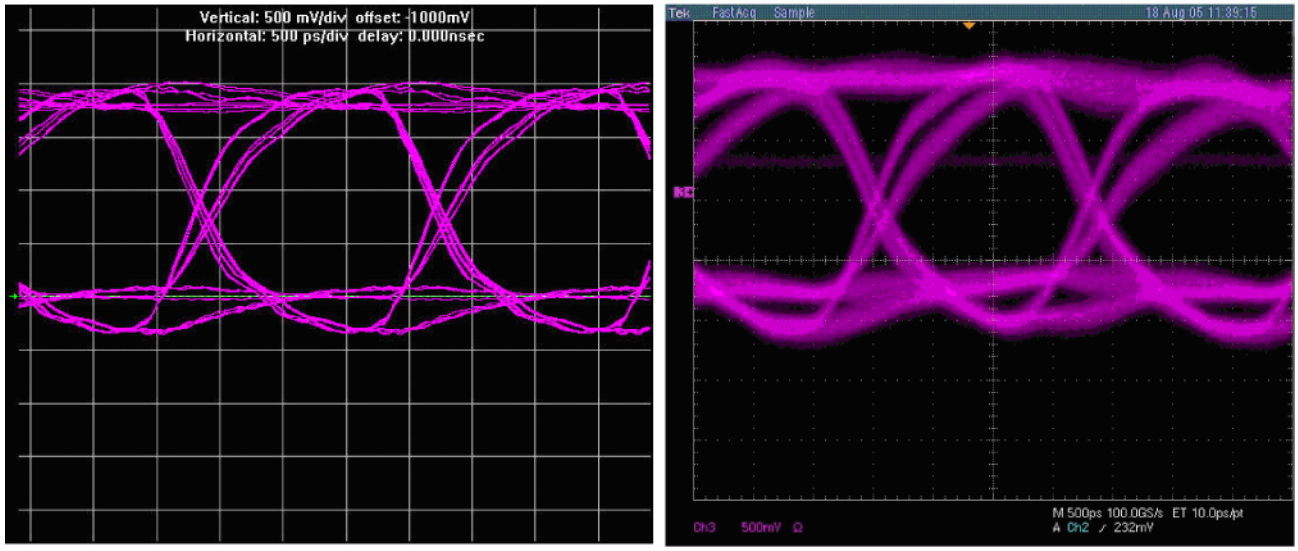
Note: You are not restricted to using only these drive strength settings for your board designs. You should perform simulations using I/O models available from Altera and memory vendors to ensure that you use the proper drive strength setting to achieve optimum signal integrity.

How Strong is Strong Enough?

Excessive drive strength can result in overshoot and undershoot in signal quality at the receiver.

Figure 19 shows a signal probed at the DDR2 SDRAM DIMM (receiver) of a far-end series-terminated transmission line when the FPGA writes to the DDR2 SDRAM DIMM using a drive strength setting of 16 mA. The resulting signal quality on the receiver shows excessive over- and undershoot. To reduce the over- and undershoot, you can reduce the drive strength setting on the FPGA from 16 mA to 8 mA. The following figure shows the simulation and measurement of the FPGA with a drive strength setting of 8 mA driving a no-parallel termination transmission line.

Figure 4-14: HyperLynx Simulation and Measurement, FPGA Writing to Memory



The following table compares the signals at the DDR2 SDRAM DIMM with no-parallel termination and memory-side series resistors when the FPGA is writing to the memory with 8-mA and 16-mA drive strength settings.

Table 4-7: Simulation and Board Measurement Results for 8 mA and 16 mA Drive Strength Settings

	Eye Width (ns)	Eye Height (V)	Overshoot (V)	Undershoot (V)
8-mA Drive Strength Setting				
Simulation	1.48	1.71	0.24	0.35
Board Measurement	1.10	1.24	0.24	0.50
16-mA Drive Strength Setting				
Simulation	1.66	1.10	0.90	0.80
Board Measurement	1.25	0.60	1.10	1.08

With a lower strength drive setting, the overall signal quality is improved. The eye width is reduced, but the eye height is significantly larger with a lower drive strength and the over- and undershoot is reduced dramatically.

To improve the signal quality further, you should use 50-ohm on-chip series termination in place of an 8mA drive strength and 25-ohm on-chip series termination in place of a 16 mA drive strength. Refer to "On-Chip Termination (Non-Dynamic)" for simulation and board measurements.

The drive strength setting is highly dependent on the termination scheme, so it is critical that you perform pre- and post-layout board-level simulations to determine the proper drive strength settings.

Related Information

On-Chip Termination (Non-Dynamic)

System Loading

You can use memory in a variety of forms, such as individual components or multiple DIMMs, resulting in different loading seen by the FPGA.

The following topics describe the effect on signal quality when interfacing memories in component, dual rank, and dual DIMMs format.

Component Versus DIMM

With discrete DDR2 SDRAM components, the additional loading from the DDR2 SDRAM DIMM connector is eliminated and the memory-side series resistor on the DDR2 SDRAM DIMM is no longer there.

You must perform board level simulations to decide whether the memory-side series resistor near the DDR2 SDRAM is required.

Single Versus DualRank DIMM

DDR2 SDRAM DIMMs are available in either single- or dual-rank DIMM. Single-rank DIMMs are DIMMs with DDR2 SDRAM memory components on one side of the DIMM. Higher-density DIMMs are available as dual-rank, which has DDR2 SDRAM memory components on both sides of the DIMM.

With the dual-rank DIMM configuration, the loading is twice that of a single-rank DIMM. Depending on the board design, you must adjust the drive strength setting on the memory controller to account for this increase in loading.

In a dual-rank DDR2 SDRAM DIMM, the additional loading leads to a slower edge rate, which affects the eye width. The slower edge rate leads to the degradation of the setup and hold time required by the memory as well, which must be taken into consideration during the analysis of the timing for the interface. The overall signal quality remains comparable, but eye width is reduced in the dual-rank DIMM. This reduction in eye width leads to a smaller data capture window that must be taken into account when performing timing analysis for the memory interface.

Single DIMM Versus Multiple DIMMs

Some applications, such as packet buffering, require deeper memory, making a single DIMM interface insufficient.

If you use a multiple DIMM configuration to increase memory depth, the memory controller is required to interface with multiple loads on data strobes and data lines instead of the point-to-point interface in a single DIMM configuration. This results in heavier loading on the interface, which can potentially impact the overall performance of the memory interface.

DDR3 and DDR4 on Arria 10 Devices

The following topics describe considerations specific to DDR3 and DDR4 external memory interface protocols on Arria 10 devices.

Related Information

www.JEDEC.org

Dynamic On-Chip Termination (OCT) in Arria 10 Devices

Depending upon the Rs (series) and Rt (parallel) OCT values that you want, you should choose appropriate values for the RZQ resistor and connect this resistor to the RZQ pin of the Arria 10 device.

- Select a 240-ohm reference resistor to ground to implement Rs OCT values of 34-ohm, 40-ohm, 48-ohm, 60-ohm, and 80-ohm, and Rt OCT resistance values of 20-ohm, 30-ohm, 34-ohm, 40-ohm, 40-ohm, 60-ohm, 80-ohm, 120-ohm and 240 ohm.
- Select a 100-ohm reference resistor to ground to implement Rs OCT values of 25-ohm and 50-ohm, and an RT OCT resistance of 50-ohm.

The following table shows I/O standards and OCT values for DDR3 1.5V.

Signal Type	I/O Standard (1)	Termination Values (ohms) (1)
address/command	SSTL-15	Rs (Output Mode) - 34, 40
	SSTL-15 Class - I	Rs (Output Mode) - 50, No termination
	SSTL-15 Class - II	Rs (Output Mode) - 25, No termination
memory clock	SSTL-15	Rs (Output Mode) - 34, 40
	SSTL-15 Class - I	Rs (Output Mode) - 50, No termination
	SSTL-15 Class - II	Rs (Output Mode) - 25, No termination

Signal Type	I/O Standard (1)	Termination Values (ohms) (1)
data bus (DQ, DQS, DM)	SSTL-15	Rs (output Mode) - 34, 40
		Rt (Input Mode) - 20, 30, 40, 60, 120
	SSTL-15 Class - I	Rs (Output Mode) - 50, No termination
		Rt (Input Mode) - 50, No termination
	SSTL-15 Class - II	Rs (Output Mode) - 25, No termination
		Rt (Input Mode) - 50, No termination

Note to Table:

1. Shown I/O standards and termination values may not include all supported modes. For detailed information about the dynamic OCT feature in the Arria 10 FPGA, refer to the I/O Features chapter of the Arria 10 Devices Handbook.

The following table shows I/O standards and OCT values for DDR3L 1.35V.

Signal Type	I/O Standard (1)	Termination Values (ohms) (1)
address/command	SSTL-135	Rs (Output Mode) - 34, 40
memory clock	SSTL-135	Rs (Output Mode) - 34, 40
data bus (DQ, DQS, DM)	SSTL-135	Rs (Output Mode) - 34, 40
		Rt (Input Mode) - 20, 30, 40, 60, 120

Note to Table:

1. Shown I/O standards and termination values may not include all supported modes. For detailed information about the dynamic OCT feature in the Arria 10 FPGA, refer to the I/O Features chapter of the Arria 10 Devices Handbook.

The following table shows I/O standards and OCT values for DDR4 1.2V.

Signal Type	I/O Standard	Termination Values (ohms)
address/command	SSTL-12	Rs (Output Mode) - 40, 60
memory clock	SSTL-12	Rs (Output Mode) - 40, 60
data bus (DQ, DQS, DM)	1.2-V POD	Rs (Output Mode) - 34, 40, 48, 60
		Rt (Input Mode) - 34, 40, 48, 60, 80, 120, 240

In cases where both Rs and Rt values are selected for the Data Bus, the OCT value will dynamically switch between Rs and Rt depending on the type of operation. Rs is applied during read (output) operations and Rt is applied during read (input) operations.

Dynamic On-Die Termination (ODT) in DDR4

In DDR4, in addition to the Rtt_nom and Rtt_wr values, which are applied during read and write respectively, a third option called Rtt_park is available. When Rtt_park is enabled, a selected (in MR5) value is applied to the DRAM when ODT is driven low.

Rtt_nom and Rtt_wr work the same as in DRR3, which is decribed in *Dynamic ODT for DDR3*.

Refer to the DDR4 JEDEC specification or your memory vendor data sheet for details about available termination values and functional description for dynamic ODT in DDR4 devices.

Choosing Terminations on Arria 10 Devices

To determine optimal on-chip termination (OCT) and on-die termination (ODT) values for best signal integrity, you should simulate your memory interface in Hyperlynx or a similar tool.

If the optimal OCT and ODT termination values as determined by simulation are not available in the list of available values in the parameter editor, select the closest available termination values for OCT and ODT.

Refer to *Dynamic On-Chip Termination (OCT) in Arria 10 Devices* for examples of various OCT modes. Refer to the *Arria 10 device Handbook* for more information about OCT. For information on available ODT choices, refer to your memory vendor data sheet.

Related Information

Dynamic On-Chip Termination (OCT) in Arria 10 Devices on page 4-24

Design Layout Guidelines

The general layout guidelines in the following topic apply to DDR2, DDR3, and DDR4 SDRAM interfaces.

These guidelines will help you plan your board layout, but are not meant as strict rules that must be adhered to. Altera recommends that you perform your own board-level simulations to ensure that the layout you choose for your board allows you to achieve your desired performance.

For more information about how the memory manufacturers route these address and control signals on their DIMMs, refer to the Cadence PCB browser from the Cadence website, at www.cadence.com. The various JEDEC example DIMM layouts are available from the JEDEC website, at www.jedec.org.

For more information about board skew parameters, refer to Board Skews in the Implementing and Parameterizing Memory IP chapter. For assistance in calculating board skew parameters, refer to the board skew calculator tool, which is available at the Altera website.

Note: The following layout guidelines include several +/- length based rules. These length based guidelines are for first order timing approximations if you cannot simulate the actual delay characteristic of the interface. They do not include any margin for crosstalk.

Altera recommends that you get accurate time base skew numbers for your design when you simulate the specific implementation.

Related Information

- **http://www.jedec.org/download/DesignFiles/DDR2/default1.cfm**
- **www.JEDEC.org**
- **www.cadence.com**
- **www.mentor.com**
- **Board Skew Parameters Tool**

General Layout Guidelines

The following table lists general board design layout guidelines. These guidelines are Altera recommendations, and should not be considered as hard requirements. You should perform signal integrity simulation on all the traces to verify the signal integrity of the interface. You should extract the slew rate and propagation delay information, enter it into the IP and compile the design to ensure that timing requirements are met.

Table 4-8: General Layout Guidelines

Parameter	Guidelines
Impedance	• All signal planes must be 50-60-ohm, single-ended, ±10% • All signal planes must be 100-ohm, differential ±10% • All unused via pads must be removed, because they cause unwanted capacitance
Decoupling Parameter	• Use 0.1 uF in 0402 size to minimize inductance • Make VTT voltage decoupling close to pull-up resistors • Connect decoupling caps between VTT and ground • Use a 0.1 uF cap for every other VTT pin and 0.01 uF cap for every VDD and VDDQ pin • Verify the capacitive decoupling using the Altera Power Distribution Network (PDN) Design Tool
Power	• Route GND and V_{CC} as planes • Route VCCIO for memories in a single split plane with at least a 20-mil (0.020 inches, or 0.508 mm) gap of separation • Route VTT as islands or 250-mil (6.35-mm) power traces • Route oscillators and PLL power as islands or 100-mil (2.54-mm) power traces
General Routing	All specified delay matching requirements include PCB trace delays, different layer propagation velocity variance, and crosstalk. To minimize PCB layer propogation variance, Altera recommend that signals from the same net group always be routed on the same layer. • Use 45° angles (*not* 90° corners) • Avoid T-Junctions for critical nets or clocks • Avoid T-junctions greater than 250 mils (6.35 mm) • Disallow signals across split planes • Restrict routing other signals close to system reset signals • Avoid routing memory signals closer than 0.025 inch (0.635 mm) to PCI or system clocks

Layout Guidelines for DDR2 SDRAM Interface

Unless otherwise specified, the following guidelines apply to the following topologies:

- DIMM—UDIMM topology
- DIMM—RDIMM topology
- Discrete components laid out in UDIMM topology
- Discrete components laid out in RDIMM topology

Trace lengths for CLK and DQS should tightly match for each memory component. To match the trace lengths on the board, a balanced tree topology is recommended for clock and address and command signal routing. In addition to matching the trace lengths, you should ensure that DDR timing is passing in the Report DDR Timing report. For Stratix devices, this timing is shown as Write Leveling tDQSS timing. For Arria and Cyclone devices, this timing is shown as CK vs DQS timing

For a table of device family topology support, refer to *Leveling and Dynamic ODT*.

The following table lists DDR2 SDRAM layout guidelines. These guidelines are Altera recommendations, and should not be considered as hard requirements. You should perform signal integrity simulation on all the traces to verify the signal integrity of the interface. You should extract the slew rate and propagation delay information, enter it into the IP and compile the design to ensure that timing requirements are met.

Note: The following layout guidelines also apply to DDR3 SDRAM without leveling interfaces.

Table 4-9: DDR2 SDRAM Layout Guidelines *(1)*

Parameter	Guidelines
DIMMs	If you consider a normal DDR2 unbuffered, unregistered DIMM, essentially you are planning to perform the DIMM routing directly on your PCB. Therefore, each address and control pin routes from the FPGA (single pin) to all memory devices must be on the same side of the FPGA.
General Routing	• All data, address, and command signals must have matched length traces ± 50 ps (±0.250 inches or 6.35 mm) • All signals within a given **Byte Lane Group** should be matched length with maximum deviation of ±10 ps or approximately ±0.050 inches (1.27 mm) and routed in the same layer.

Parameter	Guidelines
Clock Routing	• A 4.7 K-ohm resistor to ground is recommended for each Clock Enable signal. You can place the resistor at either the memory end or the FPGA end of the trace. This guideline applies only to DDR2, and not DDR3. • Route clocks on inner layers with outer-layer run lengths held to under 500 mils (12.7 mm) • These signals should maintain a10-mil (0.254 mm) spacing from other nets • Clocks should maintain a length-matching between clock pairs of ±5 ps or approximately ±25 mils (0.635 mm) • Differential clocks should maintain a length-matching between `P` and `N` signals of ±2 ps or approximately ±10 mils (0.254 mm), routed in parallel • Space between different pairs should be at least three times the space between the differential pairs and must be routed differentially (5-mil trace, 10-15 mil space on centers), and equal to the signals in the `Address/Command` Group or up to 100 mils (2.54 mm) longer than the signals in the `Address/Command` Group. • Trace lengths for CLK and DQS should closely match for each memory component. To match trace lengths on the board, a balanced tree topology is recommended for clock and address and command signal routing. For Stratix device families, ensure that Write Leveling tDQSS is passing in the DDR timing report; for Arria and Cyclone device families, verify that CK vs DQS timing is passing in the DDR timing report.
Address and Command Routing	• Unbuffered address and command lines are more susceptible to cross-talk and are generally noisier than buffered address or command lines. Therefore, un-buffered address and command signals should be routed on a different layer than data signals (`DQ`) and data mask signals (`DM`) and with greater spacing. • Do not route differential clock (`CK`) and clock enable (`CKE`) signals close to address signals.

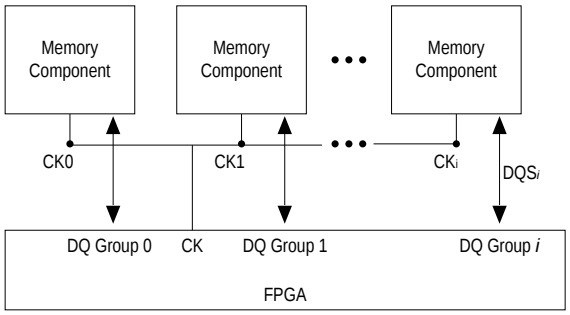
Parameter	Guidelines
DQ, DM, and DQS Routing Rules	• Keep the distance from the pin on the DDR2 DIMM or component to the termination resistor pack (VTT) to less than 500 mils for DQS[x] Data Groups. • Keep the distance from the pin on the DDR2 DIMM or component to the termination resistor pack (VTT) to less than 1000 mils for the ADR_CMD_CTL Address Group. • Parallelism rules for the DQS[x] Data Groups are as follows: • 4 mils for parallel runs < 0.1 inch (approximately 1× spacing relative to plane distance) • 5 mils for parallel runs < 0.5 inch (approximately 1× spacing relative to plane distance) • 10 mils for parallel runs between 0.5 and 1.0 inches (approximately 2× spacing relative to plane distance) • 15 mils for parallel runs between 1.0 and 6.0 inch (approximately 3× spacing relative to plane distance) • Parallelism rules for the ADR_CMD_CTL group and CLOCKS group are as follows: • 4 mils for parallel runs < 0.1 inch (approximately 1× spacing relative to plane distance) • 10 mils for parallel runs < 0.5 inch (approximately 2× spacing relative to plane distance) • 15 mils for parallel runs between 0.5 and 1.0 inches (approximately 3× spacing relative to plane distance) • 20 mils for parallel runs between 1.0 and 6.0 inches (approximately 4× spacing relative to plane distance) • All signals are to maintain a 20-mil separation from other, non-related nets. • All signals must have a total length of < 6 inches. • Trace lengths for CLK and DQS should closely match for each memory component. To match trace lengths on the board, a balanced tree topology is recommended for clock and address and command signal routing. For Stratix device families, ensure that Write Leveling tDQSS is passing in the DDR timing report; for Arria and Cyclone device families, verify that CK vs DQS timing is passing in the DDR timing report.

Parameter	Guidelines
Termination Rules	• When pull-up resistors are used, fly-by termination configuration is recommended. Fly-by helps reduce stub reflection issues. • Pull-ups should be within 0.5 to no more than 1 inch. • Pull up is typically 56-ohms. • If using resistor networks: • Do not share R-pack series resistors between address/command and data lines (DQ, DQS, and DM) to eliminate crosstalk within pack. • Series and pull up tolerances are 1–2%. • Series resistors are typically 10 to 20-ohm. • Address and control series resistor typically at the FPGA end of the link. • DM, DQS, DQ series resistor typically at the memory end of the link (or just before the first DIMM). • If termination resistor packs are used: • The distance to your memory device should be less than 750 mils. • The distance from your Altera's FPGA device should be less than 1250 mils.
Quartus II Software Settings for Board Layout	• To perform timing analyses on board and I/O buffers, use third party simulation tool to simulate all timing information such as skew, ISI, crosstalk, and type the simulation result into the UniPHY board setting panel. • Do not use advanced I/O timing model (AIOT) or board trace model unless you do not have access to any third party tool. AIOT provides reasonable accuracy but tools like HyperLynx provides better result. In operations with higher frequency, it is crucial to properly simulate all signal integrity related uncertainties. • The Quartus II software does timing check to find how fast the controller issues a write command after a read command, which limits the maximum length of the DQ/DQS trace. Check the turnaround timing in the Report DDR timing report and ensure the margin is positive before board fabrication. Functional failure happens if the margin is more than 0.

Note to Table:

1. For point-to-point and DIMM interface designs, refer to the Micron website, www.micron.com.

Figure 4-15: Balanced Tree Topology



CK_i = Clock signal propagation delay to device *i*
DQS_i = DQ/DQS signals propagation delay to group *i*

Related Information

- **External Memory Interface Spec Estimator**
- **www.micron.com**
- **Leveling and Dynamic ODT** on page 4-2

Layout Guidelines for DDR3 and DDR4 SDRAM Interfaces

The following table lists DDR3 and DDR4 SDRAM layout guidelines.

Unless otherwise specified, the guidelines in the following table apply to the following topologies:

- DIMM—UDIMM topology
- DIMM—RDIMM topology
- DIMM—LRDIMM topology
- Not all versions of the Quartus II software support LRDIMM.
- Discrete components laid out in UDIMM topology
- Discrete components laid out in RDIMM topology

These guidelines are Altera recommendations, and should not be considered as hard requirements. You should perform signal integrity simulation on all the traces to verify the signal integrity of the interface. You should extract the slew rate and propagation delay information, enter it into the IP and compile the design to ensure that timing requirements are met.

Refer to the *External Memory Interface Spec Estimator* for all supported frequencies and topologies.

For frequencies greater than 800 MHz, when you are calculating the delay associated with a trace, you must take the FPGA package delays into consideration. For more information, refer to *Package Deskew*.

Note: For device families that do not support write leveling, refer to *Layout Guidelines for DDR2 SDRAM Interface*.

Table 4-10: DDR3 and DDR4 SDRAM Layout Guidelines *(1)*

Parameter	Guidelines
Decoupling Parameter	• Make VTT voltage decoupling close to the components and pull-up resistors. • Connect decoupling caps between VTT and VDD using a 0.1 F cap for every other VTT pin. • Use a 0.1 uF cap and 0.01 uF cap for every VDDQ pin.
Maximum Trace Length *(2)*	• Even though there are no hard requirements for minimum trace length, you need to simulate the trace to ensure the signal integrity. Shorter routes result in better timing. • For DIMM topology only: • Maximum trace length for all signals from FPGA to the first DIMM slot is 4.5 inches. • Maximum trace length for all signals from DIMM slot to DIMM slot is 0.425 inches. • For discrete components only: • Maximum trace length for address, command, control, and clock from FPGA to the first component must not be more than 7 inches. • Maximum trace length for DQ, DQS, DQS#, and DM from FPGA to the first component is 5 inches.
General Routing	• Route over appropriate VCC and GND planes. • Keep signal routing layers close to GND and power planes.

Parameter	Guidelines
Clock Routing	• Route clocks on inner layers with outer-layer run lengths held to under 500 mils (12.7 mm). • Route clock signals in a daisy chain topology from the first SDRAM to the last SDRAM. The maximum length of the first SDRAM to the last SDRAM must not exceed 0.69 tCK. For different DIMM configurations, check the appropriate JEDEC specification. • These signals should maintain the following spacings: • 10-mil (0.254 mm) spacing for parallel runs less than 0.5 inches or 2x trace-to-plane distance. • 15-mil spacing for parallel runs between 0.5 and 1 inches or 3× trace-to-plane distance. • 20-mil spacing for parallel runs between 1 and 6 inches or 4× trace-to-plane distance. • Clocks should maintain a length-matching between clock pairs of ±5 ps or approximately ±25 mils (0.635 mm). • Clocks should maintain a length-matching between positive (p) and negative (n) signals of ±2 ps or approximately ±10 mils (0.254 mm), routed in parallel. • Space between different pairs should be at least two times the trace width of the differential pair to minimize loss and maximize interconnect density. • To avoid mismatched transmission line to via, Altera recommends that you use Ground Signal Signal Ground (GSSG) topology for your clock pattern—GND|CLKP|CKLN|GND. • Route all addresses and commands to match the clock signals to within ±20 ps or approximately ± 125 mil (± 3.175 mm) to each discrete memory component. Refer to the following figure.
Address and Command Routing	• Route address and command signals in a daisy chain topology from the first SDRAM to the last SDRAM. The maximum length of the first SDRAM to the last SDRAM must not be more than 0.69 tCK. For different DIMM configurations, check the appropriate JEDEC specifications. • UDIMMs are more susceptible to cross-talk and are generally noisier than buffered DIMMs. Therefore, route address and command signals of UDIMMs on a different layer than data signals (DQ) and data mask signals (DM) and with greater spacing. • Do not route differential clock (CK) and clock enable (CKE) signals close to address signals. • Route all addresses and commands to match the clock signals to within ±20 ps or approximately ± 125 mil (± 3.175 mm) to each discrete memory component. Refer to the following figure. • Parallelism rules for address and command and clock signals are as follows: • 4 mils for parallel runs <0.1 inch (approximately 1× spacing relative to plane distance) • 10 mils for parallel runs <0.5 inch (approximately 2× spacing relative to plane distance) • 15 mils for parallel runs between 0.5 and 1.0 inches (approximately 3× spacing relative to plane distance) • 20 mils for parallel runs between 1.0 and 6.0 inches (approximately 4× spacing relative to plane distance)

Parameter	Guidelines

DQ, DM, and DQS Routing Rules	• All the trace length matching requirements are from the FPGA package ball to the SDRAM package ball, which means you must consider trace mismatching on different DIMM raw cards.
	• Match in length all DQ, DQS, and DM signals within a given byte-lane group with a maximum deviation of ±10 ps or approximately ± 50 mils (± 1.27 mm).
	• Ensure to route all DQ, DQS, and DM signals within a given byte-lane group on the same layer to avoid layer to layer transmission velocity differences, which otherwise increase the skew within the group.
	• Parallelism rules for all signals (other than address and command) are as follows:
	• 5 mils for parallel runs < 0.5 inch (approximately 1× spacing relative to plane distance)
	• 10 mils for parallel runs between 0.5 and 1.0 inches (approximately 2× spacing relative to plane distance)
	• 15 mils for parallel runs between 1.0 and 6.0 inch (approximately 3× spacing relative to plane distance)
	• Do not count on FPGAs to deskew for more than 20 ps of DQ group skew. The skew algorithm only removes the following possible uncertainties:
	  • Minimum and maximum die IOE skew or delay mismatch
	  • Minimum and maximum device package skew or mismatch
	  • Board delay mismatch of 20 ps
	  • Memory component DQ skew mismatch
	  • Increasing any of these four parameters runs the risk of the deskew algorithm limiting, failing to correct for the total observed system skew. If the algorithm cannot compensate without limiting the correction, timing analysis shows reduced margins.
	• For memory interfaces with leveling, the timing between the DQS and clock signals on each device calibrates dynamically to meet tDQSS. To make sure the skew is not too large for the leveling circuit's capability, follow these rules:
	  • Propagation delay of clock signal must not be shorter than propagation delay of DQS signal at every device: (CKi) – DQSi > 0; 0 < *i* < number of components – 1
	  • Total skew of CLK and DQS signal between groups is less than one clock cycle: (CKi+ DQSi) max – (CKi+ DQSi) min < 1 × tCK(If you are using a DIMM topology, your delay and skew must take into consideration values for the actual DIMM.)

Parameter	Guidelines
Termination Rules	• When using DIMMs, you have no concerns about terminations on memory clocks, addresses, and commands. • If you are using components, use an external parallel termination of 40-ohms to VTT at the end of the fly-by daisy chain topology on the addresses and commands. • For memory clocks, use an external parallel termination of 75-ohms differential at the end of the fly-by daisy chain topology on the memory clocks. Fly-by daisy chain topology helps reduce stub reflection issues. • If you include a compensation capacitor at the first memory load, it may improve the waveform signal integrity. • Keep the length of the traces to the termination to within 0.5 inch (14 mm) . • Use resistors with tolerances of 1 to 2%.
Quartus II Software Settings for Board Layout	• To perform timing analyses on board and I/O buffers, use third party simulation tool to simulate all timing information such as skew, ISI, crosstalk, and type the simulation result into the UniPHY board setting panel. • Do not use advanced I/O timing model (AIOT) or board trace model unless you do not have access to any third party tool. AIOT provides reasonable accuracy but tools like HyperLynx provide better results.

Notes to Table:

1. For point-to-point and DIMM interface designs, refer to the Micron website, www.micron.com.
2. For better efficiency, the UniPHY IP requires faster turnarounds from read commands to write.

Related Information

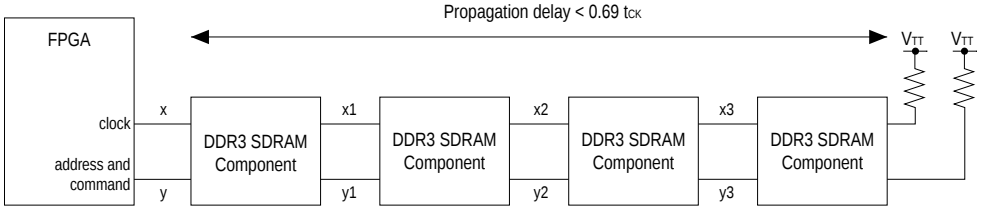
- **Layout Guidelines for DDR2 SDRAM Interface** on page 4-27
- **Package Deskew** on page 4-40
- **External Memory Interface Spec Estimator**
- **www.micron.com**

Length Matching Rules

The following topics provide guidance on length matching for different types of DDR3 signals.

Route all addresses and commands to match the clock signals to within ±20 ps or approximately ± 125 mil (± 3.175 mm) to each discrete memory component. The following figure shows the DDR3 SDRAM component routing guidelines for address and command signals.

Figure 4-16: DDR3 SDRAM Component Address and Command Routing Guidelines



If using discrete components:
x = y ± 125 mil
x + x1 = y + y1 ± 125 mil
x + x1 + x2 = y + y1 + y2 ± 125 mil
x + x1 + x2 + x3 = y + y1 + y2 +y3 ± 125 mil

If using a DIMM topology:
x=y +/- 125 mil

The timing between the DQS and clock signals on each device calibrates dynamically to meet tDQSS. The following figure shows the delay requirements to align DQS and clock signals. To ensure that the skew is not too large for the leveling circuit's capability, follow these rules:

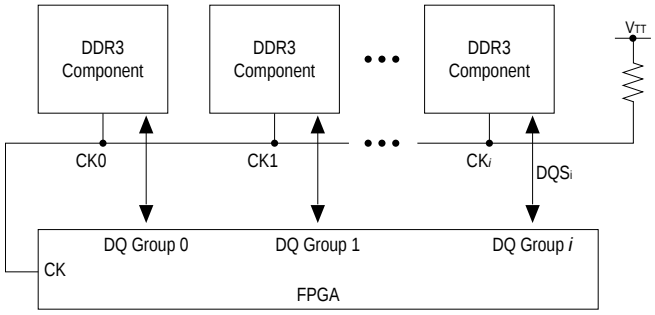
- Propagation delay of clock signal must not be shorter than propagation delay of DQS signal at every device:

  ```
  CKi  – DQSi > 0; 0 < i < number of components – 1
  ```

- Total skew of CLK and DQS signal between groups is less than one clock cycle:

  ```
  (CKi + DQSi) max – (CKi + DQSi) min < 1 × tCK
  ```

Figure 4-17: Delaying DQS Signal to Align DQS and Clock



CK*i* = Clock signal propagation delay to device *i*
DQS*i* = DQ/DQS signals propagation delay to group *i*

Clk pair matching—If you are using a DIMM (UDIMM, RDIMM, or LRDIMM) topology, match the trace lengths up to the DIMM connector. If you are using discrete components, match the lengths for all the memory components connected in the fly-by chain.

DQ group length matching—If you are using a DIMM (UDIMM, RDIMM, or LRDIMM) topology, match the trace lengths up to the DIMM connector. If you are using discrete components, match the lengths up to the respective memory components.

When you are using DIMMs, it is assumed that lengths are tightly matched within the DIMM itself. You should check that appropriate traces are length-matched within the DIMM.

Layout Guidelines for DDR3 SDRAM Wide Interface (>72 bits)

The following topics discuss different ways to lay out a wider DDR3 SDRAM interface to the FPGA. Choose the topology based on board trace simulation and the timing budget of your system.

The UniPHY IP supports up to a 144-bit wide DDR3 interface. You can either use discrete components or DIMMs to implement a wide interface (any interface wider than 72 bits). Altera recommends using leveling when you implement a wide interface with DDR3 components.

When you lay out for a wider interface, all rules and constraints discussed in the previous sections still apply. The DQS, DQ, and DM signals are point-to-point, and all the same rules discussed in "Design Layout Guidelines" apply.

The main challenge for the design of the fly-by network topology for the clock, command, and address signals is to avoid signal integrity issues, and to make sure you route the DQS, DQ, and DM signals with the chosen topology.

Related Information

Design Layout Guidelines on page 4-26

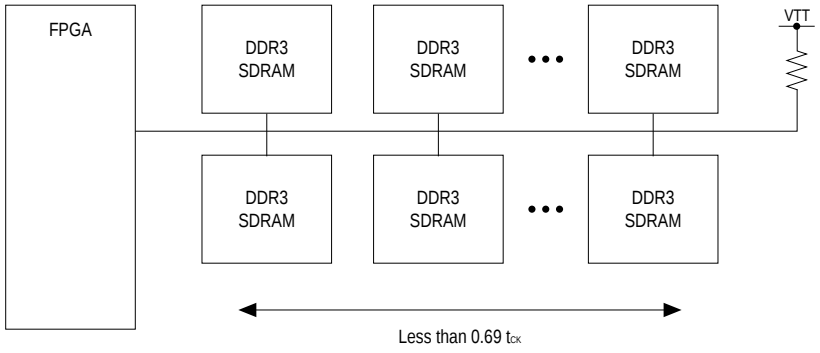
Fly-By Network Design for Clock, Command, and Address Signals

The UniPHY IP requires the flight-time skew between the first DDR3 SDRAM component and the last DDR3 SDRAM component to be less than 0.69 tCK for memory clocks. This constraint limits the number of components you can have for each fly-by network.

If you design with discrete components, you can choose to use one or more fly-by networks for the clock, command, and address signals.

The following figure shows an example of a single fly-by network topology.

Figure 4-18: Single Fly-By Network Topology

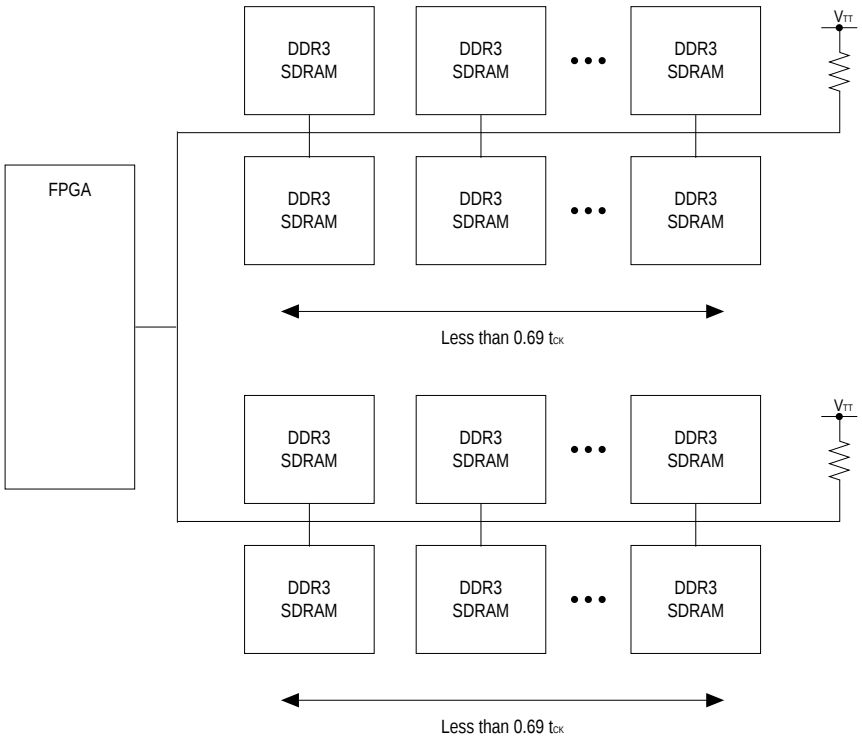


Every DDR3 SDRAM component connected to the signal is a small load that causes discontinuity and degrades the signal. When using a single fly-by network topology, to minimize signal distortion, follow these guidelines:

- Use ×16 device instead ×4 or ×8 to minimize the number of devices connected to the trace.
- Keep the stubs as short as possible.
- Even with added loads from additional components, keep the total trace length short; keep the distance between the FPGA and the first DDR3 SDRAM component less than 5 inches.
- Simulate clock signals to ensure a decent waveform.

The following figure shows an example of a double fly-by network topology. This topology is not rigid but you can use it as an alternative option. The advantage of using this topology is that you can have more DDR3 SDRAM components in a system without violating the 0.69 tCK rule. However, as the signals branch out, the components still create discontinuity.

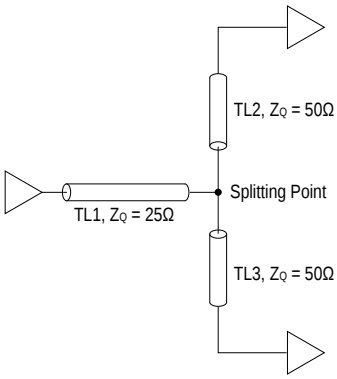
Figure 4-19: Double Fly-By Network Topology



You must perform simulations to find the location of the split, and the best impedance for the traces before and after the split.

The following figure shows a way to minimize the discontinuity effect. In this example, keep TL2 and TL3 matches in length. Keep TL1 longer than TL2 and TL3, so that it is easier to route all the signals during layout.

Figure 4-20: Minimizing Discontinuity Effect



You can also consider using a DIMM on each branch to replace the components. Because the trade impedance on the DIMM card is 40-ohm to 60-ohm, perform a board trace simulation to control the reflection to within the level your system can tolerate.

By using the new features of the DDR3 SDRAM controller with UniPHY and the Stratix III, Stratix IV, or Stratix V devices, you simplify your design process. Using the fly-by daisy chain topology increases the complexity of the datapath and controller design to achieve leveling, but also greatly improves performance and eases board layout for DDR3 SDRAM.

You can also use the DDR3 SDRAM components without leveling in a design if it may result in a more optimal solution, or use with devices that support the required electrical interface standard, but do not support the required read and write leveling functionality.

Package Deskew

Trace lengths inside the device package are not uniform for all package pins. The nonuniformity of package traces can affect system timing for high frequencies. In the Quartus II software version 12.0 and later, a package deskew option is available.

If you do not enable the package deskew option, the Quartus II software uses the package delay numbers to adjust skews on the appropriate signals; you do not need to adjust for package delays on the board traces. If you do enable the package deskew option, the Quartus II software does not use the package delay numbers for timing analysis, and you must deskew the package delays with the board traces for the appropriate signals for your design.

Package Deskew Recommendation for Stratix V Devices

Package deskew is not required for any memory protocol operating at 800 MHz or below.

For DDR3 and RLDRAM3 designs operating above 800 MHz, you should run timing analysis with accurately entered board skew parameters in the MegaWizard parameter editor. If **Report DDR** reports non-core timing violations, you should then perform the steps in the following topics, and modify your board layout. Package deskew is not required for any protocols other than DDR3 and RLDRAM 3.

DQ/DQS/DM Deskew

To get the package delay information, follow these steps:

1. Select the **FPGA DQ/DQS Package Skews Deskewed on Board** checkbox on the **Board Settings** tab of the parameter editor.
2. Generate your IP.
3. Instantiate your IP in the project.
4. Run **Analysis and Synthesis** in the Quartus II software.
5. Run the `<core_name>_p0_pin_assignment.tcl` script.
6. Compile your design.
7. Refer to the **All Package Pins** compilation report, or find the pin delays displayed in the `<core_name>.pin` file.

Address and Command Deskew

Deskew address and command delays as follows:

1. Select the **FPGA Address/Command Package Skews Deskewed on Board** checkbox on the **Board Settings** tab of the parameter editor.
2. Generate your IP.
3. Instantiate your IP in the project.
4. Run **Analysis and Synthesis** in the Quartus II software.
5. Run the `<core_name>_p0_pin_assignment.tcl` script.
6. Compile your design.
7. Refer to the **All Package Pins** compilation report, or find the pin delays displayed in the `<core_name>.pin` file.

Package Deskew Recommendations for Arria 10 Devices

The following table shows package deskew recommendations for all protocols supported on Arria 10 devices.

As operating frequencies increase, it becomes increasingly critical to perform package deskew. The frequencies listed in the table are the *minimum* frequencies for which you must perform package deskew.

If you plan to use a listed protocol at the specified frequency or higher, you must perform package deskew. For example, you must perform package deskew if you plan to use dual-rank DDR4 at 800 MHz or above.

Protocol	Minimum Frequency (MHz) for Which to Perform Package Deskew		
	Single Rank	Dual Rank	Quad Rank
DDR4	933	800	667
DDR3	Not required	800	Not required
LPDDR3	667	533	Not required
QDR IV	933	Not applicable	Not applicable
RLDRAM 3	Not required	667	Not applicable
RLDRAM II	Not required	Not applicable	Not applicable
QDR II	Not required	Not applicable	Not applicable

The recommendations in the above table are based on preliminary timing models, and may be updated in the future. If you are designing a board with Arria 10 devices and require exact package trace delays, contact Altera Support.

Deskew Example

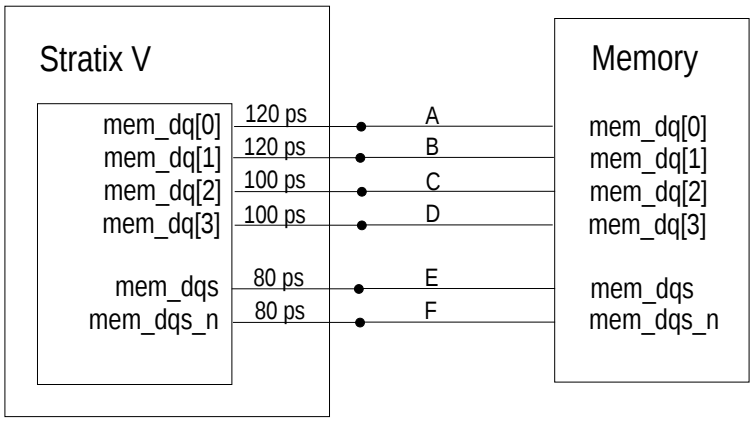
Consider an example where you want to deskew an interface with 4 DQ pins, 1 DQS pin, and 1 DQSn pin.

Let's assume an operating frequency of 667 MHz, and the package lengths for the pins reported in the **.pin** file as follows:

```
dq[0] = 120 ps
dq[1] = 120 ps
dq[2] = 100 ps
dq[3] = 100 ps
dqs   = 80 ps
dqs_n = 80 ps
```

The following figure illustrates this example.

Figure 4-21: Deskew Example

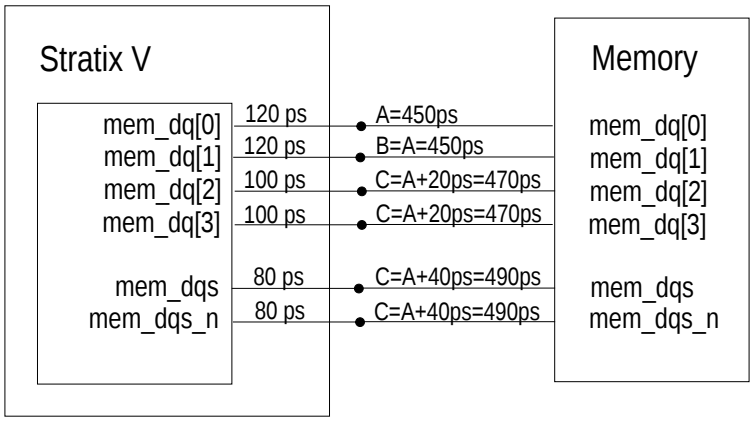


When you perform length matching for all the traces in the DQS group, you must take package delays into consideration. Because the package delays of traces A and B are 40 ps longer than the package delays of traces E and F, you would need to make the board traces for E and F 40 ps longer than the board traces for A and B.

A similar methodology would apply to traces C and D, which should be 20 ps longer than the lengths of traces A and B.

The following figure shows this scenario with the length of trace A at 450 ps.

Figure 4-22: Deskew Example with Trace Delay Calculations



When you enter the board skews into the Board Settings tab of the DDR3 parameter editor, you should calculate the board skew parameters as the sums of board delay and corresponding package delay. If a pin does not have a package delay (such as address and command pins), you should use the board delay only.

The example of the preceding figure shows an ideal case where board skews are perfectly matched. In reality, you should allow plus or minus 2 ps of skew mismatch within a DQS group (DQ/DQS/DM).

Package Migration

Package delays can be different for the same pin in different packages. If you want to use multiple migratable packages in your system, you should compensate for package skew as described in this topic.

Assume two migratable packages, device A and device B, and that you want to compensate for the board trace lengths for device A. Follow these steps:

1. Compile your design for device A, with the Package Skew option enabled.
2. Note the skews in the `<core_name>.pin` file for device A. Deskew these package skews with board trace lengths as described in the preceding examples.
3. Recompile your design for device A.
4. For Device B open the parameter editor and deselect Package Deskew option.
5. Calculate board skew parameters only taking into account the board traces for Device B and enter that value into the parameter editor for Device B.
6. Regenerate the IP and recompile the design for Device B.
7. Verify that timing requirements are met for both device A and device B.

Document Revision History

Date	Version	Changes
December 2013	2013.12.16	• Review and minor updates of content. • Consolidated General Layout Guidelines. • Added DDR3 and DDR4 information for Arria 10 devices. • Updated chapter title to include DDR4 support. • Removed references to ALTMEMPHY. • Removed references to Cyclone III and Cyclone IV devices. • Removed references to Stratix II devices. • Corrected Vtt to Vdd in *Memory Clocks for DDR3 SDRAM UDIMM* section.
November 2012	5.0	• Updated *Layout Guidelines for DDR2 SDRAM Interface* and *Layout Guidelines for DDR3 SDRAM Interface*. • Added LRDIMM support. • Added Package Deskew section.
June 2012	4.1	Added Feedback icon.
November 2011	4.0	Added Arria V and Cyclone V information.

Date	Version	Changes
June 2011	3.0	• Merged DDR2 and DDR3 chapters to *DDR2 and DDR3 SDRAM Interface Termination and Layout Guidelines* and updated with leveling information. • Added Stratix V information.
December 2010	2.1	Added *DDR3 SDRAM Interface Termination, Drive Strength, Loading, and Board Layout Guidelines* chapter with Stratix V information.
July 2010	2.0	Updated Arria II GX information.
April 2010	1.0	Initial release.