

Mid-Term Examination

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Ans 1

①

D-MOSFETStructure

- N-type semiconductor exist between source & drain.
- Source, drain, gate are connected physically.

E-MOSFET

There is no channel between source & drain.

In E-MOSFET they are not connected physically

Working

- If $V_{GS} = 0$, I_{DS} flows due to V_{DS} if $V_{GS} = 0V$, $I_{DS} = 0$ although V_{DS} is applied
- Can be used as E-MOSFET Cannot be used as D-MOSFET

Ans ①

⑥ IC fabrication steps -

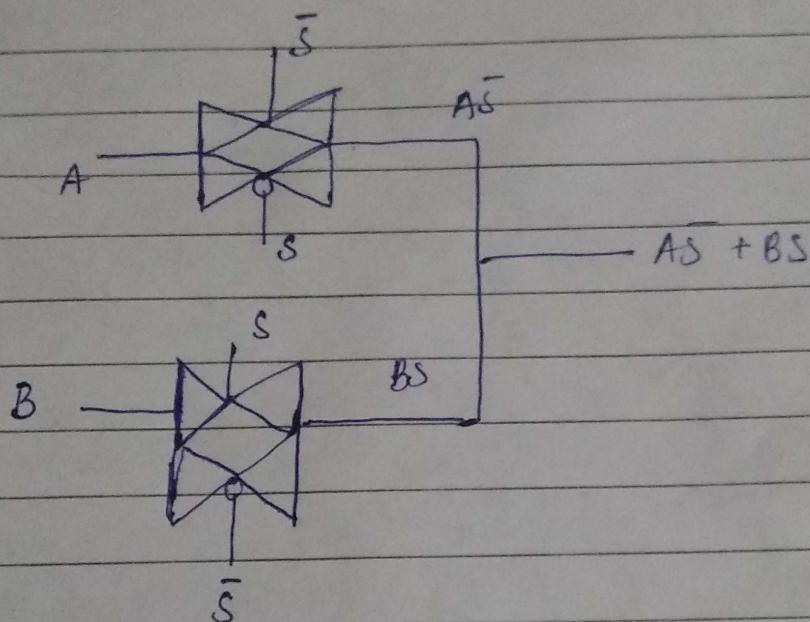
Ans 1

- Lithography
process of pattern definition by applying thin uniform layer of viscous liquid on wafer surface.
- Etching — selectively removing unwanted material from surface of wafer.
- Depositing — Films of various materials are applied on the wafer.
- Chemical Mechanical Polishing — A planarization technique by applying a chemical slurry with etchant agent to wafer surface.
- Oxidation — In this process, H_2O molecules converts silicon layers on top of wafer to silicon dioxide.
- Ion Implantation
- Diffusion.

Ans (1) (c) NAND gate is better because -

- NAND offers less delay
- NAND uses transistor of smaller sizes.
- NAND has better ratio of output high drive and output low drive as compared to NOR gates

Ans (1) (c)



Ans (1) (d)

$$n_n = 600 \times 10^{-4} \text{ cm}^2/\text{Vs} ; L = 2 \mu\text{m}$$

$$C_{ox} = 7 \times 10^{-8} \quad V_t = 1.0V$$

$$W = 20 \mu\text{m} = 20 \times 10^{-6} \text{ m} \quad V_S = 0V$$

$$V_{on} = 5V \quad V_D = 4V$$

$$\lambda = 0.05 \text{ V}^{-1} \quad V_{DS} = 0.05V$$

$$V_{GS} = BV, \quad V_D = V_S V_{DS} = 4V$$

$$V_{DS} = V_{GS} - V_t$$

saturation region

$$I_0(\text{out}) = \frac{\mu n (\text{Co})}{2} \cdot \frac{W}{L} (V_{DS} - V_{TO})^2 (1 + \alpha V_{DS})$$

$$= \frac{600 \times 2 \times 10^{-8}}{2} \times \frac{20}{2} (5 - 1)^2 (1 + 0.05 \times 4)$$

$$= 21 \times 10^{-5} \times 16 \times 1.2$$

$$= 403.2 \times 10^{-9}$$

Ans(2)

(a)

NMOS

$$V_{TO \pm n} = -0.48 \text{ V} \quad \mu_n C_{Ox} = 102 \text{ nA/V}^2$$

PMOS

$$V_{T, p} = -0.46 \text{ V} \quad \mu_p C_{Ox} = 51.6 \text{ nA/V}^2$$

$$K_n = \mu_n C_{Ox} \cdot \frac{W}{L} = 102 \times 10 \times 10^{-6}$$

$$K_p = \mu_p C_{Ox} \cdot \frac{W}{L} = 51.6 \times 19 \times 10^{-6}$$

$$\text{as } K_n = 1020 \times 10^{-6} \text{ A/V}^2$$

$$K_p = 980 \times 10^{-6} \text{ A/V}^2$$

$$V_{TH} = 0.48 \text{ V}$$

$$V_{TH} = -0.46 \text{ V}$$

We have to find V_{IL} and V_{IH} for noise margin

$$\text{as } V_{TH} \approx |V_{THP}| \text{ and } \frac{K_n}{K_p} = \frac{1020 \times 10^{-6}}{980 \times 10^{-6}}$$

$$\approx 1$$

so, V_{IL} for CMOS

$$V_{IL} = \frac{1}{8} (3V_{DD} + 2V_{TH}) = \frac{1}{8} (3 \times 12 + 2 \times 0.48)$$

$$V_{IL} = \frac{4.56}{8} = 0.56 \text{ V}$$

$$V_{IH} = \frac{1}{8} (5V_{DD} - 2V_{TH})$$

$$= \frac{1}{8} (5 \times 1.2 - 2 \times 0.48)$$

$$V_{IH} = \frac{6.96}{8} = 0.87 \text{ V}$$

$$V_{IL} = 0.56$$

$$V_{IH} = 0.87$$

$$\begin{aligned} \text{Noise margin lower} &= V_{SL} - V_{OL} = V_{IL} - 0 = 0.50 \text{ V} \\ \text{Noise margin higher} &= V_{OH} - V_{IH} = V_{DD} - V_{IH} \\ &= 0.35 \text{ V} \end{aligned}$$

Ans(2) b)

The constant field scaling is a technique by which the device dimensions and the device voltage are scaled. In this analysis both the vertical and horizontal electric field are scaled by a common factor or kept constant.

Constant field scaling provides the largest reduction in power delay product of a single transistor. But it needs a decrease in the power supply voltage if size is reduced to a large extent.

Before scaling

L

w

t

x_p

V_{DD}

V_{TH}

N_A or N_D

C_{ox}

I_{DS}

P_D

After constant
field scaling

$$L = L/s$$

$$w = w/s$$

$$t_{ox} = t_{ox}/s$$

$$x_p = x_p/s$$

$$V_{DD} = V_{DD}/s$$

$$V_{TH} = V_{TH}/s$$

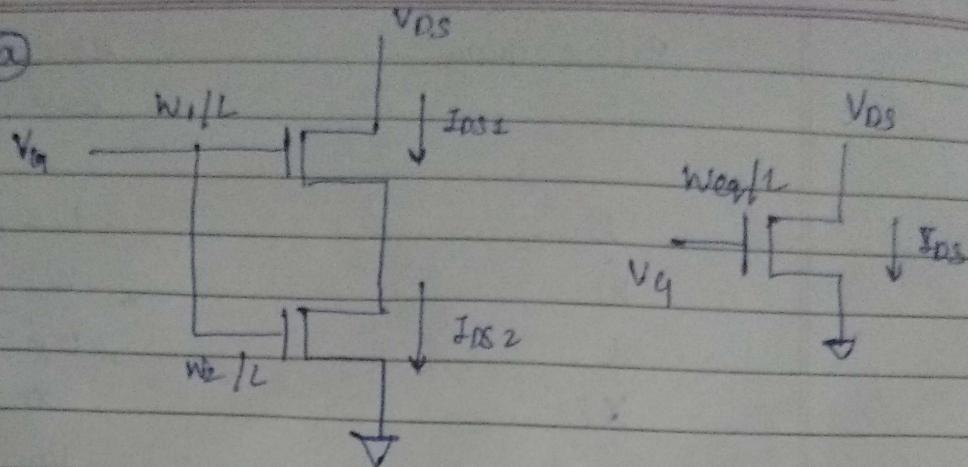
$$N_A = N_A * s \quad N_D = N_D * s$$

$$C_{ox} = C_{ox} * s$$

$$I_{DS} = I_{DS} / s$$

$$P_D = P_D / s^2$$

Ans 3 @



We know that $I_{DS} = I_{DS1} = I_{DS2}$ assuming all transistors operating in linear region

$$I_{DS} = I_{DS2} = \frac{k' w_1}{L} \left[(V_{GS} - V_{TO} - V_{DS2}) (V_{DS} - V_{DS2}) - \frac{1}{2} (V_{DS} - V_{DS2})^2 \right]$$

$$I_{DS} = I_{DS2} = \frac{k' w_2}{L} \left[(V_{GS} - V_{TO}) V_{DS2} - \frac{1}{2} V_{DS2}^2 \right]$$

$$I_{DS} = \frac{k' w_1}{L} \left[(V_{GS} - V_{TO} - V_{DS2}) V_{DS} - (V_{GS} - V_{TO} - V_{DS2}) V_{DS2} - \frac{1}{2} V_{DS}^2 + V_{DS} V_{DS2} - \frac{1}{2} V_{DS2}^2 \right]$$

Measuring,

$$\left(1 + \frac{w_1}{w_2} \right) I_{DS} = \frac{k' w_1}{L} \left[(V_{GS} - V_{TO}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

Therefore

$$W_{eq} = \frac{w_1 \cdot w_2}{w_1 + w_2} = \frac{1}{W_{eq}} = \frac{1}{w_1} + \frac{1}{w_2}$$

Ans (3) (b)

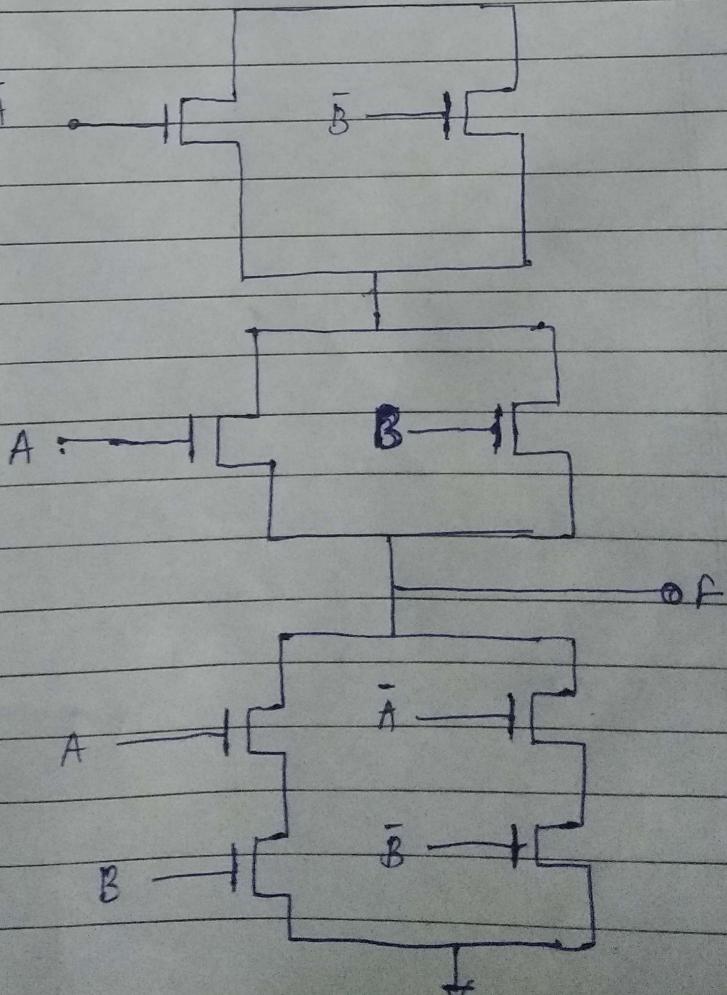
A	B	\bar{A}	\bar{B}	Part 1	Part 2	F
0	0	1	1	0	0	0
0	1	1	0	0	1	1
1	0	0	1	1	0	1
1	1	0	0	0	0	0

$$\text{Part 1} = A \cdot \bar{B}$$

$$\text{Part 2} = \bar{A} \cdot B$$

$$F = A\bar{B} + \bar{A}B$$

Using AOI gates



Using logic functions

