Course Title : Computer Architecture			
Course Code : P18CS61	**Semester : 6**	**L :T:P : 4:0:0**	**Credits: 4**
Contact Period: Lecture: 52 Hr, Exam: 3 Hr		**Weightage: CIE:50%, SEE:50%**	

Course Content

Unit-1

Fundamentals of Computer Design: Introduction, Classes of Computers, Defining Computer Architecture, Trends in Technology, Dependability, Measuring, Reporting and Summarizing Performance, Quantitative Principles of Computer Design.

Self Study Component: Trends in Power in Integrated Circuit, Trends in Cost, System Inter-connect Architecture.

10 Hours

Uni-2

Pipelining : **Basic and Intermediate Concepts:** Introduction, The major hurdle of Pipeling – pipeline hazards, How is pipelining implemented, What makes pipelining hard to implement, Extending the MIPS pipeline to handle Multicycle operations.

Self Study Component: Linear Pipeline Processors: Asynchronous and Synchronous Models, Non-linear Pipeline Processors: Reservation and Latency Analysis, Collision free scheduling.

10 Hours

Unit-3

Instruction-Level parallelism and its Exploitation: Instruction –Level Parallelism: Concepts and Challenges, Basic Complier Techniques for Exposing ILP, Reducing Branch costs with Prediction, Overcome Data Hazards with Dynamic Scheduling, Dynamic Scheduling: Examples and the Algorithm.

Self Study Component: Instruction Set Architectures, Hardware based Speculation, Studies of the Limitations of ILP

11 Hours

Unit-4

Multiprocessor and Thread Level Parallelism: Introduction, Symmetric shared- memory architectures, Distributed Shared Memory and Directory based Coherence, Synchronization-The Basic, Models of Memory Consistency – An Introduction

Self Study Component: Performance of Symmetric Shared–Memory Multiprocessors, Crossbar Switch

10 Hours

Unit-5

Parallel Programs: The Parallelization Process: Steps in The Process, Parallelization Computation Versus Data, and Parallelization of an Example Program: The Equation Solver Kernel, Decomposition, Assignment, Orchestration under the Shared address Space Model, Orchestration under the Message –Passing Model.

Self-study component: Scalable Multiprocessors: Scalability, Bandwidth scaling, Latency scaling, Cost Scaling, Physical Scaling, Realizing Programming Model: Primitive Network Transaction, Shared address Space, Message Passing.

11 Hours

Text Books:

1. John L. Hennessy and David A. Patterson : Computer Architecture, A quantitative approach, Fourth Edition, Morgan Kaufmann Publishers, Elsevier 2010

2. David E Culler Jaswinder Pal Singh with Anoop Gupta, "Parallel Computer Architecture" A Hardware/Software Approach, Morgan Kaufmann Publications Elsevier 2012.

Reference Books:

1. Kai Hwang & Naresh Jotwani," Advanced Computer Architecture", Parallelism, scalability, Programmability 2 nd edition McGraw Hill 2012.
2. John P Hayes, Computer Architecture & Organization 3rd Ed. McGraw Hill 1998.

Course Outcomes:

1. Describe the evolution of computers.
2. Analyze the basic properties of pipelining.
3. Understand the Instruction Level Parallelism and Its Exploitation.
4. Discuss system architecture of multiprocessor and Thread Level Parallelism.
5. Analyze the steps to perform parallelization of computation.

CO-PO Mapping

Semester: 6th	**Course code : P18CS61**	**Title : Computer Architecture**													
CO	Statement	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS 01	PS 02
CO1	Describe the evolution of computers	3	1	1										3	
CO2	Analyze the basic properties of pipelining	2	3	2	1									2	
CO3	Understand the Instruction Level Parallelism and Its Exploitation.	2	2	1										2	
CO4	Discuss system architecture of multiprocessor and Thread Level Parallelism.	3	2	2										3	
CO5	Analyze the steps to perform parallelization of computation	2	3	2	1									2	
		2.4	2.2	1.6	1									2.4	