Course Title : Digital Logic Design Laboratory			
Course Code : P18CSL38	Semester : 3	L :T:P:H : 0:0:3:3	Credits: 1.5
Contact Period: Laboratory : 3 Hrs/week, Exam: 3 Hr		Weightage: CIE:50%, SEE:50%	

Course Content

1. a) Show that NAND & NOR are universal gates
   b) Write the VHDL code for Basic gates realization using NAND gates.

Experiment on Code Converters:

2. a) Design BCD to Excess -3 using basic gates.
   b) Write the VHDL code for BCD to Excess -3 code conversion

Experiment on data processing circuit.

3. a) Implement the following using 8:1 multiplexer
   i) Full adder
   ii) Given 4 variable expression
   b) Write the VHDL code for an 8:1 multiplexer.

Comparator circuits

4. a) 2 bit Magnitude comparator using suitable Decoder
   b) Write the VHDL code for 2 bit comparator

Arithmetic circuits & Encoder

5. a) Implement Full Subtractor using suitable Decoder and NAND gates.
   b) Write the VHDL code for Full subtractor.
6. a) Implement a Octal to binary encoder using basic gates.

   b) Write the VHDL code for Octal to binary encoder

Shift Register

7. a) Design a 3-bit serial-in –serial out and a serial-in –parallel out shift register using J-K flip flop
   b) Write the VHDL code for Johnson counter.
8. a) Implement a ring counter and Johnson counter using 4-bit shift register.
   b) Write the VHDL code for Ring counter.

Counters

1. a) Design a **Mod n** ($n \leq 8$) Asynchronous counter using J-K flipflop
   b) Write the VHDL code for T Flip Flop
10. a) Design and implement 3 bit synchronous up counter using J-K Flip -Flop ICs.
    b) Write the VHDL code for 3 bit up counter
11. a) Design a counter for the given sequence with lock in condition using D Flip Flop
    b) Write the VHDL code for D Flip Flop
12. a) Design a 2 bit down counter using JK- Flip –Flop.
    b) Write the VHDL code for 3 bit Down Counter

Course Outcomes

1. **Design and Conduct experiments** to realize various combinational and sequential circuits using IC.
2. **Simulate** using Xilinx to synthesize their designs and perform timing analysis.

CO-PO mapping

Semester: 3		**Course code : P18CSL38**				**Title : Digital Logic Design Laboratory**									
CO	**Statement**	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PS O1**	**PS O2**
CO308.1	**Design and Conduct experiments** to realize various combinational and sequential circuits using IC	3	3	3						2				2	
CO308.2	**Simulate** using Xilinx to synthesize their designs and perform timing analysis.	2	2	3		3				2				1	
CO308.3		**2.5**	**2.5**	**3**		**3**				**2**				**1.5**	

Note: Students should design and conduct any one experiment and simulate the experiment given in the same section.(for both CIE and SEE)