Course Title : Digital Logic Design			
Course Code : P18CS32	**Semester : 3**	**L :T:P:H : 4:0:0:4**	**Credits: 3**
Contact Period: Lecture: 52 Hr, Exam: 3 Hr		**Weightage: CIE:50%, SEE:50%**	

Course Content

Unit-1

Digital Logic and Combinational Logic Circuits: Overview of Basic Gates and Universal Logic Gates, AND-OR –Invert Gates, Positive and Negative Logic,Boolean Laws and Theorems, Sum-of-products Method, Truth table to Karnaugh Map, Pairs, Quads, and Octets, Karnaugh Simplification, Don't Care Conditions, Product-of-Sum Method, Product-of-sum Simplification, Simplification by Quine-McClusky Method, Simplification by VEM Technique.

Self Study Component : Five variable Karnaugh map

11 Hours

Unit-2

Data Processing Circuits and Arithmetic Circuits: Multiplexers, Demultiplexers, Decoders, BCD-to-Decimal Decoders, Seven-segment Decoders, Encoders, Ex-OR gates, Parity Generators and Checkers, Magnitude Comparators, Design of code converters, Half Adder, Full Adder, Half Subtractor, Full Subtractor, Fast Adder, Adder- Subtractor , Arithmetic Logic Unit.

Self Study Component : Number system

10 Hours

Unit-3

Memory Devices: Read-only memory (ROM), PROM, EPROM, EEPROM, Programmable Array Logic (PAL), Programmable Logic Array (PLA).

Flip-Flops and Simple Flip-Flop Applications: RS Flip-Flops, Gated Flip-Flops, Edge – Triggered RS Flip-Flops**,** Edge – Triggered D Flip-Flops**,** Edge – Triggered JK Flip-Flops,JK Master-Slave Flip-Flops, Various representation of flip-flops, Conversion of flip-flops.

Self Study Component : Flip-Flop timing, Analysis of sequential circuits

10 Hours

Unit-4

Registers: Types of registers, Serial in Serial out, Serial in Parallel out, Parallel in Serial out, parallel in parallel out, Application of shift registers: Ring counter, Johnson counter, sequence detector and sequence generator.

Asynchronous and synchronous counter: Asynchronous counters, Decoding gates, synchronous counters, changing the counter modulus, decade counter, counter design as a synthesis problem.

Self Study Component : Universal Shift register, Digital clock

10 Hours

Unit-5

Design of Synchronous and Asynchronous Sequential Circuit : Model Selection, State Transition Diagram, State Synthesis Table, Design Equations and Circuit Diagram, Algorithmic State Machine, State Reduction Technique, Analysis of Asynchronous Sequential Circuit, Problems with Asynchronous Sequential Circuits, Design of Asynchronous Sequential Circuit

VHDL Programming: Introduction to VHDL, Describing data flow, Behavioral, Structural and Mixed design style, Simulation for Arithmetic, Combinational circuits and sequential circuits.
Self Study Component : Frequency Counter

11 Hours

Text Books:

1. Digital Principles and Applications: Donald P Leach, Albert Paul Malvino &Goutham Saha, TMH, 8th Edition, 2014.
2. A Verilog HDL Primer, 2nd Edition, J . Bhaskar, BS Publications

Reference Books:

1. Digital Principles & Design by Donald D Givone, 4th Reprint, Tata McGrawHill2009.
2. Fundamentals of Digital Logic with Verilog Design, Stephen Brown, ZVonkoVranesic, TMH, 2006

Course outcomes:

1. **Design** simplified logic circuits using Boolean equation minimization techniques.
2. **Design** the data processing circuits.
3. **Design** memory circuits.
4. **Design** shift registers and counters using flip-flops.
5. **Derive** state machine models for sequential circuits and write VHDL code for all logic circuits.

CO-PO Mapping

Semester: 3	**Course code : P18CS32**						**Title : Digital Logic Design**								
CO	Statement	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2
CO 302.1	**Apply** Boolean laws and Boolean equation minimization techniques to design logic circuits..	3	1	1										1	
CO 302.2	**Design** the data processing circuits.	3	3	2										1	
CO 302.3	**Apply** the logic to design memory circuits	3	2	3										1	
CO 302.4	**Design** shift registers and counters using flip-flops.	2	2	3										1	
CO 302.5	**Derive** state machine models for sequential circuits and write VHDL code for all logic circuits.	2	2	3		3								1	
C302		**2.6**	**2**	**2.4**		**3**								**1**	