UDYAM'24

ANNUAL TECHNICAL FEST OF ELECTRONICS ENGINEERING SOCIETY

DIGISIM PS - 2

TASK :

- **Objective:** Design a circuit using the Gift Wrapping Algorithm (Jarvis March Algorithm) to compute the convex hull of a given set of n points in x-y planes.
- **Compatibility:** Ensure the circuit is compatible even if there are any collinear points in the given set of points.
- **Constraints:** 3<=n<=10. For each i from 1 to n: 0<= xi, yi <=7. No constrain on using combinational or sequential approach for implementing any segment of circuit. (n is the no. of points, (xi,yi) are the coordinates of the 'i'th point)
- **Output Specification:** Show output as the sum of points on the convex hull using seven-segment displays. For instance, if the convex hull of points 1, 2, 3, 4, and 5 is 3, 4, 5, then the output should be the sum of these points, i.e., 12.

GIVEN :

You will be given a binary file with an array of values that are to be stored in a ROM. The first value of array will indicate the total number of points. Starting from second value, each set of three consecutive values represent the point number/name followed by its x and y coordinates.

example:
Say, the values in the bin file are in the below order

4,1,3,5,2,6,7,4,5,0,3,3,3

This implies that :
Total points = 4

- point no.1 is at (3,5)
- point no.2 is at (6,7)
- point no.4 is at (5,0)
- point no.3 is at (3,3)

Find the binary files in the below link :
click here

ELECTRONICS ENGINEERING SOCIETY

Components and Costs :

Note :

*You are allowed to use any components that **ONLY** come under the below mentioned categories , the cost of the components will be scaled up or down according to the number of bits with reference to the below mentioned base costs. For example , you're free to use any kind of multiplexer. If the base cost for n bit mux is 'x' , and if you're using 2n bit mux, then cost will be 2x.*

- Clock (Rs.40)
- ROM 2732 (Rs.75)
- Comparator (4 bit --> Rs.2)
  eg : 7485, 4585, etc
- Multiplexer (Quad 2:1 mux --> Rs.2)
  eg : 74157, 74153, etc
- Adder (4 bit --> Rs.2)
  eg : 74283, 7482, etc
- Encoder (8 : 3 --> Rs.2)
  eg : 74HC148, etc
- Decoder (4 : 16 --> Rs.2)
  eg : 74LS139 , 74HC154, etc
- Flip Flops (1 bit --> Rs.1)
  eg : 74273, 7474, 74LS175, 74LS109, etc
- Register (4 bit --> Rs.2)
  eg : 74179, 74194, etc
- Counter (4 bit --> Rs.2)
  eg : 74LS590, 74161, 74163, etc
- Logic Gates (1 or 2 i/p --> Rs 0.1 ; 3 i/p --> Rs 0.2 ; 4 i/p--> Rs 0.3..)
- Buffer (1 bit tristate buffer --> Rs 0.1)
  eg : 74HC241, 74125, etc
- 7-segment display (1-digit-->Rs.1)









Evaluation Criteria :

Evaluation would be based on following three categories, giving higher preference to top. Within a category, minimum cost will be the deciding factor.

1. Circuit passing all test cases.
2. Circuit passing all test cases of non collinear points
3. Circuit fails to pass some test cases in both categories (collinear and non collinear)

Note : To ensure that your circuit gives correct result irrespective of frequency of operation, use only stable clock source given in proteus. Use your previous knowledge on how to use ROM.