4位双向寄存器：

module REG\_74194 (CLR, S1, S0, CLK, SL, SR, A, B, C, D, QA, QB, QC, QD);

input CLR, S1, S0, CLK, SL, SR;

input A, B, C, D;

output QA, QB, QC, QD;

reg QA, QB, QC, QD;

always@(posedge CLK)

begin

if(!CLR)

begin

QA = 0;

QB = 0;

QC = 0;

QD = 0;

end

else

begin

case({S1,S0})

2'b00:begin QA = QA;QB = QB;QC = QC;QD = QD; end

2'b11:begin QA = A;QB = B;QC = C;QD = D; end

2'b01:

begin

case(SR)

1'b1:begin QD = QC; QC = QB; QB = QA; QA = 1; end

1'b0:begin QD = QC; QC = QB; QB = QA; QA = 0; end

endcase

end

2'b10:

begin

case(SL)

1'b1:begin QA = QB;QB = QC;QC = QD;QD = 1; end

1'b0:begin QA = QB;QB = QC;QC = QD;QD = 0; end

endcase

end

endcase

end

end

Endmodule

顶层文件：

module SR194\_2(A1,B1,C1,D1,A2,B2,C2,D2,QA1,QB1,QC1,QD1,QA2,QB2,QC2,QD2,

S0,S1,CLK,SL,SR,CLR);

input A1,B1,C1,D1,A2,B2,C2,D2;

input S0,S1,CLK,CLR,SL,SR;

output QA1,QB1,QC1,QD1,QA2,QB2,QC2,QD2;

REG\_74194 yiwei1(.A(A1),.B(B1),.C(C1),.D(D1),.S0(S0),.S1(S1),.CLK(CLK),.CLR(CLR),.SL(QA2),.SR(SR),

.QA(QA1),.QB(QB1),.QC(QC1),.QD(QD1));

REG\_74194 yiwei2(.A(A2),.B(B2),.C(C2),.D(D2),.S0(S0),.S1(S1),.CLK(CLK),.CLR(CLR),.SL(SL),.SR(QD1),

.QA(QA2),.QB(QB2),.QC(QC2),.QD(QD2));

Endmodule

测试文件：

`timescale 1ns/1ps

module tb;

reg CLR, S1, S0, CLK, SL, SR;

reg A1,B1,C1,D1,A2,B2,C2,D2;

wire QA1,QB1,QC1,QD1,QA2,QB2,QC2,QD2;

always # 1 CLK = ~CLK;

initial

begin

CLK = 0;

CLR = 0;//clear

A1 = 1;B1 = 0;C1 = 1;D1 = 0;

A2 = 1;B2 = 0;C2 = 1;D2 = 0;

S1 = 0;S0 = 0;

#2 //zhi song

CLR = 1;

A1 = 1;B1 = 0;C1 = 1;D1 = 0;

A2 = 1;B2 = 0;C2 = 1;D2 = 0;

S1 = 1;S0 = 1;

#2 //you yi 0

//CLR = 1;

A1 = 1;B1 = 0;C1 = 1;D1 = 0;

A2 = 1;B2 = 0;C2 = 1;D2 = 0;

S1 = 0;S0 = 1;

SR = 0;

#2 //you yi 1

//CLR = 1;

A1 = 1;B1 = 0;C1 = 1;D1 = 0;

A2 = 1;B2 = 0;C2 = 1;D2 = 0;

S1 = 0;S0 = 1;

SR = 1;

#2 //zuo yi 0

//CLR = 1;

A1 = 1;B1 = 0;C1 = 1;D1 = 0;

A2 = 1;B2 = 0;C2 = 1;D2 = 0;

S1 = 1;S0 = 0;

SL = 0;

#2 //zuo yi 1

//CLR = 1;

A1 = 1;B1 = 0;C1 = 1;D1 = 0;

A2 = 1;B2 = 0;C2 = 1;D2 = 0;

S1 = 1;S0 = 0;

SL = 1;

end

SR194\_2 uut(.A1(A1),.B1(B1),.C1(C1),.D1(D1),.A2(A2),.B2(B2),.C2(C2),.D2(D2),

.SR(SR),.SL(SL),.CLK(CLK),.CLR(CLR),

.QA1(QA1),.QB1(QB1),.QC1(QC1),.QD1(QD1),.QA2(QA2),.QB2(QB2),.QC2(QC2),.QD2(QD2),

.S0(S0),.S1(S1));

endmodule