`timescale 1ns / 1ps

module adder4(

input[3:0] ina,

input[3:0] inb,

output count,

output[3:0] sum

);

assign {count,sum}=ina+inb;

endmodule

`timescale 1ns / 1ps

module test();

reg[3:0] ina;

reg[3:0]inb;

wire cout;

wire [3:0]sum;

adder4 u1(ina,inb,cout,sum);

endmodule

