Ryan Kwong

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Education

University of California, Berkeley – BS in Electrical Engineering and Computer Science Expected Dec 2026
Relevant Coursework: Introduction to Digital Design and Integrated Circuits, Microelectronic Devices
Diablo Valley College – AS in Computer Science May 2024

Skills

Design Tools: Cadence Genus, Cadence Innovus, Synopsys Design Compiler, Vivado, TCL, VCS, KiCAD, LTSpice
Protocols: I2C, SPI, CAN, UART, USB
Languages: Verilog, SystemVerilog, C, C++, Python, Go, Javascript

Experience

Systems Engineering Intern, Mizuho OSI – Union City, CA June 2025 – Present

- Characterized magnetic positioning sensor performance and enhanced company-wide standard operating procedures for sensor calibration during testing protocols, improving measurement accuracy and consistency verified against a hand-calculated magnetic field model
- Designed and prototyped a surgical table manipulator arm accessory for use in cadaver laboratory validation testing, demonstrating clinical viability for future accessory releases
- Executed comprehensive verification and validation testing protocols for surgical table systems, ensuring compliance with FDA regulations and contributing to product quality assurance processes

Projects

Custom RISC-V Verilog CPU

- Designed and implemented a 3-stage pipelined RISC-V RV32I processor in Verilog with full ISA and F extension support, achieving functional RTL and gate-level verification via the official RISC-V ISA compliance tests as well as unit-level testbenches using VCS and Python
- Developed direct-mapped write-back cache subsystem featuring 64-line capacity with 512-bit cache lines, implementing 4-state FSM for hit/miss handling, refill operations, and writeback logic using dual-ported SRAM arrays
- Implemented a pipelined IEEE 754-2008 compliant floating-point unit with full support for the RISC-V F extension, including special case handling for zero, infinity, NaN and invalid operations
- Synthesized design using Synopsys Design Compiler and Cadence Genus targeting the SKY130 PDK, performed place-and-route with Cadence Innovus to generate complete ASIC floorplan with optimized power distribution network and clock tree
- Integrated processor with BIOS, UART, and memory-mapped I/O peripherals for FPGA prototyping (Xilinx FPGA xc7z020clg400-1), enabling any C program compiled with the RISC-V GCC Toolchain to run and display on a serial monitor

Calsol E-Load Project Lead

- Developed 6kW electronic load system handling 60A current from 120V battery sources by implementing an ESP32 and MOSFET-based topology for vehicle battery performance analysis
- Enabled cross-team data integration between the battery and logistics teams by developing CAN bus interface for real-time battery telemetry and USB protocol bridge connecting hardware systems to a logistics software stack to simulate real-time vehicle performance
- Designed a 4-layer PCB that utilized thermal vias, copper planes, heat sinks and fans to prevent the system from overheating during high loads
- Led a team of 3 other members to develop a fully functional PCB within 6 months through the use of LTSpice simulations, rapid protoboarding, PCB design via KiCAD, and thermal/load testing