TÉCNICO LISBOA

Mircroeletronics

2nd LAB Report

Design of a nand2 Standard Cell

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Conteúdo

1 Introduction

In the second lab of Microelectronics there are two main goals:

- By following the tutorials "Full-Custom Design with Cadence Tutorial"and "Simulação típica e em corners"get familiar with other tools of cadence and learn to do a layout and all its characteristics, like corner simulation, by designing a CMOS Inverter.
- To solidify the knowlege obtain, it's studied a CMOS NAND2, i.e. a 2-input CMOS NAND. Subsequently, it's introduced theoretically and implemented for simulation, similarly to the CMOS Inverter.

This report is divided in three main sections:

First, it's written an CMOS Inverter and CMOS NAND theory review, necessary for this report. In this section, it's discussed the model, the design and the outputs, regarding different inputs of both gates. Second, through *Cadence virtuoso* it's performed various simulations and analysis, for the the CMOS Inverter (by way of the tutorials provided) and, similarly, for the CMOS NAND. By delineating the schematic and the symbol of both gates, it's created a testbench to simulate the circuit and to test the worst-case scenarios (corner analysis) aswell. Subsequently, it's designed the layout of both gates and both are verified with DRC and LVS, assuring that the layout and the schematic match with no particular errors. Finally, a comparison between the theory and the simulation results is commented in the conclusion.

2 Theoretical Analysis

2.1 CMOS Inverter

The CMOS Inverter performs the logical inversion operation of the input signal, i.e. is a NOT-gate.

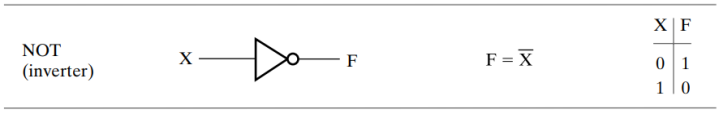


Figura 1: Symbol, function and outputs of NOT-gate [3]

It is designed with a PMOS transistor, an NMOS transistor and supply rails (see figure 1). When the input voltage is V_- (the value of the negative supply rail), the output V_o goes to V_+ (the positive supply voltage): the NMOS device shuts off and the PMOS device is on. When the input voltage goes to V_+, the output goes to V_-, turning off the PMOS and turning on the NMOS.(Moris Mando, Kime, 2014)
`(Note: comparison between figures -> X=X and F=Y)`

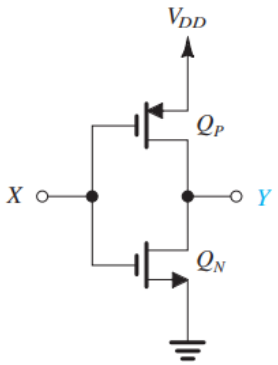


Figura 2: CMOS Inverter, i.e. NOT-gate, transistor design [2]

2.2 CMOS NAND

The NAND gate is regarded as the universal gate since it can be used to obtain all of the basic gates, such as AND, OR, NOT, and NOR. The NAND gate represents the complement of the AND operation, thus only yields a low output, when there are only high inputs.

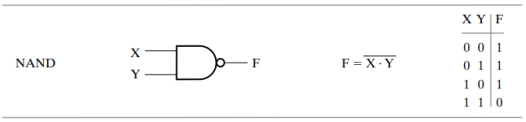


Figura 3: Symbol, function and outputs of NAND-gate [3]

The design a NAND2-gate (i.e.2-Input NAND-gate) with CMOS technology consists of two networks: the pull-down network (PDN) constructed of NMOS transistors, and the pull-up network (PUN) constructed of PMOS transistors.
`(Note: comparison between figures -> X=A, B=Y and F=Y)`

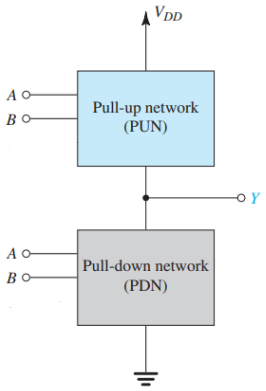


Figura 4: The PUN comprises PMOS transistors, and the PDN comprises NMOS transistors [2]

The two networks are operated by the input variables, in a complementary fashion.

- To synthesize the PDN, it's considered the input combinations that require Y to be low. There is only one such combination, namely, A and B both high. Thus, the PDN simply comprises two NMOS transistors in series.
- To synthesize the PUN, we consider the input combinations that result in Y being high. These are found as A low or B low. Thus, the PUN consists of two parallel PMOS.

(Sedra, Smith, 2015)

Putting the PDN and PUN together results in the CMOS NAND gate implementation is shown below:

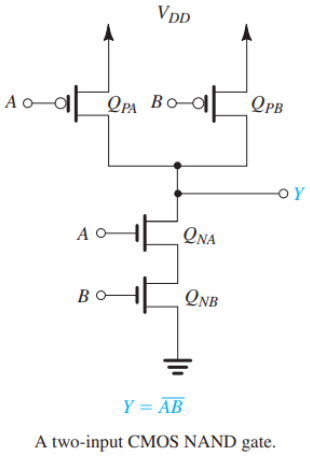


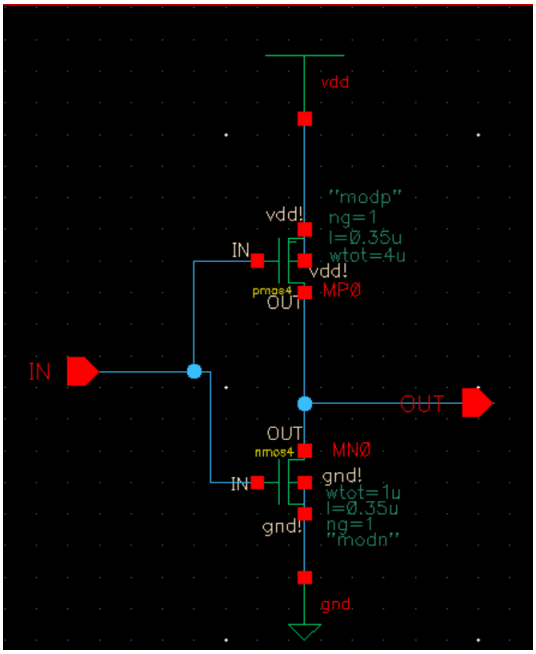
Figura 5: CMOS NAND-gate transistor design [2]

3 Candence Virtuoso Analysis

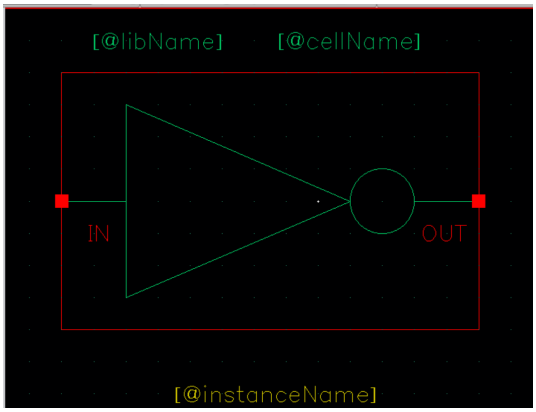
3.1 Inverter

3.1.1 Schematic, Symbol and Simulation

The first step was to follow the tutorial provided, thus the schematic and symbol of an inverter were created. In the design of the schematics, the library *PRIMLIB* was used to obtain the MOSFETs (nmos4 and pmos4) altering their width to 4 μm for the PMOS and 1 μm for the NMOS.
In NMOS, the body and the source were connected and in PMOS the body and the drain were connected. The ground supply cell (*gnd*) and the voltage supply (*vdd*) were provided by the library *analogLib* and an input pin and an output pin were also created. Likewise, the symbol was designed.



(a) Schematic



(b) Symbol

Figura 6: Inverter schematic and symbol in *Candence virtuoso*

The second step was to creat a new library for the simulation and for the testbench.

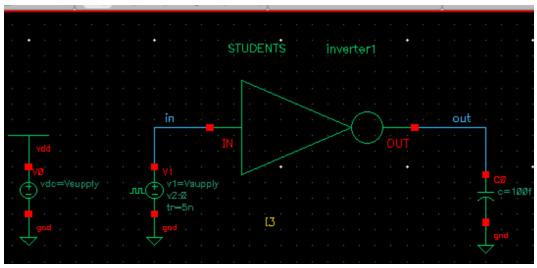
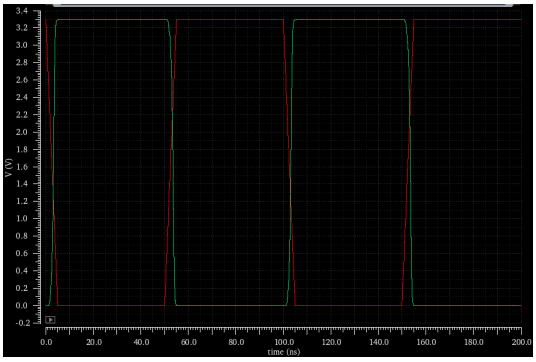
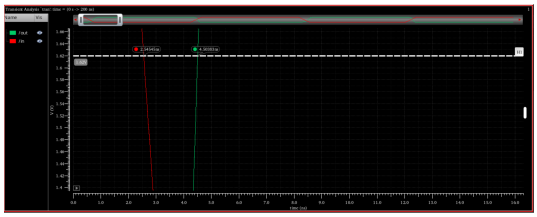


Figura 7: CMOS Inverter testbench

In this testbench, the entrance of the inverter was connected to a voltage source that forms a rectangular symbol with Voltage 1=*vdd_val* V, Voltage 2=0.0V, Delay time=0s, Rise time= 5ns, Fall time= 5ns, Pulse width= 45ns and Period= 100ns. This voltage supply was provided by the library "analogLib", having cell name "vpulse"and connected to gnd. The output of the inverter was connected to a capacitor with C= 100fF from library "analogLib"and this capacitor is connected to gnd. A DC voltage source with voltage equal to *vdd_val* V was created between vdd and gnd, this DC voltage has cell name "vdc"and was originated from library "analogLib". Finally, the waveform of the input and output of the inverter was simulated using *ADE GXL*, setting *vdd_val* =3.3V, obtaining the plot shown below.



(a) Plot of the input(green) and output(red) of the inverter

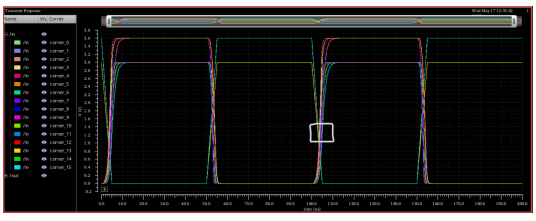


(b) Delay between input and output

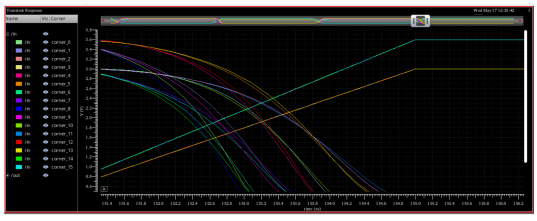
Figura 8: Inverter simulation graphs

The results of the simulation are accordingly, being the output voltage an inversion of the input, with delay between logic level transitions. In response to a change on the input voltage, the MOSFETs in the circuit go through a transition phase. During this phase, the output voltage does not change instantaneously, but gradually reaches the desired logic level. So, an inverter has a delay because it takes a finite amount of time for the output voltage to transition from one logic level to another. This delay is primarily caused by the charging and discharging of the in herent capacitance's of the MOSFETs.

A corner simulation was also created, for temperature of -40ºC and 125ºC and *vdd_val* of 3.3V and 3.6V.



(a) without Zoom



(b) with Zoom

Figura 9: Inverter corner simulation in *Candence virtuoso*; In subfigure (b), the area inside the gray square, drawn in subfigure (a), is amplified

`(Note1: the 'Nominal' corner isn't represented in this figure)`

Analyzing this corner case involves evaluating the impact of these extreme operating conditions on the inverter's performance. In this case, we are assessing the delay of the inverter under both temperature and supply voltage corner cases. Temperature extremes can affect the mobility of the transistors, leading to changes in their switching speed. Lower temperatures tend to slow down transistor operation, while higher temperatures tend to speed it up. For the supply voltage, higher values generally result in faster switching and reduced delay, while lower values tend to slow down the switching speed and have higher delay values. This performance description can be observed in Figure 9 graphs.

3.1.2 Layout

The layout of the inverter is given as shown in the tutorial.

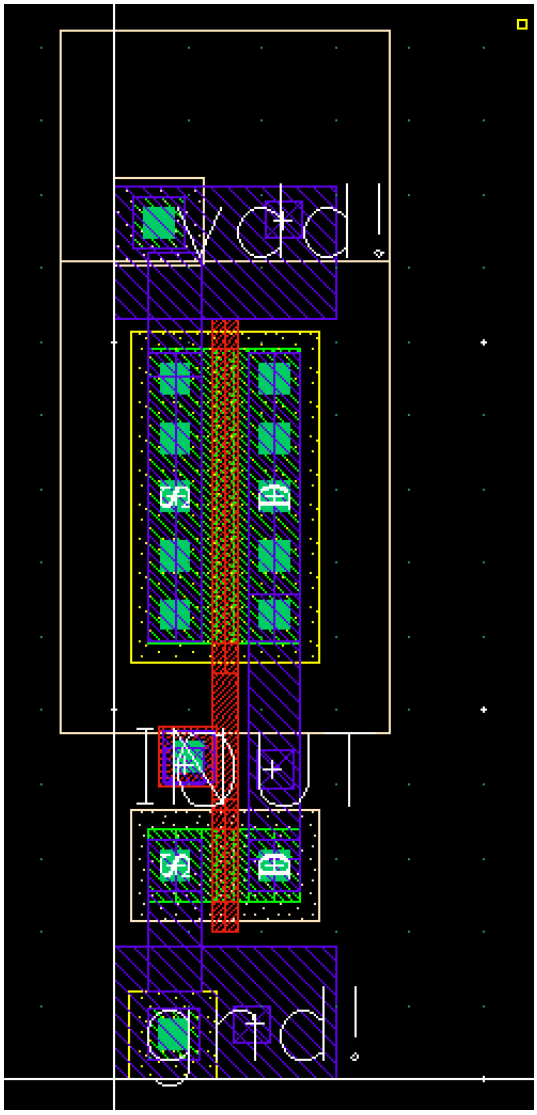


Figura 10: Layout in *Cadence virtuoso*

Afterwards, it's performed a verification with *assura*'s DRC and LVS.

- DRC:

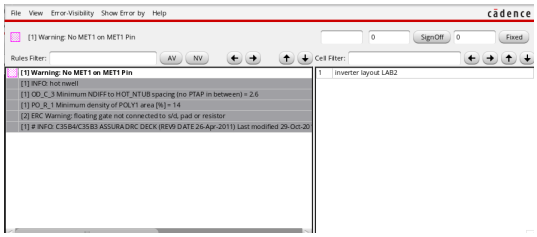


Figura 11: DRC *assura* in *Cadence virtuoso*

- LVS:

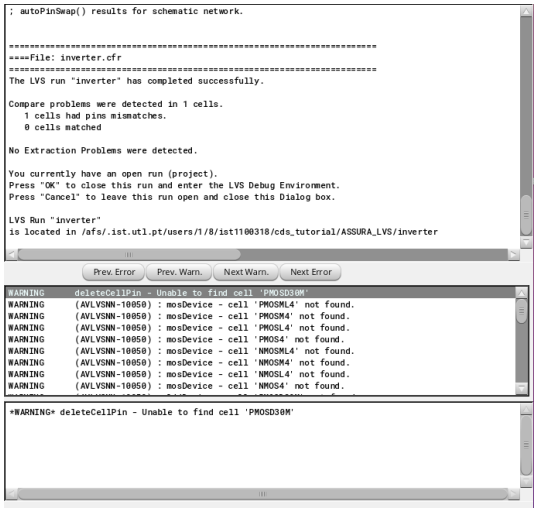


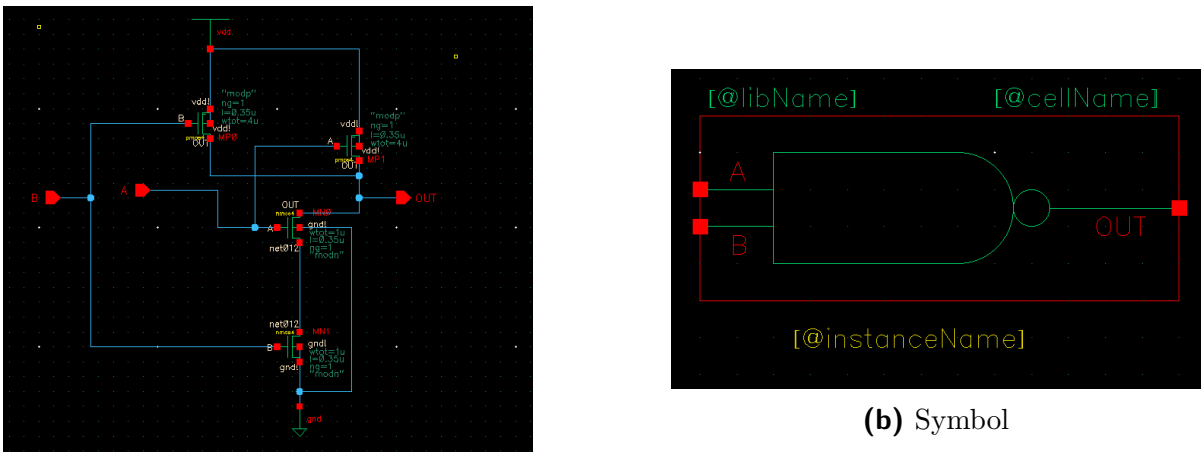
Figura 12: LVS *assura* in *Cadence virtuoso*

Through the figures, it's shown that some warnings appear. The group noticed, specially in DRC, that the resultant warnings were exactly the same for different layouts done by the different members of the group.

3.2 NAND-gate

3.2.1 Testbenach and Simulation

In order to create a NAND gate, the schematic and symbol of this structure was created. The schematic is composed of two NMOS ("nmos4"from library "PRIMLIB") and two PMOS ("pmos4"from library "PRIMLIB"). The connections between this transistors and the inputs, outputs, "gnd"and "vdd"were performed has shown in figure... Then, the symbol was generated has shown in figure 13.



(a) Schematic

(b) Symbol

Figura 13: NAND gate schematic and symbol in *Candence virtuoso*

Next the simulation testbench was created has shown in figure 22. The testbench was similar to the created for the inverter, with the exception that two voltage supplies that create rectangular signals were used with two different periods (100ns for A input and 150ns for B input), so that it is easier to distinguish the different signals. Finally, corner simulation was performed for temperature equal t0 -40ºC and 125ºC and *vdd_val*=3.3V.

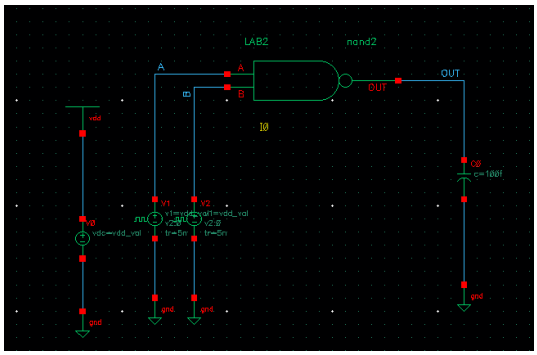


Figura 14: CMOS NAND gate testbench

3.2.2 Layout

The layout of the nand2 is given as shown below:

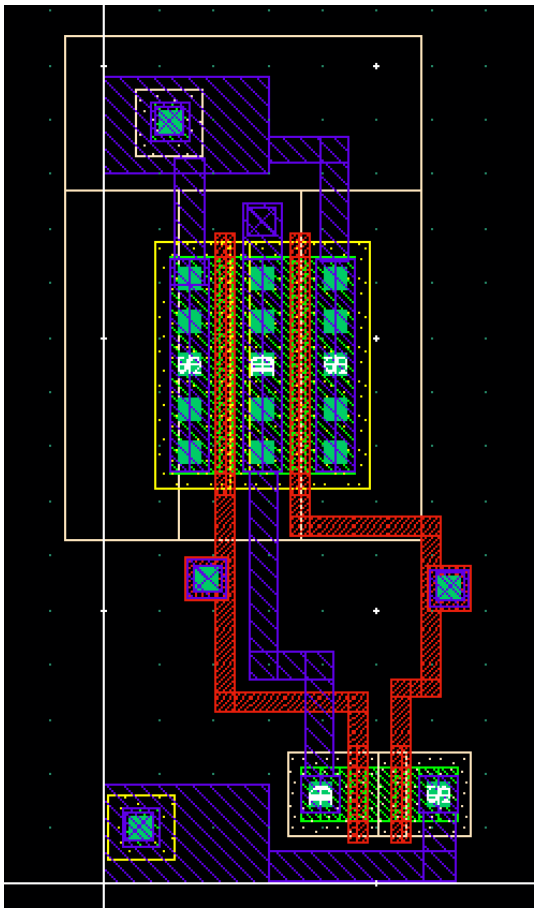


Figura 15: Layout

Afterwards, it's performed a verification with *assura*'s DRC and LVS.

- DRC:

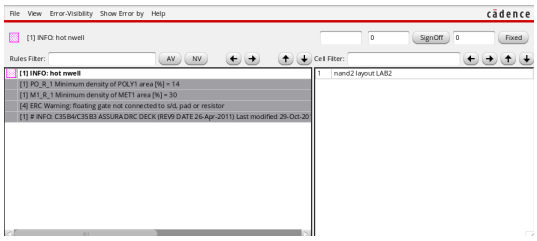


Figura 16: DRC *assura* in *Cadence virtuoso*

- LVS:

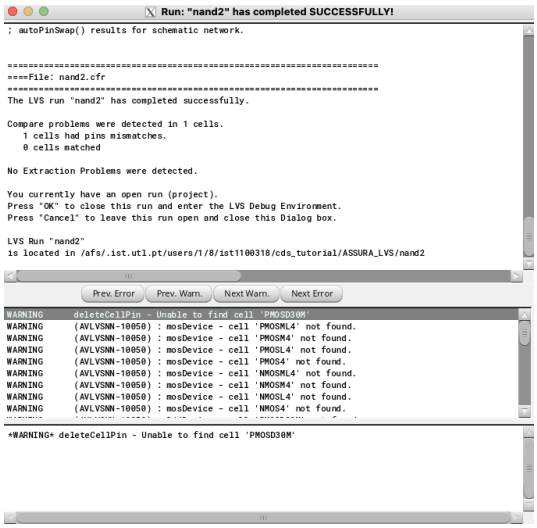


Figura 17: LVS *assura* in *Cadence virtuoso*

Similarly to the *assura*'s DRC and LVS verifications in the inverter, in the NAND-gate there are some warnings too.

3.3 Corner Analysis

In order to analyze the different limiting cases, it's performed a corner analysis with the *virtuoso cadence* software, gaining a general understanding of the time intervals during which the device can function as intended. In this instance, the corners analysed are WS, WP, WO and WZ, which are explained below.

- **WS** – Worst Speed:
  In this situation, both NMOS and PMOS mobility will diminish, decreasing the current values. As a result, the output signal's slope is reduced while its transition time between states gets increased. The two transistors' threshold voltage increases, indicating that both pull-up and pull-down circumstances happen later. Thus, the transistors' response to input impulses is slower, i.e. takes longer. Hence, worst speed.

- **WP** – Worst Power:
  In this case, both NMOS and PMOS mobility rises while the threshold voltage falls, which is the opposite of the **WS** scenario. Thus, it may be said that the output signal's slope increases along with the increase of the transistors' current, resulting in a quicker change between logical states. Both transistors' threshold voltages drop over time, meaning that both pull-up and pull-down scenarios happen earlier. As a result, transistors react to incoming impulses more quickly. Hence, worst power.

- **WO** – Worst One:
  This situation aims to study the worst-case scenario of PMOS transistors, responsible for the transition from 0 to 1. To achieve it, the PMOS' mobility decreases while its

threshold voltage increases. However, the mobility and threshold voltage in the NMOS transistor must evolve in the opposite way, enabling a great asymmetry between pull-down (transition from 1 to 0) and pull-up (transition from 0 to 1). Therefore, when the NMOS mobility increases, the PMOS mobility decreases, and when the NMOS threshold voltage decreases, the PMOS mobility increases. As a result, it takes longer for the transistors to respond to an input signal that causes the output level to transition from 0 to 1. Hence, worst one.

- **WZ** – Worst Zero:
  This situation aims to study the worst-case scenario of NMOS transistors. responsible for the transition from 1 to 0. To accomplish it, the NMOS' mobility rises while its threshold voltage falls, which is the opposite of the WO situation. As a consequence, the mobility voltage in the PMOS transistor must behave in the opposite way, enabling a great asymmetry between pull-down and pull-up. Therefore, when the PMOS mobility increases, the NMOS mobility decreases, and when the PMOS threshold voltage decreases, the NMOS mobility increases. As a result, transistors take longer to respond to input signals that cause the output level transition from 1 to 0. Hence, worst zero.

All the cases, described above, are summarized in the table below:

	NMOS	PMOS
WS	$\mu\downarrow V_t\uparrow$	$\mu\downarrow V_t\uparrow$
WP	$\mu\uparrow V_t\downarrow$	$\mu\uparrow V_t\downarrow$
WO	$\mu\uparrow V_t\downarrow$	$\mu\downarrow V_t\uparrow$
WZ	$\mu\downarrow V_t\uparrow$	$\mu\uparrow V_t\downarrow$

Because the mobility (μ) and the threshold voltage (V_t) vary with temperature, to perform the simulation, it's considered two different temperatures: -40ºC and 125ºC.

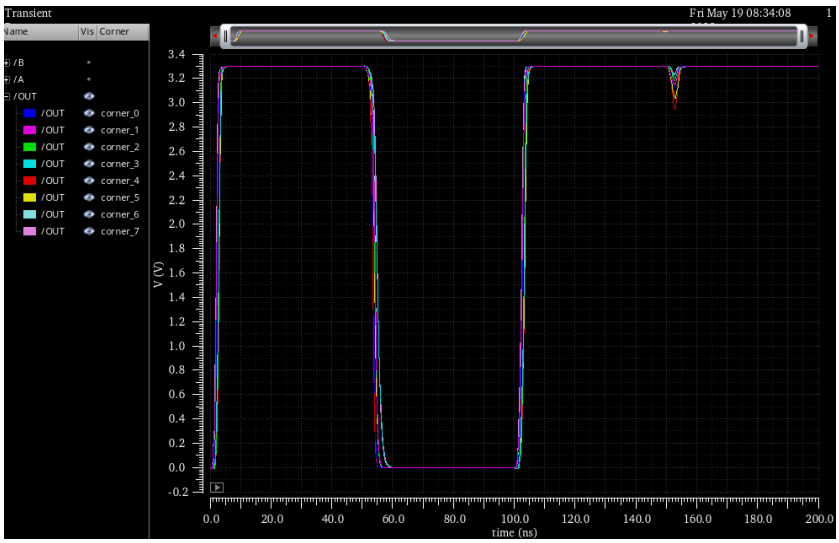


Figura 18: NAND output gate corner analysis.

The corners with an even number signify a temperature of -40°C, while those with an odd number reflect a temperature of 125°C. Furthermore, the pairs (0, 1), (2, 3), (4, 5) and (6, 7) correspondingly, characterize the wp, ws, wo, and wz of a corner.

Finally, the pull-down and the pull-up analysis are discussed.

- Temperature of -40ºC:

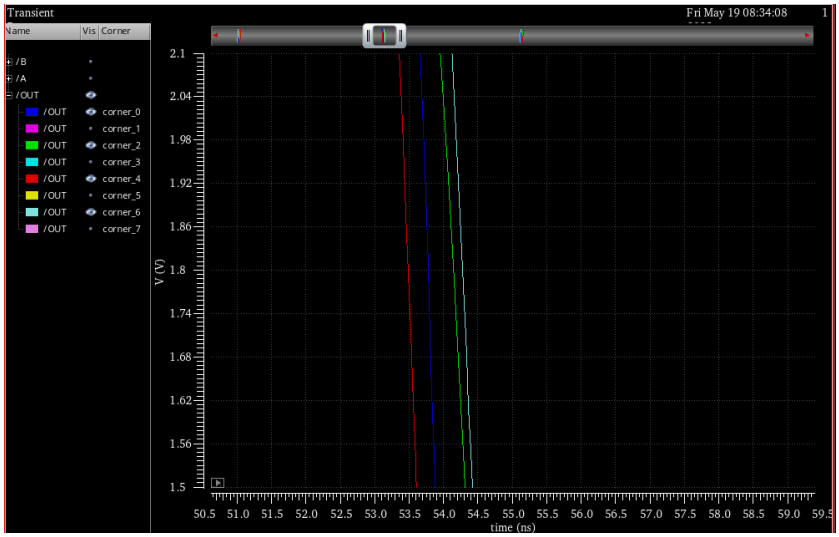


Figura 19: Zoomed pull-downs

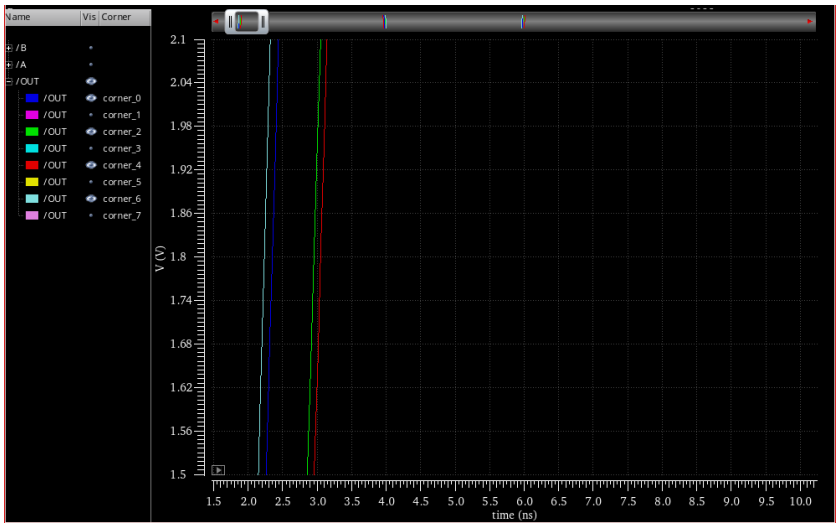


Figura 20: Zoomed pull-ups

- Temperature of 125ºC:

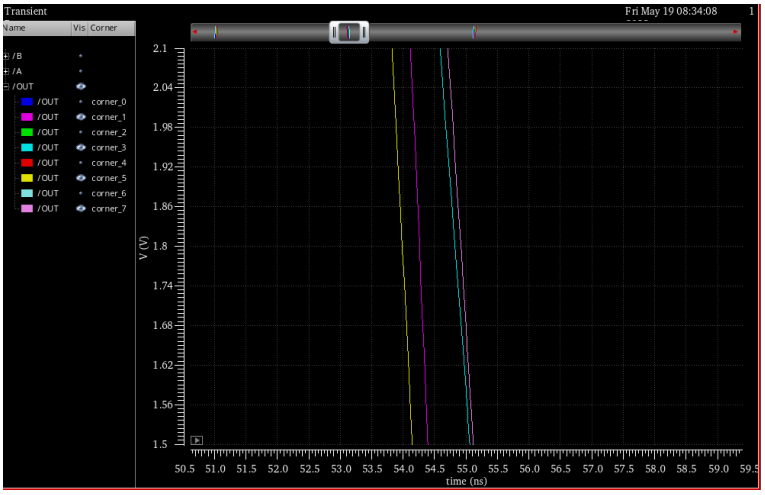


Figura 21: Zoomed pull-downs

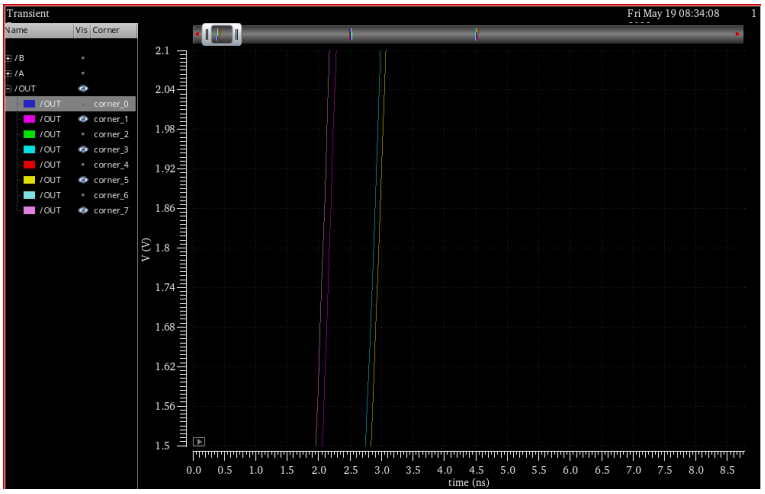


Figura 22: Zoomed pull-ups

The pull-up situations (Figures 20 and 22), the voltage 1.65V ($V_{dd}/2$) is more rapidly attained by the worst zero (WO) and worst power (WP) cases. The worst speed (WS) and worst one (WO) cases attain this value afterwards.

For the pull-down situations (Figures 19 and 21), the voltage 1.65V is attained in the following order: W0, WP first and WS, WZ after. So, the opposite of the pull-up situation.

For a 125ºC temperature, the threshold voltage will be lower than for -40ºC. Therefore, is possible to conclued that:

In one hand, for the pull-up situation, for each corner, the NAND output gate voltage will rise more quickly to the 1.65V when the temperature is 125ºC.

In another hand, for the pull-down situation, is the opposite way around, the -40ºC is the temperature for which the 1.65V are more quickly attained.

4 Conclusion

Throughout this lab report, it's intended use other tools of *Cadence virtuoso* and learn to do a layout and all its characteristics, speacially corner simulation, by designing a CMOS Inverter. Afterwards, as a way to practice and more understanding, it's analised a CMOS NAND2, i.e. a 2-input CMOS NAND.

On the first part, through the books "Microelectronic Circuits"[2] and "Logic and Computer Design Fundamentals"[3], was written a CMOS Inverter and CMOS NAND theory review, necessary for this report. In this section, it's discussed the symbol, the function, the CMOS-transistor model and the outputs, regarding different inputs, for both gates, shown through tables.

On the second part, through *Cadence virtuoso*, it's performed various simulations and analysis, for the the CMOS Inverter (by way of the tutorials provided) and, likewise,for the CMOS NAND.

On one hand, the delineation for the schematic and for the symbol of both gates, by creating a testbench to simulate the circuit and to test the worst-case scenarios (corner analysis), was achieved successfully. Particularly, in the corner analysis it was tested two different temperatures (-40^{o}C and 125^{o}C) and depicted how both influenced the mobility and the threshold voltage, as well as, how they influence the pull-down and pull-up situations. It was concluded that for the pull-up situation, for each corner, the NAND output gate voltage will rise more quickly to the 1.65V when the temperature is 125^{o}C; for the pull-down situation, is the opposite way around, the -40^{o}C is the temperature for which the 1.65V are more quickly attained.
Subsequently, the layout of both gates were designed. To design the inverter, it was followed the tutorial, as explained. To design the nand2, by following the equivalent steps to the tutorial's, specially, using the same rullers, it's possible to understand that both gates could be laid out next to each other, which is a positive situation. (shown in the section 'Appendix':23) This way both gates could be linked to each other by a connection of MET1 (metal 1) as sketched with purple squares. Hence, it could be created a common vdd and a common gnd.

On another hand, however, throughout the layout sections, it was depicted that there were some warnings, after the *assura*'s verification in DRC and LVS, as the schematic and the layout didn't seem to completely match. The group followed the tutorial separately, yet got the same warnings in some cases. Therefore, the layout analysis wasn't fully attained.

In general, throughout this lab report, the group had some difficulties to reach the setted goals, and will try to improve, in order to fullfil a better understanding of designing the layouts of different circuits.

5 Referências

[1] R. J. Baker, "CMOS: Circuit Design, Layout, and Simulation", 3rd edition, p.7, 2010.
[2] Adel S. Sedra, Kenneth C. Smith, "Microelectronic Circuits", 7th edition, p.1092, p.1096, 2015.
[3] M. Morris Mano, C. Kime, "Logic and Computer Design Fundamentals", 4th edition, p.85, 2014.

6 Appendix

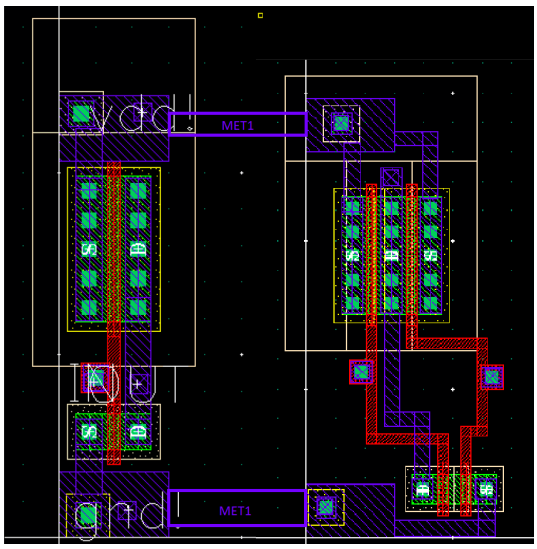


Figura 23: vdd and gnd linked