Microeletronics

1^{st} Lab Report

$ID(VGS)$ and $ID(VDS)$ simulation with virtuoso

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Contents

1 Introduction

In the first lab of Microelectronics there are two main goals:

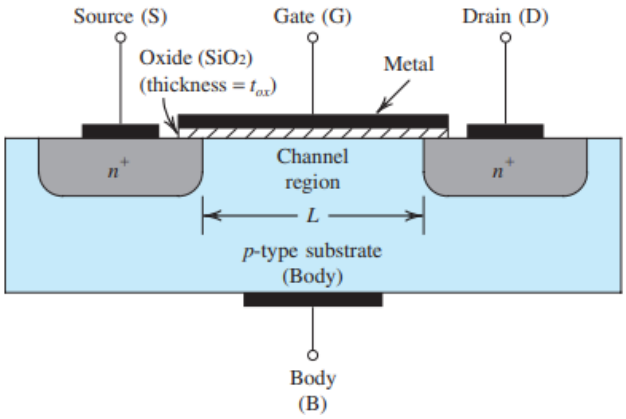
- By following the tutorials available in the course page, get familiar with the software *Candence Virtuoso* and its tools.
- Analyze the behavior of the drain's current in relation to the change in terminal voltages and identify, from the graphics obtained, the operating stages of the transistor, both for NMOS and PMOS.

This report is divided in three main sections.
First, it's written a MOSFET theory review, necessary for this report. In this section, the structure, the model, the working regions of the two types of MOSFET (NMOS and PMOS) are discussed and, to complete the analysis, a comparison between NMOS and PMOS is explored likewise. Second, the I-V characteristics of the NMOS and the PMOS are simulated. In this section, it's described the method to create the schematics and symbols used to generate the graphs of the simulation. Furthermore, through the graphs obtained, it's possible to point out the three different working regions of both transistor models (Cut-Off, Triode and Saturation) and, also, to verify that the construction of a PMOS transistor is the opposite of an NMOS transistor, given that the I-V characteristics are opposite as well. Finally, a comparison between the theory and the simulation results it's commented in the conclusion.

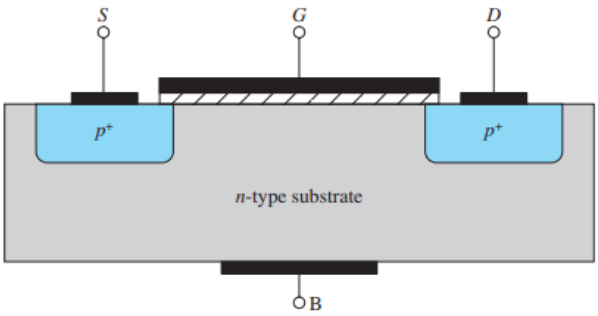
2 Theoretical Analysis

2.1 MOSFET Structure

MOSFET stands for Metal-Oxide-Semiconductor Field-Effect Transistor and are widely used in analog and digital circuits. MOSFET are a four-terminal device, having a source(S), a gate (G), a drain (D) and a body (B) terminals.



(a) NMOS cross section



(b) PMOS cross section

Figure 1: MOSFET physical structures

There are two types of MOSFETs: NMOS and PMOS. The NMOS is fabricated on a p-type substrate (also called the "bulk" or the "body") and has two heavily-doped n regions form the source and drain terminals, a heavily-doped conductive piece of polysilicon1 ("poly1") operates as the gate, and a thin layer of silicon dioxide (SiO2, simply called "oxide") insulates the gate from the substrate. The useful action of the device occurs in the substrate region, under the gate oxide. In practice, NMOS and PMOS devices must be fabricated on the same wafer and substrate, so usually one of the device's types is placed in a "local substrate", called "well". (Behzad Razavi, 2001) The PMOS device is fabricated in a n-well, and this substrate must be connected to a potential such that the source to drain junction remains reverse-biased, so, in most circuits, the n-well is tied to the most positive supply voltage. Some modern CMOS processes offer a "deep n-well," a well substrate that contains an NMOS device and its p-type body.

2.2 MOS Model

In MOSFETs, the generation and transport of charges as a function of the terminal voltages were analysed. One important concept is the threshold voltage (V_t), which is the value of the gate voltage for which the transistor is "turned on": an "inversion layer" of charge carriers is formed under the gate oxide, between the source and the drain, after the formation of a depletion region, forming a "channel". The graphics below illustrates the three major different operating regions of MOSFET:

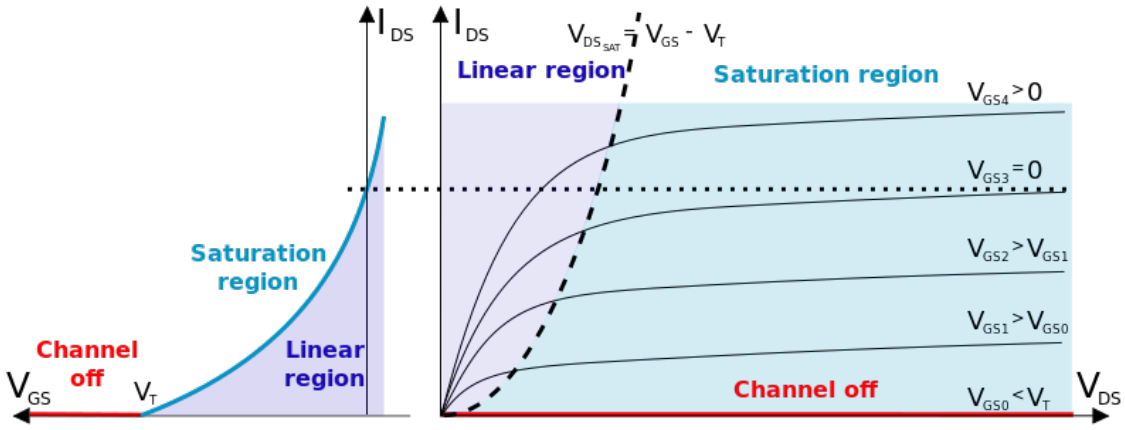


Figure 2: Drain current depending on gate to source voltage, V_{gs} (left) and drain to source voltage, V_{ds} (right).

Operation Mode	Type	Condition	Equation
Cut-Off	NMOS	$V_{GS} < V_{TH}$	$I_D = 0$
	PMOS	$\|V_{GS}\| < \|V_{TH}\|$	$I_D = 0$
Linear	NMOS	$V_{GS} \geq V_{TH}$ $V_{DS} \leq V_{GS} - V_{TH}$	$I_D = K_n(2(V_{GS} - V_{TH}) V_{DS} - V_{DS}^2)$
	PMOS	$\|V_{GS}\| \geq \|V_{TH}\|$ $\|V_{DS}\| \leq \|V_{GS}\| - \|V_{TH}\|$	$I_D = K_p(2(V_{GS} - V_{TH}) V_{DS} - V_{DS}^2)$
Saturation	NMOS	$V_{GS} \geq V_{TH}$ $V_{DS} \geq V_{GS} - V_{TH}$	$I_D = K_n(V_{GS} - V_{TH})^2(1 - \lambda V_{DS})$
	PMOS	$\|V_{GS}\| \geq \|V_{TH}\|$ $\|V_{DS}\| \geq \|V_{GS}\| - \|V_{TH}\|$	$I_D = K_p(V_{GS} - V_{TH})^2(1 - \lambda V_{DS})$

Figure 3: Equations for each operating regions, for NMOS and PMOS.

Channel OFF This region is operating when the potential at the oxide-silicon interface and the width of the depletion region are still rising, so the "channel" is not formed yet and the transistor is "turned off". The V_{gs} is lower than the V_t, so the drain current is close to zero.

Triode (also called Ohmic or Linear Region) This region occurs after the transistor is turned on, so with V_{gs} higher than V_t and when the V_{ds} is lower than $V_{gs} - V_t$. The drain current raises proportionally to the V_{ds} and the peak of the parabola occurs at $V_{ds} = V_{gs} - V_t$. It is also possible to observe that the "current capability" of the device increases with V_{gs}, in other words, an higher V_{gs} maintains the transistor longer in the triode region, for the same V_{ds} values.

Saturation This region occurs when the V_{ds} is higher than the $V_{gs} - V_t$. This region occurs when the V_{ds} is higher than the V_{gs}-V_t. The drain current (I_d) becomes relatively constant and the device functions as a "voltage controlled current source": higher V_{gs} result in higher I_d. The channel is "pinched off": the inversion layer stops at the length lower or equal to L (the length of the gate).

2.3 PMOS vs NMOS

It is important to refer that the "turn-on" phenomenon and the operating regions in a PMOS device are similar to the NMOS, but with all the polarities reversed. So, the gate to source voltage becomes sufficiently negative and an inversion layer, consisting in this case of holes, is formed at the oxide-silicon interface, providing the conduction path between the source and the drain to form the "channel". That is, the threshold voltage of a PMOS device is typically negative. Also, the hole's mobility of the PMOS device is lower than the electron's mobility on the NMOS device, so the current increase with higher $|V_{gs}|$ is also lower. Thus, NMOS transistors are faster than PMOS transistors because electrons are more mobile than holes in semiconductors. However, NMOS consume more power than PMOS because they require a constant flow of current to maintain their states.

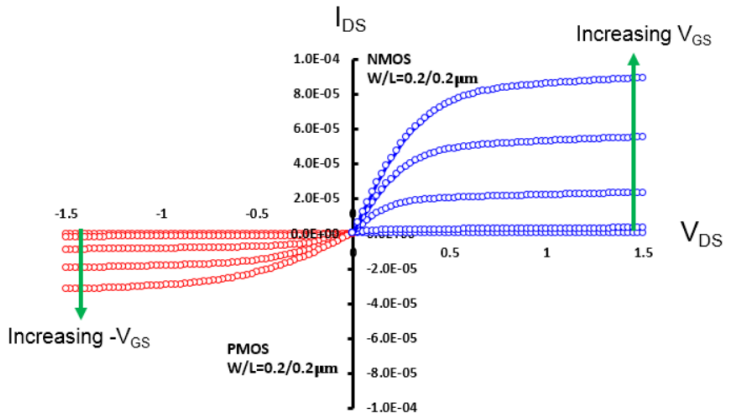


Figure 4: Operating regions for PMOS (left) and NMOS (right).

3 Simulation Analysis

In order to analyse the operation modes of NMOS and PMOS, a schematic and its symbol were created on Cadence on the library "1LAB" for NMOS and on the library "1stLAB" for PMOS since this simulations were perfomed by two different elements of the group. The schematics and symbols for each one of the MOSFETs are represented on figure 5 and 6. In the design of the schematics, the library "PRIMLIB" was used to obtain the MOSFETs (nmos4 and pmos4) and their width and length were altered to 4 μm and 1 μm, respectively. In NMOS, the body and the source were connected and in PMOS the body and the drain were connected. The ground supply cells were provided by the library "analogLib" and connected to the source, one input pin (V_{gs}) and an inputoutput (V_{ds}) pin were also created. After designing the symbol and the schematic, a new library was created with the name "1LAB_sim" for NMOS ("1stLAB_sim" for PMOS) to perform the simulations of the MOSFETs, which are represented in figure 7. For each of the MOSFETs a new cell was created with the same name as the respective cell of "1LAB" ("1stLAB"), in each cell the respective MOSFET symbol previously designed was added from the library "1LAB" ("1stLAB") and its gate and drain were connected to two different voltage sources ("vdc") obtained from the library "analogLib", each of these sources were connected to ground supply cells obtained from the same library. Finally, the simulation curves for the current on the drain in function of V_{gs} and V_{ds} were acquired for both the NMOS and the PMOS.

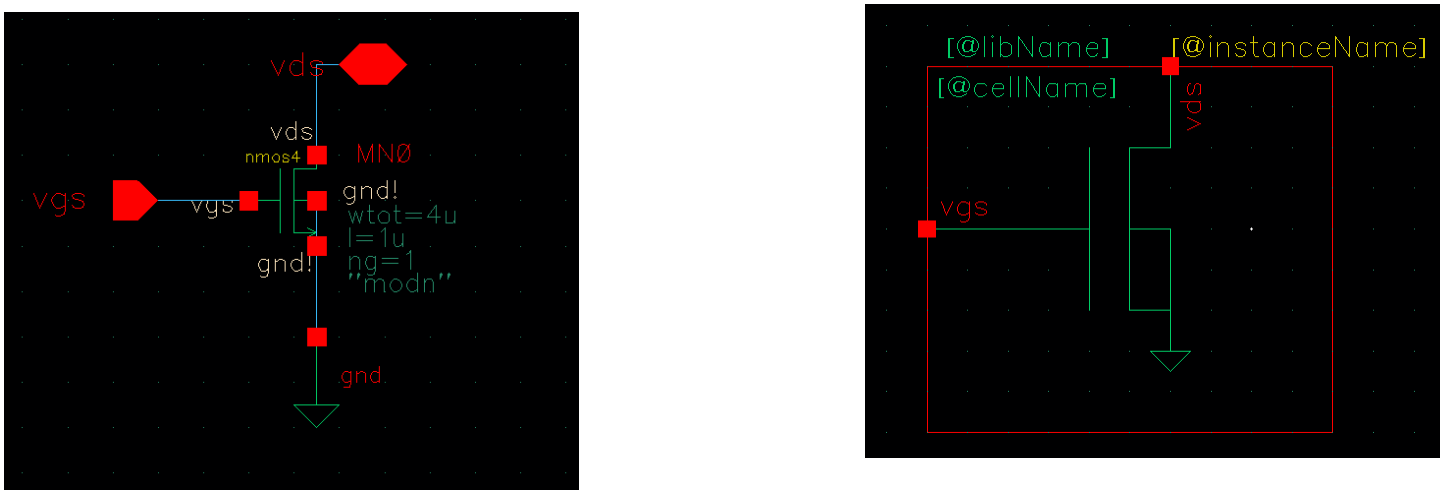


Figure 5: NMOS schematic and symbol

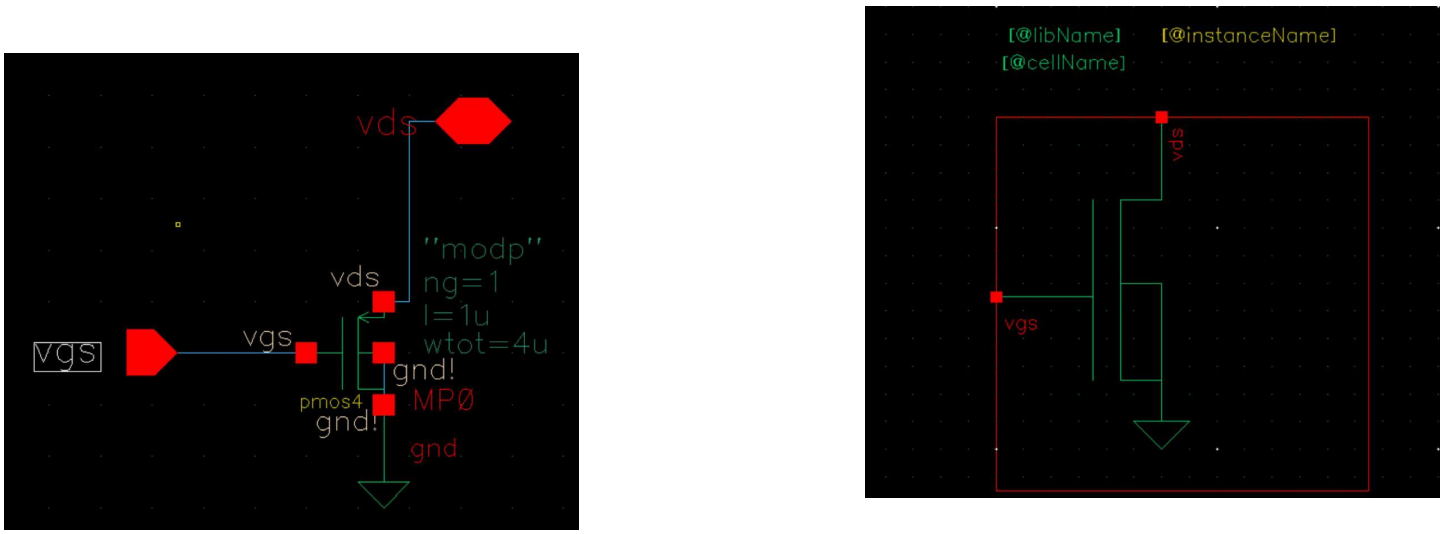


Figure 6: PMOS schematic and symbol

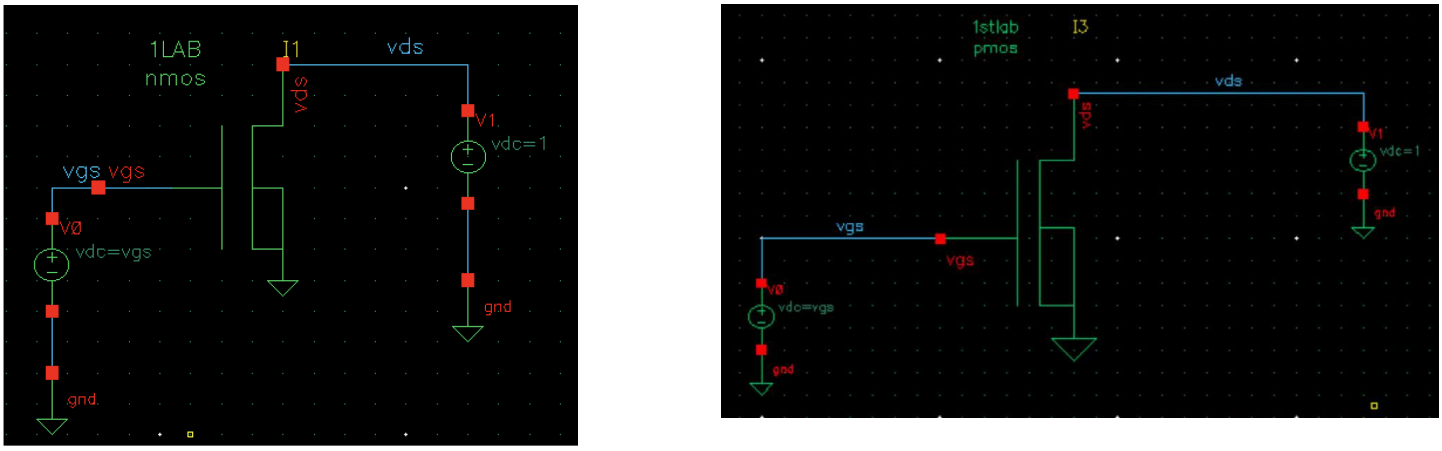


Figure 7: NMOS simulation on the left and PMOS simulation on the right

3.1 NMOS simulation

Firstly, the drain current in function of V_{gs} was simulated, obtaining the result in the left graph of figure 8, for V_{ds}= 1V, 1.4V, 1.8V, 2.2V, 2.6V, 3V. In the graph obtained, it is possible to distinguish the three operation modes of the NMOS. The first zone is the cut-off region, where V_{gs} is lower than V_t, and there is no current flowing through the NMOS, so the MOSFET behaves as an open switch and it is OFF. In the second region, V_{gs} is capable of surpassing V_t, but $V_{gs} - V_t$ is not greater than V_{ds}, so the NMOS is in the saturation region. V_{gs} will continue increasing until its difference with V_t becomes greater than V_{ds}, when this occurs the NMOS is in the triode region. Since, the simulation was tested for different values of V_{ds}, it is possible to observe that the triode region is not attained at the same time for this different values. Larger values of V_{ds} take longer to reach the triode region, since a larger value of V_{gs} is needed so that its difference with V_t is capable of surpassing the value of V_{ds}. The right graph of figure 8 shows the approximate position of each mode of operation of the NMOS.

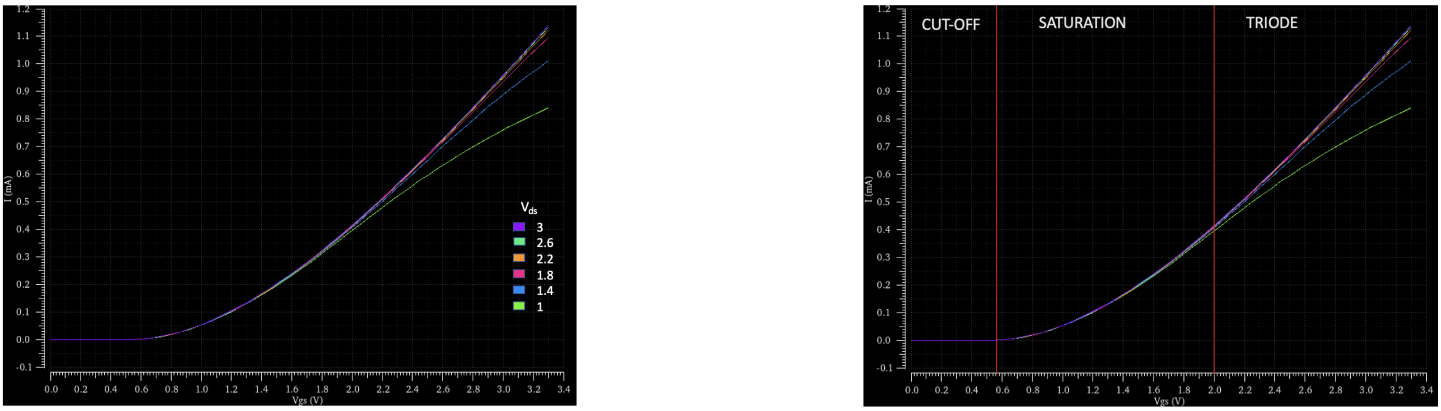


Figure 8: ID(VGS) simulation for NMOS

Secondly, the drain current in function of V_{ds} was simulated for V_{gs}= 0V, 0.8V, 1.6V, 2.4V, 3.2 V, obtain the graph from figure 9. As in the previous simulation, it is possible to distinguish the three operation modes of the NMOS. The first is the cut off region, which is not visible in the graph, since it occurs when V_{ds} is negative, in this case there is no current flowing on the MOSFET. The second region is the first one possible to observe in the graph, it is the triode region, where V_{ds} is smaller then the difference between V_{gs} and V_t. When V_{ds} surpasses the difference between V_{gs} and V_t, the NMOS is in the saturation region, which is the zone where the value of I_d becomes constant as represented in the graph obtained on the simulation. In this image, one can see that the saturation region is not attained at the same time for all the values of V_{gs}, for higher values of V_{gs} the value of V_{ds} necessary to reach the saturation region is higher, since the difference is also bigger

V_{gs} and V_t, so it takes longer to reach this zone. For V_{gs}=0, the NMOS never leaves the cut-off region, since V_{gs} is not able to reach V_t.

Thus, the results obtained in the simulation are the expected when comparing with the theoretic models for the NMOS.

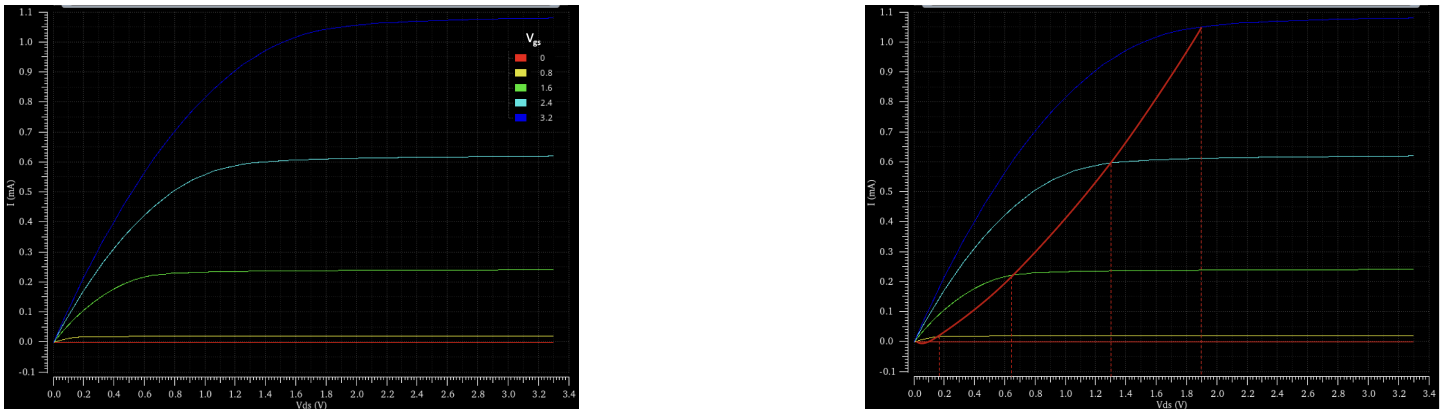


Figure 9: ID(VDS) simulation for NMOS

3.2 PMOS simulation

The analyzes made in the NMOS simulation section is analogous to the PMOS, with the only difference being the fact that the values of V_{ds} and V_{gs} are negative. So, the graphics resemble an "inverted version" of the NMOS graphics obtained above.

Similarly to the NMOS, the drain current in function of V_{gs} was simulated, obtaining the result in the graph of figure 10, for V_{ds}= -3V, -2.6V, -2.2V, -1.8V, -1.4V, -1V. In the graph obtained, it is possible to distinguish the three operation modes of the PMOS. Initially, $|V_{gs}|$ surpasses $|V_t|$ and $|V_{gs}| - |V_t|$ is higher than $|V_{ds}|$, so the PMOS is in the triode region. $|V_{gs}|$ decreases continually until its difference with $|V_t|$ reaches a value lower than $|V_{ds}|$ and the PMOS is now in the saturation region. Finally, $|V_{gs}|$ becomes lower than $|V_t|$ and the PMOS reaches the cut-off region. In this case the PMOS behaves as an open switch, since there is approximately no current flowing through it. Since, the simulation was tested for different values of V_{ds}, it is possible to observe that the saturation region starts at different points for different values. Smaller values of $|V_{ds}|$ have initially a higher drain current and take more time to reach the saturation region, since it is needed a lower value of $|V_{gs}|$ so that $|V_{ds}|$ is able surpass the value of $|V_{gs}| - |V_t|$. The right graph of figure 10 shows the approximate position of each mode of operation of the PMOS.

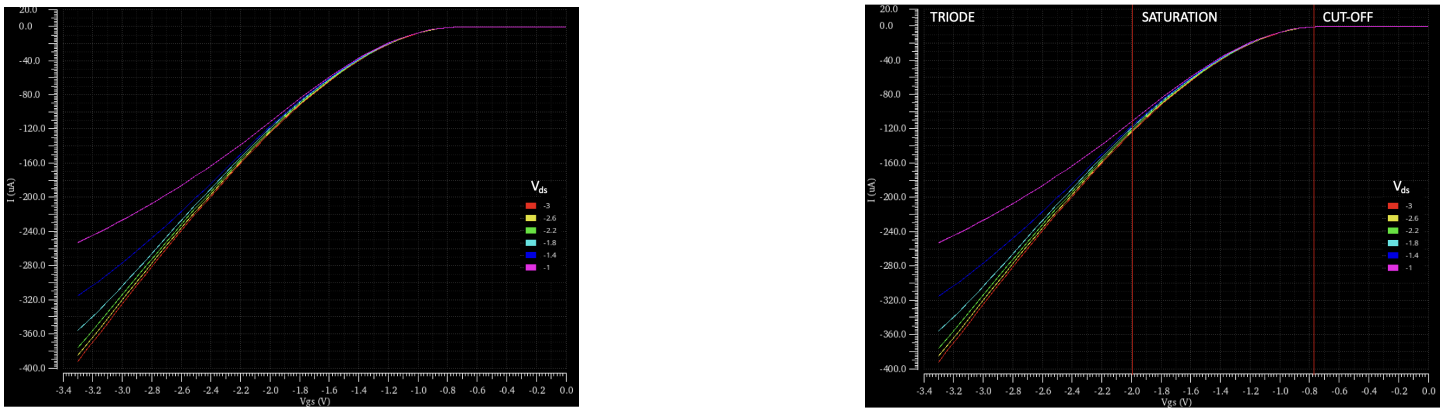


Figure 10: ID(VGS) simulation for PMOS

Finally, the drain current in function of V_{ds} was simulated for V_{gs}= -3.2V, -2.4V, -1.6, -0.8V, 0V, obtaining the graph on figure 11. It is again possible to distinguish the three operation zones of the PMOS. The first is the zone of saturation,

where the value of $|V_{gs}|$ is higher than $|V_t|$ and the difference between this two values is lower than $|V_{ds}|$. In this region, I_d is approximately constant as represented in the graph obtained. The second zone is the triode region, where $|V_{ds}|$ becomes smaller then the difference between $|V_{gs}|$ and $|V_t|$, since the value of $|V_{ds}|$ is decreasing. Then, PMOS reaches the cut-off region which is not visible in the graph, since it occurs when V_{ds} is positive, in this region there is no current flowing on the MOSFET. In this image, one can see that the for different values of V_{gs} the transition for the triode regions does not occur at the same time, for higher values of $|V_{gs}|$ the value of $|V_{ds}|$ necessary to reach the triode region is lower, so it takes less time to reach this zone. For V_{gs}=0, the PMOS never leaves the cut-off region, since $|V_{gs}|$ is not able to reach $|V_t|$.

Thus, the results obtained in the simulation are the expected when compared with the theoretical models for the PMOS.

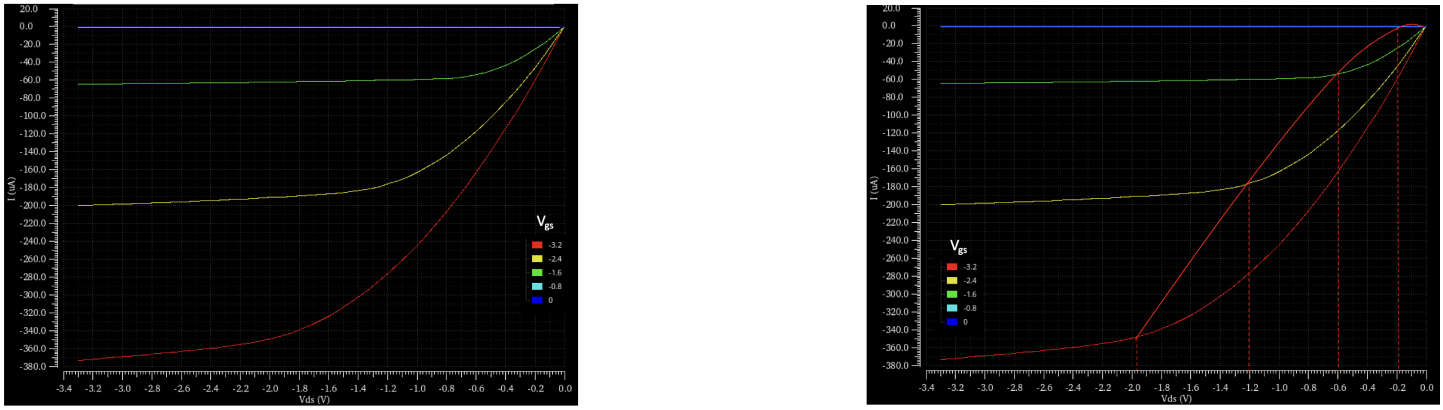


Figure 11: ID(VDS) simulation for PMOS

4 Conclusion

Throughout this lab report, it's intended to study and analyze the behavior of the drain's current in function of the change in terminal voltages and, likewise, to identify, from the graphics obtained, the operating stages of the transistor for both transistor models, NMOS and PMOS. As a result, in one hand, it's learnt how to use the software *Candence Virtuoso*, designed to project and create schematics and layouts of electronic devices, such as, transistors. In the other hand, it was possible to observe the differences between the operating regions (Cut-Off, Triode and Saturation), as well as how changing terminal voltages can contribute to manipulate the current values of the circuit, in each of the different operating regions.

Therefore, following the theoretical analysis written, reviewing the structure, the model and the operating stages of both NMOS and PMOS, it's verified that the simulations performed in this laboratory are in accordance with the results given by the theoretical analysis of the MOSFET transistors. Comparing the graphs obtained theoretically and in the simulation, it is possible to conclude that the results obtained with *Candence Virtuoso* where the expected and the same as the theoretical graphs presented in the Theoretical Analysis.

It is concluded that the main goals of this laboratory were achieved successfully.

5 Referências

- RAZAVI, B. (2001) "Desgin of Analog CMOS Integrated Circuits" (page 10)
- Figura 1: SEDRA, A. (2015) "Microeletronic Circuits" (SEVENTH EDITION)(page 249 and page 262)
- Figura 2: JFET n-channel (2009) "I–V characteristics and output plot of a JFET n-channel transistor" Visitado a 11/5/23 em: https://commons.wikimedia.org/wiki/File:JFET_n-channel.svg
- Figura 3: Anysilicon "Introduction to NMOS and PMOS Transistors". Visitado a 10/5/23 em: https://anysilicon.com/introduction-to-nmos-and-pmos-transistors/
- Figura 4: Eletronics and Applied Physics Projects (2012) "MOSFET Logic Inverter". Visitado a 12/5/23 em: http://ekim616.blogspot.com/2012/05/