TÉCNICO LISBOA

Mircroeletronics

3rd LAB Report

Current Mirror Design

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1 Introduction

"The current mirror is one of the most important building blocks of analog integrated circuits." (Sedra, Smith, 2015) In the third laboratory of Microeletronics, there are two main goals: the first one is to study the MOS transistor as a current source, and, for that, throughout this report, a circuit of a basic current mirror is analysed, as the transistor Q2 works like a current source; the second one is to understand the impact of a side-diffusion phenomenon, denominated **channel-length modulation**.

This lab report is divided in two mains sections:

The first section is a theoretical preparation, in which is presented the circuit of a basic current mirror whose transistors are analysed according to their working regions and to their behavior towards the impact of channel-length modulation (*clm*). In one hand, it's studied their working-regions and their behavior without the influence of *clm*; in another hand, it's studied their working regions and their behavior with the effect of *clm*. This study is associated with eqautions that guide, mathematically, the transistors characteristics.

The second section is a *Cadence virtuoso* analysis, in which are presented the schematic, the symbol of the basic current mirror and its performed simulations. In this section, the proposed activity is completed, i.e. the following items are achieved:

- Assuming that the input current and the output current are the same (10uA), design the W and L of the NMOS transistors to have an overdrive voltage of 200mV;
- Simulate the current mirror with a DC sweep output voltage range of 0 to 3.3V with comments about the simulation results referring in particular to the overdrive voltage, to the V_{DS} that ensures the output current identical to the input current and to the channel-length modulation impact;
- Perform a corner analysis;
- Keeping the same W/L, simulate, for typical conditions, the current mirror with MOS transistors with L=0.35um, 1um, 4um and comment the channel-length modulation impact of L.

Finally, a comparison between the theory and the simulation results is commented in the conclusion.

2 Theoretical Preparation

2.1 Current Mirror with two NMOS

The basic current mirror designed with two NMOS transistors it's shown in 1.

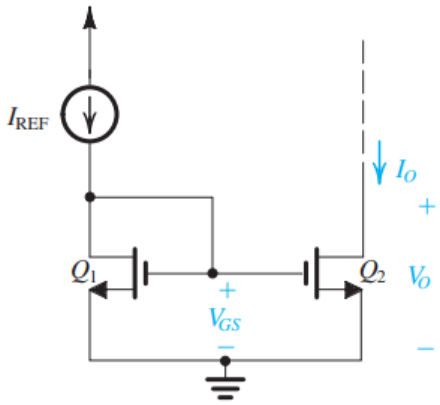


Figure 1: Design with two NMOS

The design starts with a complex circuit that is used to generate a stable reference current I_{REF}. In this case, the NMOS transistors are identical, meaning that $I_o = I_{REF}$, thus the circuit simply replicates or mirrors the reference current in the output terminal, hence **current mirror**.

The connection of Q_1's and Q_2's gates provides an output current I_o that is related to the reference current I_{REF}, whose relationship is solely determined by the geometries of the transistors, which makes it "a simple and attractive relationship".

The connection between the gate and the drain of Q1 implies that $V_G = V_D$. Considering that $V_{GS} > V_t$. trough the the equation

$$V_{DS} \geq V_{GS} - V_t \tag{1}$$

it's concluded that Q1 is in saturation's region. Therefore, the drain's current of Q1 is given by:

$$i_{DS1} = \frac{\mu C_{ox}}{2} \frac{W_1}{L_1} (V_{GS} - V_{th})^2 \tag{2}$$

If Q2 is to supply a constant-current output, it is essential that Q2 operates in saturation, like Q1. To ensure that Q2 is saturated, the circuit to which the drain of Q2 is to be connected must establish a drain voltage V_o that satisfies the equation

$$V_o \geq V_{GS} - V_t \tag{3}$$

Equivalently, in terms of the overdrive voltage V_{OD} of Q1 and Q2, $V_o \geq V_{OD}$. Hence, the drain's current of Q2 is given by:

$$i_{DS2} = \frac{\mu C_{ox}}{2} \frac{W_2}{L_2} (V_{GS} - V_{th})^2 \tag{4}$$

Considering that both transistors gate's current is zero, it's concluded that:

$$I_{REF} = I_{DS1} \tag{5}$$

and

$$I_o = I_{DS2} \tag{6}$$

In both transistors, the characteristic i_D in function of v_{DS} if given by the following graph:

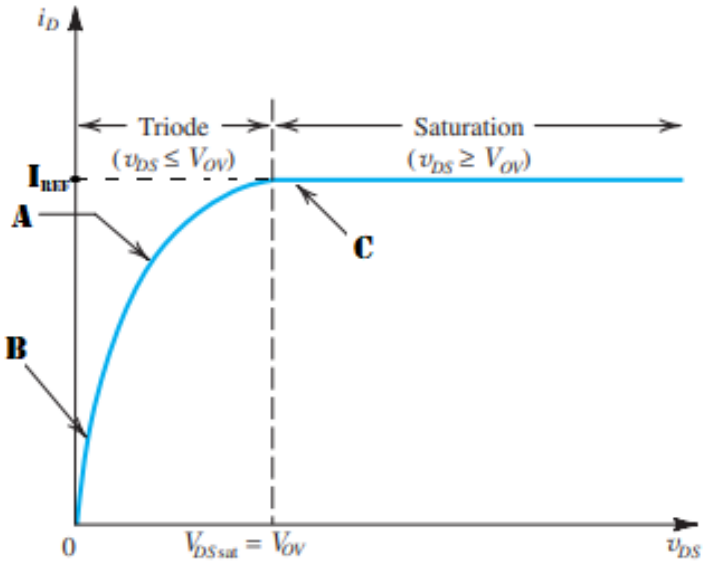


Figure 2: Working regions of the both transistor, until saturation

The triode region is satisfied for $v_{DS} \leq V_{OD}$.
The transition between triode and saturation regions is given by $v_{DS_{sat}} = V_{OD}$. The saturation region is satisfied for $v_{DS} \geq V_{OD}$.

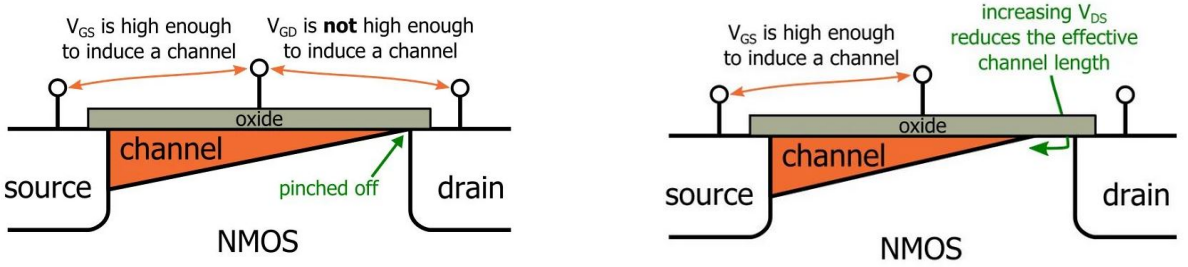
- Region A: Curve bends because the channel resistance increases with v_{DS};
- Region B: Almost a straight line with slope proportional to V_{OD};
- Region C: Current saturates because the channel is pinched off at the drain end, and v_{DS} no longer affects the channel. Along this area, the equation $v_{GS} = V_t + V_{OD}$ is satisfied.

`Note: As a way of comparing both characteristics (with and without impact of channel-length modulation), it is dashed with cyan blue the curve without the impact of clm and with darker blue is the curve being study in this subsection.`

(Sedra, Smith, 2015)

2.2 channel-length modulation

The saturation-region develops, in both transistors, as a result of the channel being "pinched-off" at the end of the drain, shown in figure 3a. Unfortunately, the "pinching-off" doesn't mean that the drain-to-source voltage's influence is over. The channel is still affected by additional increases since the pinch-off point is getting closer to the source, shown in figure 3b.



(a) Pinch-off point

(b) Pinch-off point is getting closer to the source

Figure 3: Channel "Pinching-off"

In addition to 3b, as the channel pinch-off point moves slightly away from the drain, because V_{DS} increases beyond $V_{DS_{sat}}$, the effective channel length reduces by ΔL, as shown in the figure below.

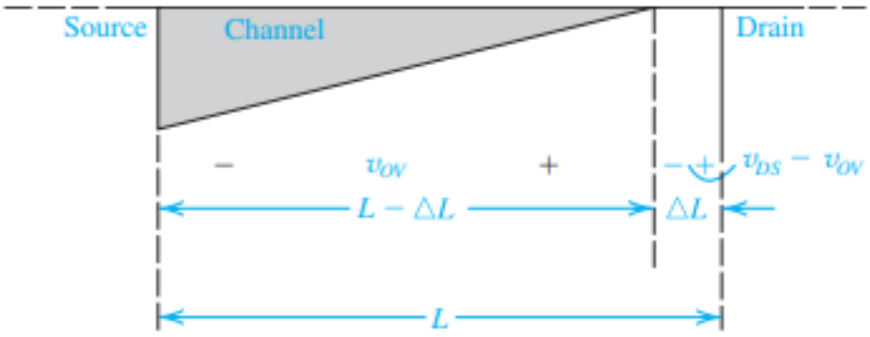


Figure 4: Channel length is affected

i.e. for high values of V_{GS} (voltages greater than $V_{DS_{sat}}$), this side-diffusion phenomenon reduces the length of the channel: $L_{eff} = L_{real} - \Delta L$.

As a result, the saturation-region drain-current expression **must be adjusted**, taking into account the **channel-length modulation**.
By incorporating the incremental channel-length reduction, the i_D equation is now written as

$$i_{DS} = \frac{\mu C_{ox}}{2} \frac{W}{L - \Delta L} (V_{GS} - V_{th})^2 \tag{7}$$

which can also be written as

$$i_{DS} = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \frac{\Delta L}{L}) \tag{8}$$

and, since, $\frac{\Delta L}{L} = \lambda V_{DS}$, the equation results in

$$i_{DS} = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS}) \tag{9}$$

It's possible to say that the channel-length modulation impact can be reduced by increasing the transistor length.
In fact, generally, a length $L < 1\mu m$ has significant impact of channel-length modulation, hence, a length $L \geq 1\mu m$ is recommended for all transistors in saturation. However, increasing the length to values higher than 1µm has no significant benefit for channel-length modulation.

The transistor Q1 is always saturated, so the point where $V_{DS_{sat}} = V_{OD}$ is simultaneously the point where V_{DS} is equal to V_{GS} (intersection point), i.e. $I_{REF} = I_{DS1}$ (shown in figure 2) However, in the transistor Q2 the point where V_{DS} is equal to V_{GS} (intersection point), i.e. $I_{out} = I_{DS2}$ happens **after** the point $V_{DS_{sat}} = V_{OD}$ (saturation transition point), like is shown in the figure below.

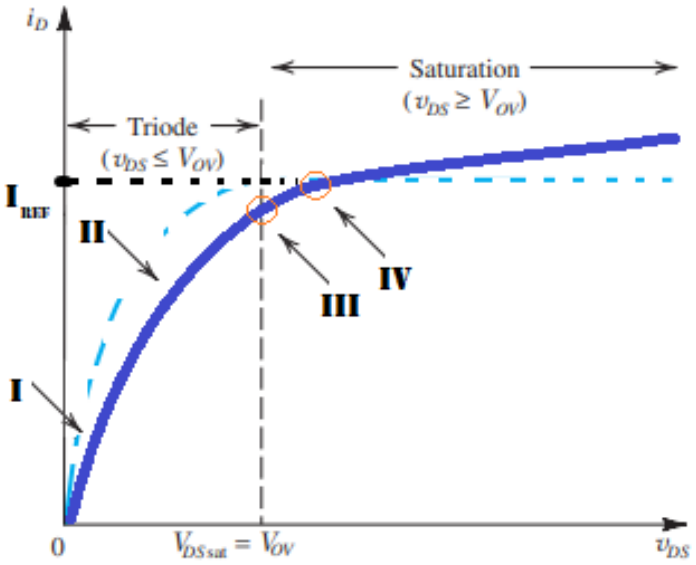


Figure 5: Working regions of the transistor Q2, with emphasis on the intersection point

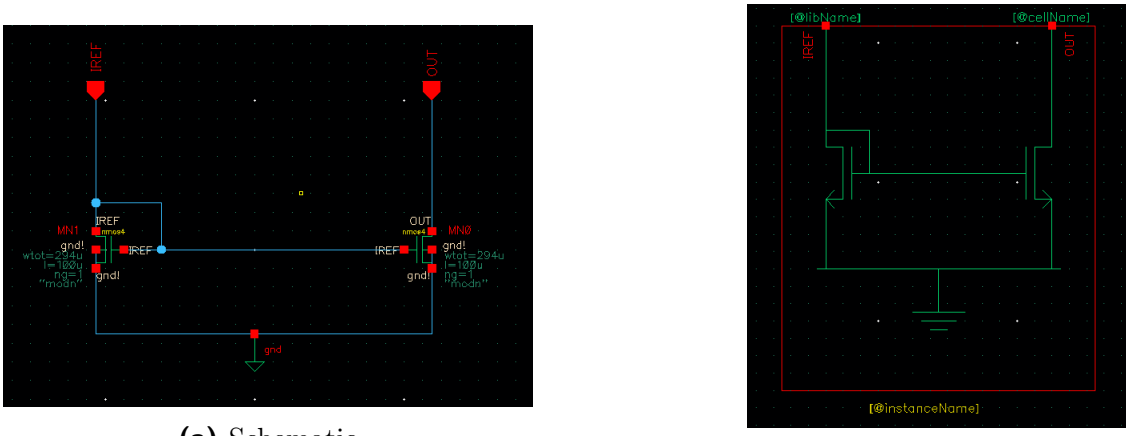
The triode region is satisfied for $v_{DS} \leq V_{OD}$.
The transition between triode and saturation regions is given by $v_{DS_{sat}} = V_{OD}$.
The saturation region is satisfied for $v_{DS} \geq V_{OD}$.
The regions I and II are similar to the the regions B and A, respectively, of fig 2.

- Region III: The transistor enters the saturation region, but V_{DS} is different than V_{GS}, so V_{GS} continues to increase;
- Region IV: V_{DS} is equal to V_{GS}, meaning that, only now, $I_o = I_{DS2}$.

3 Current Mirror Schematic, Symbol and Simulation

3.1 Neglecting Channel-Lenght Modulation

In order to design the current mirror, it is necessary the use of two nmos, both from the library "PRIMLIB" ("nmos4"), a gnd supply cell from "analogLib" and two pins one INPUT and an OUTPUT. This components where connected has shown in figure 6a.



(a) Schematic

(b) Symbol

Figure 6

To determine the width and length of the two NMOS, assuming that the current on the input and output are both equal to $10\mu A$ and the overdrive voltage $(V_{GS} - V_{th})$ is equal to 200mV the following equation was used:

$$i_{DS} = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{th})^2 \tag{10}$$

Now replacing the values of i_{DS}, V_{OD} and $K_{pn} = \mu C_{ox} = 170\mu A/V^2$, which is given in the document "0.35 m CMOS C35 Process Parameters":

$$\frac{W}{L} = \frac{2 \times 10}{170 \times (200 \times 10^{-3})^2} \approx 2.94. \tag{11}$$

For $I_{REF} = I_{OUT} = 10\mu$A, $I_{OUT} = \frac{W_2/L_2}{W_1/L_1} I_{REF}$, thus $\frac{W_2/L_2}{W_1/L_1} = 1$, so the same value of width to length ratio can be used in both transistors, which is 2.94. Regarding this value, the transistors were simulated with a $294\mu m$ width and $100\mu m$ length. The symbol of the current mirror was designed as shown in figure 6b.

Then, the library for the simulation was created, and the symbol of the current mirror previously created was connected to an current source providing $10\mu A$ (idc from library "analogLib") and a vdd from "analogLib" on its input, and to a voltage source with value vdc V (vdc from library "analogLib") and a gnd supply cell on its output.

The simulation schematic is shown in the figure bellow.

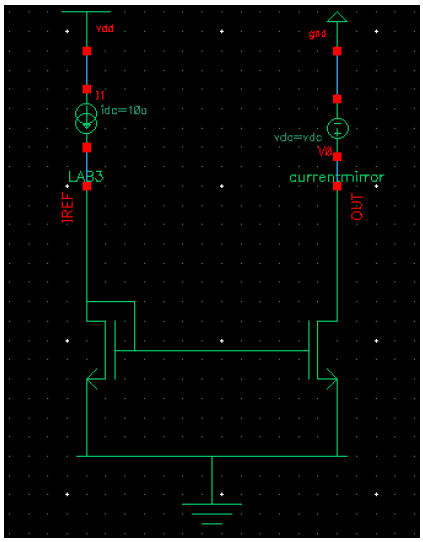


Figure 7: Simulation of the current mirror

3.1.1 DC Sweep

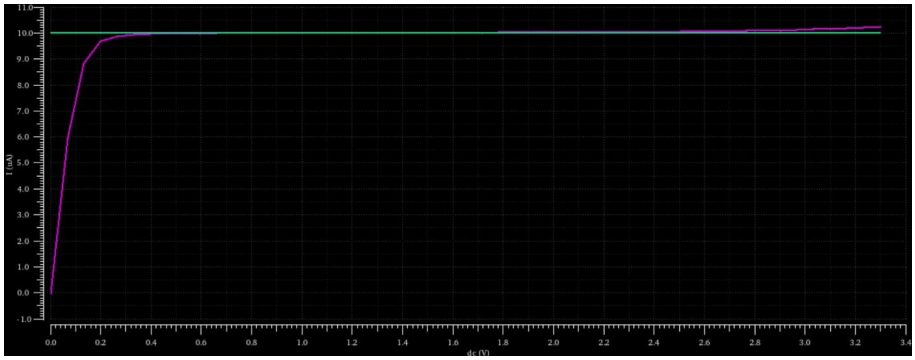


Figure 8: Cadence Virtuoso analyses: current mirror behavior, neglecting channel-length modulation; in pink, the output and in green, the input.

In this simulation, V_{DS} is varying between 0V and 3.3V (x axis) and the y axis corresponds to I_D.

It is possible to observe that I_D is nearly constant with the increase of V_{DS} in the zone of saturation, confirming that current mirrors are useful to copy current sources. This occurs when the value of V_{DS} of the two NMOS transistors is the same. Channel-length modulation is being neglected, this behavior is a result of the channel's length being $100\mu m \gg 1\mu m$. The value of I_D for the first NMOS stays constant, while the value of I_D for the second NMOS increases until it reaches a value of I_D equal to the one of the first NMOS, reaching saturation (for V_{DS} approximately equal to 0.42V), and having from then on a value of I_D approximately constant and equal to the first transistor ($I_{OUT} = I_{REF}$). The V_{OD} initially is higher than the value of V_{DS}, being equal to the value of V_{DSsat} when the transistor reaches the zone of saturation, from then on the value of V_{OD} is lower than V_{DS}, since V_{DS} is continually increasing.

3.1.2 Corner Analysis

The corner analysis was then performed, for temperatures of -40ºC and 125ºC. In the corner analysis, it is possible to observe that overall the same behaviour as described in the previous section was observed. Once more, the x axis corresponds to V_{DS} and the y axis to I_D.

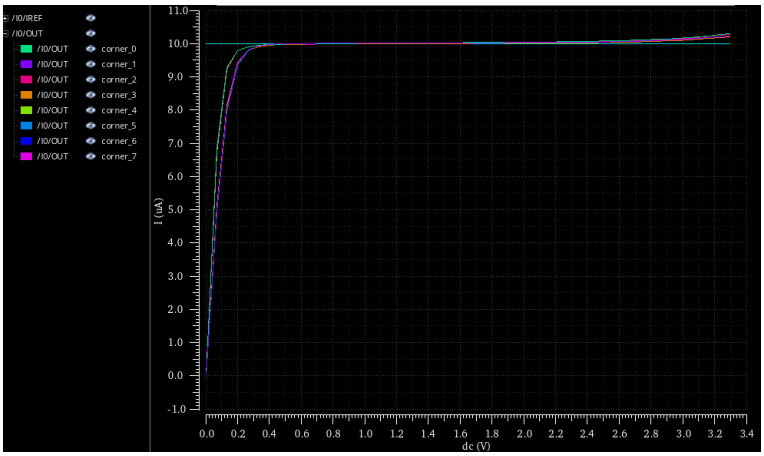
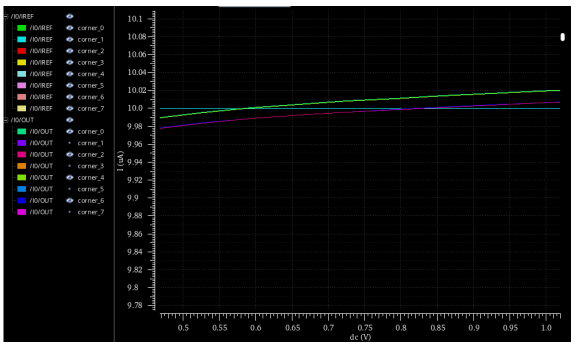


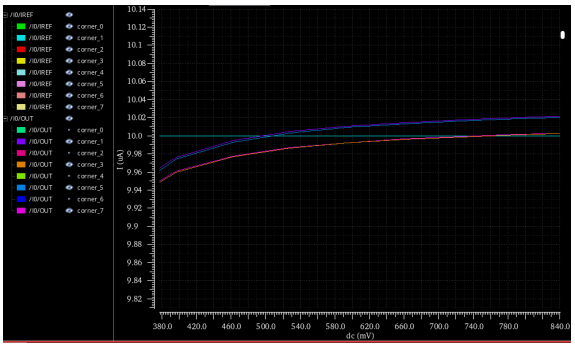
Figure 9: Corner analysis

In the corner analysis with T=-40ºC (10a), the worst power and worst one (corners 0 and 4) reach saturation faster and maintain a slightly higher value of I_D than the other two corners (2 and 6 which correspond to worst speed and worst zero). This occurs, since V_{th} is higher for worst speed and worst zero, so a higher V_{GS} is needed to reach the same V_{OD} as the other two corners, this leads to a higher value of V_{DS} needed to reach saturation. It is possible to observe that worst power and worst one (corners 0 and 4) reach saturation approximately at the same time, but worst power reaches it slightly faster. For worst speed and worst zero, worst speed reaches saturation faster.

The same behaviours for T=-40ºC occur to T=125ºC (10b), where worst power, worst speed, worst one and worst zero correspond to corners 1, 3, 5 and 7 respectively. The line that stays constant corresponds to I_{REF} of the first NMOS.



(a) For T=-40ºC



(b) For T=125ºC

Figure 10: Corner analysis

Comparing the two temperatures, for 125ºC the value of V_{th} is lower, so the corners for this temperature reach saturation faster than for T=-40ºC which has a higher value of V_{th}.

3.2 Analyzing channel-length modulation

In this analysis, the value of length was changed to $0.35\mu m$, $1\mu m$ and $4\mu m$, without altering $\frac{W}{L}$, so the width was also changed to prevent the alteration of this ratio.

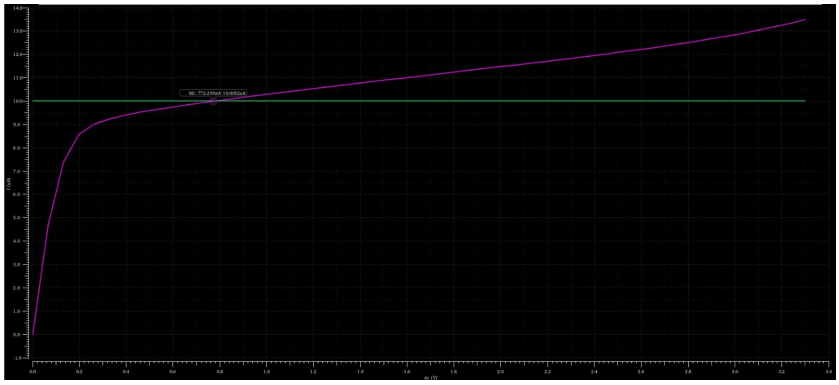


Figure 11: Cadence Virtuoso analyses: current mirror behavior, including channel-length modulation, with transistor length $L = 0.35\mu m$; in pink, the output and in green, the input.

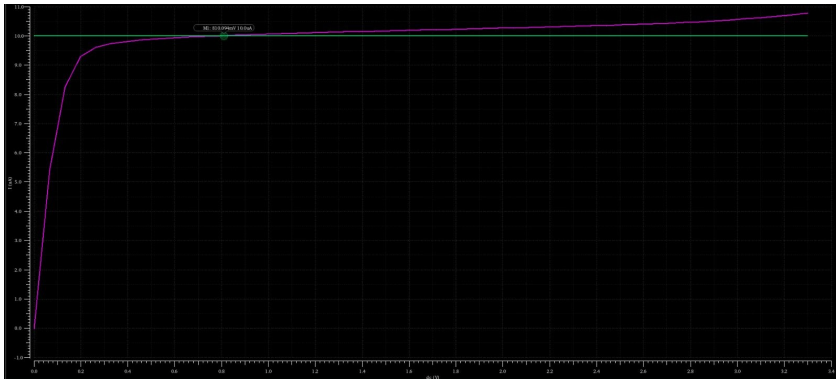


Figure 12: Cadence Virtuoso analyses: current mirror behavior, including channel-length modulation, with transistor length $L = 1\mu m$; in pink, the output and in green, the input.

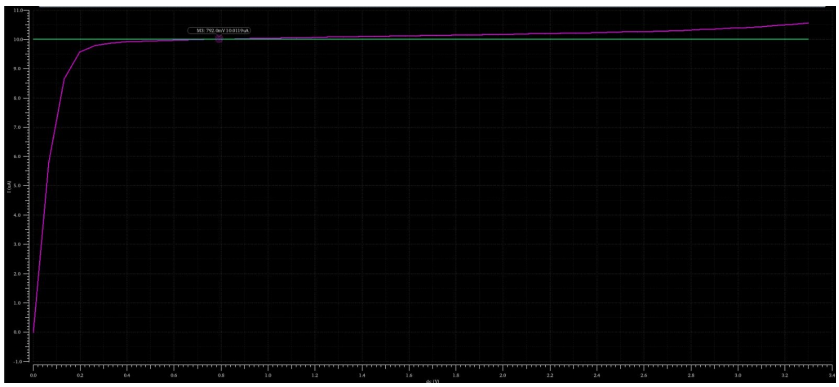


Figure 13: Cadence Virtuoso analyses: current mirror behavior, including channel-length modulation, with transistor length $L = 4\mu m$; in pink, the output and in green, the input.

The value where the input and output lines intersect is when $I_{OUT} = I_{REF}$, so, when both transistors have the same value of V_{DS}. For $L = 0.35\mu m$, this value is around $772mV$, for $L = 1\mu m$ is $810mV$ and for $L = 4\mu m$ is $792mV$, so this value is around $0.8V$. It is important to recall that, in the second transistor, $V_{OD} = V_{GS} - V_{th} = V_{DS}$ when entering the saturation region, but, because of channel-length modulation, for $I_{OUT} = I_{REF}$, V_{GS} still needs to increase so that it can reach the same value as V_{DS} (and then all voltages became the same for both transistors, and so the currents too). This value when $V_{DS} = V_{GS}$ is around $0.8V$, as simulated. It is also possible to withdraw from the graphics that, for different lengths, the slope in the saturation region differs, which is also because of channel-length modulation. To analyse this behavior, the channel-length modulation coefficient λ was calculated using the derivative of the equation 9 in function of V_{DS} obtaining:

$$\frac{di_{DS}}{dV_{DS}} = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{th})^2\lambda \tag{12}$$

Since, $\mu C_{ox} = 170\mu A/V^2$, $\frac{W}{L} = 2.94$, $V_{GS} - V_{th} = V_{0D} = 200mV$, but the value of $\frac{di_{DS}}{dV_{DS}}$ is still needed, to obtain this value the slope of the graph after $I_{OUT} = I_{REF}$ was obtained. For $L = 0.35\mu m$ it is approximately $1.24\mu A/V$, $0.2284\mu A/V$ for $L = 1\mu m$ and for $L = 4\mu m$ is $0.1746\mu A/V$. Isolating λ in the previous equation, the values obtained for the channel-length modulation coefficient are 0.125 for $L = 0.35\mu m$, 0.0229 for $L = 1\mu m$ and 0.0175 for $L = 4\mu m$. The results obtained are the expected, for the lower value of length ($L = 0.35\mu m$) the value obtained for the channel-length modulation coefficient is higher than for the other lengths, and the difference in the channel-length modulation coefficient for the other two lengths is very small, which shows that for lengths $L > 1\mu m$ λ has less influence in I_D.

Furthering the analyses, it is clear that channel-length modulation affects I_D significantly for length values below $1\mu m$. It is also clear that increasing the channel's length mitigates channel-length modulation, because ΔL is diluted in bigger lengths and so causes less impact. So, for $L < 1\mu m$ the channel-length coefficient λ is bigger and I_D varies more; for $L > 1\mu m$, λ is smaller, decreases with the increase of L and I_D varies less.

4 Conclusion

Throughout the thrid lab report, it was intended to study the transistor as a current source and, for that, it's analysed a current mirror circuit.

The first part, was written a theoretical preparation about the current mirror circuit, in which the transistor Q2 works like a current source. In this part, it was able to understand the effects of the channel-length modulation, which were explored further in the second main part of the report.

The second part, it was given a deep dive analysis to the simulations performed to the current mirror circuit, projected in *Cadence virtuoso*. In this analysis it was possible to observe that when neglecting channel-length modulation coefficient, the second NMOS reaches saturation for $V_{OD} = V_{DS}$, in this case $I_{OUT} = I_{REF}$ and both transistors have the same V_{DS}, this occurs for length values very superior to $1\mu m$, as one was expecting to occur theoretically. However, for different values of length one observed the effect of channel-length modulation coefficient. For lower values of length (less than $1\mu m$) the effect of this coefficient was more present, in this cases the NMOS transistor reached saturation for $V_{OD} = V_{DS}$, but it was still needed an increase in V_{GS} to obtain $I_{OUT} = I_{REF}$, so after reaching saturation I_{DS} doesn't stay approximately constant. It was also possible to understand that, experimentally, the value of $I_{OUT} = I_{REF}$ does not stay always constant, not even when neglecting channel-length modulation coefficient as one would expect from the theoretical models. In the corner analysis, one can understand that for T=125^{o}C the saturation region is reached faster than for T=-40^{o}C, since the value of V_{th} is higher for T=-40^{o}C. It was also possible to conclude that the corners with lower V_{th} reach saturation faster.

As the group was able to reach the settled goals, the third lab of Microeletronics is completed successfully.

5 Referências

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[2] Adel S. Sedra, Kenneth C. Smith, "Microelectronic Circuits", 7th edition, p.257-258, p.271, p.509, p.513, 2015.

[3] "0.35 m CMOS C35 Process Parameters", Document Number: ENG -182, Revision: 2.0

[4] Robert Keim, "MOSFET Channel-Length Modulation", 2016. Visited in 26/5/23: https://www.allaboutcircuits.com/technical-articles/mosfet-channel-length-modulation/