Mircroeletronics

5th LAB Report

Current Bias Generator

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1 Introduction

In the last laboratory of Microelectronics, it is studied how to design a current bias generator. This report is divided in three main sections:
First, starting with a theoretical preparation, in this section, it's discussed the model and, then it's determined the initial design parameters.
Second, through *Cadence virtuoso* it's performed various simulations and analysis, after delineating the schematic and the symbol. This section has two parts. In the first part, it's studied the circuit discussed in the theoretical preparation, while, in the second part, it's studied the possible improvements for the circuit. For both, it's created a testbench to simulate the circuit and to test the worst-case scenarios (corner analysis), as well as, with another testbench, to analyse the **P**ower **S**upply **R**ejection **R**atio (PSRR).
Third, it's presented the comparison of results and the conclusions for this lab.

2 Theoretical Preparation

In the section '11.2 Supply-Independent Biasing' of [1], it's presented the simple circuit to establish supply-independent currents, shown in figure 1. However, there's no control on the amount of current flow, i.e. there is no design parameter to control I_{REF} or I_{out} (also named I_{copy}), which is a meaningful drawback.

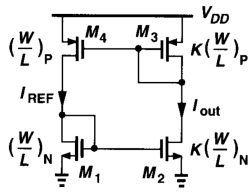


Figure 1: Simple Supply-Independent Biasing

The solution to establish control over the circuit or to uniquely define the currents is achieved by adding a resistor R_S, as shown is the figure 2.

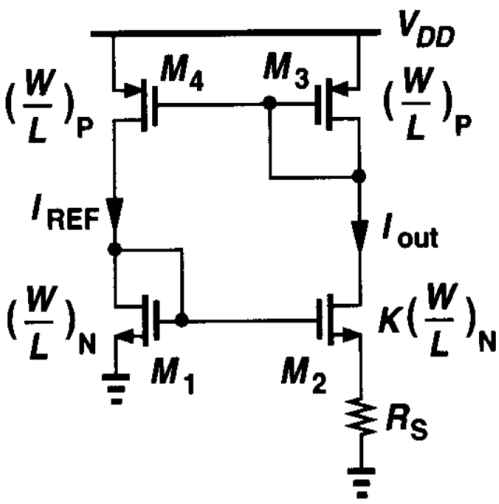


Figure 2: Supply-Independent Biasing with resistor R_S

Following the **assumptions**

- (i) M_{1-4} work in saturation region;
- (ii) M_{1-4} are long-channel devices, i.e. $\lambda_{1-4} \approx 0$;
- (iii) $(\frac{W}{L})_3 = (\frac{W}{L})_4$;
- (iv) $(\frac{W}{L})_2 = K(\frac{W}{L})_1$;

By adding the resistor, the previous equation, $V_{GS1} = V_{GS2}$, changes into equation (1):

$$V_{GS1} = V_{GS2} + R_S.I_{out} \tag{1}$$

And, by knowing the equation (2):

$$I_D = \frac{1}{2}.\mu_n.C_{OX}.\frac{W}{L}.(V_{GS} - V_{th})^2 \Leftrightarrow V_{GS} = \sqrt{\frac{2I_D}{\mu_n.C_{OX}.\frac{W}{L}}} + V_{th} \tag{2}$$

It's possible to determine the equation (3):

$$\sqrt{\frac{2I_{out}}{\mu_n.C_{OX}.(\frac{W}{L})_N}} + V_{th1} = \sqrt{\frac{2I_{out}}{\mu_n.C_{OX}.K(\frac{W}{L})_N}} + V_{th2} + R_S.I_{out} \tag{3}$$

By neglecting the body, ie. by assuming that V_{th1} =V_{th2}, the equation (3) modifies accordingly, changing into equation (4):

$$\sqrt{\frac{2I_{out}}{\mu_n.C_{OX}.(\frac{W}{L})_N}}.(1 - \frac{1}{\sqrt{K}}) = R_S.I_{out} \Leftrightarrow I_{out} = \frac{2}{\mu_n.C_{OX}.(\frac{W}{L})_N}.\frac{1}{R_S^2}.(1 - \frac{1}{\sqrt{K}})^2 \tag{4}$$

In equation (4), as expected, it's possible to verify that the current is independent of the supply voltage, which is an important achievement. However, there are two drawbacks: first, the current I_{out} is still dependent on the process, the temperature and R_S value; second, in practice, $V_{th1} \neq V_{th2}$, hence, the body effect for M_2 cannot be neglected.

The second drawback can, actually, be solved by moving the resistor, like shown in figure 3.
Since $I_{REF} = I_{out}$, the equation 1 still stands. Thus, if $V_{th1} = V_{th2}$, it's possible to verify that the equation (4) withstands too, implying that the current is still independent of the supply voltage. Nevertheless, M_2 has, now, no body effect. Therefore, the sole remaining problem is the reliance on the procedure, the temperature, and the R_S value. However, this is just a parenthesis in the preparation, as this improved version won't be studied in this report. As required in the lab guide, it will be studied the circuit shown in figure 2.

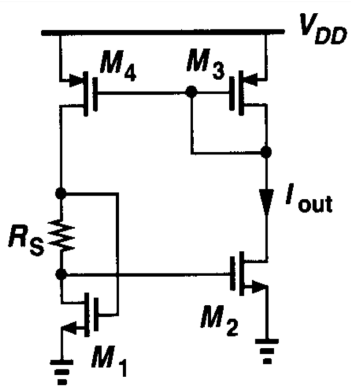


Figure 3: Improved Supply-Independent Biasing

2.1 Parameters Calculation

The requirements for this lab's current bias generator are the following:

- The supply assumes to be $3,3V \pm 10\%$
- The maximum current for the current reference generation must be $4\mu A$;
- $V_{OD} = 0,2V$ in all transistors, which implies $2\mu A$ of current in both branches;
- The channel-length must be superior to $1\mu m$ (as it constrains the channel-length modulation effect)
- Four current outputs (from PMOS) with $1\mu A$ each;
- Ratio of 2:1 between the current bias generator and the outputs;
- The transistores adaptados perguntar prof $ngates = 2$;
- K=4, to guarantee a good balance between the transistors size and the difference of V_{GS} voltages of both NMOS;

Through the equation (5), it's possible to determine the $\frac{W}{L}$ for each transistor:

$$I_{DS/SD} = \frac{K_{PN/PP}}{2}\frac{W}{L}V_{OD}^2 \Leftrightarrow \frac{W}{L} = \frac{2I_{DS/SD}}{K_{PN/PP}.V_{OD}^2} \tag{5}$$

And, through [2], it's possible to verify KPN and KPP values, like shown in the following figure:

Parameter	Symbol	Min	Typ	Max	Unit	Note
gain factor	KPN	150	170	190	μA/V²	7
gain factor	KPP	48	58	68	μA/V²	7

Figure 4: KPN and KPP typical values

First, starting with the NMOS transistors, $(\frac{W}{L})_N$.

– M_1 (left transistor):

$$(\frac{W}{L})_N = \frac{2I_{DS}}{KPN_{Typ}.V_{OD}^2} = \frac{(2)(2\times10^{-6})}{(170\times10^{-6})(0,2^2)} \Leftrightarrow (\frac{W}{L})_N = (\frac{W}{L})_1 = 0,5883 \Rightarrow (\frac{W}{L})_1 = 0,6$$

– M_2 (right transistor): Succeeding the **assumption** (iv), and following the requirement a ratio of 1:K (K=4),

$$(\frac{W}{L})_2 = K(\frac{W}{L})_1 = 4.(\frac{W}{L})_1 \Rightarrow (\frac{W}{L})_2 = 2,4$$

Second, for the output PMOS transistors:
Succeeding the requirement of current outputs with $1\mu A$ each,

$$(\frac{W}{L})_{out} = \frac{2I_{SD}}{KPP_{Typ}.V_{OD}^2} = \frac{(2)(1 \times 10^{-6})}{(58 \times 10^{-6})(0,2^2)} = 0,8621 \Rightarrow (\frac{W}{L})_{out} = 0,9$$

Third, for the reference PMOS transistor:
Succeeding the requirement of a ratio of 2:1,

$$(\frac{W}{L})_P = 2 \times (\frac{W}{L})_{out} \Rightarrow (\frac{W}{L})_P = 1,8$$

Finally, through equation 4, knowing that $\mu_n.C_{OX} = KPN$, it's possible to determine the value of R_S,

$$R_S = \frac{\sqrt{\frac{2I_{out}}{\mu_n.C_{OX}.(\frac{W}{L})_N}}.(1 - \frac{1}{\sqrt{K}})^2}{I_{out}} = 49507\Omega \Rightarrow R_S = 50k\Omega$$

3 Cadence Virtuoso

3.1 Basic Current Bias Generator

3.1.1 Schematic, Symbol and Simulation

`Note: Throughout this report the main simulations are performed with 'rpolyh'. When it's performed with another type of resistor it's indicated and its solely purpose is to compare the results with 'rpolyh'.`

- Schematic

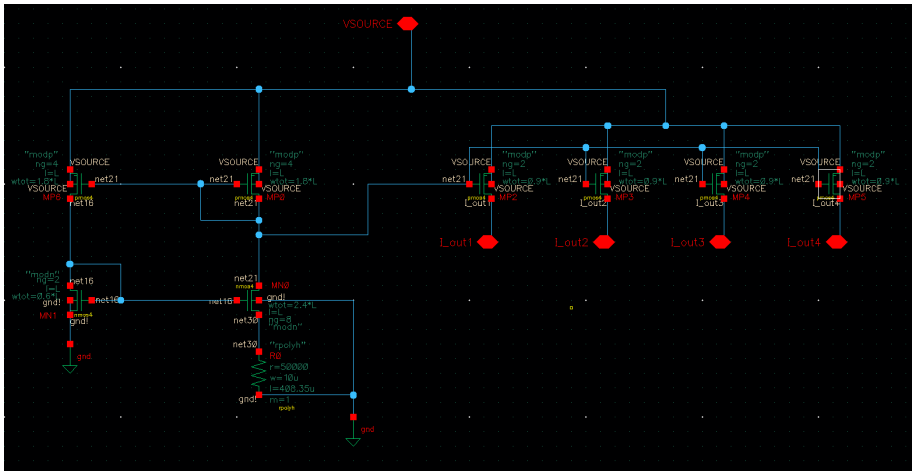


Figure 5: Schematic with parameters determined in section 2.1

The 'Width' property of the transistor is defined as a function of L, a variable which represents the length of the transistor.
The 'Width Stripe' property is defined as the quotient of 'Width' and the 'Number of Gates'.
The 'Number of Gates' property is chosen according to the ratios 1:K (K=4) and 2:1.
The ratio 1:K (K=4) regards the NMOS trasistors, whose 'ngates' or 'ng' is equal to 2 and $2 \times 4 = 8$ gates, for M_1 and for M_2 trasistors, respectively;
The ratio 2:1, between the current mirror and the outputs, regards the PMOS transistors. The number of gates, for the output PMOS transistors, is equal to 2. Hence, the number of gates, for the PMOS transistors of the current mirror, is equal to $2 \times 2 = 4$.

- Symbol
  The symbol represents four current sources, connected to a common voltage source, diverging into four outputs, each with a reference current supply for any arbitrary circuit block.

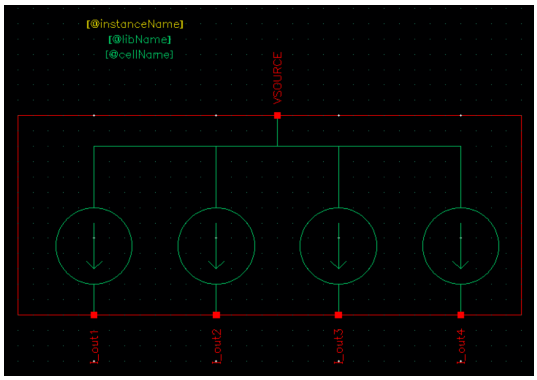


Figure 6: Symbol

- Simulation

  – **Testbench**

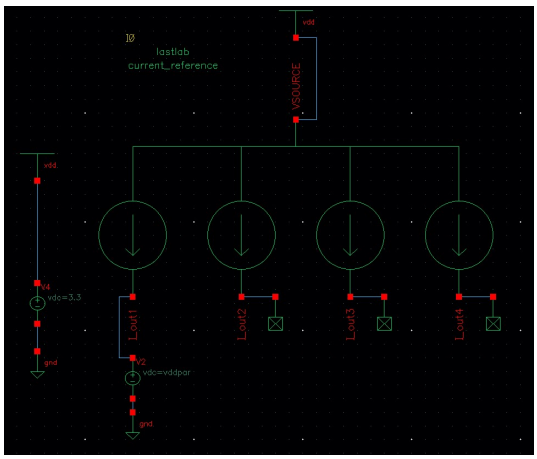


Figure 7: Testbench

In the testbench there's a voltage source ('vdc' from 'analogLib') that define 'vdd', which is a source with a DC voltage of 3.3V.
Because all outputs have the same response, it is also connected a 'noConn', from 'Basic', to the I_{out2}, I_{out3} and I_{out4}, allowing the analysis solely for one output and preventing the remain output nets of floating. Therefore, subsequently, is added a 'vdc' defined with the variable 'vddpar', which will be "sweeped".

– **DC Operating Point**

In order to confirm and ajust the parameters calculated in section 2.1, the first simulation is a DC Operating Point. Using the testbench 7, when choosing the DC analysis, by checking the box 'DC Operating Points', it's possible to get parameters that define the transistors, as shown in the figure below:

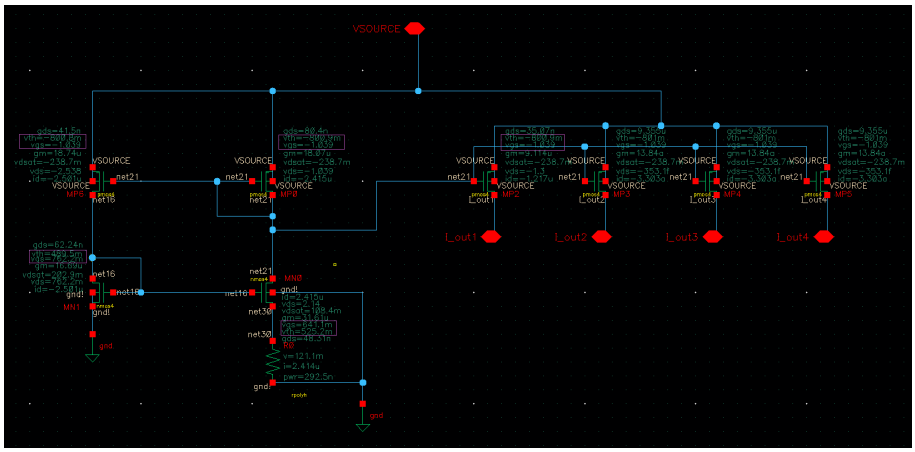


Figure 8: DC Operating Points

It's important to guarantee that $V_{OD} = (V_{GS} - V_{th}) = 0,2V$, as it is a requirement of this lab, yet it's possible to notice, in the figure above, that $(V_{GS} - V_t) \neq 0,2V$. Thus, the parameters must be adjusted. To achieve the desired V_{OD}, the value of R_S has to be modified. After observing this simulation resultant graph, shown in the figure below, it's possible to see that the input current is much above of the desired $4\mu A$ and the the output current is a bit above the desired $1\mu A$, thus, R_S must be increased, as bigger the resistance the smaller the current, for the same voltage.

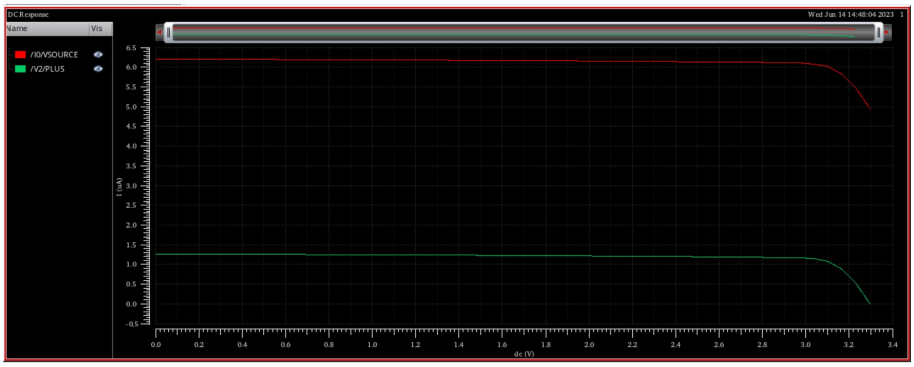


Figure 9: Input Current and Output Current for $R_S = 50k\Omega$, determined in 2.1

After a few trials, it is chosen the value $R_S = 55k\Omega$. This value allows, as expected, a output current closer to $1\mu A$, the input current for the symbol closer to $4\mu A$, like shown in the picture 10 and $V_{OD} \approx 0,2V$, as shown in the figure 11.

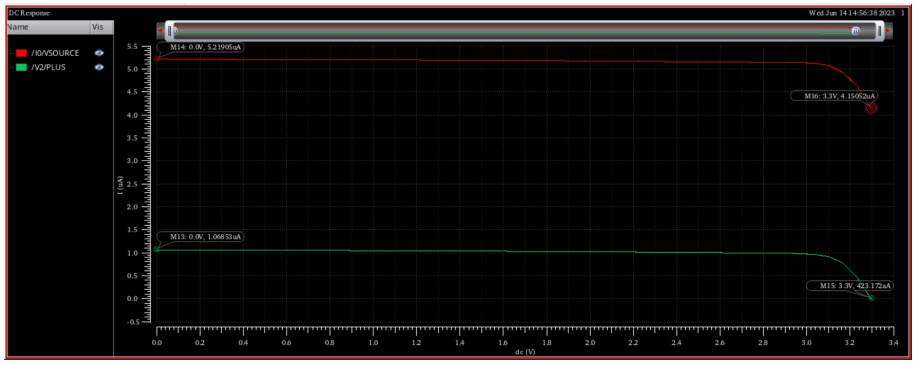


Figure 10: Input Current and Output Current for $R_S = 55k\Omega$

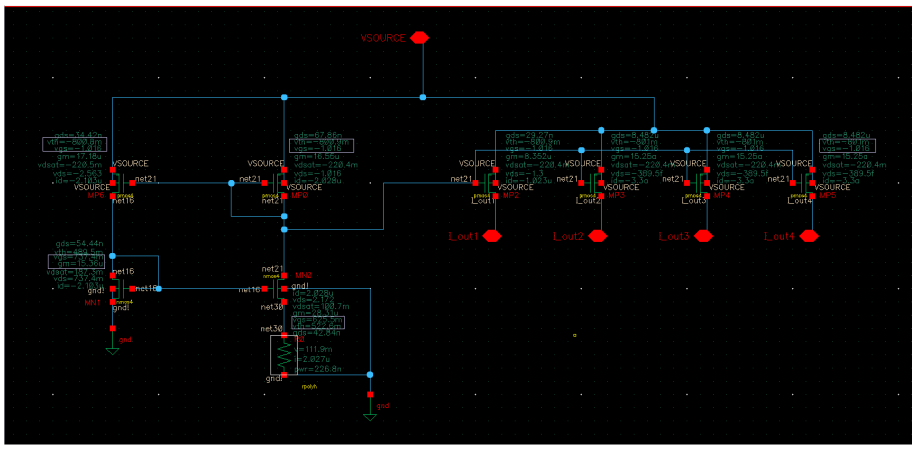


Figure 11: $V_{OD} \approx 0,2V$ para $R_S = 55k\Omega$

Throughout this analysis, it's used the resistor type is 'rpolyh' from the library 'PRIMLIB', however there are other types, such as 'rpoly1', 'rpoly2' and 'rnwell'.

Figure 12: 'rpoly1', 'rpoly2' and 'rnwell' from up to bottom, respectively

As shown in the picture, comparing with the simulation of the figure 10, the difference between resistor types it's imperceptible in this curves. To know more decide which is the best, a corner analysis must be performed.

3.1.2 Corner Analysis

This corner analysis allows the understanding of the behavior of the circuit with critical supply voltages, such as $3V$ and $3.6V$, each at $-40°C$ or $125°C$.
It was created the corner analysis:

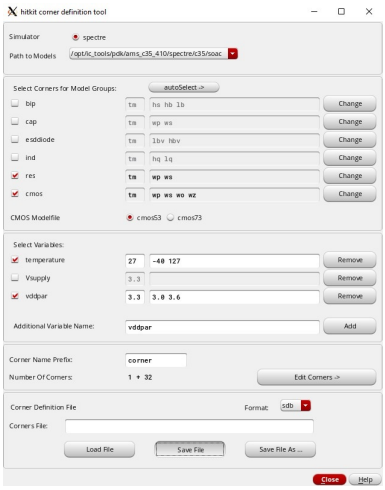
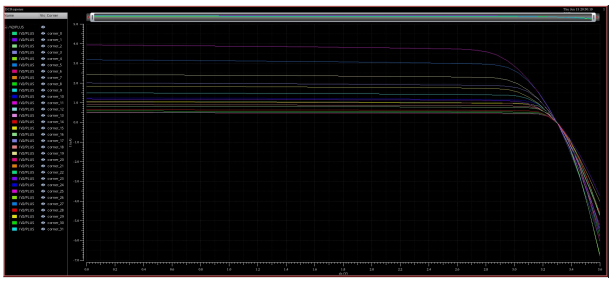


Figure 13: Corner Analysis "Programming"

After the simulation, it's possible to get the following corners:

Corner	cmos53_scs	res.scs	temperature	vddpar
corner_0	cmoswp	reswp	-40	3
corner_1	cmoswp	reswp	125	3
corner_2	cmoswp	reswp	-40	3.6
corner_3	cmoswp	reswp	125	3.6
corner_4	cmoswp	resws	-40	3
corner_5	cmoswp	resws	125	3
corner_6	cmoswp	resws	-40	3.6
corner_7	cmoswp	resws	125	3.6
corner_8	cmosws	reswp	-40	3
corner_9	cmosws	reswp	125	3
corner_10	cmosws	reswp	-40	3.6
corner_11	cmosws	reswp	125	3.6
corner_12	cmosws	resws	-40	3
corner_13	cmosws	resws	125	3
corner_14	cmosws	resws	-40	3.6
corner_15	cmosws	resws	125	3.6
corner_16	cmoswo	reswp	-40	3
corner_17	cmoswo	reswp	125	3
corner_18	cmoswo	reswp	-40	3.6
corner_19	cmoswo	reswp	125	3.6
corner_20	cmoswo	resws	-40	3
corner_21	cmoswo	resws	125	3
corner_22	cmoswo	resws	-40	3.6
corner_23	cmoswo	resws	125	3.6
corner_24	cmoswz	reswp	-40	3
corner_25	cmoswz	reswp	125	3
corner_26	cmoswz	reswp	-40	3.6
corner_27	cmoswz	reswp	125	3.6
corner_28	cmoswz	resws	-40	3
corner_29	cmoswz	resws	125	3
corner_30	cmoswz	resws	-40	3.6
corner_31	cmoswz	resws	125	3.6

(a) Corner Details



(b) Corner Curves

Figure 14: Corner Simulation

By this two images, it's possible to select the cases:

- Corner Simulation: $-40°C$ & 3V

Figure 15: Corner Curves

- Corner Simulation: $-40°C$ & 3.6V

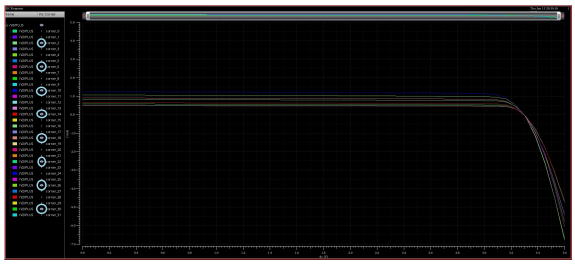


Figure 16: Corner Curves

- Corner Simulation: $125°C$ & 3V

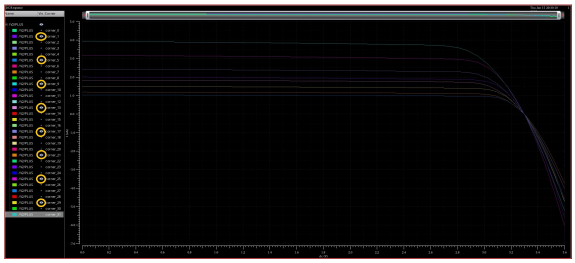


Figure 17: Corner Curves

- Corner Simulation: $125°C$ & 3.6V

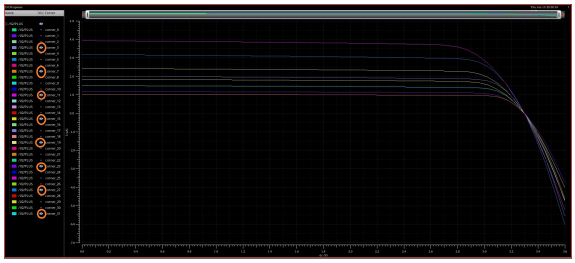


Figure 18: Corner Curves

- Corner Simulation for resistors 'rpoly1', 'rpoly2' and 'rnwell'
  Finally, as mentioned in the 'Schematic' section, there are other resistor types, and by performing a corner analysis it's possible to differentiate them, in order to choose the best one.

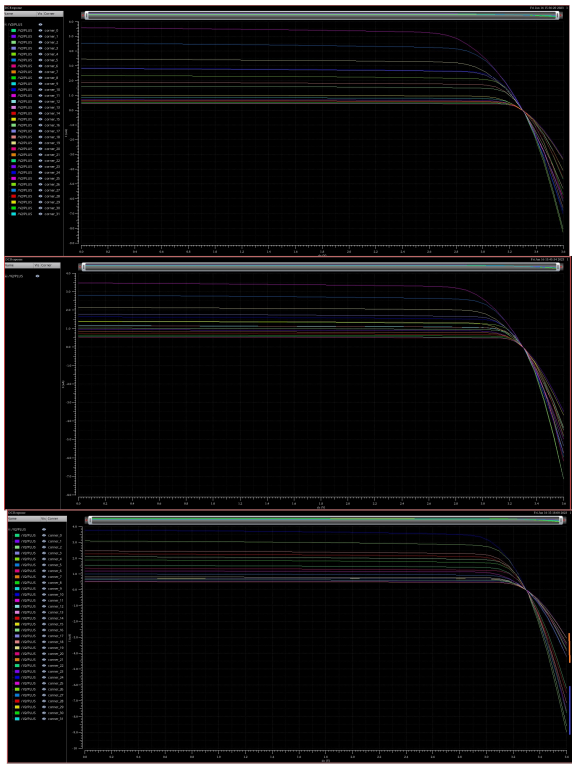


Figure 19: Corner Curves for 'rpoly1', 'rpoly2' and 'rnwell' from up to bottom, respectively

The resistor 'rpoly1' is immediately the odd one out, as the current values deviate a lot from the expected, as shown in figure 14. The resistors 'rpoly2' and 'rnwell' current values are very similar, however 'rnwell' is closer to the expected result for the output current, additionally, the 'rnwell' differentiates the temperatures $-40°C$ (denoted with blue stripe) and $125°C$ (denoted with orange stripe), which means its behavior with temperature is well composed. Thus, for the next section, as improvements are introduced, the resistor 'rnwell' it's the best complementary choice, in series, with the resistor 'rpolyh'.

3.1.3 PSRR

To study the PSRR (**P**ower **S**upply **R**ejection **R**atio) it is necessary to modify the testbench shown previously.

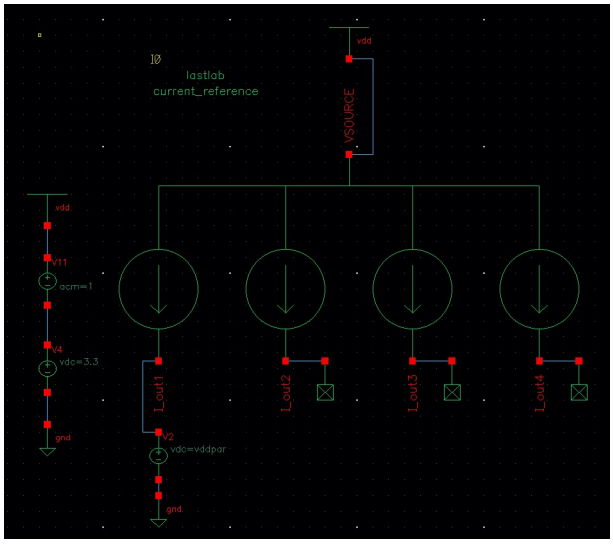


Figure 20: Modified Testbench

Comparing with the first testbench, used for 'DC Operating Points' simulation and for the 'Corners Analysis', the new testbench has a new 'vdc' source. This added source has 'AC magnitude = 1V' and it's meant to inject oscillations in the circuit.
In order to maintain the working region of the PMOS outputs, the 'vdc', connected with the first output, must have a value inferior to 2.8 V, thus it is chosen 1V. This voltage source, could also be a simple current mirror, whose NMOS's design is the same as the design in the third laboratory.
By performing a AC analysis, sweeping from 10Hz to 10MHz, it's possible to get the following curve:

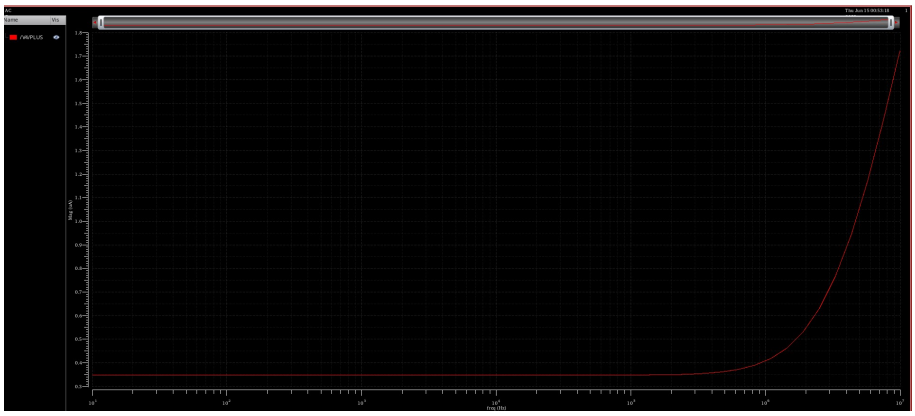


Figure 21: PSRR

3.2 Cascode Current Bias Generator

In order to improve the results obtained throughout section 3.1. Through the knowledge obtained in the last laboratory, it was verified that the cascode current mirror has a better performance, thus all the current mirrors are substituted with cascode current mirrors.

3.2.1 Schematic, Symbol and Simulation

`Note: The symbols and the testbenchs are all are maintained as the ones from the basic current bias generator, explored in section 3.1.`

- Schematic

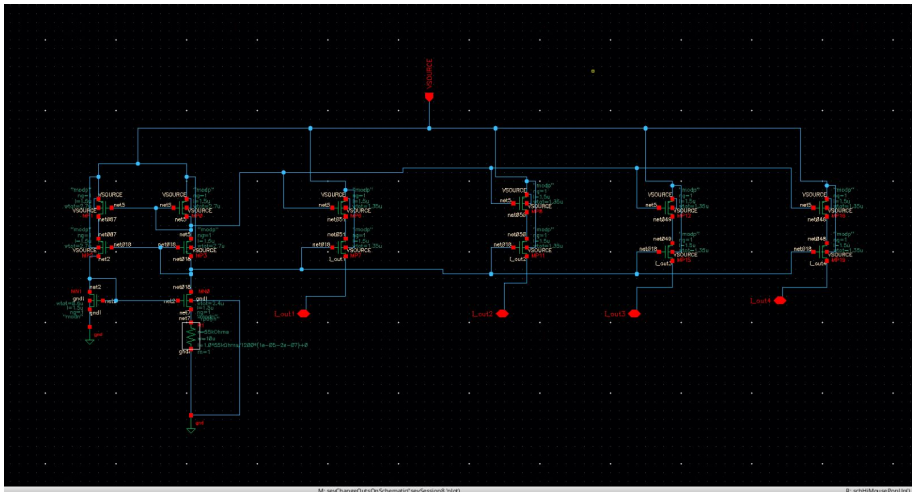


Figure 22: Schematic

- Simulation
  The first step is to guarantee that the two NMOS transistors are working in subtreshold region, which allows the saturation of the transistors with few *ampères* of current. To achieve it, the ratio $\frac{W}{L}$ has to increase, i.e. W has to increase. Thus, the ratio was modified until it was verified that V_{th} was bigger than V_{GS} by less than $100mV$. Then it's performed a DC Sweep to the output current, resulting in the curve below:

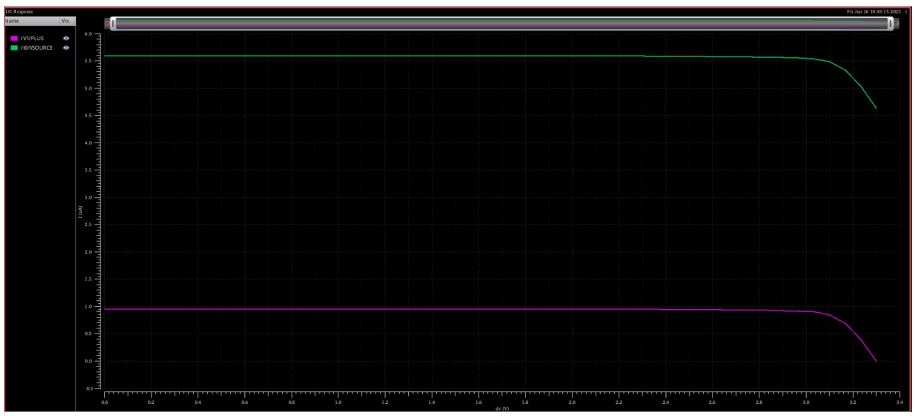


Figure 23: Input Current and Output Current Simulation

3.2.2 Corner Analysis

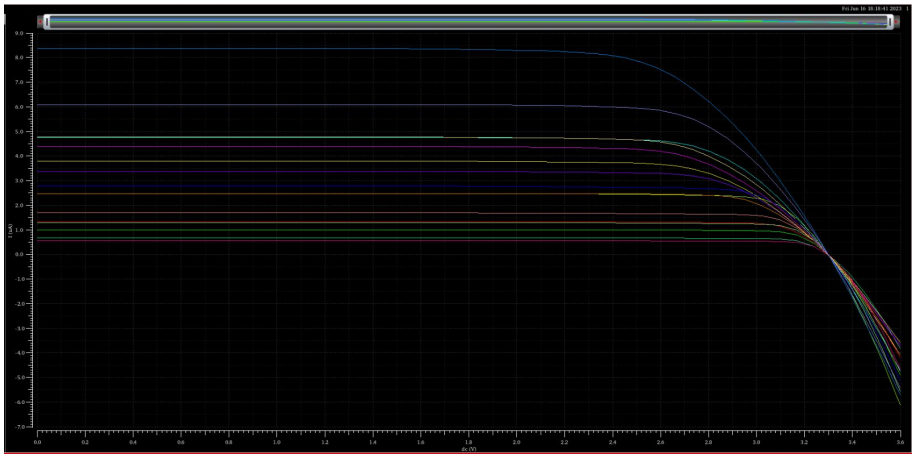


Figure 24: Corner Curves

As it's possible to observe in the graph, the response is unsatisfactory, when compared solely with the response obtained in figure 14. This response could be improved by an addition resistor in series with the 'rpoly', which is a solution discussed further.

3.2.3 PSRR

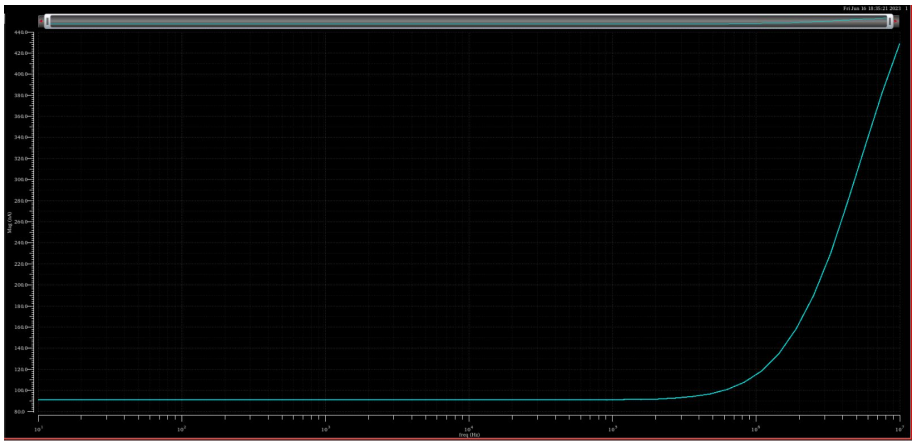


Figure 25: PSRR

The PSRR maintains the curve shape, however the currents values, displayed on the y-axis are lower than the expected, as this improved circuit should have a greater rejection than the basic circuit.

3.2.4 Unexplored improvements

In this section, it's presented unexplored improvements, i.e. improvements that weren't simulated.

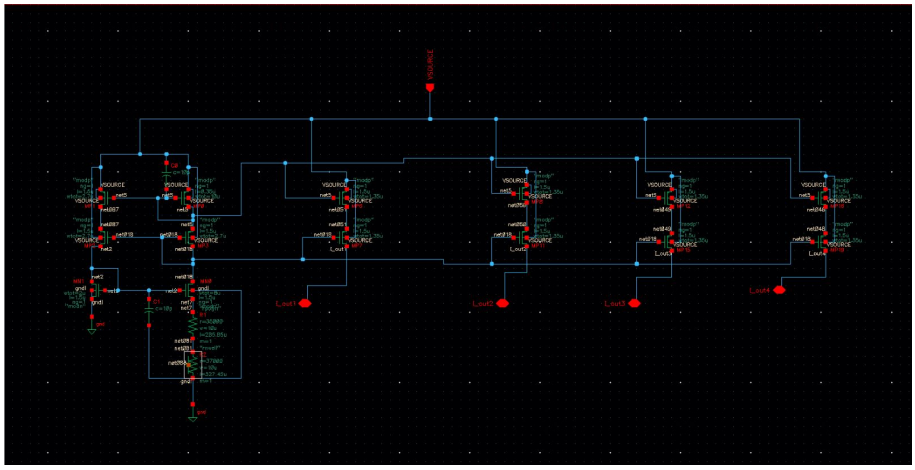


Figure 26: Unexplored Improvements Schematic

In the schematic above, it's added a capacitor and a 'rnwell' resistor in series with 'rpolyh'. Individually, the addition of capacitors would improve the start-up of the circuit, as it would be faster. The placement of the capacitors it's very strategic, because takes advantage of the transistors' current leakage. Because the current in a capacitor is given by the capacitance times the variation of voltage, current will start to flow, and, therefore, start-up the circuit; the addition of a resistor in series, in particular 'rnwell' because it's the best choice, among the resistor types tested in section 3.1.2, would improve the temperature behavior/response. As explored the resistor 'rnwell' has a favorable corner analysis, which, in series with 'rpolyh' would a circuit well-defined with temperature.

4 Conclusion

Initially, the basic current bias generator was studied determining the value of the resistance R_S necessary to have the desired output current. Different resistances from the library "PRIMLIB" were compared to determine which one revealed the best performance. The "rnwell" was the resistor that showed the best behaviour. Next the PSRR was studied, for the basic current bias generator higher frequency values led to less rejection of the oscillations created by the AC tension source. Thus, the signal suffers more variation for higher frequency.

The implementation of the cascode current bias generator led to less effect of the channel-length modulation, allowing a more stable output current than what is obtained for the basic current bias generator. The PSRR was also studied for this circuit, obtaining again less rejection of the oscillations of the AC voltage source when the frequency is higher, although in this case the noise created has a higher effect on the output current. However, the expected result for the cascode current bias generator would be less effect of the noise, so probably there was a problem on the performed simulation. Hence, the PSRR in the cascode current bias generator should be superior than on the simple current bias generator. The use of the cascode current bias generator should improve the circuit both when using the AC tension source and when not using it. When not using the AC tension the cascode current bias generator improved the circuit. When using it, the results obtained were not the expected.

5 Referências

[1] Behzad Razavi,"Design of Analog CMOS Integrated Circuits", International edition, p.378-379, p.401, 2001.

[2] "0.35µm CMOS C35 Process Parameters Document", p.11, p.12. Available in the course's *fénix* page.