TÉCNICO LISBOA

Mircroeletronics

4th LAB Report

Cascode Current Mirror Design

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Contents

1 Introduction

In the fourth laboratory of Microeletronics there are four main goals:

- Study the cascode current mirror (CCM);
- Study the low-voltage cascode current mirror circuit (LV-CCM);
- Compare the CCM with a simple current mirror and compare the LV-CCM with both CCM and CM;
- Analyse, experimentally, the operation with low-voltage and, afterwards, with power down added;

This lab report is divided in three main sections.
The first section addresses the theoretical preparation necessary for this lab. This part is achieved by analysing the cascode current mirror (CCM), as well as, analysing the low-voltage cascode current mirror (LV-CCM).

The second section approaches the simulations performed in the *Cadence virtuoso* software. This part is achieved by projecting the schematic and the symbol of the CCM and performing different simulations, such as the operation with low-voltage with and without power down added.
The final section it's a conclusion, intended to compare CCM with the simple CM (studied in the previous lab, LAB3), as well as, the LV-CCM with the CCM, and also, to compare the simulations results with the theoretical inferences and comment about the difficulties and the successes throughout this laboratory.

2 Theoretical Preparation

A current mirror should have low input impedance and high output impedance for proper functionality. Other desirable features of a current mirror include wide input and output current swings, high linearity, accurate current copy, and low standby power dissipation. (Ghibaudo, 2014)

2.1 Cascode Current Mirror

In the previous lab report, it was studied the basic current mirror, in which it was analysed the effect of the channel-length modulation, concluding that:

$$I_{OUT} = I_{REF} \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}} \tag{1}$$

However, the channel-length modulation effect produces a significant error in copying currents, especially with minimum-length transistors. As a consequence, there's the problem of V_{DS} of both transistors not being exactly the same value.

To suppress this effect, we can force V_{DS2} (Q_2 transistor) to be constant and equal to V_{DS1} (Q_1 transistor). For this purpose, it's projected a cascode current mirror, shown in the figure 1.

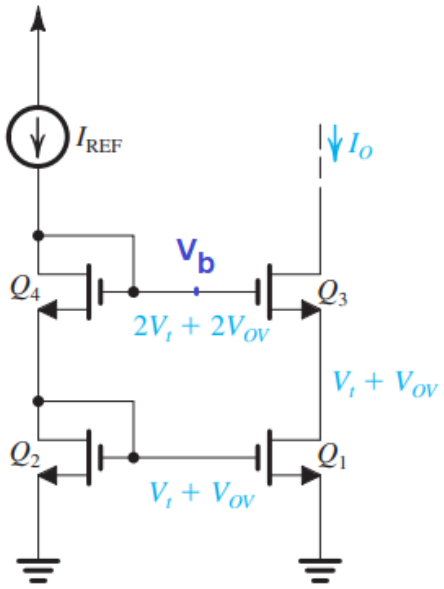


Figure 1: Cascode Current Mirror

To ensure $V_{DS2} = V_{DS1}$, we must generate V_b, which is the gate voltage of Q_4 and Q_3.

$$V_b = V_{GS3} + V_{DS2} \leftrightarrow V_b - V_{GS3} = V_{DS2} \tag{2}$$

and, since $V_{DS2} = V_{DS1}$,

$$V_b - V_{GS3} = V_{DS1} = V_{GS1} \implies V_b = V_{GS1} + V_{GS3} \tag{3}$$

in conclusion, to get $V_{DS2} = V_{DS1}$, it must be applied $V_b = V_{GS1} + V_{GS3}$.
Through the figure, it's noted two main ideas:

First, it's observed that Q_1 is operating with a drain-to-source voltage $V_t + V_{OD}$, which is V_t volts greater than it needs to operate in saturation.

Second, it's that the minimum voltage allowed at the output is $V_t + 2V_{OD}$. This is because the gate of Q_3 is at $2V_{GS} = 2V_t + 2V_{OV}$. In other words, the cascode mirror reduces the voltage swing by V_t volts, this is because the voltage at the gate of Q_3 is $2V_t + 2V_{OV}$, the minimum voltage permitted at the output (while Q_3 remains saturated) is $V_t + 2V_{OD}$, hence the extra V_t. Thus, the minimum voltage required across the output of the cascode mirror limits the signal swing at the output of the mirror. (Sedra, Smith, 2015)

Therefore, wide-swing/low-voltage cascode mirror shall be studied in the next subsection.

2.2 Wide-Swing/Low-Voltage Cascode Mirror

A low voltage cascode current mirror (LV-CCM) is one of the efficient and simple current mirrors. It provides low input impedance and high output impedance with reduced power supply requirement.

A modification of the CCM that results in the reduction of the minimum output voltage to V_{OD}, results in the LV-CCM, whose circuit requires a bias voltage V_{BIAS}, like show in the figure below.

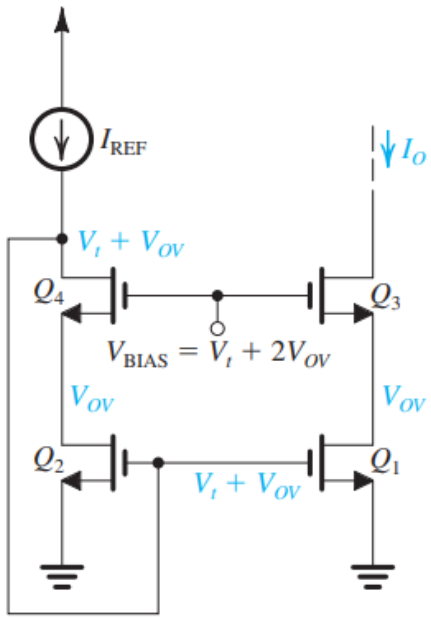


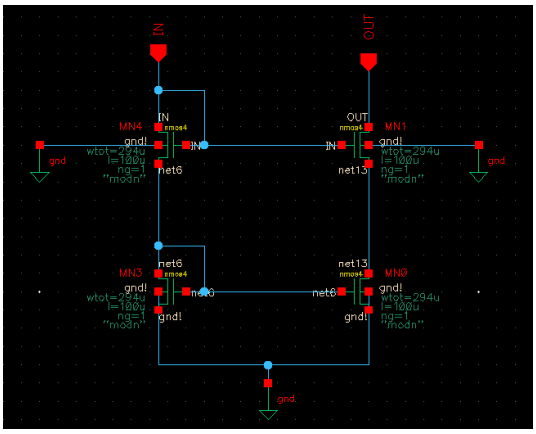
Figure 2: Low-Voltage Cascode Current Mirror

The observations above lead us to the conclusion that to permit the output voltage at the drain of Q_3 to swing as low as $2V_{OD}$, we must lower the voltage at the gate of Q_3 from $2V_t+2V_{OV}$ to $V_t + 2V_{OD}$. This is exactly what is done in the modified mirror circuit in 2. The gate of Q_3 is now connected to a bias voltage, thus the output voltage can go down to $2V_{OD}$ with Q_3 still in saturation. Also, the voltage at the drain of Q_1 is now V_{OD} and thus Q_1 is operating at the edge of saturation, as well as, Q_2. (Sedra, Smith, 2015)

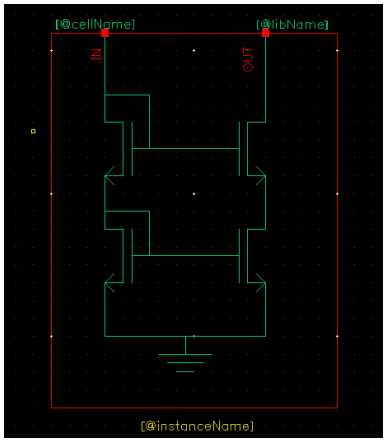
3 Cadence virtuoso

3.1 Schematic and Symbol

Firstly the schematic of the CCM was designed, using four NMOS transistors from the library "PRIMLIB" ("nmos4") with the same properties as the ones used in the last laboratory (length=100/*mum*, width=294/*mum*), gnd supply cells from library "analogLib" and two pins (one input and one output). Figure 3a shows the connections made to create this schematic. Secondly, the symbol of the CCM was designed has shown in figure 3b.



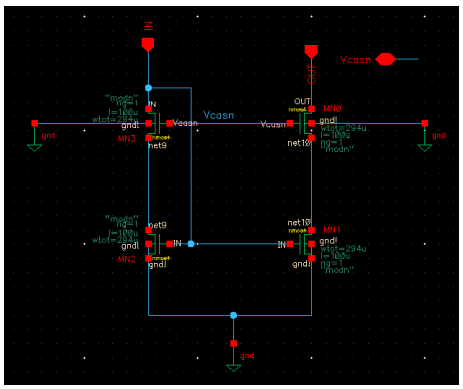
(a) Schematic of Cascode Current Mirror



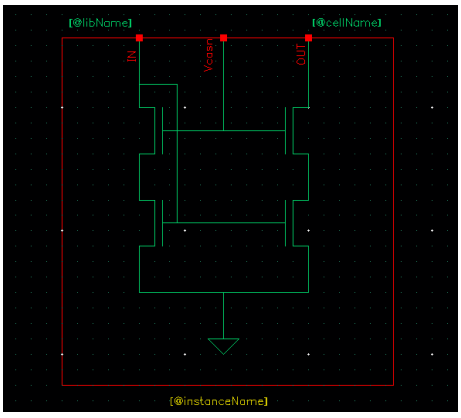
(b) Symbol of Cascode Current Mirror

Figure 3

For the LV-CCM, the same cells were use adding an input-output pin, and the connections were performed as shown in figure 4a. Then, the symbol was also created (figure 4b). The cells were created on the library "LAB4" and are named "cascode_current_mirror" and "cascode_current_mirror_lowvoltage"



(a) Schematic of low voltage Cascode Current Mirror



(b) Symbol of low voltage Cascode Current Mirror

Figure 4

3.2 Testbenchs and Simulations

The simulation schematics (testebenchs) were created on library "LAB4_sim" and have the same name as the schematics on library "LAB4". For CCM, a voltage source ("vdc"), current source ("idc"), "vdd" and "gnd" from library "analogLib" were added to the symbol of CCM previously created and connected as shown in figure 5.

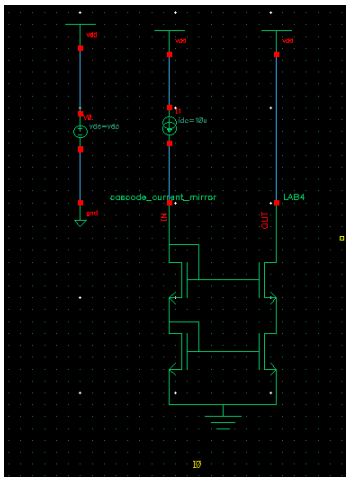


Figure 5: Schematic for simulation of the cascode current mirror

For LV-CCM a similar simulation, showed in the figure below, was created with the exception of an additional voltage source and gnd added to the input-output pin named "Vcasn".

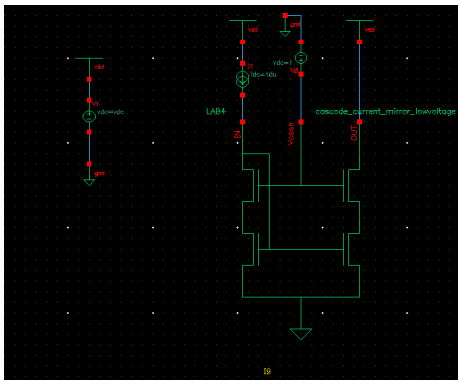


Figure 6: Schematic for simulation of the low voltage cascode current mirror

3.2.1 CCM simulation

For CCM, the plot obtained of the current in the output in function of the voltage applied to the output is the one showed bellow. It is possible to observe that the effect of channel length modulation is basically nonexistent, since the curve maintains approximately constant once it reaches the same current as the input.

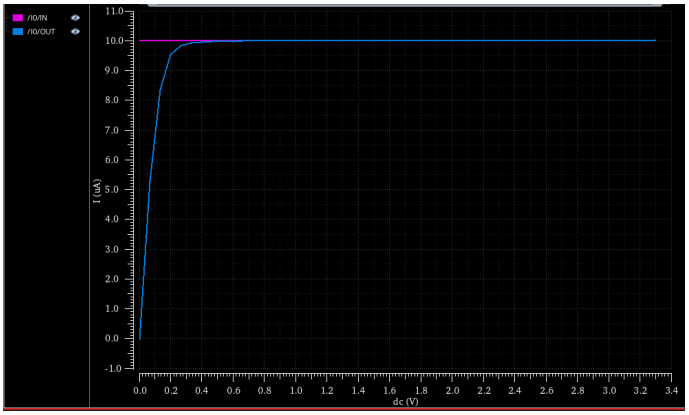


Figure 7: DC sweep for CCM

This occurs since two NMOS transistors are added to the simple current mirror, this transistors limit the tension, reducing the effect of channel length modulation. The upper-right NMOS limits V_D of the down transistor, leading to equal V_{DS} in the two down transistors. So, the output current becomes similar to the current in the input after reaching saturation and the same value of V_{DS}. Thus, CCM is very proximate to an ideal current mirror, since the output and input current become approximately constant after reaching saturation. Contrarily, the simple current mirror simulated on the last laboratory does not exhibit this behavior, since the output current would stay approximately equal to the input one until it reaches an value of voltage that leads to an increase in the output current as shown in figure 8. This occurs due to channel length modulation.

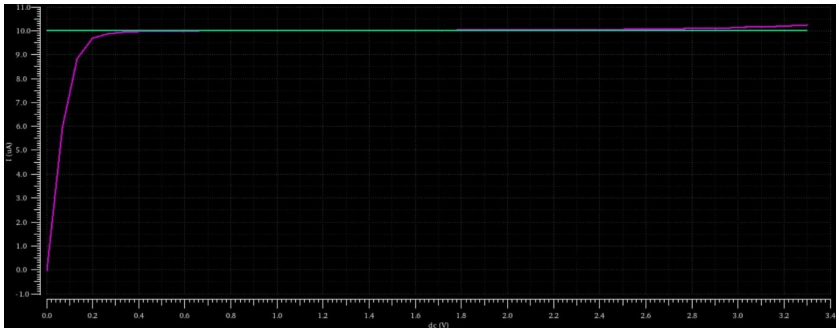


Figure 8: DC sweep for simple current mirror

It's also important to notice that, the minimum V_D for the upper left transistor is $2V_{OD}+2V_t$ in CCM and $V_{OD}+V_t$ for the simple CM. As a result, CCM's required voltage is two times the one used in the simple current mirror, which is a problem.

3.2.2 Low-voltage CCM simulation

In order to try to solve the problem above, after projecting the LV- CCM, it's perfomed a simulation, obtaining the plot shown on figure 9.

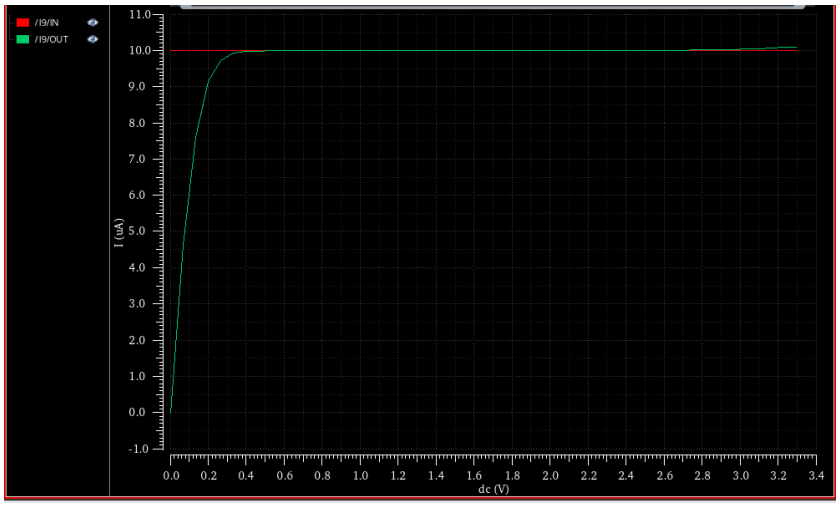


Figure 9: DC sweep for LV-CCM

In this plot it's possible to observe that the LV-CCM curve is slower than the CCM curve. For example, for 0.2V, in LV-CCM is approximately $9.0\mu A$ and in CCM is approximately $9.7\mu A$. At the end, it's also possible to observe that the LV-CCM's slope, approximately $10.1\mu A$, is smaller that the CCM's slope, approximately $10.8\mu A$.

The schematic of the LV-CCM is similar to the CCM, with some exceptions namely the connection between the drain of the upper left NMOS to the gates of the down NMOS, instead of the two connections drain-gate present in the CCM. This connection allows the LV-CCM to work with a smaller voltage, since it polarizes the down transistor with V_{DD} instead of $V_{DD} - V_t$. Thus, this current mirror needs the same voltage as the simple current mirror. This current mirror requires an extra voltage, which needs to lead to the saturation of the inferior transistors, so this tension must have a value that satisfies $V_{casn} \geq V_t + 2V_{OD}$, since the value of V_{OD}=200mV and $V_t \approx 600mV$ (obtained on cadence) the value of V_{casn} is, approximately, 1V.

Thus, this circuit has the advantage of requiring a lower voltage than a CCM to work properly and has a saturation zone similar to the simple current mirror. The disadvantage is the need of a new voltage source and it suffers slightly more from the effect of channel length modulation then CCM. Nonetheless, it still suffers less from channel length modulation then the simple current mirror, working as an ideal current mirror that requires less voltage to work then CCM.

3.2.3 Power Down

- **Schematic**
  The circuit's current may be cut when it's not necessary to use the circuit. Thus, in other to turn off or power down the circuit, it's used two transistors as switches, one on the top connected to the drain of the upper-left transistor and the other on the bottom connected between the transistors gates and ground . However, there are three questions:

  – 1. why do we need two transistors as switches?

  – 2. what MOS type should be chosen?

  – 3. can we guarantee the input signal of this transistors is '0' or '1'?

  For the **first question**, in order to "cut the supply" to this circuit, is important to put a switch that interrupts the flowing of the I_{REF} current from the upper-right transistor. However, this transistor alone isn't enough, because the right side of the circuit won't be completely shut down, having still some voltage across ($\approx V_t$). To solve this problem, it's added another switch on the bottom, to open the ground and guarantee that the circuit has no voltage across

  For the **second question**, is considered the body effect, which is a phenomenon that occurs in MOSFETs when the voltage between the source and the body is different from zero. This effect it's caused by the depletion region that forms around the body of the MOSFET when a voltage is applied to the source. The depletion region changes the threshold voltage of the MOSFET, which in turn affects its performance.

  In an NMOS transistor, the body effect causes the threshold voltage to increase as the source-to-body voltage increases.
  In a PMOS transistor, the body effect causes the threshold voltage to decrease as the source-to-body voltage increases.
  This means that the PMOS transistor is less sensitive to changes in the source-to-body voltage than the NMOS transistor. In other words, the PMOS transistor has a smaller body effect than the NMOS transistor. Thus, considering the body effect, PMOS should be the transistor type connected to the bulk of upper-left transistor. For the lower transistor, since it's connected to two other NMOS transistors, it's chosen to be a NMOS transistor as well, as shown in the figure below, (10).

  Finally, for the **third question**, in order to guarantee that the signal received by the added transistors is '0' or '1', it's added two NOT-gates, studied in the 2nd lab report. By connecting the first NOT-gate to the ground (GND), the analog signal received is just an approximation of zero, but this gate will "reset" the signal, turning it into '1', and this '1' will be connected to the chosen NMOS transistor. In serires, there is another NOT-gate, which will transform the previous '1' signal into a '0' signal, and this '0' will be connected to the chosen PMOS transistor, as shown in the figure below, as well. The main purpose to do this is to guarantee that the erratic changes in logic state don´t affect the actual signal going to the input of the switch. It is important to know that this switch implementations can be done in various ways: by using two nmos transistors, two pmos transistors, or be using one pmos and one nmos. In conclusion, the choice of which

combinations of transistor's types we want to use will depend on the consequences of the body effect in our circuit, affecting also the placement of the inverters.

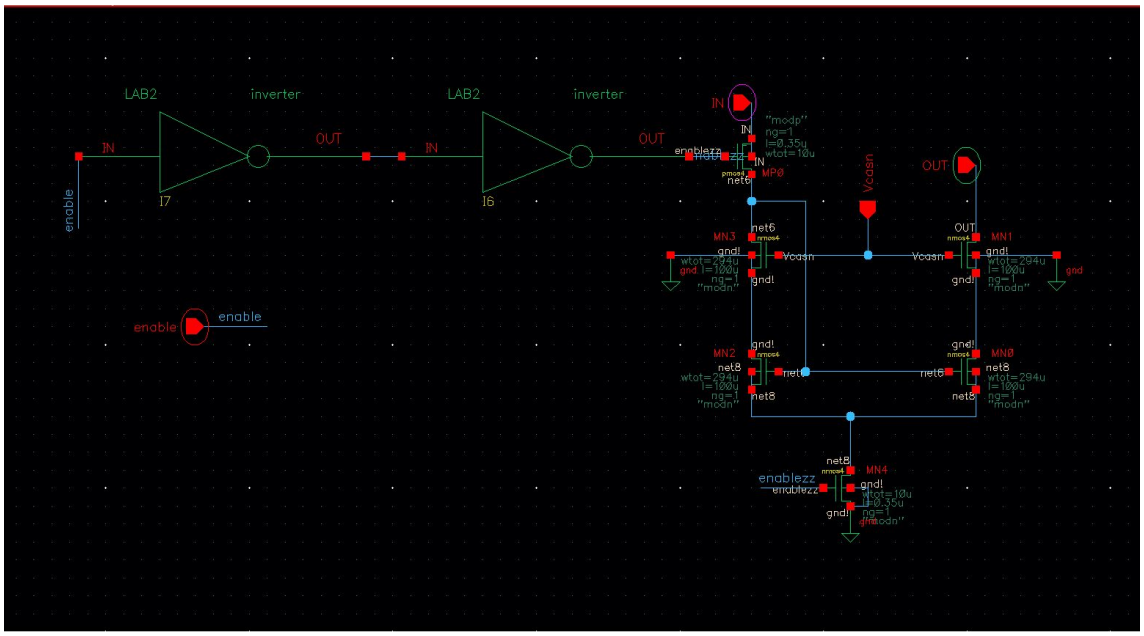


Figure 10: Turn-OFF/Power Down Circuit

- **Testbench**
  After creating a general symbol, it was projected the testbench, shown in the figure below.

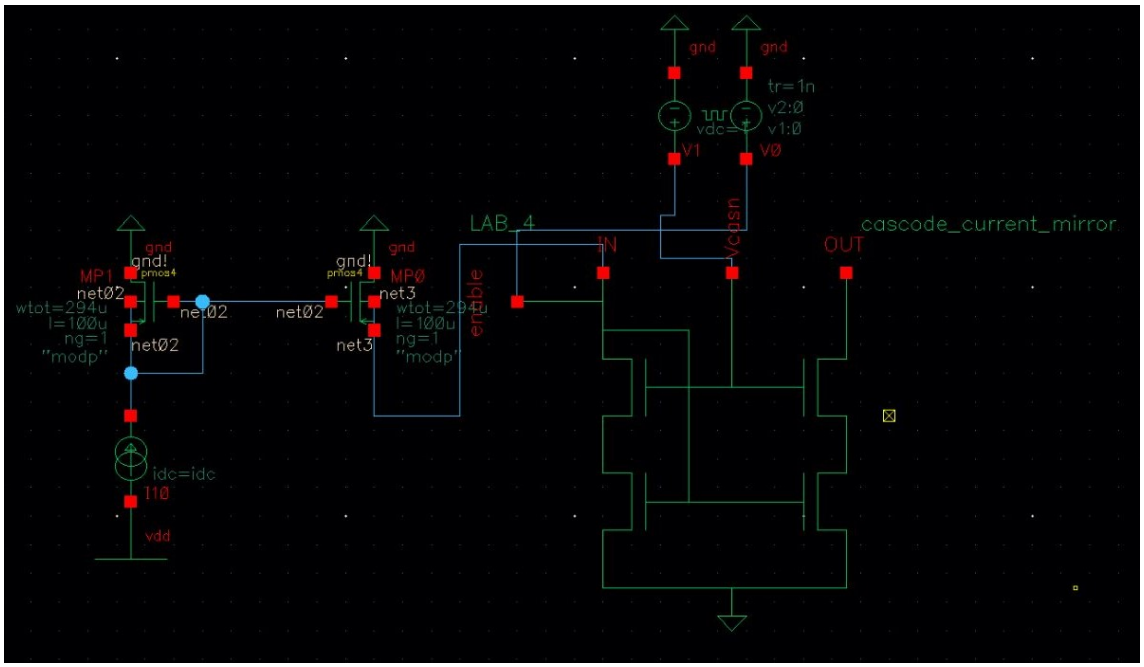


Figure 11: Turn-OFF/Power Down Circuit

The enable input is a pulse that controls whether the circuit is in power on or power down mode. When the pulse is in '0', the circuit is in power down mode. When is in '1' it's in power on. It's also possible to observe that a **PMOS current mirror** is connected to the input-pin of the symbol. However, a question remains: why is it used a PMOS current mirror instead of a NMOS current mirror? The only structure difference between PMOS mirroring and NMOS mirroring is the placement of I_{REF}, to source current or sink current, i.e. sources current from V_{DD} (positive supply) or sinks current to GND (ground), respectively. However, this only difference is the reason why the PMOS current mirror is the best choice. By having the I_{REF}, an ideal current source, sinking to GND, it prevents a direct connection to the PMOS-switch added to the circuit in the schematic 10, which also means that the PMOS-switch is connected to the current mirror instead. This is a must, as the ideal current source is continuously supplying current. Therefore, the current mirror guarantees that there is no current flowing into the PMOS-switch when the circuit is in power down mode.

- **Simulation** To understand if the circuit is powering down or turning off, it's performed a *transient*, in which it's possible to observe that the circuit goes to zero, hence it's turned off.

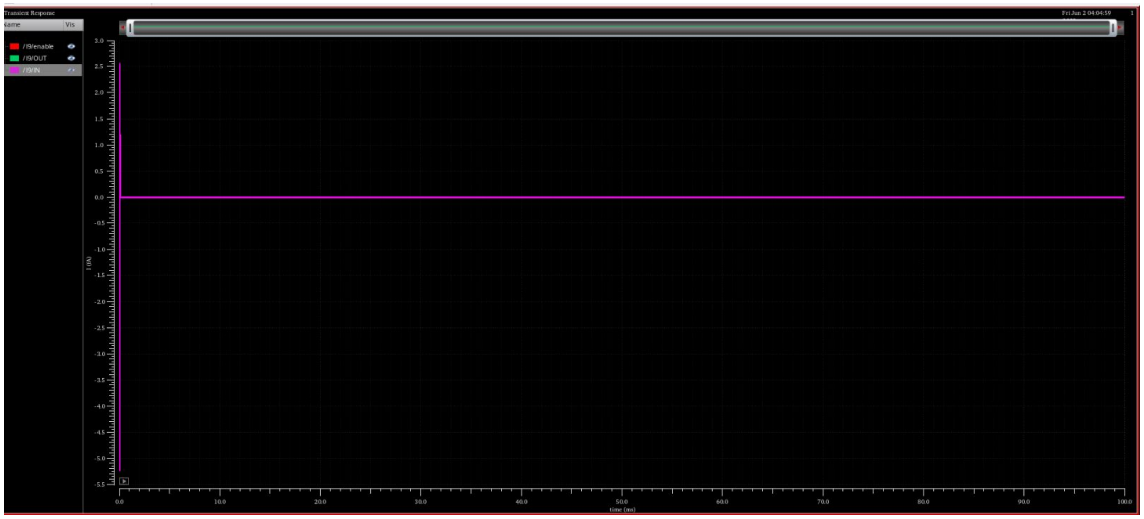


Figure 12: Transient of Turn-OFF/Power Down Circuit

NOTE: In the 'Conclusion' the group discusses more about this transient.

4 Conclusion

Throughout this laboratory, it's intended to study the cascode current mirror (CCM) and the low-voltage cascode current mirror circuit (LV-CCM), as well as, understand the power down mode, which consists in turning off the circuit.

This lab report is divided in three main sections.

In the first section, it was addressed the theoretical preparation for this lab. This part was attained with the analysis of the cascode current mirror (CCM), as well as, analysis the low-voltage cascode current mirror.

In the second section, it was performed the simulations in *Cadence virtuoso* software.
In this section, throughout the power down study, the group reached a stalemate, as the simulation seemed unexpected. In the figure 12, the transition until zero seems very abrupt, as it goes almost immediately to zero, which is very unexpected for the group. In addition, it was only possible to observe the power down mode, i.e. it wasn't possible to observed the power up mode.

Finally, the two sections conclude into a comparison between the CCM and the simple current mirror (studied in the previous lab, LAB3) and between the LV-CCM and both CCM and CM:

- CCM vs. CM In CCM, the channel-length modulation effect is negligible, which makes it an ideal CM. In this case, the output current perfectly follows the reference current, however, in order to the transistors to operate, it's required a supply voltage two times higher than the simple CM. As a consequence the saturation region of CCM is smaller than the CM, as the overdrive voltage is bigger.
  In the simple CM, the modulation effect of the length of the channel is considered. Although, within the range of the saturation zone, there's a voltage whose output current corresponds to the reference current, through LAB3, it was possible to observe that, after exceeding this voltage value, the current continues to increase. This verifies the presence of the modulation effect of the channel length concluding that the simple CM isn't ideal.

- LV-CCM vs. CCM and LV-CCM vs. CM The LV-CCM it's presented to rectify CCM's "double-voltage problem". This solution has the advantage of using the same supply voltage as the transistors of the simple current mirror. However, in one hand, the channel-length modulation effect has to be considered and it's found to be superior to the channel-length modulation effect in the CCM. In another hand, the effect is lower than the one observed in the simulation of the simple current mirror.

Ultimately, after weighing the attributes of each current mirror circuit, the low voltage cascade current mirror is determined to be the best current mirror circuit.

In general, throughout this lab report, the group was able to achieve the settled goals, however had some difficulties on the powerdown unit, as explained above. The group will try to improve, in order to fulfill a better understanding of *Candece virtuoso* simulations.

5 Referências

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[2] R. J. Baker, "CMOS: Circuit Design, Layout, and Simulation", 3rd edition, 2010.

[3] Adel S. Sedra, Kenneth C. Smith, "Microelectronic Circuits", 7th edition, p.1026, p.559-560, 2015.

[4] Gerard Ghibaudo, "Bandwidth Extension of High Compliance Current Mirror by Using Compensation Methods", 2014. Visitado a 31/05/2023 em: `https://www.researchgate.net`