KIIT UNIVERSITY, BHUBANESWAR

SPRING MID SEMESTER EXAMINATION-2014

DIGITAL ELECTRONIC CIRCUITS [EC- 402]

Full Marks: 25 **Duration: 2Hrs**

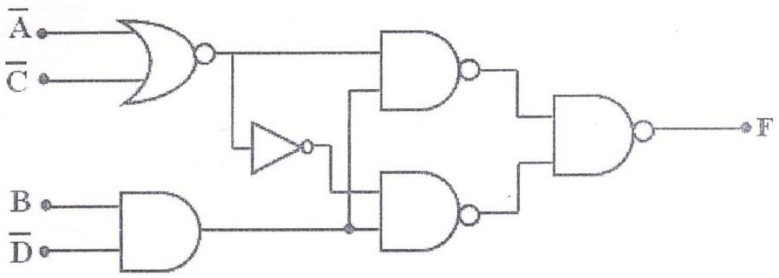
Answer any FIVE questions including question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

(1) a) 'XOR and XNOR gates can be used as a buffer as well as an inverter', Justify. [1x5]
b) Perform following arithmetic: (i) BCD addition (895+648),
(ii)(**-13**) **- (-6**) using 2's complement method.
c) Show that, $\mathbf{V.W + \overline{W}.X + X.Y.Z.V = \overline{W}.X + V.W}$, where V,W,X,Yand Z are Boolean variables.
d) What is the difference between active LOW and active HIGH terminals?
e) 'XS-3 codes are sequential & self-complementing but not cyclic', Justify.

(2) Obtain the minimized expression for the following 4-variable Boolean expression using K-map method and implement the minimized expression using **only NAND gates.** [5]
$$\mathbf{F(P,Q,R,S) = \Pi M(9,10,12,15) \cdot d(1,2,4,7)}$$

(3) a) What is the difference between Ripple carry adder and Look- ahead carry adder explain in brief and draw the circuit diagram of 3-bit Look-ahead carry generator. [4]
b) What is 'BCD to Seven Segment Decoder'? [1]

(4) a) Simplify the given logic circuit and implement the simplified expression using **only NOR gates**. [4]

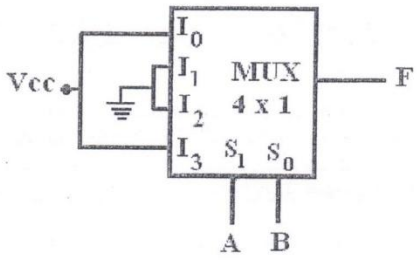


b) Encode 4-bit data word '1000' into a 7-bit even-parity Hamming code. [1]

(5) a) What is Decoder?.Explain it with a block diagram and implement the Full-Subtractor circuit using a **3-8 decoder having active-LOW output lines** and **2-input AND** gates. [4]

b) Determine the decimal value of the binary string '110011' in [1]
(i) Sign-Magnitude form,
(ii) Sign-1's Complement form,
(iii) Sign-2's Complement form,
(iv) Unsigned binary number

(6) a) Identify the Boolean function **F (A, B)** implemented with 4x1 MUX and then implement the identified Boolean function **F (A, B)** using **minimum number of NOR gates only.** [4]



b) Design a 8x1 MUX using two 4x1 MUX and one 2x1 MUX. [1]