KiiT

EEE

IV-B.Tech (Regular & Back)
DEC EC 401
(CSE, IT, E&EE, E&TC)

FOURTH SEMESTER EXAMINATION-2010

DIGITAL ELECTRONIC CIRCUITS

[EC 401]

Full Marks: 70 Time: 3 Hours

Answer any SIX questions including Question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. a) What is the difference between a latch and a flip flop? [2
   b) What is race-around condition? [2
   c) What is a priority encoder? [2
   d) Define fan in and fan out. [2
   e) Realise the gate diagram for the given equation – [2
   $f = \Sigma (0, 1, 2, 3, 8, 9, 10, 11) + d(4, 5, 6, 7, 15)$
   f) Differentiate between combinational and sequential logic circuits with examples. [2
   g) $(AD)_{16} - (BE)_{16} = ?$: use 1's complement method. [2
   h) $(101011011)_2) = (?)_{16}$. [1
   i) What is tristate inverter? [1
   j) Draw the truth table and block diagram of a 2:1 Multiplexer. [2
   k) Write the Truth table & Excitation table of T flip flop. [2

2. a) Design a BCD to 7 segment display decoder for common cathode connection. [5

b) $f(A, B, C) = \sum m\ (0, 3, 5, 7)$ realize the expression using minimum number of 2×1 MUX and minimum number of NOR Gate. [5

3. a) Design a BCD adder for addition of two 4 bit numbers. [5

b) Design a 2 bit ripple counter using T flip flop. [5

4. a) Design a 4 bit asynchronous UP/DOWN counter using J-K flip flop. [5

b) $f(A, B, C) = \sum m\ (0, 1, 3, 5, 7)$ simplify the expression using K-map and realize it using minimum number of NAND gate. [5

5. a) Design a 3 bit high priority Decimal to Binary Encoder. [5

b) Design a parallel in serial out shift register using D flip flops. [5

6. a) Design a JK flip flop using D flip flop, 2:1 MUX and a NOT Gate. [5

b) Implement the given expression using 8:1 Multiplexer– [5

$f(A, B, C, D) = \sum\ (0, 1, 3, 4, 8, 9, 15)$

7. a) Design a synchronous mod-10 counter using T flip flop. [5

b) Design a full subtractor using minimum no. of 2 × 4 decoder. [5

8. Write short notes on <u>any four (4)</u> from the following – [2.5 × 4

a) TTL

b) A stable multivibrator design using IC 555

c) Successive Approximation type ADC

d) Comparison between different types of RAM and ROM.

e) 2 bit parity generator and checker circuit

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