SPRING MID SEMESTER EXAMINATION-2020

COMPUTER ORGANIZATION & ARCHITECTURE(COA)

[CS-2006]

Full Marks: 20 **Time: 1.5 Hours**

Answer any four questions including question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only

[1X5]

Q1. Write short answers or do as directed.

a) What is Von Neumann architecture? How does it differ from Harvard architecture?

b) The content of register R1 is 10100110. What will be the decimal value after execution of the following individual instructions? Assume the number is represented in 2's complement format.

(i) LShiftL #2, R1

(ii) AShiftR #2, R1

c) ADD takes 1 clock cycle and MULT takes 3 clock cycles. If a program consists of 20 ADD and 10 MULT instructions, and clock rate is 1GHz, what is the average CPI and the execution time?

d) Consider a computer that has a byte-addressable memory organized in 32-bit words. A program reads ASCII characters entered at a keyboard and stores them in successive byte locations, starting at location 5000. Show the contents (in hexa) of the two memory words at locations 5000 and 5004 after the name "Disney" has been entered. Solve this problem for both big-endian and little-endian scheme. The ASCII values: D=44H, i=69, s=73H, n=6EH, e=65H, y=79H

e) Why is the WFMC needed in control step.

Q2. a) What do you mean by register transfer notation (RTN) and straight-line-sequencing? Consider a task of adding a list of n numbers, draw the program outline for the above task. Assume that each word takes 4 bytes, machine is byte addressable and the starting address is 1000. **[2.5]**

b) Suppose that a stack runs from location 2000 (BOTTOM) to no further than location 4000 (TOP) and each stack word consumes 4 bytes and machine is byte addressable. The stack pointer is loaded initially with the address value 1996. Write a routine for both PUSH and POP operation for a machine that does not allow auto increment and decrement mode. **[2.5]**

Q3. a) Explain the basic performance parameter equation for an application program. Discuss the functionality of two data transfer instructions and two data manipulation instructions with examples. **[2.5]**

b) Let each memory word consumes 4 bytes and machine is byte addressable. The memory stores numbers from 1 to 50 starting from memory location 1000. The register R2 and R3 contain value 10 and 20 respectively. After performing the following operations, find out the content of Register R3 **[2.5]**

(i) Move #1000, R1
(ii) Add 20(R1), R2
(iii) Sub (R1)+, R2
(iv) Add R2, R3

Q4. a) What is branch target address? Explain the control steps for conditional and unconditional branch instruction. **[2.5]**

b) Write the assembly code to evaluate the following arithmetic expression: **[2.5]**

$$X = A + (B - C) * D$$

i) Using a stack organized computer with zero-address operation instructions.
ii) Using an accumulator type computer with one address instructions.

Q5. a) Draw the schematic diagram of the architecture of a three-bus organization of the Datapath inside a processor. Explain the function of each component. **[2.5]**

b) Write the sequence of control steps for the instruction ADD (R1)-, R2 for single bus CPU organization. **[2.5]**

Q6. a) How control signals are generated in a computer? Explain with neat diagram the working of each unit of Hardwired control organization. **[2.5]**

b) What is the advantage and disadvantage of microprogrammed control over hardwired control approach? Explain the organization of the control unit to allow conditional branching in the microprogram. **[2.5]**