**KIIT, Deemed to be University**
**School of Electronics Engineering**
**Digital System Design Laboratory [EC 29005]**

# EXPERIMENT - 2

## Aim:

Design and Simulation of Full Adder circuit using Verilog HDL.

Hardware implementation of Full Adder circuit using logic gates.

## Component/Software Used:

| Component/Software | Specification |
|---|---|
| ICs | 7408, 7432, 7486 |
| Bread Board, Power supply, LEDs, Resistors,Switches, Connecting wires | As per requirement |
| Software(s) Used | Vivado 2016.1 |

## Theory:

### Full adder:

A full adder is a combinational circuit that forms the arithmetic sum of three bits. It consists of three inputs and two outputs. Two of the input variables, denoted by **A** and **B**, represent the two significant bits to be added. The third input $\mathbf{C_{in}}$ represents the carry from the previous lower significant position. Two outputs are required because the arithmetic sum of three binary digits ranges in value from 0 to 3, and binary representation of 2 or 3 needs two bits. The two outputs are designated by **Sum** and $\mathbf{C_{out}}$ for output carry.

When all input bits are 0, the output is 0. The Sum output is equal to 1 when only one input is equal to 1 or when all three inputs are equal to 1. The $\mathbf{C_{out}}$ output has a carry of 1 if two or three inputs are equal to 1.

The truth table of the full adder is listed in Table 2.1. The eight rows under the input variables designate all possible combinations of the three variables. The Block diagram of the full adder is shown in the Figure 2.1. Then find out the Boolean expression for **Sum** and $\mathbf{C_{out}}$ using Boolean Algebra. In Figure 2.2 the Logic diagram of the full adder is shown.

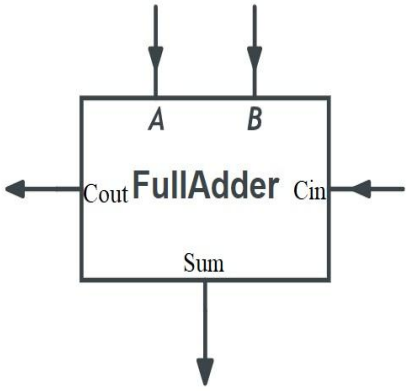


**Figure 2.1: Block diagram of the full adder**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **A** | **B** | **$C_{in}$** | **$C_{out}$** | **Sum** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**Table 2.1: Truth table of the full adder**

$$\text{Sum}(A, B, C_{in}) = \sum m(1,2,4,7) = \bar{A}\,\bar{B}C_{in} + \bar{A}B\overline{C_{in}} + A\,\bar{B}\,\overline{C_{in}} + ABC_{in}$$

$$= (A \oplus B) \oplus C_{in}$$

$$C_{out}(A, B, C_{in}) = \sum m(3,5,6,7) = \bar{A}BC_{in} + A\bar{B}C_{in} + AB\overline{C_{in}} + ABC_{in}$$

$$= (\bar{A}B + A\bar{B}) \cdot C_{in} + AB(\overline{C_{in}} + C_{in}) = (A \oplus B) \cdot C_{in} + (A \cdot B)$$

**Boolean expressions of Sum and $C_{out}$ of Full Adder**

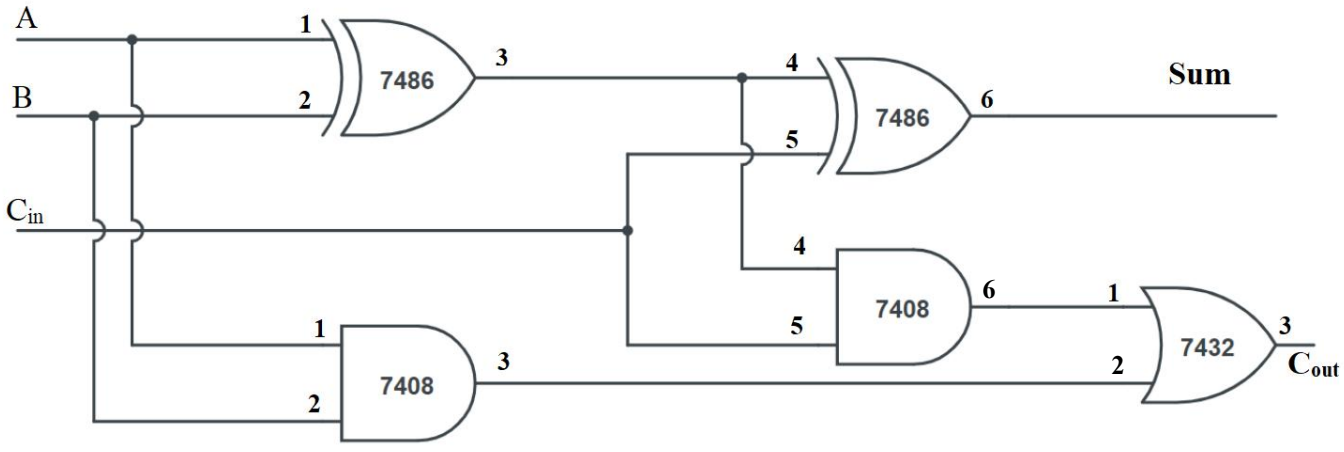


**Figure 2.2: Logic diagram of the full adder**

**Procedure**

**For Software Simulation:**

a) Create a module with required number of variables and mention it's input/output.
b) Write the description of given Boolean function using operators or by using the built in primitive gates.
c) Synthesize to create RTL Schematic.
d) Create another module referred as test bench to verify the functionality and to obtain the waveforms of input and output.
e) Follow the steps required to simulate the design and compare the obtained output with the corresponding truth table.
f) Take the screenshots of the RTL schematic and simulated waveforms.

**Note:** Students need to write the Verilog HDL code by their own for which they can refer Appendix - A if required.

**For Hardware implementation:**

a) Turn off the power of the Trainer Kit before constructing any circuit.
b) Connect **power supply (+ 5 V DC)** pin and **ground** pin to the respective pins of the trainer kit.
c) Place the ICs properly on the bread board in the Trainer Kit.
d) Connect VCC and GND pins of each chip to the power supply and ground bus strips on the bread board.
e) Connect the input and output pins of chips to the input switches and output LEDs respectively in the Trainer Kit.
f) Check the connections before you turn on the power.
g) Apply various combinations of inputs according to truth tables and observe outputs of LEDs.

**Observation:**

To be written by students

**Design Problem:**

Design and Simulation of Full-Subtractor circuit using Verilog HDL.
Hardware implementation of Full-Subtractor circuit.

**Solution:**

Full subtractor is a combinational circuit that performs a subtraction of two bits, taking into account borrowing form the lower significant stage. This circuit has three inputs named minuend (X), subtrahend (Y), and previous borrow (Z) and two outputs, called difference (D) and a borrow (B).

Then find out the boolean expression for difference (D) and a borrow (B) using Boolean Algebra. In Figure 2.3 the Logic diagram of the full subtractor is shown.

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **X** | **Y** | **Z** | **D** | **B** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**Table 2.2: Truth table of the full subtractor**

$$D(X,Y,Z) = \sum m(1,2,4,7) = \bar{X}\,\bar{Y}Z + \bar{X}Y\bar{Z} + X\bar{Y}\,\bar{Z} + XYZ$$
$$= (X \oplus Y) \oplus Z$$

$$B(X,Y,Z) = \sum m(1,2,3,7) = \bar{X}\,\bar{Y}Z + \bar{X}Y\bar{Z} + \bar{X}YZ + XYZ$$
$$= \bar{X}Y\,(\bar{Z} + Z) + Z(\bar{X}\,\bar{Y} + XY)$$
$$= \bar{X}\,Y + Z\,\overline{(X \oplus Y)}$$

**Boolean expressions Difference and Borrow of Full Subtractor**

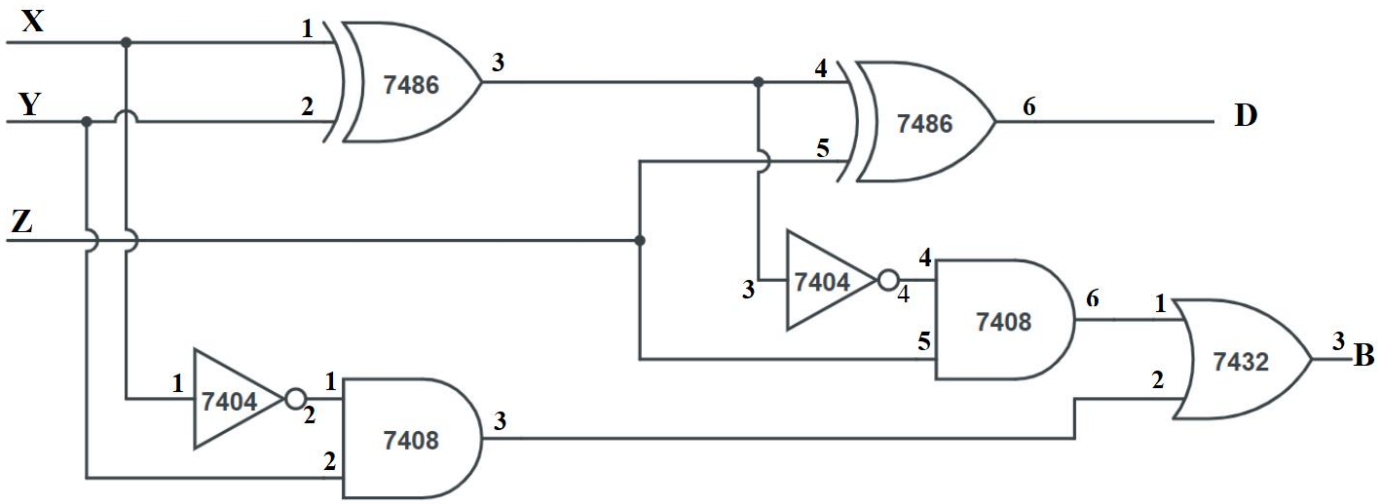


**Figure 2.3 : Logic diagram of the Full Subtractor**

## Conclusion:

To be written by students.

## Sample viva-voice questions

1. Draw the circuit diagram of half adder.
2. Draw the circuit diagram of full adder.
3. Draw the full adder circuit by using half adder circuit and minimum no. of logic gates.
4. Write Boolean functions for half adder.
5. Design the half adder and full adder using NAND-NAND logic.
6. Draw circuit diagram of half subtractor.
7. Draw circuit diagram of full subtractor.
8. Draw full subtractor circuit by using half subtractor circuit and minimum no. of logic gates.
9. Write Boolean functions for half-subtractor.
10. Write Boolean functions for full-subtractor.