MID SEMESTER EXAMINATION 2019
SOLUTION SCHEME (COA)

1. (a) Frequency = 20 MHz — 1

clock cycle time = $1/20\times10^6$ sec

50% of 200 inst^n are register reference inst^n, then

time taken = $0.5\times200\times4\times1/20\times10^6$ sec — (1)

30% of 200 inst^n's are memory reference inst^n, then

time taken = $0.3\times200\times8\times1/20\times10^6$ sec — (2)

20% of 200 inst^{n}s are branch inst^n, then

time taken = $0.2\times200\times6\times1/20\times10^6$ sec — (3)

So, Total time = eq^n (1) + eq^n (2) + eq^n (3)

(b) — 1

$-125 = 1\ 0\ 0\ 0\ 0\ 0\ 1\ 1$

$-5 = 1\ 1\ 1\ 1\ 1\ 0\ 1\ 1$

$1)\ 0\ 1\ 1\ 1\ 1\ 1\ 1\ 0$

V	S	Z	C
1	0	0	1

(c) — 1

opcode	Src Reg 1	Src Reg 2	Dest Reg	I value
4-bits	6-bits	6-bits	6-bits	12-bits

Inst^n size = 4+6+6+6+12 = 34-bits = 34/8 byte

= 4.25 byte

Due to byte alignment, 0.75 byte is wasted.

So, total byte required per inst^n is 5.

Amount of byte required for 100 inst^n is

= 100×5 = 500 bytes.

(d) Big endian vs Little endian 1

(e) R1 = 10110011 1

Ashift L #2, R1

After: R1 = 11001100

Decimal value = -52

2. (a)

Two Add. Inst^n 1

One Add. Inst^n 1

Zero Add. Inst^n 1

(b) Single bus CPU diagram 1

Explanation 1

3. (a) 1. PCout, MARin, Read, Select 4, ADD, Zin 3

2. Zout, PCin, Yin, WMFC

3. MDRout, IRin

4. R1out, Yin

5. R2out, Select Y, ADD, Zin

6. Zout, Yin

7. offset_field_of_IRout, Select Y, ADD, Zin

8. Zout, MARin, Read

9. WMFC

10. MDRout, Yin

11. R3out, Select Y, DIV, Zin

12. Zout, R3in, End

3. (b) Two data transfer Instn with example. 1
Two data manipulation Instn with example 1

4. (a) I. EA = 5000 1
operand = 6500

II. EA = 3002 1
operand = 4000

III. EA = 2200 1
operand = 3500

(b) 1. PCout, R=B, MARin, Read, IncPc 2
2. WMFC
3. MDRoutB, R=B, IRin
4. R1outB, Select 4, SUB, R1in, MARin, Read
5. R2outA, WMFC
6. MDRoutB, SelectA, ADD, R3in, End

5. (a) I. PC = 2000 II. PC = 3000 3
SP = 3996 SP = 3992
TOS = 1008 TOS = 2008

III. PC = 2008
SP = 3996
TOS = 1008

(b) Block diagram of hardwired control unit 1
Explanation 1