SPRING END SEMESTER EXAMINATION-2013

8th Semester B.Tech

ADVANCE COMPUTER ARCHITECTURE CS-810

[Regular-2009 Admitted Batch]

Full Marks: 60 Time: 3 Hours

Answer any SIX questions including Question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. (a) Enumerate 3C's related to memory organization? [2 × 10

(b) Assume a pipelined processor has shared a single memory pipeline for data and instructions. What type of hazard this may lead to and why?

(c) State the difference between write allocate and no-write allocate technique.

(d) State the criteria on which Fleng has done the classification of computer system.

(e) Differentiate between precise and imprecise pipeline architecture.

(f) Which of the dynamic scheduling technique allows the instruction to be executed by having the hazard?

(g) Expand the following terms: VLIW, COMA, NUMA, UMA

(h) What is the complexity of bus interconnection network? (Assume there are 'n' number of nodes.)

(i) Write the difference between RAW and WAR hazard with example.

(j) Enumerate two limitation to the benefits of branch prediction.

2. (a) Machine A has a clock cycle time of 2 nsec and a CPI of 4.0 for a program and machine B has a clock cycle time of 2 nsec and a CPI of 1.2 for the same program. Which machine is faster and by how much? [4

(b) State and explain Amdhal's Law. [4

3. (a) With suitable example explain that Data hazard require stalls for complete execution of instruction. [4

(b) What is dependency? Discuss different types of dependency with suitable example. [4

4. (a) Discuss different techniques for scheduling the branch delay slot. [4

(b) Assume that we have 3 multipliers, 2 adders, 1 divide unit and a single integer unit. The following set of MIPS instructions is going to be executed in a pipelined system. [4

L.D	F6, 34(R2)
L.D	F2, 45(R3)
MUL.D	F0, F2, F4
SUB.D	F8, F6, F2
DIV.D	F10, F0, F6
ADD.D	F6, F8, F2

Consider the above set of instructions and follow the given conditions like, 1st LOAD instruction completed its write result phase and 2nd LOAD instruction completed its execution phase and other remaining instructions are in their issue state. Draw the instruction status table, reservation station table and register status table using Tomasulo Approach.

5. (a) What do you mean by cache coherence? Discuss directory based protocol in detail. [4

(b) Explain the different categories of cache misses. Suggest your opinion to overcome the performance gap between processors and main memory. Whether you should make the cache faster to keep pace with the speed of the CPU or make the cache larger to overcome the widening gap between the CPU and main memory. [4

6. (a) Explain the architecture of a super scalar processor. [4

(b) Explain the advantage of two bit prediction over one bit prediction with example. [4

7. (a) What do you mean by register renaming? Explain how it can overcome the hazard. [4

(b) Enumerate the advantage of message passing. [4

8. Write Short note: (Any Two) [8

(a) Interconnection network

(b) Inverted Page Table

(c) Loosely coupled and tightly coupled Multiprocessor

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