SPRING END SEMESTER EXAMINATION-2018

4th Semester B.Tech & B.Tech Dual Degree

COMPUTER ORGANIZATION & ARCHITECTURE

CS-2006

[For 2017(L.E.), 2016 & 2015 Admitted Batches]

Time: 3 Hours | Full Marks: 60

Answer any SIX questions including question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. Answer all Questions. [2 × 10]

(a) Execute the following instruction where R_0 is of 8 bit data and its content is 11111001.

a) Rshift L #2, R_0

b) Ashift R #1, R_0

(b) Differentiate between horizontal and vertical organization.

(c) In IA-32, which registers are used to fetch the instruction from memory as the PC does in other processor? Explain.

(d) What is the hit ratio of the cache memory if cache memory access time is 5ns and main memory access time is 25ns and average access time is 140ns?

(e) A processor is connected to a 2GB × 32 bit memory module. A program is kept in 256th address of the memory and the maximum length of each instruction of the program is of 32 bits. Then find out size of MAR, MDR, IR and also the content of PC?

(f) Write "ENGINEER" using Big Endean and Little Endean format considering word length as 32 bits.

(g) Specify the size of instruction decoder and step decoder size if the system supports 36 different instructions and each instruction requires maximum up to 7 steps to complete the execution.

(h) Design the 2MB × 32 memory using 1024K × 8 RAM chip.

(i) "Block replacement is not possible in Direct mapped cache"-Justify the statement.

(j) Given the following program fragment

Main Program	First Subroutine		Second Subroutine	
1004 SUB R1, R2	6000 SUB1	ADD R1,R2	8012 SUB2	SUB R6, R1
1008 ADD R3, R4	6004	DIV R5, R1	8016	MUL R1, R5
1012 CALL SUB1	6008	CALL SUB2	8020	RETURN
1016 MUL R4, R5	6012	RETURN		

Initially the stack pointer SP contains 4000.

What are the content of PC, SP, and the top of the stack?

i) After the subroutine call instruction is executed in the main program?

ii) After the subroutine call instruction is executed in the subroutine SUB1?

iii) After the return from SUB2 subroutine?

2. (a) An instruction is stored at location 202 with its address field at location 203. The address field has the value 55. A processor register R_{55} contains the value 350. Evaluate the effective address if the addressing mode of the instruction is :- [4]

i. Direct addressing mode

ii. Immediate addressing mode

iii. Relative addressing mode

iv. Register indirect addressing mode

(b) Represent the decimal number -101.425 using IEEE 754 single precision floating point format. [4]

3. (a) Consider the following program below where A,B,C,D and X are memory locations. [4]

ADD A,B,R1;

DIV C,D,R2;

MUL R1,R2,X

Write down the equivalent code for following computers

(i) Stack Based computer

(ii) Accumulator Based Computer

(b) Multiply (-15 × -8) using Booth's multiplication algorithm. [4]

4. (a) A cache consists of a total of 512 blocks. The main memory contains 16K blocks, each consisting of 32 words. [4]

i. What is the size of the main memory and cache memory?

ii. How many bits are there in each of the TAG, INDEX, and BLOCK OFFSET field in case of direct mapping?

iii. How many bits are there in each of the TAG, and BLOCK OFFSET field in case of associative mapping?

iv. How many bits are there in each of the TAG, SET, and BLOCK OFFSET field in case of 4-way set-associative mapping?

(b) Perform division using restoring technique. [4]

$13 \div 4 = ?$

5. (a) Draw and explain multi-bus organization inside the CPU with the help of a suitable diagram. Write down the required control signals for the following instruction:- [4]

ADD $R_1, R_2, \#5$

Where→ R_2 specifies the source and R_1 specifies the destination register.

(b) Discuss the organization of SRAM cell with neat diagram. [4]

6. (a) How daisy chain method is used for handling simultaneous interrupt request? Explain. [4]

(b) What is virtual memory? Explain the address translation mechanism of virtual memory using TLB. [4]

7. (a) What are the different data transfer techniques present? Briefly explain DMA technique. [4]

(b) Give two examples from each of the following categories of instruction explaining their functions. [4]

I. Data Transfer operation
II. Arithmetic operation
III. Shift operation
IV. Program Control operation

8. Write short notes on *any two*. [4+4]

(a) Memory Interleaving

(b) IA-32 Addressing modes

(c) Memory Mapped I/O Vs I/O mapped I/O

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