KIIT UNIVERSITY, BHUBANESWAR
AUTUMN MID-SEMESTER EXAMINATION – 2017
DIGITAL ELECTRONIC (EC-2011)

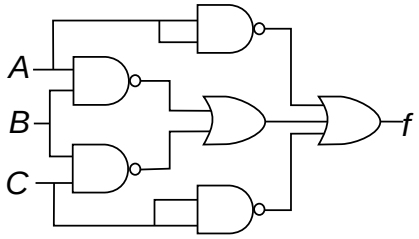
Full Marks: 25 **Duration: 1hour 30 mins**

- ***Answer any FIVE questions including question No.1 which is compulsory.***
- ***The figures in the margin indicate full marks.***
- ***Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.***

1) A. The two numbers represented in signed 2's complement form are ***P=11101101*** & ***Q=11100110***. If Q is subtracted from P, then obtain the value in ***signed 2's compliment*** form. ***[1X5]***

B. Represent $\mathbf{29_{10}}$ in Hexadecimal & BCD.

C. Simplify and minimize the output(f) of the logic circuit given below:



D. Design a **XNOR** gate using ***NAND logic***.

E. Why the rows and columns of K-map are ordered in Gary code rather than binary numerical order. Explain in brief.

2) Obtain the minimized expression for the following 4-variable Boolean expression using K-map method. Implement the minimized expression using ***minimum numbers of NAND gates only.*** ***[5]***

$$\boldsymbol{F = \pi M(4,5,8,9,12,13).d(1,6,11)}$$

3) A. 'XOR and XNOR gates can be used as a buffer as well as an inverter'. Justify ***[1]***

B Design a 4-bit **Full adder/subtractor** circuit using **XNOR** gates only. ***[2]***

C. Implement 1-bit magnitude comparator using **2:4 active HIGH output decoder** and basic gates. ***[2]***

4) A. Design a Combinational circuit **using 2-input basic gates only** which has three inputs A, B & C and three outputs X, Y & Z. When the decimal equivalent of the binary input is 0, 1, 3 or 5, the decimal equivalent of the binary output is one greater than the input and when decimal equivalent of the binary input is 2, 4, 6 or 7, the decimal equivalent of the binary output is one less than the input. ***[3]***

B. (i) Simplify Boolean Expression $\boldsymbol{AB + AC + A\overline{C} + A\overline{B} + BC}$ ***[2]***

(ii) Perform BCD addition **(397+158)**

5) What is Decoder? Implement a Full-Substractor circuit using 3-8 decoder having active-Low output lines and **2-input AND gates**. ***[5]***

6) A. Define **'positive logic system'** and **'negative logic system'**. ***[2]***

B. Perform **BCD Subtraction** : (206.7-147.8) ***[2]***

C. What is the **disadvantage** of binary parallel adder circuit? ***[1]***

7) A. Draw a **Full Subtractor** using two **Half Subtractor** Circuits. ***[2]***

B. State and Prove **Concensus Theorem.** ***[2]***

C. **Minterms** and **Maxterms** are complement of each other. Justify ***[1]***