6. a) Design a J-K Flip-Flop using a D Flip-Flop and basic gates as required. [4

b) With the help of a neat diagram, explain the working of a 4-bit Successive Approximation type ADC with Analog input of 11.6 V. Find the digital output. What would be its conversion time if clock frequency is 1 MHz? If the analog input voltage is now increased to 14.8 V, what would be the new conversion time? Explain. [4

c) In a T Flip-Flop, the output is initially in SET state. If the input clock frequency is 6 MHz, find the frequency of the output waveform when (i) T = 0, (ii) T = 1. [2

7. a) Design a Combinational circuit **using 2-input basic gates only** which has three inputs A, B & C and three outputs X, Y & Z. When the decimal equivalent of the binary input is 0, 1, 5 or 3, the decimal equivalent of the binary output is one greater than the input and when decimal equivalent of the binary input is 4, 2, 6 or 7, the decimal equivalent of the binary output is one less than the input. [4

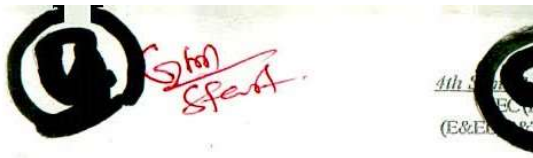
b) Design a 3-bit Odd Parity Generator circuit using a Decoder with Active-Low outputs. [4

c) Design a 2-bit Asynchronous UP/DOWN Counter using Negative Edge Triggered JK Flip Flops with Mode (M) as a control input. Given that, when M=0, the counter should count UP and when, M=1, it should count DOWN. [2

8. a) Design a synchronous sequential circuit using D flip-flop, which produces an output Z = 1, whenever the following input sequence '0101' occurs. (***Assume overlapping is allowed and use Mealy Model***) [6

b) With the help of a neat diagram, explain the working of a TTL NAND gate with Totem-pole output and also mention the advantages of this configuration. [4

XXXXX



Spring End Semester Supplementary Examination-2015

4th Semester B.Tech & B.Tech Dual Degree

DIGITAL ELECTRONIC CIRCUITS

(EC-2009)

Full Marks: 60 Time: 3 Hours

Answer any SIX questions including Question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. a) $F(A, B) = A \oplus B$, implement this Boolean function using 4x1 MUX. [1 × 10

b) State Noise Margin High (NM_H) and Noise Margin Low (NM_L), with suitable diagram.

c) Show that $PQ + \overline{P}R = (P + R)(\overline{P} + Q)$ where P, Q and R are Boolean variables.

d) What is Asynchronous input of a Flip-Flop? Write down the Table of Operation of **Active Low Asynchronous input** of flip-flop.

e) Draw the state Diagram of S-R Filp-Flop using Moore Model with suitable State Table.

f) What is 'Lock out problem' in case of counters?

g) What is a Carry Look Ahead Adder? What is its advantage over Ripper Carry adder?

h) Implement XNOR gate by using **minimum number of NOR** gates.

i) How many OR gates are there in a 64 × 8 ROM and how many inputs does each OR gate of a 64 × 8 ROM have?

j) The logic levels used in a 4-bit R-2R ladder DAC are: 1 = 5 V and 0 = 0 V. Find the output voltage for a digital input of 1010 = 3.125 V.

2. a) Implement the following Boolean function using **minimum number of NAND gates.** [4

$$F(A,B,C,D) = \prod M(2,3,6,9,12)\,.\,d(5,8,15)$$

= $\bar{A}\bar{C} + BD + AC$

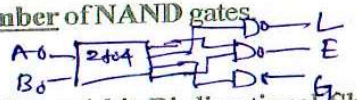
b) Design a **4:2 Priority Encoder** such that the order of priority of the decimal inputs is given as $D_3 > D_2 > D_1 > D_0$, where all D_i's are inputs to the priority encoder. [4

$A = D_3 + D_2$

$B = D_3 + \bar{D}_2 D_1$

$V = D_3 + D_2 + D_1 + D_0$

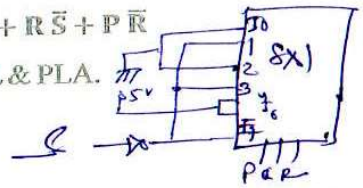
c) Implement a 1-bit Magnitude Comparator using a 2 to 4 Decoder having **ACTIVE LOW** output lines and **minimum number** of NAND gates. [2



3. a) Design a 4-bit Bi-directional Shift register using D-Flip Flops and Four 2x1 MUX. The Shift register should Shift Right when a Control input is **RIGHT/LEFT** = 1, it should shift left when the control input **RIGHT/LEFT** = 0. [4

b) Implement the following logic function using an 8:1 MUX. [4

$$F(P,Q,R,S) = P\,\bar{Q} + R\,\bar{S} + P\,\bar{R}$$



c) Differentiate between PAL & PLA. [2

4. a) Design an Asynchronous, Mod-12 Up-counter using **D Flip-Flops** and a **single NAND** gate. [4

b) What will be the output for L, E & G respectively of the 1-bit magnitude Comparator from the Figure below? Given that, the input at the Hamming Encoder is D3 = 1; D5 = 0; D6 = 1; D7=0 and it's an EVEN Parity Hamming Encoder. [4

The order of Priority of input for 8 to 3 Priority Encoder is **D0 > D1 > D2 > D3 > D4 > D5 > D6 > D7.**

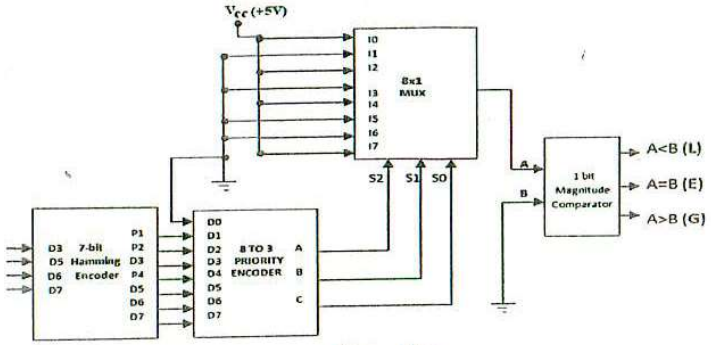


Figure-4(b)

c) Draw the circuit diagram of a 2-input CMOS NOR gate and explain its working in brief. [2

5. a) Design a **Synchronous counter** that goes through states **0, 7, 4, 3, 6, 0, 7, 4...** using J-K Flip-Flops. [4

b) A Cold Storage has three Cooling Fans namely **FAN1, FAN2** and **FAN3**. To maintain the temperature, at least two fans MUST be ON at any instant of time, so there is an ALARM connected with STATUS of The FANs. If, at least two FANs are not ON the ALARM would be triggered. Consider FAN ON as logic '1' and FAN OFF as logic '0' and implement the above ALARM digital logic circuit using **3 to 8 Decoder with ACTIVE LOW output lines** and **minimum number of 2 input AND gates only**. [4

c) A certain memory has a capacity of 128K × 8. [2

(i) How many data input and data output lines does it have? = 8

(ii) How many address lines does it have? = 2^{17}