Sample Question Format
(For all courses having end semester Full Mark=50)

KIIT Deemed to be University
Online End Semester Examination(Spring Semester-2021)

Subject Name & Code: Computer Organization (CS 3042)
Applicable to Courses:

Full Marks=50 **Time:2 Hours**

SECTION-A(Answer All Questions. Each question carries 2 Marks)

Time:30 Minutes **(7×2=14 Marks)**

Question No	Question Type (MCQ/SAT)	Question	CO Mapping	Answer Key (For MCQ Questions only)
Q.No:1	**SAT**	Write the basic performance equation. Explain how N and S can be reduced for better timings.	CO1	
	SAT	Why is the compiler's job easier in CISC computers?	CO1	
	SAT	Add 10111000 in 2's complement to 10001111 in 1's complement and write the answer in sign-magnitude form. Show your calculations.	CO1	
	SAT	If 14 bits are allocated for encoding a branch target and the instruction uses PC relative addressing, then how far on each side of the current instruction can a branch be made?	CO1	
Q.No:2	**SAT**	Arrange cache, main memory, registers, hard disk and tape drive in increasing order of speed and cost.	CO2	
	SAT	Explain how a stack can be used to make function calls. What kinds of data can be pushed on to it?	CO2	
	SAT	Mention two different addressing modes that can	CO2	

		be used to access arrays conveniently. How?		
	SAT	If a machine uses 25 bit instructions, has 32 opcodes, and 128 registers can we have an instruction that uses the three register format? Why?	CO2	
Q.No:3	**SAT**	The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB). The IF, ID, OF and WB stages take 2 clock cycle each for every instruction. Consider a sequence of 50 instructions. In the PO stage, 20 instructions take 4 clock cycles each, 10 instructions take 1 clock cycle each, and the remaining 20 instructions take 2 clock cycle each. Assume that there are no data hazards and no control hazards. What is the number of clock cycles required for completion of execution of the sequence of instructions? Show your calculations.	CO3	
	SAT	Consider an 8-stage instruction pipeline, where all stages are perfectly balanced. Assume that there is no cycle-time overhead of pipelining. When an application is executing on this 8-stage pipeline, what is the speedup achieved with respect to non-pipelined execution if 30% of the instructions incur 4 pipeline stall cycles?	CO3	
	SAT	A 5-stage pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform	CO3	

		Operation (PO) and Write Operand (WO) stages. The IF, ID, OF and WO stages take 1 clock cycle each for any instruction. The PO stage takes 3 clock cycle for ADD and SUB instructions, 5 clock cycles for MUL instruction, and 10 clock cycles for DIV instruction respectively. There is no operand forwarding. What is the number of clock cycles needed to execute the following sequence of instructions? Instruction Meaning of instruction I0 :MUL R2 ,R0 ,R1 R2 ← R0 *R1 I1 :DIV R5 ,R3 ,R4 R5 ← R3 /R4 I2 : ADD R2 ,R5 ,R2 R2 ← R5 + R2 I3 :SUB R5 ,R2 ,R6 R5 ← R2 - R6 Show your work clearly.		
	SAT	We have 2 designs D1 and D2 for a synchronous pipeline processor. D1 has a 3 stage pipeline with execution time of 8 ns, 5 ns, and 4 ns. While the design D2 has 8 pipeline stages each with 3 ns execution time. How much time can be saved using design D2 over design D1 for executing 100 instructions? Show your calculations.	CO3	
Q.No:4	**SAT**	Consider a main memory with four-page frames and the following sequence of page references: 3, 7, 2, 3, 9, 2, 6, 3, 7, 9, 3, 6, 2, 8, 3. How many page faults occur if the optimal page replacement policy is used? Show your calculations.	CO4	
	SAT	Consider a main memory	CO4	

		with five-page frames and the following sequence of page references: 4, 3, 6, 3, 9, 1, 6, 3, 6, 9, 3, 6, 2, 9, 3. How many page faults occur if the FIFO page replacement policy is used? Show your calculations.		
	SAT	Consider a main memory with five-page frames and the following sequence of page references: 3, 7, 2, 3, 9, 2, 7, 5, 2, 9, 3, 7, 2, 8, 3. How many page faults occur if LRU page replacement policy is used? Show your calculations.	CO4	
	SAT	Assume that for a certain processor, a read request takes 120 nanoseconds on a cache miss and 2 nanoseconds on a cache hit. Suppose while running a program, it was observed that 98% of the processor's read requests result in a cache hit, what is the average read access time in nanoseconds is? Show your calculations.	CO4	
Q.No:5	**SAT**	A block-set associative cache memory consists of 512 blocks divided into 16 block sets. The main memory consists of 32K blocks and each block contains 128 words. How many bits are required for addressing the main memory? How many bits are needed to represent the TAG, SET and WORD fields? Assume word addressable memory. Show your calculations.	CO4	
	SAT	An 8-way set associative cache memory unit with a capacity of 32 KB is built using a block size of 16 words. The word length is 64 bits. The size of the	CO4	

		physical address space is 2 GB. What is the number of bits for the TAG field? Show your calculations.		
	SAT	Consider a direct mapped cache with 4 cache blocks (0-3). If the memory block requests are in the order- 3, 5, 2, 8, 0, 6, 3, 10, 16, 20, 17, 29, 18, 30, 23, 2, 63, 5, 79, 19, 24, calculate the cache hit ratio. Show your calculations.	CO4	
	SAT	Consider a fully associative cache with 16 cache blocks (0-15). The memory block requests are in the order- 4, 3, 27, 8, 19, 2, 27, 8, 16, 35, 44, 22, 8, 7, 16, 25, 5 If LRU replacement policy is used, which cache block will have memory block 5? Show your calculations.	CO4	
Q.No:6	**SAT**	Give an example of a pipeline data hazard. How can you prevent it?	CO3	
	SAT	Give an example of a pipeline instruction hazard. How can you prevent it?	CO3	
	SAT	Give an example of a pipeline structural hazard. How can you prevent it?	CO3	
	SAT	Give an example of a branch delay slot with respect to pipelining.	CO3	
Q.No:7	**SAT**	How can daisy-chaining be used to handle interrupts from multiple sources?	CO6	
	SAT	Why do ISRs need to be as short as possible?	CO6	
	SAT	What is the need to have DMA when interrupts are better than polling usually?	CO6	
	SAT	How are polling and interrupts different from each other?	CO6	

SECTION-B(Answer Any Three Questions. Each Question carries 12 Marks)

Time: 1 Hour and 30 Minutes **(3×12=36 Marks)**

Question No	**Question**	**CO Mapping (Each question should be from the same CO(s))**
Q.No:8	Consider a pipelined processor with the following four stages- IF : Instruction Fetch ID : Instruction Decode and Operand Fetch EX : Execute WB : Write Back The IF, ID and WB stages take two clock cycles each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 5 clock cycle and the MUL instruction need 10 clock cycles in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions? ADD R2, R1, R0 R2 ← R0 + R1 MUL R4, R3, R2 R4 ← R3 + R2 SUB R6, R5, R4 R6 ← R5 + R4 Show detailed steps of your work.	CO3
	Consider a pipeline having 5 phases with duration 60 ns, 50 ns, first two digits of your roll number ns, last two digits of your roll number ns (If the last two digits are 00 then assume 01 ns), and 24 ns. Given latch delay is 2 ns. Calculate- 1. Pipeline cycle time 2. Non-pipeline execution time 3. Speed up ratio 4. Pipeline time for 50 tasks 5. Sequential time for 50 tasks	

	6. Throughput	
	Consider a non-pipelined processor operating at 4 GHz. It takes 4 clock cycles to complete an instruction. You are going to make a 4-stage pipeline out of this processor. Overheads associated with pipelining force you to operate the pipelined processor at 3 GHz. In a given program, assume that 30% are memory instructions, 40% are ALU instructions and the rest are branch instructions. 20% of the memory instructions cause stalls of 8 clock cycles each due to cache misses and 5% of the branch instructions cause stalls of 10 cycles each. Assume that there are no stalls associated with the execution of ALU instructions. What is the speedup achieved by the pipelined processor over the non-pipelined processor? Show detailed steps of your work.	
Q.No:9	A byte-addressable computer has a small data cache capable of holding 16 32-bit words. Each cache block consists of one 32-bit word. When a given program is executed, the processor reads data sequentially from the following hex addresses: 216, 204, 208, 28C, 2F4, 2F0, 240, 204, 216, 21C, 248, 2F4 This pattern is repeated four times. Assume that the cache is initially empty. Show the contents of the cache at the end of each pass through the loop if a direct-mapped cache is used, and compute the hit rate.	CO4
	Make a 64M × 64-bit memory using 2M × 16-bit memory chips. Draw a detailed diagram.	
	Consider a 8-way set associative mapping with 32 cache blocks. The memory block requests are in the order- 1, 255, 1, 4, 3, 8, 135, 159, 216, 130, 62, 8, 48, 32, 74, 92, 155 If LRU replacement policy is	

	used, what is the state of the cache in the end? Draw a detailed diagram.	
Q.No:10	Derive an effective memory access time equation that takes into account the page fault rate, TLB hit rate, memory access time, and TLB processing time.	CO4
	Describe how a two-level paging scheme works with the help of a detailed diagram.	
	Describe with the help of a diagram how demand paging works and mention all the steps involved in it. Are all page faults cases of demand paging? Why?	
Q.No:11	Write a subroutine called EXCLAIM in assembly that accepts a single parameter in a register representing the starting address STRNG in the main memory for a string of ASCII characters in successive bytes representing an arbitrary collection of sentences, with the NUL control character (value 0) at the end of the string. The subroutine should scan the string beginning at address STRNG and replace every occurrence of a period (‘.’) with an exclamation mark (‘!’).	CO2
	Write a subroutine called ALLCAPS in assembly that accepts a parameter in a register representing the starting address STRNG in the main memory for a string of ASCII characters in successive bytes, with the NUL control character (value 0) at the end of the string. The subroutine should scan the string beginning at address STRNG and replace every occurrence of a lower-case letter (‘a’–‘z’) with the corresponding upper-case letter (‘A’–‘Z’).	
	Write a subroutine called WORDS in assembly that accepts a parameter in a register representing the starting address STRNG in the main memory for a string of ASCII characters in successive	

	bytes, with the NUL control character (value 0) at the end of the string. The string represents English text with the space character between words. The subroutine has to determine the number of words in the string (excluding the punctation characters). It must return the result to the calling program in a register.	