Sample Question Format
(For all courses having end semester Full Mark=50)

KIIT Deemed to be University
Online End Semester Examination(Spring Semester-2022)

Subject Name & Code: COA(CS- 2006)
Applicable to Courses: B.Tech 4th Semester

Full Marks=50 **Time:2 Hours**

SECTION-A(Answer All Questions. Each question carries 2 Marks)

Time:30 Minutes **(7×2=14 Marks)**

Question No	Question Type (MCQ/SAT)	Question	CO Mapping	Answer Key (For MCQ Questions only)
Q.No:1	MCQ	Question -1 on concept 1 Consider a main memory size is 1024words, cache memory size is 64 words and block size is 8 words. If 570 word of main memory is mapped to cache memory then obtain to which cache block it will map to and the tag value of respective cache block in direct mapping? A. CB-7, TAG-1000 B. CB-6, TAG-100 C. CB-7, TAG-1100 D. CB-6, TAG-110	CO4	A
	MCQ	Question -2 on concept 1 Consider a main memory size is 1024words, cache memory size is 64 words and block size is 8 words. Find no. of tag comparator for direct, associative and 4 way set associative mapping? A. Direct-1, Associative-8, Set associative-4 B. Direct-1, Associative-4, Set-associative-8 C. Direct-1, Associative-4, Set-associative-4 D. Direct-1, Associative-8, Set-associative-8	CO4	A
	MCQ	Question -3 on concept 1	CO4	A

		Consider a main memory size is 1024words, cache memory size is 64 words and block size is 8 words. Find tag memory for direct, associative and 4 way set associative mapping? A. Direct-32 bits, Associative- 56bits, Set-associative-48bits B. Direct-24 bits, Associative-48 bits, Set-associative-56 bits C. Direct-32bits, Associative-48 bits, Set-associative-56bits D. Direct-24bits,Associative-56bits, Set-associative-48bits		
	MCQ	Question -4 on concept 1 Consider a main memory size is 1024words, cache memory size is 64 words and block size is 8 words. How many multiplexer are used for direct, associative and 4 way set associative mapping? A. Direct-4, Associative-0, Set associative-24 B. Direct-4, Associative-0, Set-associative-6 C. Direct-0, Associative-4, Set-associative-24 D. Direct-0, Associative-4, Set-associative-6	CO4	A
Q.No:2	**MCQ**	Question -1 on concept 2 Which memory chip provides least no. of external connection to provide 2048 memory cell. A. 1024 x 2 B. 512 x 4 C. 256 x 8 D. 128 x16	CO4	A
	MCQ	Question -2 on concept 2 Which two memory chip provides same no. of external connection to provide 2048 memory cell. A. 1024 X 2, 2048 X 1 B. 64 X 32, 1024 X 2 C. 128 X 16, 512 X4 D. 256 X 8, 128 X16	CO4	A
	MCQ	Question -3 on concept 2 How many chips required of size 128 x 16 to design 512 x 32. Also find the decoder size. A. No. Of chips=8, Decoder size=2:4 B. No. Of chips=8, Decoder size=3:8 C. No. Of chips=4, Decoder size=2:4 No. Of chips=4, Decoder size=3:8	CO4	A

	MCQ	Question -4 on concept 2 Consider a cache with write back protocol where cpu will write only in cache, where write hit is 80%, cache access time is 2msec, data transfer time between cache and main memory is 100msec per word. If block size is 8 words then find average access time. A. 322 msec B. 284msec C. 162msec D. 150msec	CO4	A
Q.No:3	**MCQ**	Question -1 on concept 3 Which one is exponent value and matissa value to represent a NaN(Not a Number) A. E'=0, M is not equal to 0 B. E'=255, M is not equal to 0 C. E'=255, M =0 D. E'=0, M =0	CO5	B
	MCQ	Question -2 on concept 3 Find the Hexa decimal number represention of memory to save a number -37. 25 in IEEE single precission format. A. 4 2 1 5 0 0 0 0 B. C 2 1 5 0 0 0 0 C. 4 2 1 7 0 0 0 0 D. C 2 1 7 0 0 0 0	CO5	B
	MCQ	Question -3 on concept 3 In division process after subtraction, the content of accumulator is negative, then which option is not true A. 2A+M B. Left shift of accumulator and then add M to A C. Subtract M from A, then Left shift of accumulator and then add M to A D. Add M to A, then Left shift of accumulator and then subtract M from A	CO5	C
	MCQ	Question -4 on concept 3 Find the Hexa decimal number represention of memory to save a number -15. 75 in IEEE single precission format. A. C 1 6 C 0 0 0 0 B. C 2 1 5 0 0 0 0 C. 4 6 1 C 0 0 0 0 D. 4 2 6 5 0 0 0 0	CO5	A
Q.No:4	**MCQ**	Question -1 on concept 4 How many clock cycles required to obtain sum and carry in 12 bit carry look ahead adder. A. 7 B. 8 C. 9 D. 10	CO5	B
	MCQ	Question -2 on concept 4 Find booth recording pattern of a number +41 A. +1 -1 +1 -1 0 +1 -1	CO5	A

		B. +1 -1 +1 -1 0 +1 C. -1 +1 -1 0 +1 -1 D. -1 -1 +1 -1 0 +1 -1		
	MCQ	Question -3 on concept 4 Find bit pair recording pattern of a number +41 A. +1 -1 -2 +1 B. +1 -1 +2 +1 C. +1 -1 -1 +1 D. -1 +1 -1 +1	CO5	A
	MCQ	Question -4 on concept 4 In carry save addition of summands methods, find out no. of CSA level and no. of clock cycles are required to complete the multiplication if Q=8 bits, and final sum and carry is 16 bit. A. 4, 22 B. 4, 19 C. 3, 15 D. 3, 17	CO5	B
Q.No:5	**MCQ**	Question -1 on concept 5 If a 10GHz computer takes 5 clock cycles for ALU instructions, 10 clock cycles for branch instructions and 3 clock cycles for data transfer instructions. Then Find the total time taken by the computer to execute the program. The program has 200 instructions and 50% ALU instructions, 25% branch instructions and 25% data transfer instructions. A. 57.5nsec B. 115nsec C. 58nsec D. 100nsec	CO1	B
	MCQ	Question -2 on concept 5 The content of register R1 is 11100101. What will be the decimal value after execution of AshiftR #2, R1. A. 7 B. 14 C. -7 D. -14	CO1	C
	MCQ	Question -3 on concept 5 The contents of memory locations 1000, 1200 and 1500 are 100, 1500 and 20 respectively before the following program is executed. (i) MOV #1000, R1 (ii) ADD 200(R1),(1200) (iii) SUB 1500, 1200. What will be the contents memory locations 1000, 1200, 1500 after the program is executed? A. 100, 20, 1500 B. 100, -20, 1500 C. 100, 20, 1520 D. 100, -20, 1520	CO1	D
	MCQ	Question -4 on concept 5 Which one is not correct for the expression in stack based organization: X = A-B+C*D A. PUSH A, PUSH B, SUB, PUSH C, PUSH D, MULT, ADD, POP X	CO1	C

		B. PUSH C, PUSH D, MULT, PUSH A, PUSH B, SUB, ADD, POP X C. PUSH A, PUSH B, PUSH C, PUSH D, MULT, ADD, SUB, POP X D. None of these		
Q.No:6	**MCQ**	Question -1 on concept 6 Direct memory access is direct data transfer between A. CPU and main memory B. CPU and I/O processor C. CPU and I/O device D. Main memory and I/O devices	CO6	D
	MCQ	Question -2 on concept 6 Which is not a program data transfer scheme A. Synchronous data transfer scheme B. Asynchronous data transfer scheme C. Interrupt driven data transfer scheme D. DMA data transfer scheme	CO6	D
	MCQ	Question -3 on concept 6 For the daisy chain scheme of connecting I/O devices, which of the following statement is true? A. It gives non-uniform priority to various devices B. It gives uniform priority to all devices C. It is only useful for connecting slow devices to a processor device D. It requires a separate interrupt pin on the processor for each device.	CO6	A
	MCQ	Question -4 on concept 6 The correct matching of the following pairs is a. DMA I/O — 1. High speed RAM b. Cache — 2. Disk c. Interrupt I/O — 3. Printer d.Condition code register — 4. ALU A. a-4, b-3, c-1, d-2 B. a-2, b-1, c-3, d-4 C. a-3, b-1, c-2, d-4 D. a--2, b-3, c-4, d-1	CO6	B
Q.No:7	**MCQ**	Question -1 on concept 7 Which of the following control steps are required to execute the instruction "mov R1, NUM"? [Where R1 is the source operand]. A) 1. Address_field_of_IRout, MARin 2. R1out, MDRin,Write, 3. WMFC 4. End B) 1. R1out,Addrress_field_of_IRin, end C) 1. WMFC 2.Addrress_field_of_IRout, MARin 3. MDRin, R1out, end D) 1.Address_field_of_IRout, MARin 2.R1out, MDRin,Read 3.WMFC 4. end	CO3	A

	MCQ	Question -2 on concept 7 Which of the following control steps are required to execute the instruction "mov #100, R1"? [Where R1 is the destination operand] A) 1. Address_field_of_IRout, MARin,Read 2. WMFC 3. MDRout,R1in,end B) 1.Addrress_field_of_IRout,R1in end C) 1.Addrress_field_of_IRout, MARin 2.MDRin,R1out,Write 3.WMFC 4. end D) 1.Address_field_of_IRout, MARin 2.R1out, MDRin,Read 3.WMFC 4. end	CO3	B
	MCQ	Question -3 on concept 7 The CONSTANT 4 at input A of the ALU is useful ----------, in a Three-bus organization of the datapath inside of a processor. A. for Branching B. to add 4 to the contents of PC for updating its location to point to the next instruction in the given sequence in memory. C. to increment other addresses like memory addresses in LOADMULTIPLE and STOREMULTIPLE type instructions. D. None of the Above	CO3	C
	MCQ	Question -4 on concept 7 In Three-bus organization of the datapath inside of a processor, Which one of the following is the correct Sequence of Control Steps for Fetching an instruction from memory? A. 1. PCout, R=B, MAR in, Read 2. IncPC, WMFC 3. MDRoutB, R=B, IRin B. 1. PCout, R=B, MAR in, 2. IncPC, Read, WMFC 3. MDRoutB, R=B, IRin C. 1. PCout, R=B, MAR in, IncPC 2. Read, WMFC 3. MDRoutB, R=B, IRin D. None of the above	CO3	A

SECTION-B(Answer Any Three Questions. Each Question carries 12 Marks)

Time: 1 Hour and 30 Minutes **(3×12=36 Marks)**

Question No	Question	CO Mapping (Each question should be from the same CO(s))
Q.No:8	**Q.No:8-1st question** A. Define memory interleaving technique with proper diagram. Why is memory interleaving technique used? B. Consider a memory of 32 words per block. If 1 clock cycle are required to transfer address from CPU to main memory and 8 clock cycle to access the 1st word and 4 clock cycle each for consecutive words and 1 clock cycle for transferring the word from memory to cache. Then calculate the total clock cycle required to transfer the block with inter leaving and without interleaving if the number of module is eight.	CO4
	Q.No:8-2nd question A. Define and discuss the different mapping function with hardware diagram. Discuss the merit and demerit of the different types of mapping function. (6 marks) B. Consider a main memory of 1GByte and a cache memory of 1MBytes partitioned into 512 words. Each word consumes 64bits (i) Find out the physical address length. (ii) How many bits are there in each of the TAG, BLOCK and WORD field in case of direct mapping? (iii)How many bits are there in each of the TAG and WORD field in case of associative mapping? (iv)How many bits are there in each of the TAG, SET, and WORD field in case of 4-way set-associative mapping? (v) How many tag comparators for each of the mapping techniques (vi) Obtain tag memory for each of the mapping techniques.	
	Q.No:8-3rd question	

	A. How many 512X8 RAM chips are needed to provide a memory capacity of 4096X32 ? Give the specifications with suitable diagram. B. Consider a cache with 4 cache blocks (0-3). The memory block requests are in the order- 2, 3, 4, 7, 8, 6, 5, 8, 6, 5, 2, 4, 3, 5, 4 Calculate the hit ratio and miss ratio using **(i)** Direct mapping **(ii)** LRU Replacement policy	
Q.No:9	**Q.No:9-1st question** A. Perform the following division operation using restoring and non-restoring method. 17 ÷ d Where d= **your roll number last digit** If your roll no is 2005325, then d= 5 B. **Perform the addition of the following two numbers represented in IEEE format and give the result in IEEE format.** **Number 1:** S=0 E'= 1001 0101 M=0111 0000 0000 0000 0000 000 **Number 2:** S=0 E'= 1000 1010 M=0101 0000 0000 0000 0000 000	CO_5
	Q.No:9-2nd question A. Multiply (-13 X M) using BOOTH ALGORITHM. Where M= **your roll number last digit** If your roll no is 2005236, then M= 6 B. **Subtract Number 2 from Number 1. (Numbers are represented in IEEE format and give the result in IEEE format.** **Number 1:** S=0 E'= 1000 0100 M=0110 0000 0000 0000 0000 000 **Number 2:** S=0 E'= 1000 0011 M=0100 0000 0000 0000 0000 000	
	Q.No:9-3rd question A. Multiply (-11 X M) using Bit pair recording technique. Where M= **your roll number last digits** If your roll no is 2005123, then M= 3 B. **Perform the addition of the following two numbers represented in IEEE format and give the result in IEEE format.** **Number 1:** S=0 E'= 1001 0111 M=0101 0000 0000 0000 0000 000 **Number 2:** S=0	

	E'= 1000 1011 M=0001 0000 0000 0000 0000 000	
Q.No:10	**Q.No:10-1st question** A.Distinguish between memory mapped I/O and I/O mapped I/O B. Write an assembly language program to derive the expression X = A-(R+C)+H*I/T+E-(C*T)/(U-R)+E i) in a stack based computer with zero address instructions. ii) in a accumulator based CPU with one address instructions.	CO1, CO6
	Q.No:10-2nd question A. Explain different techniques for data transfer. B. Write an assembly language program to derive the expression X = O-(R+G)+A*N/I+Z-(A*T)/(I-O)+N i) in a stack based computer with zero address instructions. ii) in a accumulator based CPU with one address instructions.	
	Q.No:10-3rd question A. Distinguish between cycle stealing and burst mode data transfer in DMA. B. Explain FLYNN'S classification with neat diagram C. Write an assembly language program to derive the expression using RICS instruction X = A-(R+C)+H*I/T+E-(C*T)/(U-R)+E	
Q.No:11	**Q.No:11-1st question** A. Write the sequence of control steps for the given instructions for single bus architecture and design the logic function for MAR_{in} and Y_{in} control signal with reference to given instructions. i) ADD #10, (R1) ii) SUB (R1), R2 B. Given the following program fragment Main Program / Subroutine SUB1 / Subr 1000: ADD R1, R2 / 2050: MUL A, B / 200: 1004: SUB R3, R4 / 2054: CALL SUB2 / 204: 1008: CALL SUB1 / 2058: ADD #10, R2 / 208: 1012: ADD R5, R6 / 2062: RETURN Initially stack pointer SP contains 5000 and top of stack is 500. What are the content of SP, PC, top of stack? I) After the subroutine call instruction is executed in the main	CO2, CO3

program?
II) After the subroutine call instruction is executed in the subroutine SUB1?
III) After return from the subroutine SUB2?
IV) After return from the subroutine SUB1?

Q.No:11-2nd question

A. Write the sequence of control steps for the given instructions using multiple bus architecture.

i. ADD #10, (R1)
ii. SUB (R1), R2
iii. MUL (1000), R2

B. Assume that each memory word consumes 4 bytes and computer is byte addressable. The memory stores numbers from 1 to 20 sequentially starting from memory location 1000. The register R2 and R3 contain value 10 and 20 respectively.

```
        Move #1000, R0
        Move #5, R1
LOOP:   Add R2, 4(R0)
        Add #4, R0
        Add (R0), R3
        Move R3, 4(R0)
        DEC R1
        Branch>0 LOOP
```

Find out the contents of first ten words locations starting at 1000.

Q.No:11-3rd question

A. Write the micro-instruction for the following instruction

MUL (R1), R2

B. A computer has 32 bit instruction. It uses two register operands and one memory operand. There are 64 general purpose registers and 32K bytes of RAM. How many different operations the computer can perform? If there are 10 three address operations which uses two registers and one memory, then how many one address operations (which use only memory) are possible.