SUPPLEMENTARY EXAMINATION-2018

3rd Semester B.Tech & B.Tech Dual Degree

DIGITAL ELECTRONIC CIRCUITS

EC-2009

(For 2014 & 2013 Admitted Batches)

Time: 3 Hours | Full Marks: 60

Answer any SIX questions including question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. (a) What is the difference between active LOW and active HIGH terminals? [1 × 10]

   (b) Perform following arithmetic :
   (i) BCD addition **(397+158)**
   (ii) **(-10) - (-6)** using 2's complement method

   (c) Show that, $\mathbf{U\,\overline{V} + U\,W + V\,\overline{W} = U + V\,\overline{W}}$ where U, V and W are Boolean variables.

   (d) With the help of a **2:1 MUX**, implement a **XOR** gate.

   (e) Differentiate synchronous and asynchronous input terminals of flip-flop, explain with the help of **J-K** flip-flop.

   (f) A 8-bit DAC has a step size of 50 mV. Determine the full-scale output voltage and the percentage of resolution.

   (g) Implement **XNOR** gate using minimum numbers of **XOR** gates only.

   (h) How many OR gates are there in a 32 x 8 ROM and how many inputs does each OR gate of a 32 x 8 ROM have ?.

   (i) "**Excess-3** codes are self-complementing & Sequential but not cyclic", justify.

   (j) Find out the characteristic equation of a **T** flip flop.

2. (a) Design a T- Flip-Flop using a D Flip-Flop and a multiplexer having one select line. [4]

(b) Design a 4:2 Priority Encoder such that the order of priority of the decimal inputs is given as $\mathbf{D_2 > D_0 > D_1 > D_3}$, where all $\mathbf{D_i}$**'s** are inputs to the priority encoder. [4]

(c) What is the difference between SRAM and DRAM? [2]

3. (a) Obtain the minimized expression for the following 4-variable Boolean expression using K-map method and implement the minimized expression using minimum numbers of NAND gates only. [4]
F(P,Q,R,S) = ∑m (0,2,5,10,11,15)+ ∑d(1,3,7)

(b) Draw the logic diagram of **Full-Subtractor** using minimum number of 2-input **NAND** gates. [4]

(c) Draw the logic diagram of a 2-input **CMOS NOR** gate and explain its working in brief. [2]

4. (a) Design a synchronous sequential circuit which produces an output Z = 1, whenever the following input sequence '1101' occurs. (*Assume **overlapping** is allowed and use **Mealy Model***) [6]

(b) With the help of a neat diagram, explain the working of a **TTL NAND** gate with Open-Collector Output and also mention the disadvantages of this configuration. [4]

5. (a) Design a **Mod-6** Asynchronous Up-counter using **JK** Flip-Flops. [4]

(b) Design a **2-bit** magnitude comparator using two **1-bit** magnitude comparator modules and additional basic gates. [4]

(c) Design a Half adder using **2:4 active HIGH output decoder** and basic gates. [2]

6. (a) 'A **decoder** with an enable input can be used as a **DEMUX**'. Justify and design a **3:8** decoder **using 2:4** decoder so that it can also be used as a **1:8 DEMUX**. [4]

(b) Design a **synchronous counter** that goes through states **0,2,3,5,6,7,0,2,3**..... using **J-K** FFs.(Consider unused states as don't cares.) [4]

(c) A certain memory has a capacity of 64K x 16. [2]
(i) How many data input and data output lines does it have?
(ii) How many address lines does it have ?

7. (a) With the help of a neat diagram, explain the working of a **TTL NAND** gate with **Open-Collector** Output and also mention the disadvantages of this configuration. [4]

(b) Explain **Counter type A/D** converter using neat circuit diagram and discuss the disadvantage of this converter. [4]

(c) Design a **MOD-4 Ring counter** and explain its operation. [2]

8. (a) Implement the following logic function using a Multiplexer having three select lines. [4]
F(P,Q,R,S) = P $\bar{Q}$ + R$\bar{S}$ + P$\bar{R}$.

(b) Design and explain 4-bit **bidirectional** shift register using **D** FFs. [4]

(c) What is the difference between **PROM** and **PLA**? [2]

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