KIIT UNIVERSITY, BHUBANESWAR
SPRING MID-SEMESTER EXAMINATION – 2016
DIGITAL ELECTRONIC CIRCUITS (EC-2009)

Full Marks: 25 **Duration: 2 hours**

- *Answer any FIVE questions including question No.1 which is compulsory.*
- *The figures in the margin indicate full marks.*
- *Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.*

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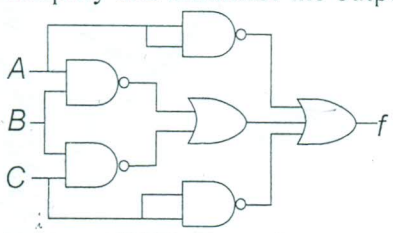
1) A. The two numbers represented in signed 2's complement form are ***P=11101101*** & ***Q=11100110***. If Q is subtracted from P, then obtain the value in ***signed 2's compliment*** form.

B. Represent 43_{10} in Hexadecimal & BCD.

C. Simplify and minimize the output(f) of the logic circuit given below:



[1X5]

D. Design a **XOR** gate using *NAND logic*.

E. Detect & correct the error in the hamming code 1001001 transmitted through a noisy channel.

2) Obtain the minimized expression for the following 4-variable Boolean expression using K-map method. Implement the minimized expression using ***minimum numbers of NAND gates only.*** *[5]*

$$F = \pi M(4, 5, 8, 9, 12, 13).d(1, 6, 11)$$

3) A. 'XOR and XNOR gates can be used as a buffer as well as an inverter'. Justify *[1]*

B. Design a 4-bit **Full adder/subtractor** circuit using **XNOR** gates only. Explain the design & the control logic. *[2]*

C. Implement 1-bit magnitude comparator using **2:4 active HIGH output decoder** and basic gates. *[2]*

4) A. Design a Combinational circuit **using 2-input basic gates only** which has three inputs A, B & C and three outputs X, Y & Z. When the decimal equivalent of the binary input is 0, 1, 3 or 5, the decimal equivalent of the binary output is one greater than the input and when decimal equivalent of the binary input is 2, 4, 6 or 7, the decimal equivalent of the binary output is one less than the input. *[3]*

B. (i) Simplify Boolean Expression $AB + AC + A\overline{C} + A\overline{B} + BC$ *[2]*

(ii) **Show that** $P\overline{Q} + Q\overline{R} + PR = P + Q\overline{R}$

5) What is Decoder? Implement a Full-Substractor circuit using 3-8 decoder having active-Low output lines and **2-input AND gates**. *[5]*

6) Design a **2-bit Priority Encoder** where the input priorities are defined as $D_1 > D_3 > D_0 > D_2$; where all D_i**'s** are inputs to the priority encoder. *[5]*