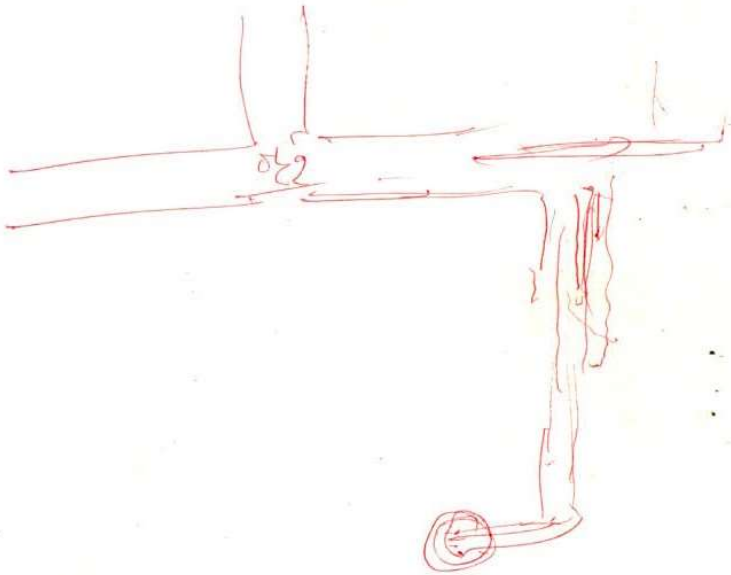

Ghanashyam Rout

(II [illegible] Regular)

DE[illegible] EC 402

(CSE, [illegible] E&TC, EE)

FOURTH SEMESTER EXAMINATION-2011

DIGITAL ELECTRONIC CIRCUITS

[EC 402]

Full Marks: 60 Time: 3 Hours

Answer any SIX questions including Question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. a) Show that NAND and NOR operations are not associative. [1 × 10
   b) What is the range of signed decimal numbers that can be represented by 6 bit binary number in 1's compliment form? Justify.
   c) What is the difference between positive and negative logic?
   d) What is the number of 4 × 16 decoders required to design a 8 × 256 decoder? Justify.
   e) What is the difference between SRAM and DRAM?
   f) Why is the fan-out of CMOS very high?
   g) Design a two-input n-mos NOR gate (only n-mos).
   h) In a 4-bit weighted resistor D/A converter, the resistance value corresponding to LSB is 32 KΩ. Find the resistance value corresponding to the MSB.
   i) A 4-bit synchronous counter uses Flip-Flop with overall propagation delay time of 15ns each. What will be the maximum possible time required for the change of state?

j) Find out the resulting output (Q(t)) of the FF for next 6 clock cycles assuming initial condition (Q=0 and $\overline{Q}$=1) for the following circuit in Figure-1(J).

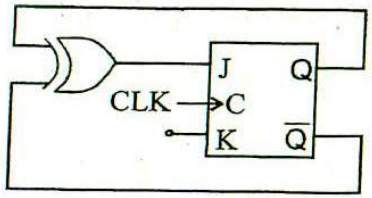

Figure-1(j)

2. a) Design a Johnson counter using D-FF to generate 8 timing signals. Make sure that the counter will be initialized with count value 0 (all FFs in reset state) when it is turned ON. Determine the count sequence for this counter and draw the decoding circuit needed to decode each state. [5

b) Find out all the states and the modulus of the counter shown in Figure-2(b). (Assume initially $Q_2\ Q_1\ Q_0$=111). [3

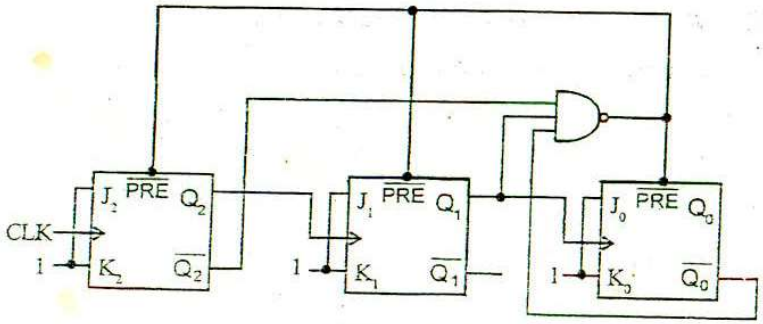

Figure-2(B)

recognized as logic-1 output is 4.5V. A negative noise voltage signal of 0.5V is added in the interconnecting wire between A and B. The noise margin is given as 0.3V. Find out the output of inverter B. Justify.

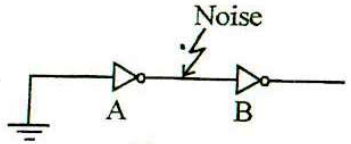

Figure-8(c)

d) Derive the Boolean expression f for the circuit implemented in Figure-8(d) using 2-input multiplexers. [2

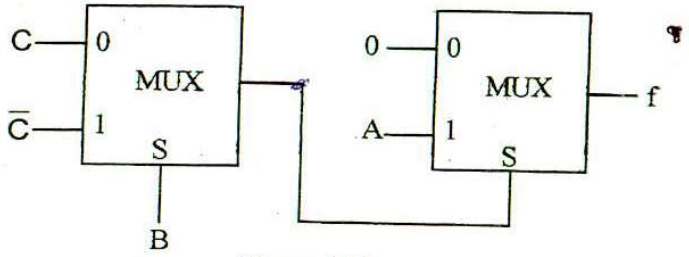

Figure-8(d)

xxxxx

8. a) Reduce the number of states in the state diagram given in the Figure-8(a). [4

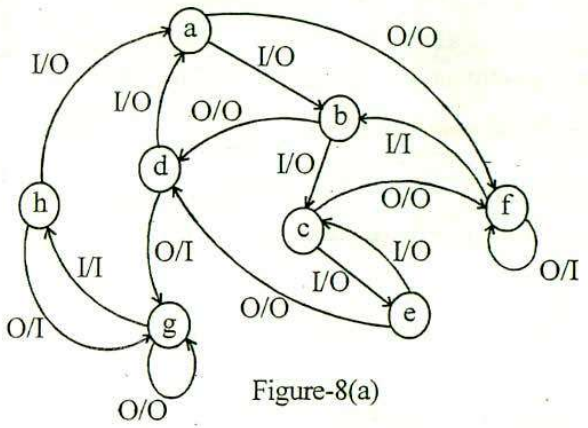

Figure-8(a)

b) The waveform shown in the Figure-8(b) are applied to a positive edge-triggered JK-FF with active low $\overline{PRESET}$ and $\overline{CLEAR}$. Draw the output waveform (Assume initially Q(t)=0). [2

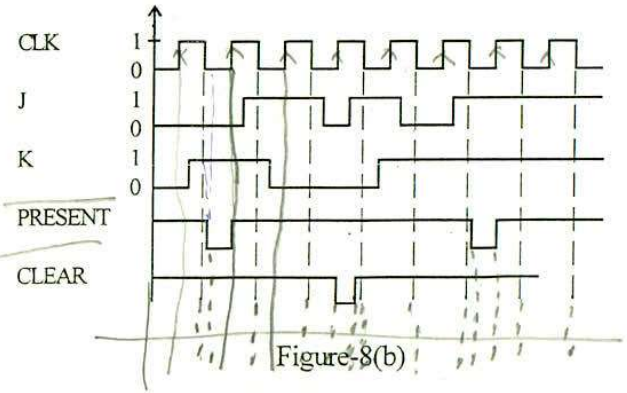

Figure-8(b)

c) In the circuit given in Figure-8(c), inverter A is driving inverter B. The minimum output voltage that can be [2

c) For the ring oscillator circuit shown below. Draw the output waveform $v_0(t)$ and find out the fundamental frequency of the oscillator if the propagation delay of each inverter is 100 pico sec. (Assume $v_0(t)=0$ for t=0). Figure-2(c). [2

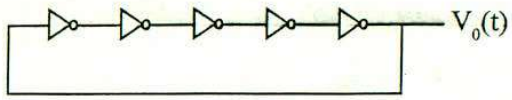

Figure-2(c)

3. a) Give the PLA realization of the following functions using PLA with 3 inputs (A, B, C) and 4 outputs. [4

$F_1(A, B, C) = \Sigma\, m(0, 1, 2, 4, 6)$

$F_2(A, B, C) = \Sigma\, m(0, 2, 6, 7)$

$F_3(A, B, C) = \Sigma\, m(3, 6)$

$F_4(A, B, C) = \Sigma\, m(1, 3, 5, 7)$

b) Design a complex CMOS function as given below [3

$$F = \overline{(A.B + C.D).E}$$

c) A 4-bit DAC circuit (Resolution=IV) is connected to a 3-bit up counter, as shown in the following figure. Draw the output waveform $v_0(t)$. (Assume Q_2 Q_1 Q_0=000 at t=0) {Figure-3(c)}. [3

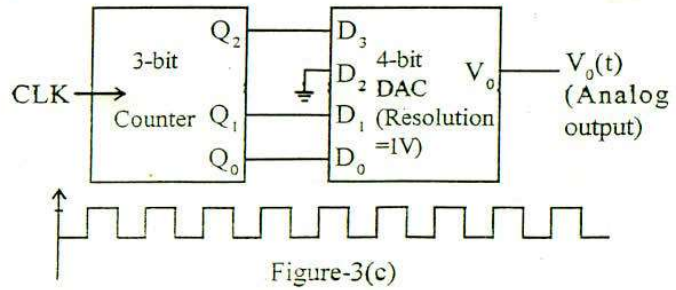

Figure-3(c)

4. a) Design an Astable multivibrator using 555 timer to generate a square wave of 2KHz frequency with 50% duty cycle. [3

b) With the help of a neat diagram explain the working of a two-input open-collector TTL NAND gate. [4

c) A certain memory has a capacity of 8K × 16. [1

(i) How many data I/P and O/P lines does it have?

(ii) How many address lines does it have?

d) Design a 4K RAM using 1K RAM chip with chip select input. [2

5. a) Design a synchronous sequential circuit which produces an output z=1, whenever any of the following input sequences 1101 or 1001 occurs. The circuit resets to the initial state after a 1 output is generated. [6

b) Draw the logic symbol and logic diagram of a 4-bit PISO shift Register using D-FF. [3

c) Determine the number of Flip-Flops and decoding gates required to design MOD-10 counter for the following topology: [1

(i) Ring Counter (ii) Johnson Counter

6. a) With the help of a neat diagram and suitable example explain the working of successive approximation type [4

A/D converter circuit. Compare its conversion time with the counter type A/D for a clock speed of 500 KHz.

b) Implement the following Boolean function using one 4:1 MUX and external gates [4

$$F(A\,B\,C\,D) = \sum(1, 3, 4, 11, 12, 13, 14, 15)$$

c) (i) Add $(-31.5)_{10}$ and $(-93.125)_{10}$ using 2's compliment arithmatic. [2

(ii) What is the Radix of the numbers if the solution to the quadratic equation $x^2-10x+31=0$ is x=5 and z=8?

7. a) Design a MOD-6 Ripple down counter using negative edge triggered JK-FF. [3

b) Design an alarm circuit using logic gates for which the specification is given as following: [3

"The ALARM output is 1 if the PANIC input is 1, or if the ENABLE input is 1, the EXITING input is 0 and the house is not SECURE; the house is SECURE if WINDOW, DOOR and GARAGE inputs are all 1".

c) State the differences between Mealy and Moore model for the following: [2

(i) Output (ii) Speed (iii) No. of states

d) What is the main problem associated with Binary parallel adder circuit and how is that overcome by using the look-ahead-carry adder circuit? [2