Digital Electronics
Question Paper Solution

Section A

Q 1- Illustrate with examples cyclic, reflective and self-complementary nature of codes. Also design a 4-bit binary to gray and gray to binary code converter circuits with minimum number of NAND gates

Solution –

Cyclic Codes - Cyclic codes are those in which each successive code word differs from preceding one in only one-bit position. They are also called unit distance codes.
e.g. Gray code in shafter **[1.5 Marks]**

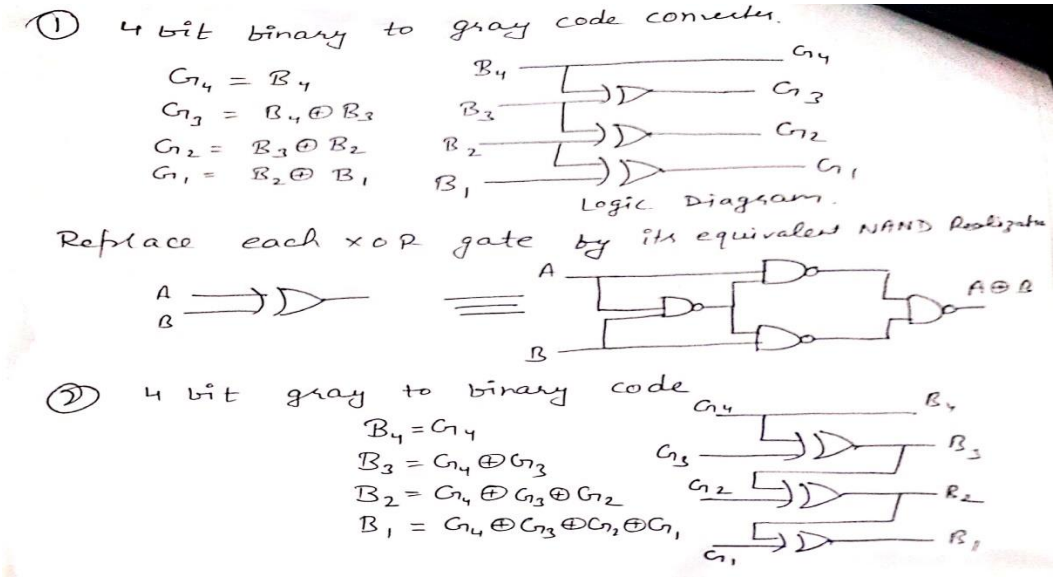
Reflective Codes – A reflective code is a binary code in which the n significant bits for code words 2^nThrough $2^{n+1} - 1$ are the mirror images of those for 0 through $2^n - 1$.
e.g Gray code **[1.5 Marks]**

Self-complementary Codes – A code is said to be self-complementary if the code word of the 9's complement of N i.e. 9-N can be obtained from the code word of N by interchanging all the 0s and 1s.
e.g. 2421,5211,642-3, 84-2-1 and XS-3. **[1.5 Marks]**

Design of 4 bit binary to gray -- **[3 Marks]** – Page 351-353 (FoDC by Anand Kumar)

Design of 4 bit gray to binary -- **[3 Marks]**

NAND Gate Realization **[2 Marks]**



Q 2- Design a counter that goes through the prime number states 0, 1, 3, 5, 7, 11, N, 0, 1… using D flip flop where N=17. If N=60, how many flip-flops are required. Also, Distinguish between Ring counter and Johnson counter. Comment on the states.

Solution – Counter States are 0,1,3,5,7,11,13,17, 0,1,…..

Q → Design of counter → 0, 1, 2, 3, 5, 7, 11, 13, 17, ; ②

Present State					Next State					Required Excitation				
Q_4	Q_3	Q_2	Q_1	Q_0	Q_4^+	Q_3^+	Q_2^+	Q_1^+	Q_0^+	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	1	0	0	0	1	0	0	0	0	1	0
0	0	0	1	0	0	0	0	1	1	0	0	0	1	1
0	0	0	1	1	0	0	1	0	1	0	0	1	0	1
0	0	1	0	1	0	0	1	1	1	0	0	1	1	1
0	0	1	1	1	0	1	0	1	1	0	1	0	1	1
0	1	0	1	1	0	1	1	0	1	0	1	1	0	1
0	1	1	0	1	1	0	0	0	1	1	0	0	0	1
1	0	0	0	1	0	0	0	0	0	0	0	0	0	0

By solving K-map – 5 variable →

$$D_4 = Q_3 Q_2$$

$$D_3 = Q_3 \overline{Q_2} + Q_2 Q_1$$

$$D_2 = Q_3 \overline{Q_2} + \overline{Q_3} Q_2 Q_1 + Q_1 Q_0 \overline{Q_2}$$

$$D_1 = \overline{Q_3} Q_2 + Q_1 \overline{Q_0} + Q_3 \overline{Q_2} + Q_4 \overline{Q_3} \overline{Q_2} \overline{Q_1} Q_0$$

$$D_0 = Q_1 + Q_2 + Q_3 + \overline{Q_0}$$

[7 Marks]

If N=60, how many flip-flops are required. - 6 Flip- Flops **[0.5 Marks]**

Distinguish between Ring counter and Johnson counter. **[4 Marks]**

Comment on the states. **[1 Marks]**

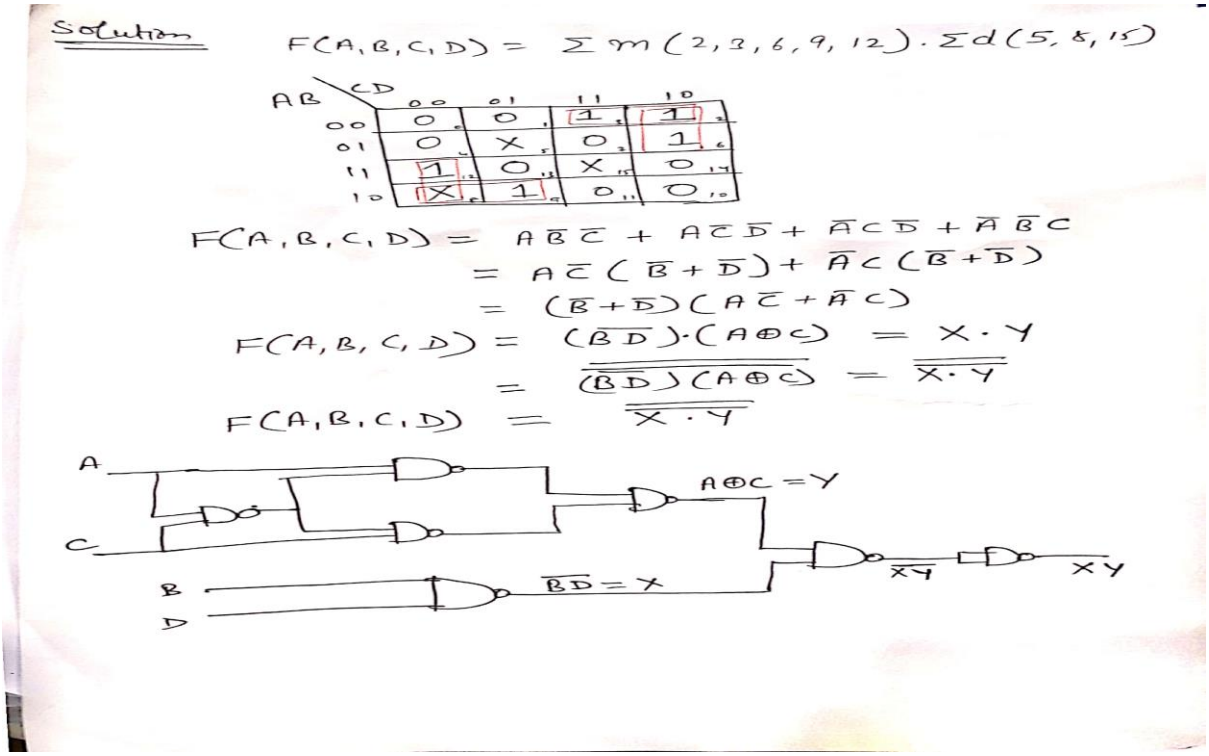
Section B

Q3 - Obtain a minimized expression for the following Boolean expression using K Map and implement the same using minimum number of NAND gate.

$$F(A,B,C,D) = \sum m(2,3,6,9,12) \cdot \sum d(5,8,15)$$

If F1 = ∑m(1,2,4,7) and F2 = ∑m(3,5,6,7), implement them using 3 to 8 line decoder. Comment on their logic operations.

Solution -



[5 +2 Marks]

F1 = ∑m(1,2,4,7) = Sum and F2 = ∑m(3,5,6,7)= Carry Out - [1 Marks]

Diagram Implementation of 3-8 Decoder [4.5 Marks]

$$S = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in} = A \oplus B \oplus C_{in} = \Sigma\, m(1, 2, 4, 7)$$

and $$C_{out} = \bar{A}BC_{in} + A\bar{B}C_{in} + AB\bar{C}_{in} + ABC_{in} = AB + (A \oplus B)C_{in} = \Sigma\, m(3, 5, 6, 7)$$

Since there are 3 inputs and a total of 8 minterms, we need a 3-to-8 line decoder. The implementation is shown in Figure 7.71. The decoder generates the 8 minterms for A, B, C_{in}. The OR gate for output S forms the logical sum of minterms 1, 2, 4 and 7. The OR gate for C_{out} forms the logical sum of the minterms 4, 5, 6 and 7.

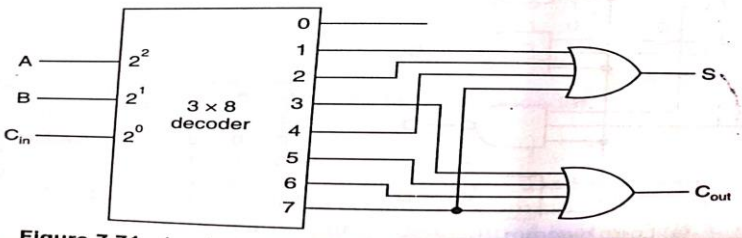


Figure 7.71 Logic diagram of a full adder using a decoder.

Q4 - Explain the working of Successive Approximation and Flash type analog to digital converter. Which one is the fastest and why? How many bits are required for a DAC so that full scale output is 15 V and resolution 200 mV.

Solution –

working of Successive Approximation and Flash type analog to digital converter. **[3 + 3 Marks]**

Fastest and Why ? - Flash type **[0.5 + 1 Marks]**

$$\text{resolution} = \frac{1}{\text{no. of steps}} \Rightarrow 200 \times 10^{-3} = \frac{1}{\text{no. of steps}}$$

$$no.\ of\ steps = \frac{1}{200 \times 10^{-3}} = 2^n - 1$$

$$2^n - 1 = 5 \Rightarrow 2^n = 6$$

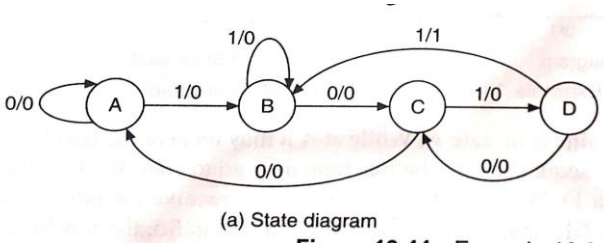
$$n = log_2 6 = 2.58 \cong 3bits$$ **[5 Marks]**

Q5 - Distinguish between Mealy and Moore model. Design a synchronous sequential circuit using Mealy model and D Flip flops which produces an output Z=1, when "1011" is detected. Assume Overlapping Detection is used.

Solution –

Distinguish between Mealy and Moore model **[5 Marks]**

Design of Sequence Detector **[3+1+1+2.5=7.5 Marks]**



(a) State diagram

PS	NS, z	
	x = 0	x = 1
A	A, 0	B, 0
B	C, 0	B, 0
C	A, 0	D, 0
D	C, 0	B, 1

(b) State table

[3 Marks]

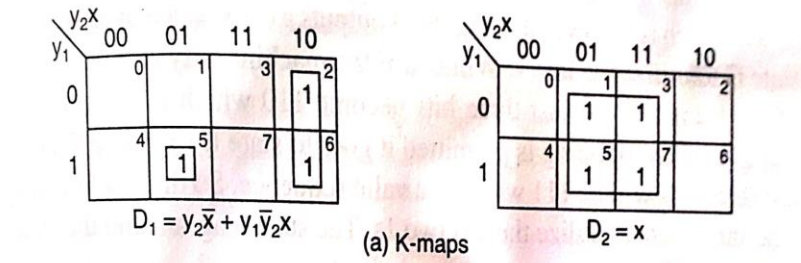
PS	NS (Y_1Y_2)		O/P (z)	
$y_1\ y_2$	x = 0	x = 1	x = 0	x = 1
A → 0 0	0 0	0 1	0	0
B → 0 1	1 0	0 1	0	0
C → 1 0	0 0	1 1	0	0
D → 1 1	1 0	0 1	0	1

[1 Marks]

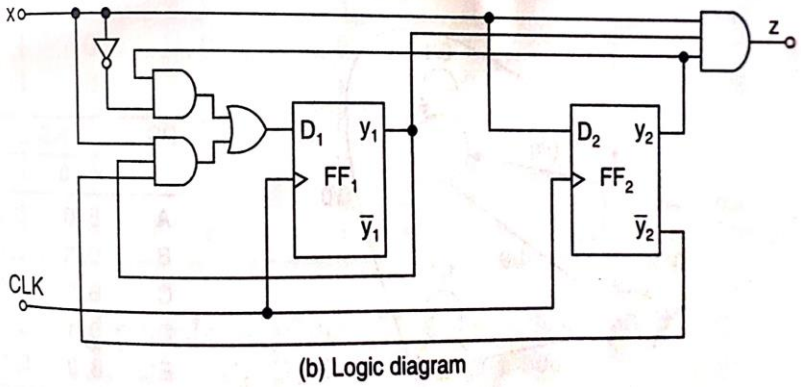
Table 13.19 Example 13.9: Excitation table

PS		I/P	NS		I/P to FFs		O/P
y_1	y_2	x	Y_1	Y_2	D_1	D_2	z
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0
0	1	0	1	0	1	0	0
0	1	1	0	1	0	1	0
1	0	0	0	0	0	0	0
1	0	1	1	1	1	1	0
1	1	0	1	0	1	0	0
1	1	1	0	1	0	1	1

[1 Marks]



(a) K-maps



(b) Logic diagram

[2.5 Marks]