no

unsigned no. (+ve)

Signed no. (+ve / -ve)

3 bit Reg.

Range = 0 - 7

n bit = 0 to $(2^n - 1)$

2^2	2^1	2^0	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

2's Compl.

MSB		LSB	
0	0	0	+0
0	0	1	+1
0	1	0	+2
0	1	1	+3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

+ve

-Ve

-3

01 10

(11)

2. What will be the content of the PC before and after SUB instruction is Fetched

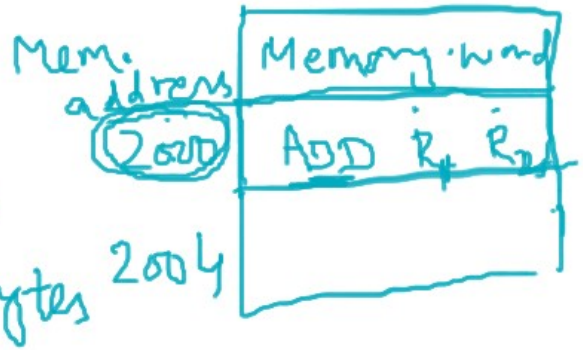
Mem Address	Memory word
2000	ADD
2004	SUB
2008	MOV
2012	CALL SUB1 (4000)
2016	OR

ans. : 2016

4000

3. What is difference between memory location, memory address and memory word. Give with an example

Memory Location



1 word = 4 bytes

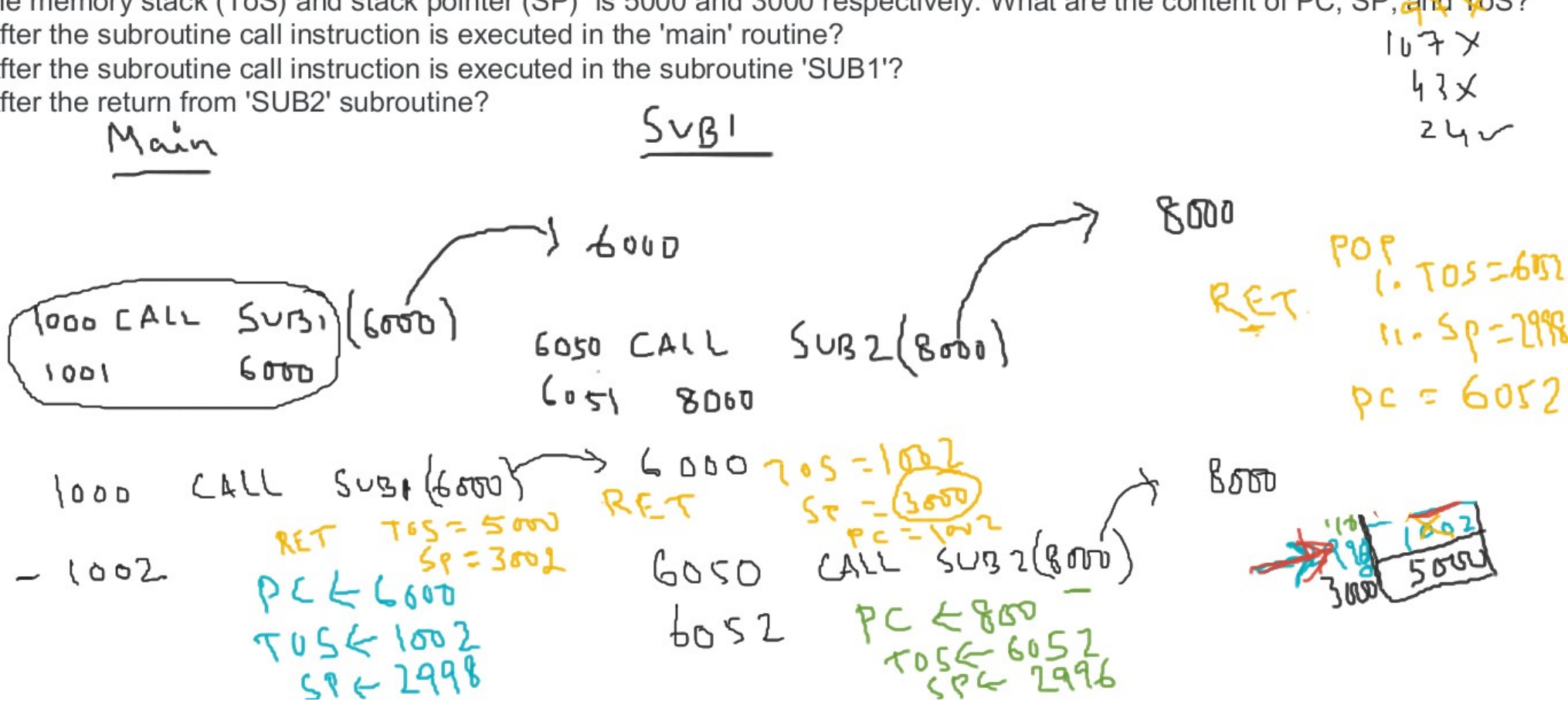
$R_1 \leftarrow [R_1] + [R_2]$

4. Assume you want to organize a nested subroutine calls on a computer as follows: the routine 'main' calls a subroutine 'SUB1' by executing a two-word call subroutine instruction located in memory at address 1000 followed by the address field of 6000 at location 1001. Again subroutine 'SUB1' calls another subroutine 'SUB2' by executing a two-word call subroutine instruction located in memory at address 6050 followed by the address field of 8000 at location 6051 . The content of the top of the memory stack (ToS) and stack pointer (SP) is 5000 and 3000 respectively. What are the content of PC, SP, and ToS?

i) After the subroutine call instruction is executed in the 'main' routine?

ii) After the subroutine call instruction is executed in the subroutine 'SUB1'?

iii) After the return from 'SUB2' subroutine?



Additional Instructions

Types of Instruction:

i. Arithmetic Instructions: ADD, SUB, DIV, MUL

ii. Logical Instruction : OR AND, XOR etc.

iii. Control Instruction : JMP, JC,

iv. Data transfer Instruction : MOV ,LOAD, Store

v. Input Output : IN, OUT

Control Instruction :

-> Do not execute the next PC value.
-> Transfer control to another part of the instruction space

Two Types :

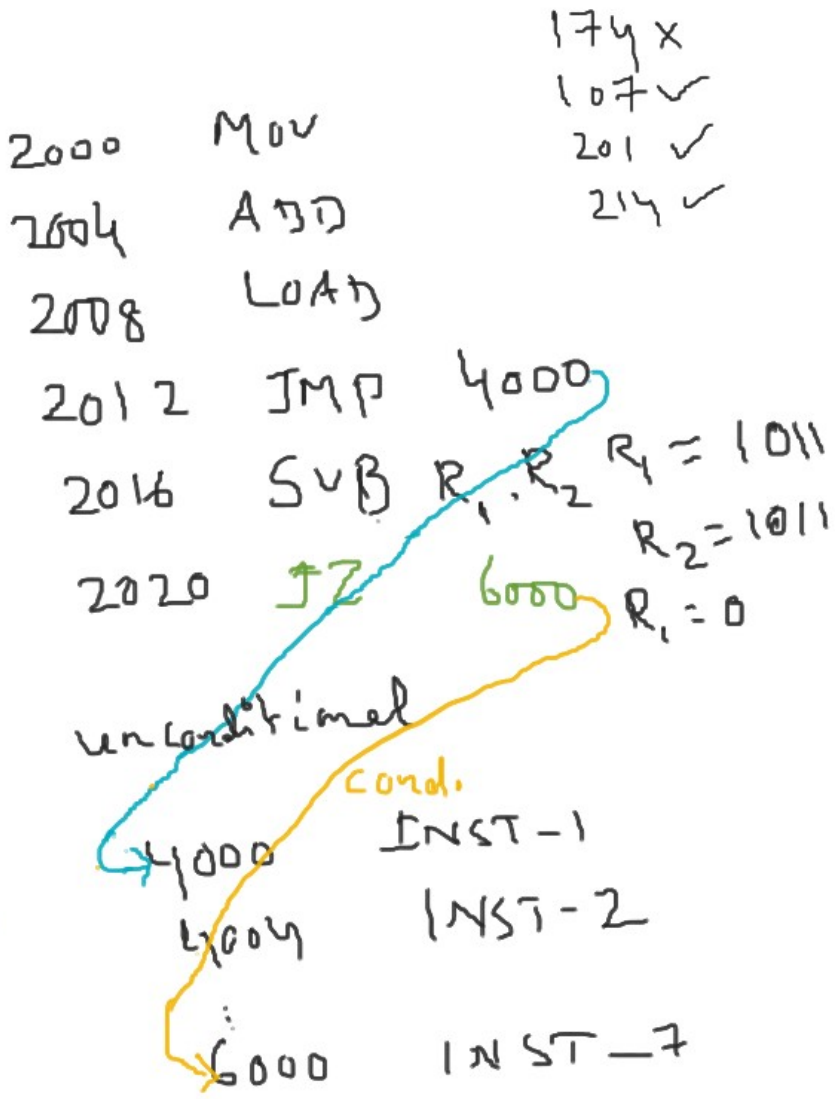
unconditional JMP , CALL of a Subroutine etc

Conditional Only jump to branch target if the condition is true

Ex: JC //Jump if Carry

JZ //Jump if Zero

JN // Jump on negative



Logical Instruction

D/S_2 S_1

AND R1,R2

MSB LSB

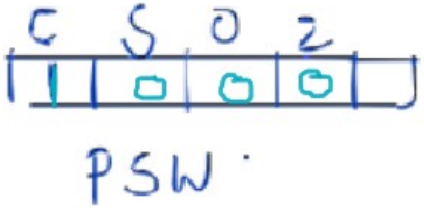
R1 0101

R2 1001

R1 0001

Program Status Word: 8 bits

One of the register is used as PSW which contains the status of different flag bit (carry bit, Sign bit, Overflow bit, zero bit etc)



PSW

Carry ✓

+ve no.

result not erroneous

result o/p is nonzero

Additional Instructions :

i. Shift Instructions
   - Arithmetic Shift
   - Logical Shift

ii. Rotate Instructions:

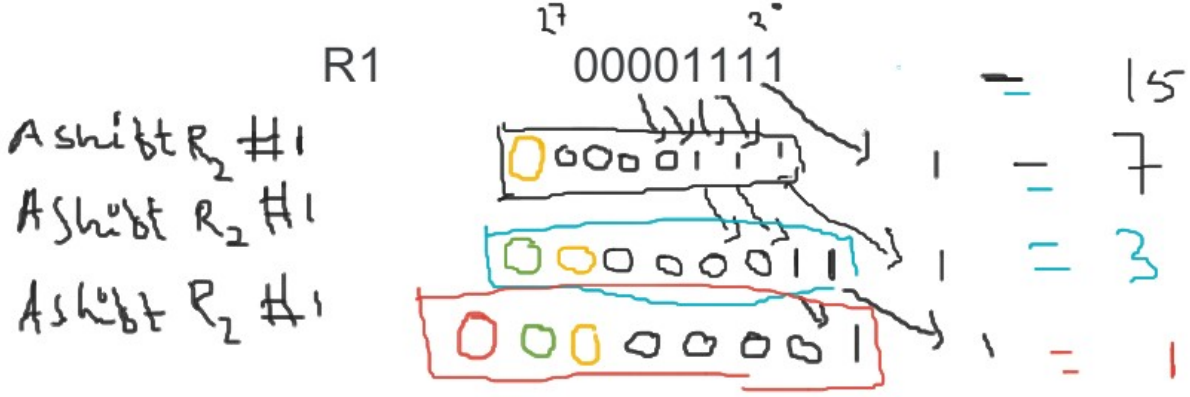
Arithmetic Shift

- Arithmetic Left — `AshiftL R1, R1, #n` (dst, src, no. of bit) — `AshiftL R1,R1, #2`
- Arithmetic Right — `AshiftR R2, R2, #n` (dst src, no. of bits) — `AshiftR R2,R2,#3`

Unsigned Number

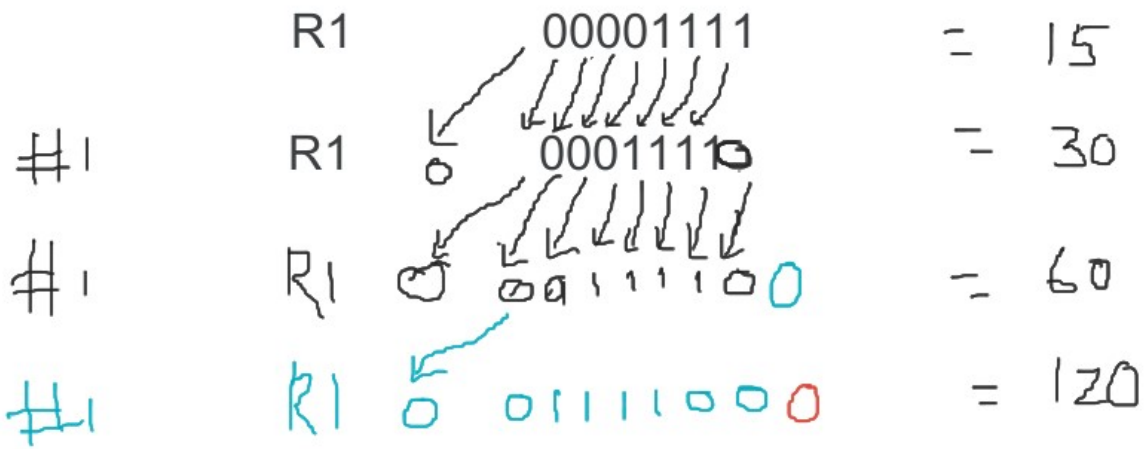
AshiftR R1,R1 #3

Right shift = division



AshiftL R1,R1 #3

Left shift = multiply



Signed Representation (using 2's Compliment)

How to represent -5 using 2s compliment

Sign bit is the MSB if 0 +ve no., if 1 -ve no

8-bit representation of +12 and – 12

+ 12 = 00001100

MSB

Signed Magnitude

LSB

Signed 1's Complement

Signed 2's Complement

MSB

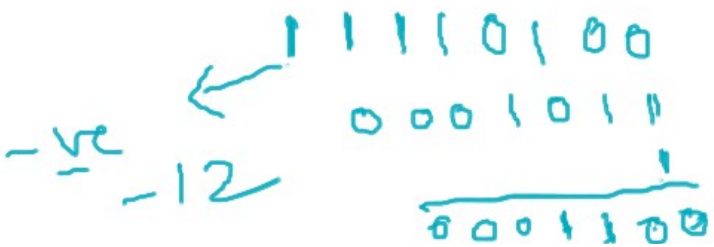
– 12 = 10001100

Signed Magnitude

Signed 1's Complement

Signed 2's Complement

+1



AshiftL R1,R1 #1

R1 110 = −2

R1 100 = −4

AshiftL R1,R1 #2

R1 111 = −1

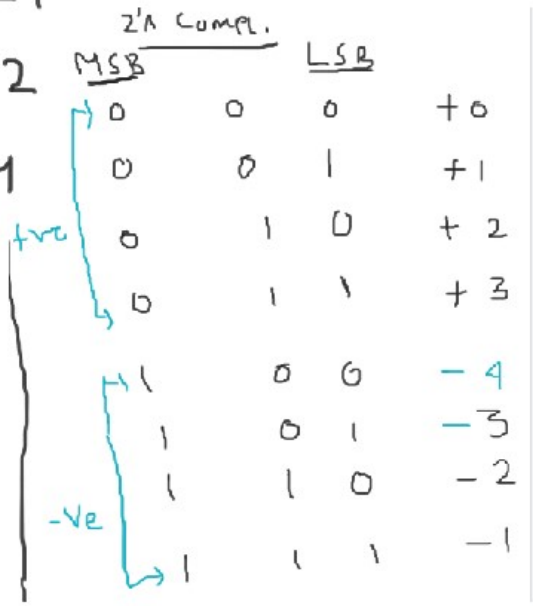
110 = −2

100 = −4

AshiftR R1,R1 #2

R1 111 = −1

111 = −1



AshiftR R1,R1 #1

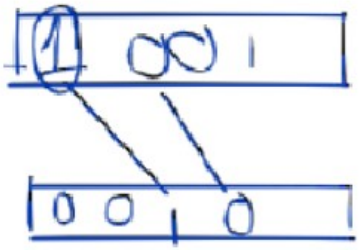
R1 110 = −2

1 1 1 → 0 = −1

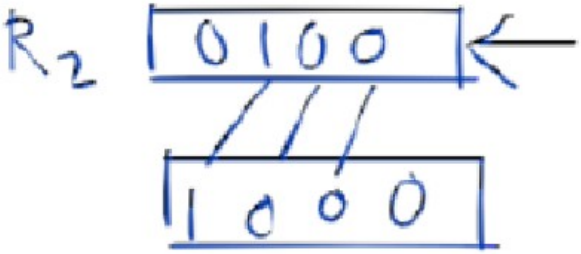
In signed no when we shift the bits in right the MSB must be filled with bit 1

Logical Shift

```
LShiftR R1,R1, #2
```

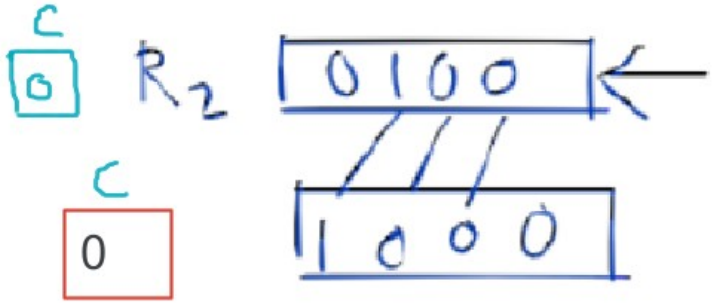



```
LshiftL  R2,R2, #1
```

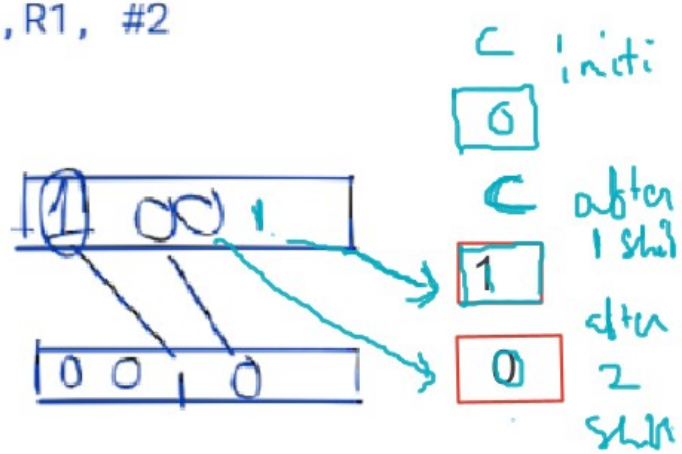


Shift with Carry

LshiftLc R2, R2, #1



LShiftRc R1, R1, #2



Rotate Instruction

ROT R R1,R1 #2

R1 1001

R1 1100

R1 0110

ROT L R1,R1 #2

R1 1001

R1 0011

R1 0110

1. Represent -12 in 2s compliment in a reg. of 8bits(including the sign bit) perform the arithmetic left and right shift by 2 bits and present the results in decimal value

-12 8+4

Reg. 8 bits

10001100 = -12

1 1 1 0 0 1 1 1's

+ 1

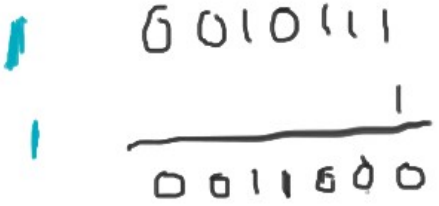
R1  -6

-3

Ashift L

#1  = -24 ✓

#1 1 1 0 1 0 0 0 0 = -48



2. The content of register R1is 11010101. What will be the decimal value after execution of AShiftR #2, R1. [Assume the number is represented in 2's complement format]

8 bit

11010101 in (-ve)

Sign

01010101's

1

01011

2 | 43
2 | 21
2 | 10

3. The content of Register R1 is 00001100. What will be the decimal value in R1 after executing the AShiftR #2,R1.

$2^3\ 2^2$

+Ve = +12

#1 R_1 = 00000110 + 6

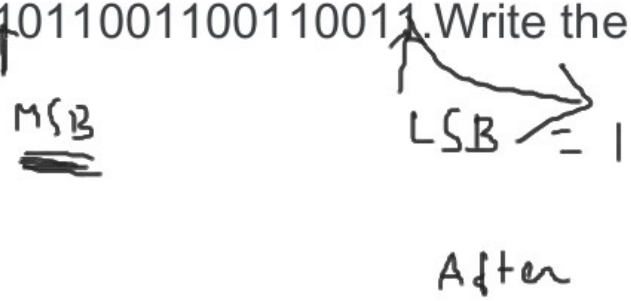
#1 = 00000011 + 3

(ans)

4. The content of register R1 is 1011001100110011. Write the instruction for performing the following operations:

i. Clear the LSB of R1 to 0.

ii. Set the MSB of R1 to 1.



RISC	VS	CISC
Reduced Instruction Set Computer		Complex Instruction Set Computer
Format of inst is fixed one		Format of the Instr is Varying
Pipeline is easy in RISC machine	→	Pipeline is very difficult to implement