Sequential Circuits

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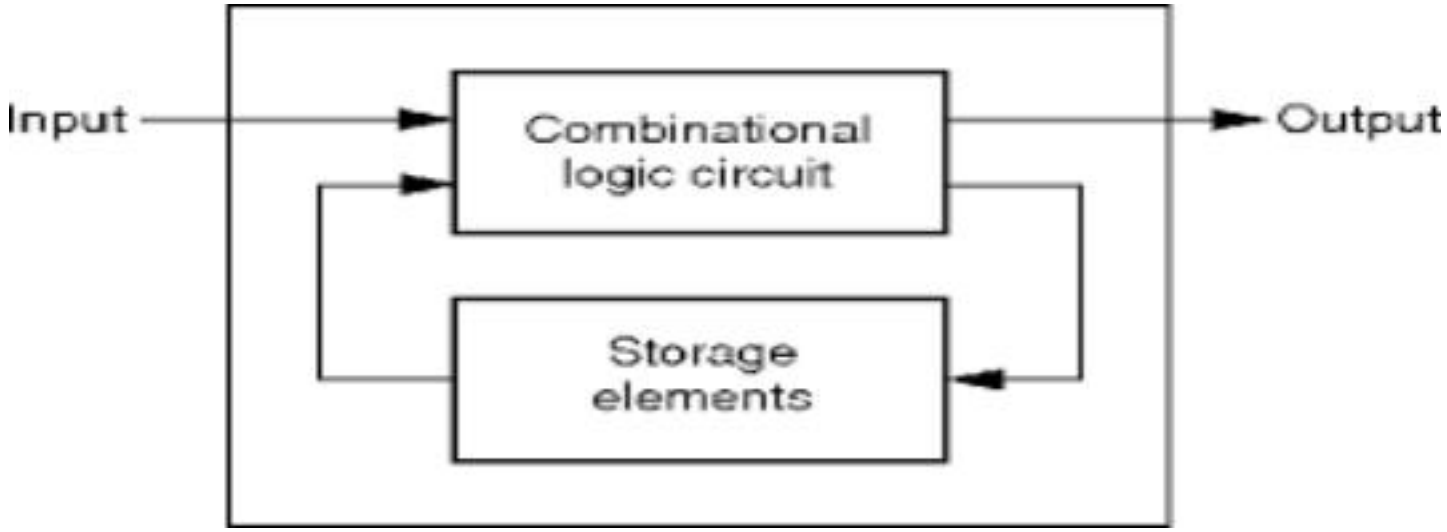
Sequential Logic circuits

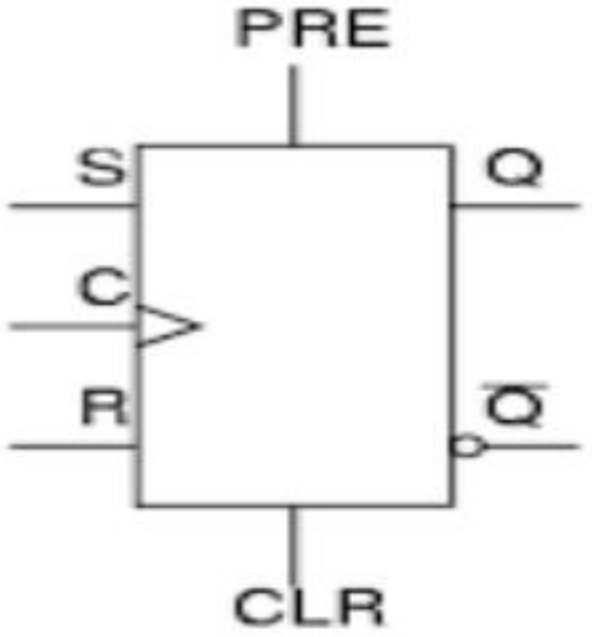


Sequential Logic circuits

- Sequential Logic circuits have some form of inherent “Memory” built in.
- The output state of a “sequential logic circuit” is a function of the “present input”, and/or the “past output”.

SR Flip-Flop

- Synchronous Inputs are S (set) and R (reset)
- Asynchronous inputs are PRE(preset) and CLR(clear)



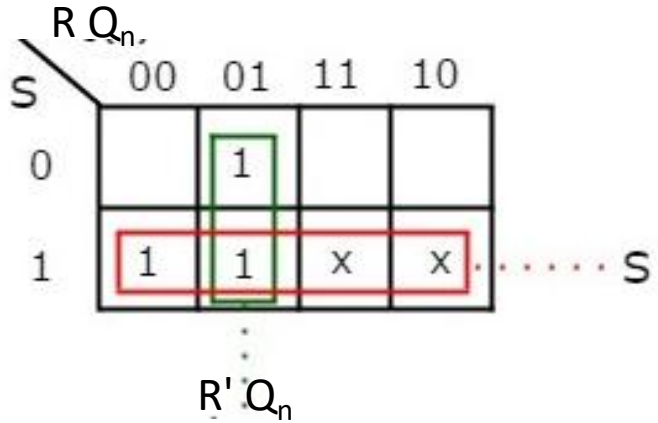
S	R	Q_{n+1}	
0	0	Q_n	No change in state
0	1	0	Reset condition
1	0	1	Set condition
1	1	-	Forbidden state

State Table of S-R Flip-flop

Where Q_n represent the present state of the flip-flop.
Where Q_{n+1} represent the next state of the flip-flop.

Truth table of SR flip-flop

Inputs		Present State	Next State
S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X



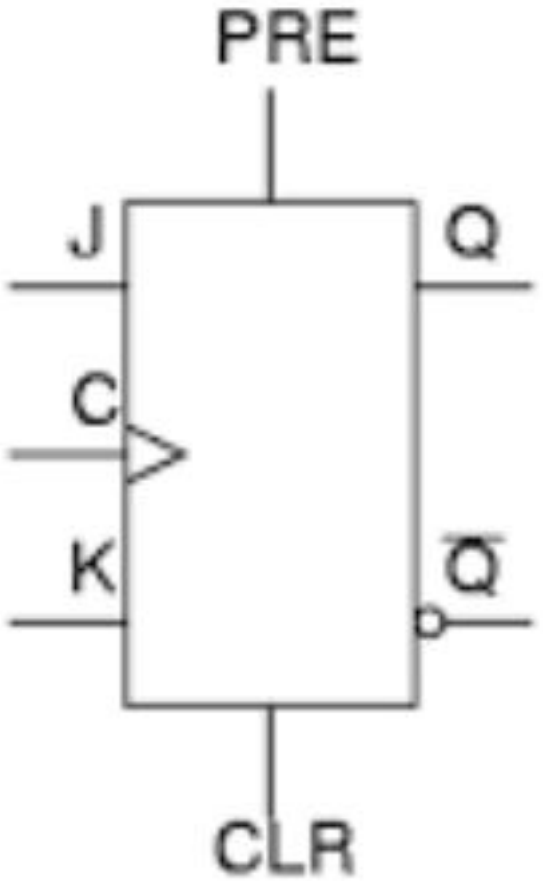
$$Q_{n+1} = S + R' Q_n$$

Charecteristic Equation of SR flip-flop

JK Flip-Flop

J	K	Q_{n+1}	
0	0	Q_n	No change in state
0	1	0	Reset Condition
1	0	1	Set Condition
1	1	Q_n'	Toogle

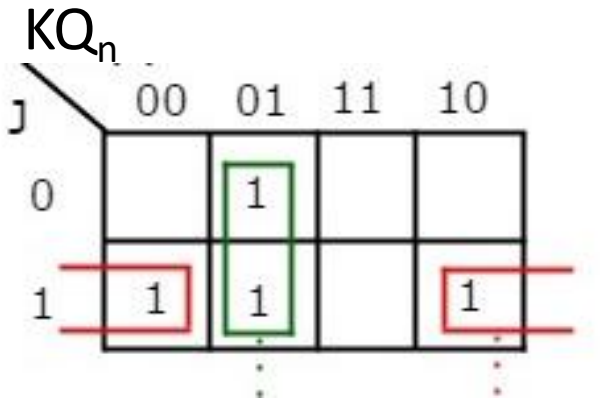
State Table of J-K Flip-flop



Where Q_n represent the present state of the flip-flop.
Where Q_{n+1} represent the next state of the flip-flop.

Truth table of JK flip-flop

Present Inputs		Present State	Next State
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



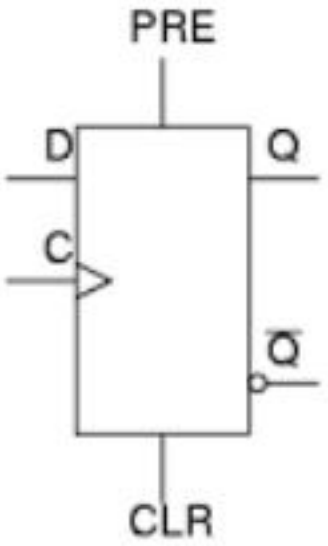
$$Q_{n+1} = J\,Q_n' + K'\,Q_n$$

Charecteristic Equation of JK flip-flop

D Flip-Flop

D	Q_{n+1}
0	0
1	1

State Table of D Flip-flop



D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Truth Table of D Flip-flop

Where Q_n represent the present state of the flip-flop.
Where Q_{n+1} represent the next state of the flip-flop.

$$Q_{n+1} = D$$

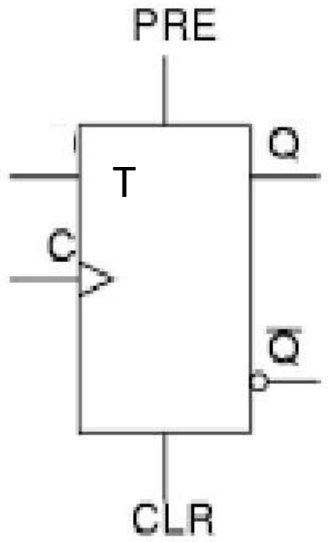
Charecteristic Equation of D flip-flop

T Flip-Flop

T	Q_{n+1}	
0	Q_n	No change
1	Q_n'	Toggle

State Table of T Flip-flop

Where Q_n represent the present state of the flip-flop.
Where Q_{n+1} represent the next state of the flip-flop.



T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Truth Table of D Flip-flop

$$Q_{n+1} = T' Q_n + T Q_n'$$

Charecteristic Equation of D flip-flop

Excitation Table of Flip-flops

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

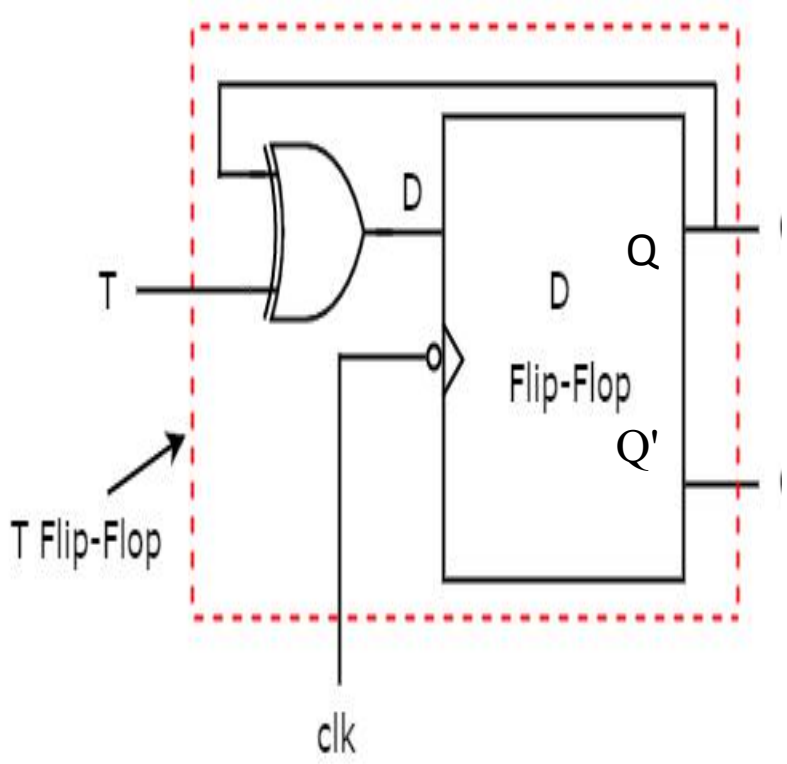
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

D flip-flop to T flip-flop conversion

T flip-flop input	Present State	Next State	D flip-flop input
T	Q_n	Q_{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

Conversion table

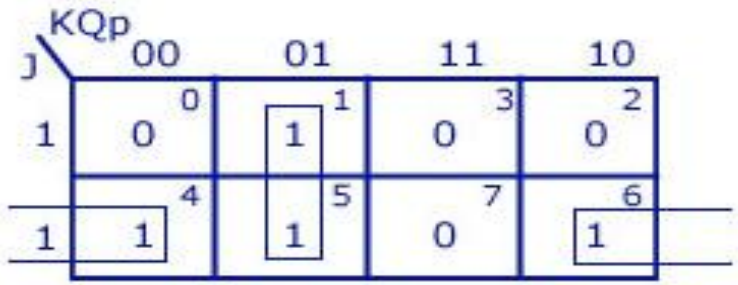


$$D(T,Q_n) = \sum m\,(1,2) = (T \oplus Q_n)$$

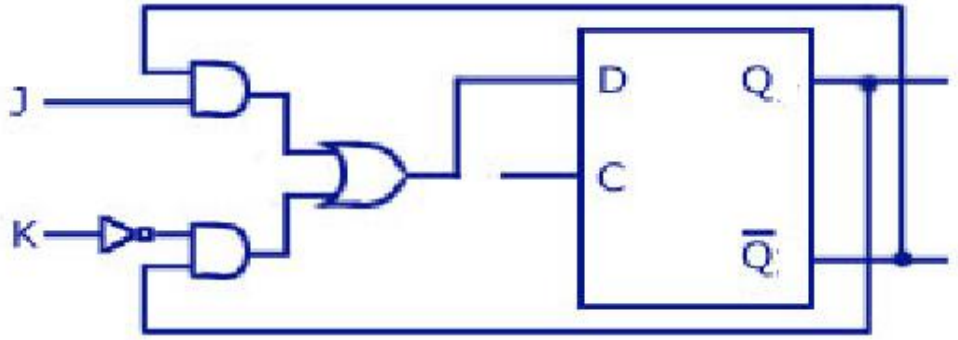
D Flip Flop to JK Flip Flop conversion

J	K	Q_n	Q_{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

Conversion table

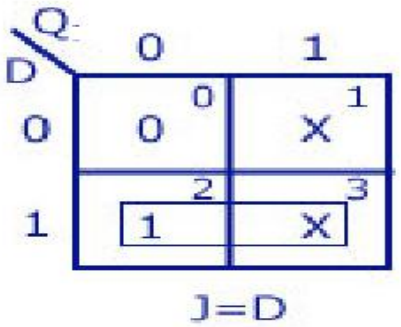


$D\ (J,K,Q_n) = \sum m\ (1,4,5,6) = JQ_n' + K'\ Q_n$

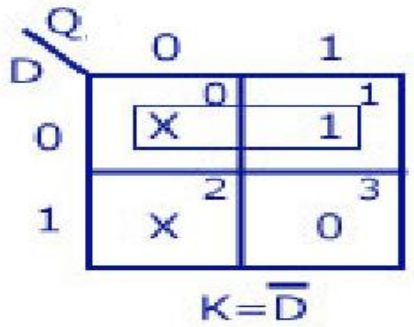


JK Flip Flop to D Flip Flop

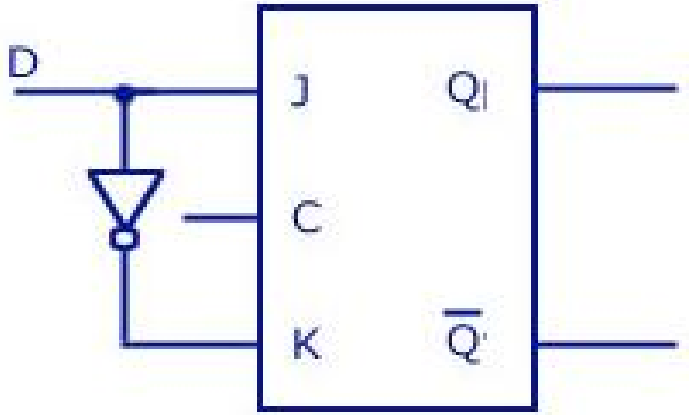
D	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0



J=D



$K=\overline{D}$

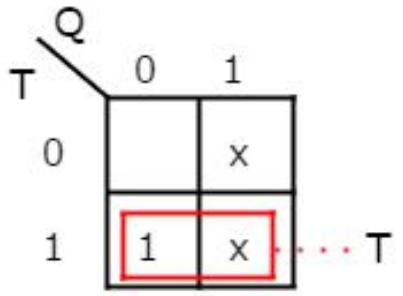


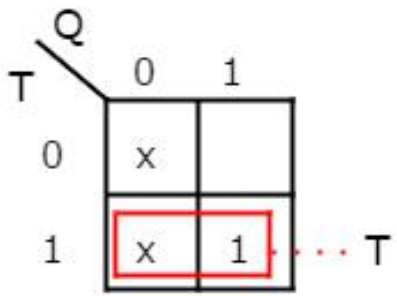
$J(D,Q_n) = \sum m\,(2) + d(1,3)$

$K(D,Q_n) = \sum m\,(1) + d(0,2)$

JK Flip Flop to T Flip Flop

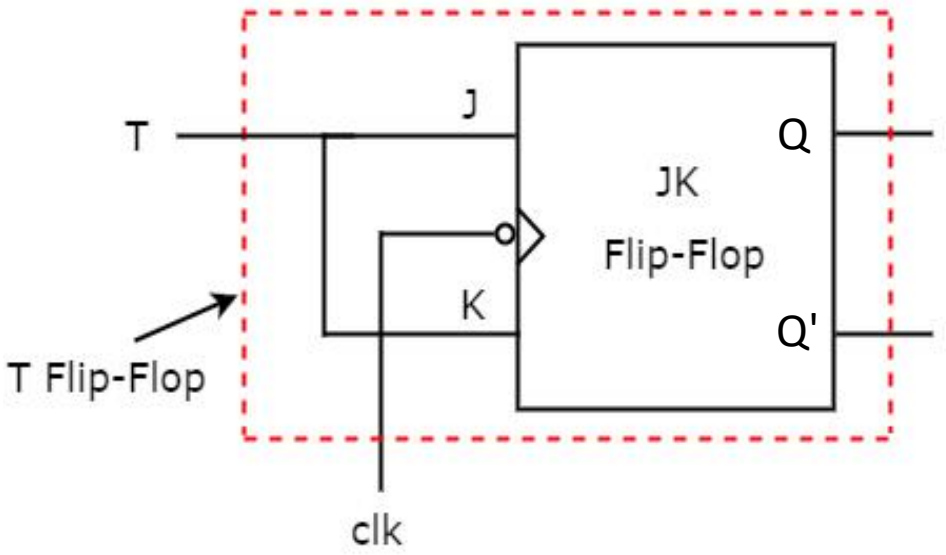
T	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1



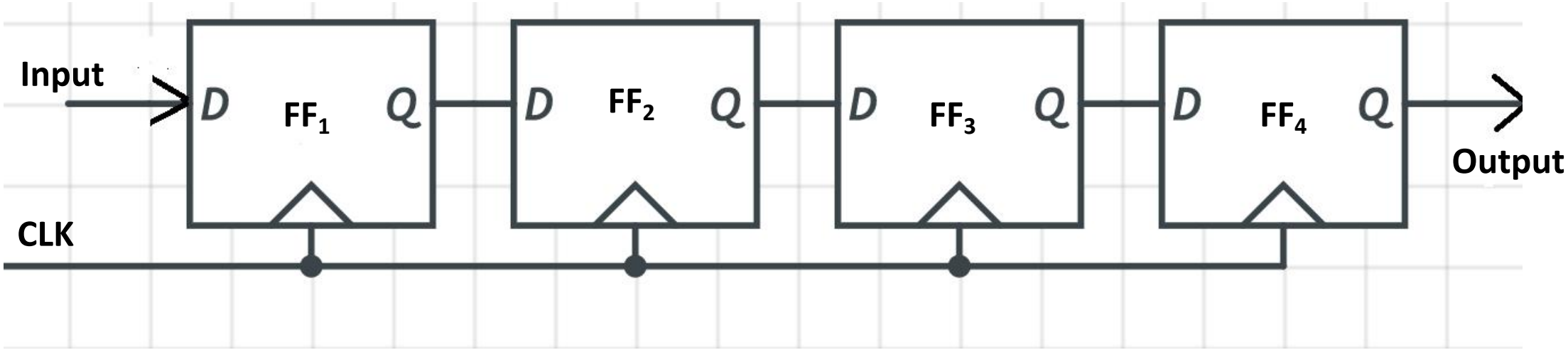


$$J(T,Q_n) = \sum m\,(2) + d(1,3)$$

$$K(T,Q_n) = \sum m\,(3) + d(0,2)$$



4 -bit Serial input Serial output register (SISO)



All these flip-flops are synchronous with each other since, the same clock signal is applied to each one.
The output of one D flip-flop is connected as the input of next D flip-flop.
In this shift register, we can send the bits serially from the input of left most D flip-flop. Hence, this input is also called as **serial input**.
For every positive edge triggering of clock signal, the data shifts from one stage to the next.
So, we can receive the bits serially from the output of right most D flip-flop. Hence, this output is also called as **serial output**.

Working of 4-bit SISO shift register

C P	Serial Input	Q_1	Q_2	Q_3	Q_4
0	-	0	0	0	0
1	b_1	b_1	0	0	0
2	b_2	b_2	b_1	0	0
3	b_3	b_3	b_2	b_1	0
4	b_4	b_4	b_3	b_2	b_1
5	-	-	b_4	b_3	b_2
6	-	-	-	b_4	b_3
7	-	-	-	-	b_4

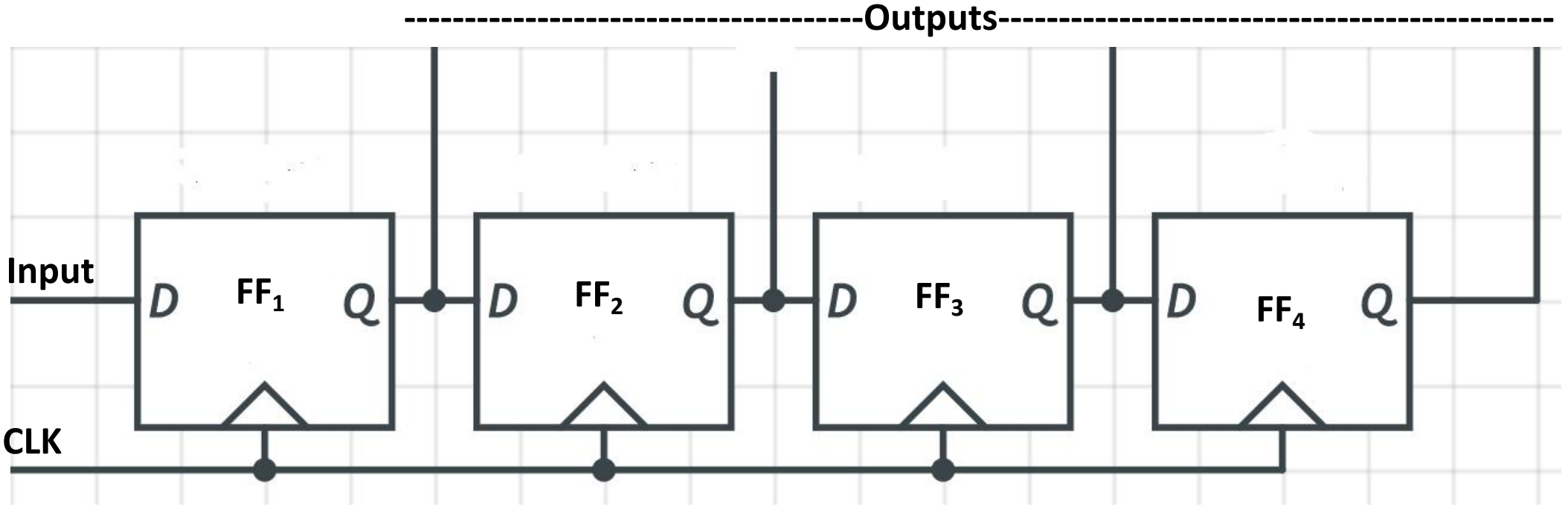
Where b_1, b_2, b_3, b_4 , binary either 0 or 1.
Assume, initial status of the D flip-flops from leftmost to rightmost is $Q_1\ Q_2\ Q_3\ Q_4$ = "0000"
Here, the serial output is coming from Q_4.

So, the LSB b_1 is received at 4th clock and the MSB b_4 is received at 7th clock.

Therefore, the 4-bit SISO shift register requires 7 clock pulses in order to produce the output.

Similarly, the N-bit SISO shift register requires (2N-1)clock pulses in order to shift 'N' bit information i.e N clock pulses to load the data and next N-1 clock pulses to take the data out.

4 -bit Serial input Parallel output register (SIPO)



In this shift register, we can send the bits serially from the input of left most D flip-flop. Hence, this input is also called as **serial input**.

For every positive edge triggering of clock signal, the data shifts from one stage to the next.

In this case, we can access the outputs of each D flip-flop in parallel. So, we will get **parallel outputs** from this shift register.

Working of 4-bit SIPO shift register

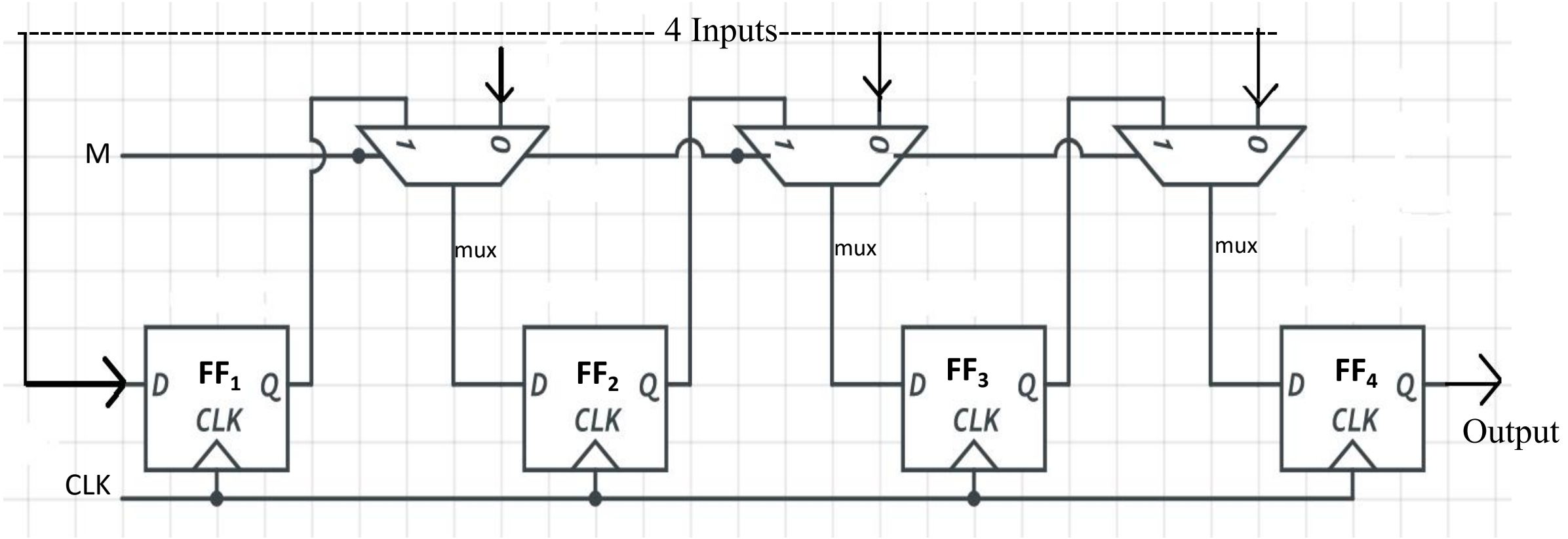
C P	Serial Input	Q_1	Q_2	Q_3	Q_4
0	-	0	0	0	0
1	b_1	b_1	0	0	0
2	b_2	b_2	b_1	0	0
3	b_3	b_3	b_2	b_1	0
4	b_4	b_4	b_3	b_2	b_1

Where b_1, b_2, b_3, b_4 , binary either 0 or 1.
Assume, initial status of the D flip-flops from leftmost to rightmost is $Q_1\ Q_2\ Q_3\ Q_4$ = "0000"
The binary information is obtained in parallel at the outputs of D flip-flops at 4th clock pulse.

So, the 4-bit SIPO shift register requires four (4) clock pulses in order to produce the output.

Similarly, the N-bit SIPO shift register requires "N" clock pulses in order to shift 'N' bit information i.e "N" clock pulses to load the data and no extra clock pulses to take the data out.

4 -bit Parallel input Serial output register (SIPO)



In this shift register, we can apply the **parallel inputs** to each D flip-flop.
For every positive edge triggering of clock signal, the data shifts from one stage to the next. So, we get the **serial output** from the right most D flip-flop.

Working of 4-bit PISO shift register

C P	Parallel Input	Q_1	Q_2	Q_3	Q_4
0	$b_4b_3b_2b_1$	0	0	0	0
1	-	b_4	b_3	b_2	b_1
2	-	-	b_4	b_3	b_2
3	-	-	-	b_4	b_3
4	-	-	-	-	b_4

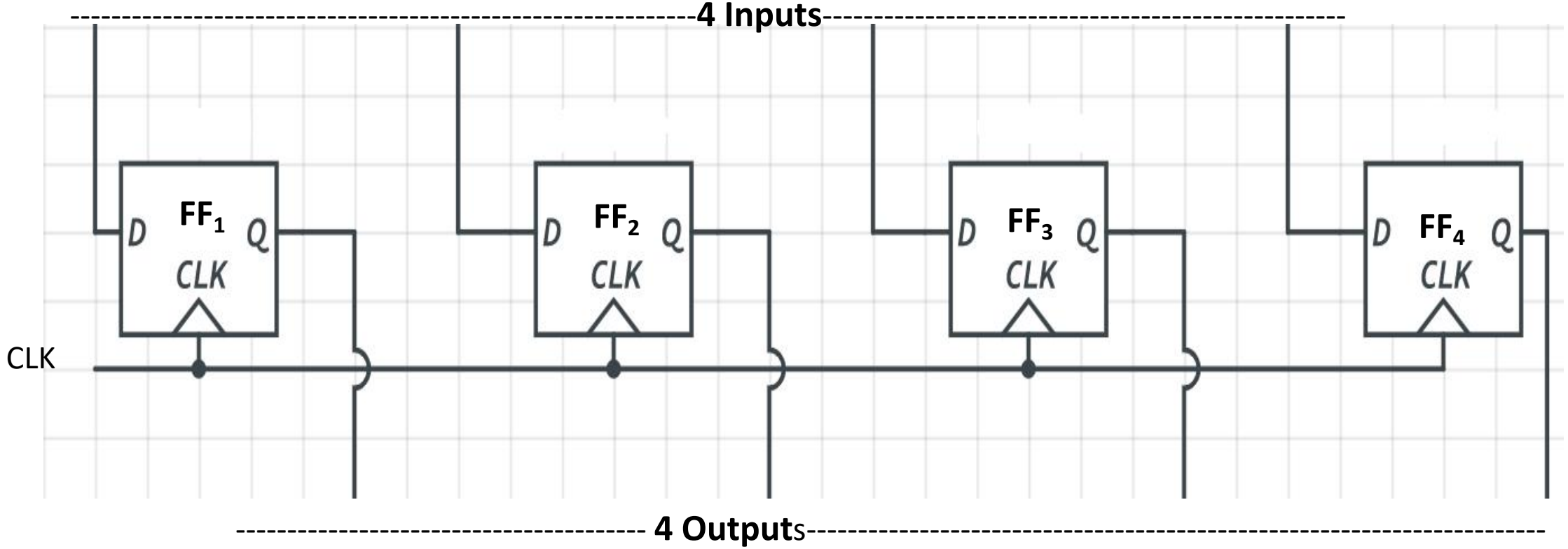
Where b_1,b_2,b_3,b_4 , binary either 0 or 1.
Assume, initial status of the D flip-flops from leftmost to rightmost is Q_1 Q_2 Q_3 Q_4 = "0000"

Here, the serial output is coming from Q_4 .
So, the LSB b_1 is received before applying 1st clock pulse and the MSB b_4 is received at 4th clock pulse.

Therefore, the 4-bit PISO shift register requires 4 clock pulses in order to produce the valid output.

Similarly, the N-bit PISO shift register requires (N-1) clock pulses in order to shift 'N' bit information i.e "1" clock pulses to load the data and next "N-1" clock pulses to take the data out.

4 -bit Parallel input Paralle output register (PIPO)



In this shift register, we can apply the **parallel inputs** to each D flip-flop.

In this case, the effect of outputs is independent of clock transition. So, we will get the **parallel outputs** from each D flip-flop.

Working of 4-bit PIPO shift register

C P	Parallel Input	Q_1	Q_2	Q_3	Q_4
0	$b_4b_3b_2b_1$	0	0	0	0
1	-	b_4	b_3	b_2	b_1

Where b_1,b_2,b_3,b_4 , binary either 0 or 1.
Assume, initial status of the D flip-flops from leftmost to rightmost is Q_1 Q_2 Q_3 Q_4 = "0000"

So, the binary information is obtained in parallel at the outputs of D flip-flops applying clock pulse.

Therefore, the 4-bit PIPO shift register requires one(1) clock pulses in order to produce the output.

Similarly, the N-bit PIPO shift register require one(1) clock pulse in order to shift 'N' bit information.

Counters

Counter is a sequential circuit which is used for a counting pulses. Counter is the widest application of flip-flops.

- There are two types of counters based on the clock connected in flip-flops.

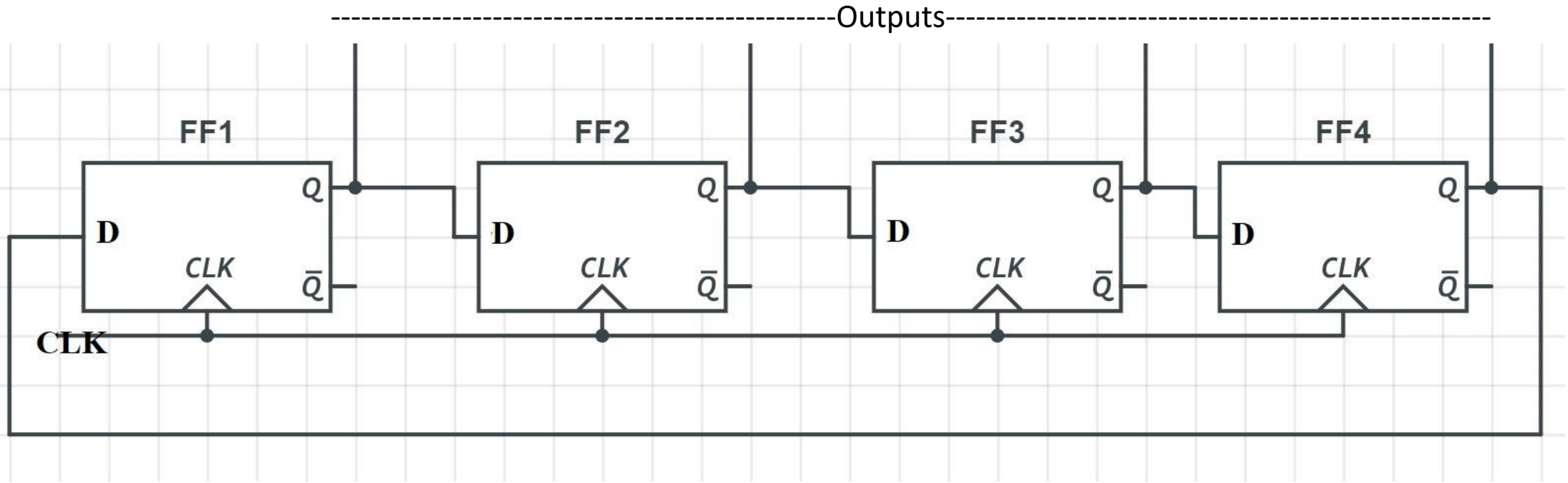
1. Asynchronous counters - If the flip-flops do not receive the same clock signal, then that counter is called as Asynchronous counter.The output of system clock is applied as clock signal only to first flip-flop. The remaining flip-flops receive the clock signal from output of its previous stage flip-flop. Hence, the outputs of all flip-flops do not change affect at the same time. It is also called RIPPLE counter.

2. Synchronous counters - If the flip-flops receive the same clock signal, then that counter is called as Synchronous counter.If all the flip-flops receive the same clock signal, then that counter is called as Synchronous counter. Hence, the outputs of all flip-flops change affect at the same time

Design Procedure of Counter

1. Find the number of FFs (flip-flop) required.
2. Draw a state diagram for a given sequence.
3. Draw the FF transition table (excitation table).
4. Use K-map to derive the logic expressions of inputs of FFs.
5. Implemention using FFs and required combinational logic(gates).

4-bit or MOD-4 Ring Counter



The 4-bit Ring counter contains only a 4-bit SIPO shift register.
The output of rightmost D flip-flop(FF4) is connected to serial input of left most D flip-flop(FF1).

Working of 4-bit or MOD-4 Ring Counter

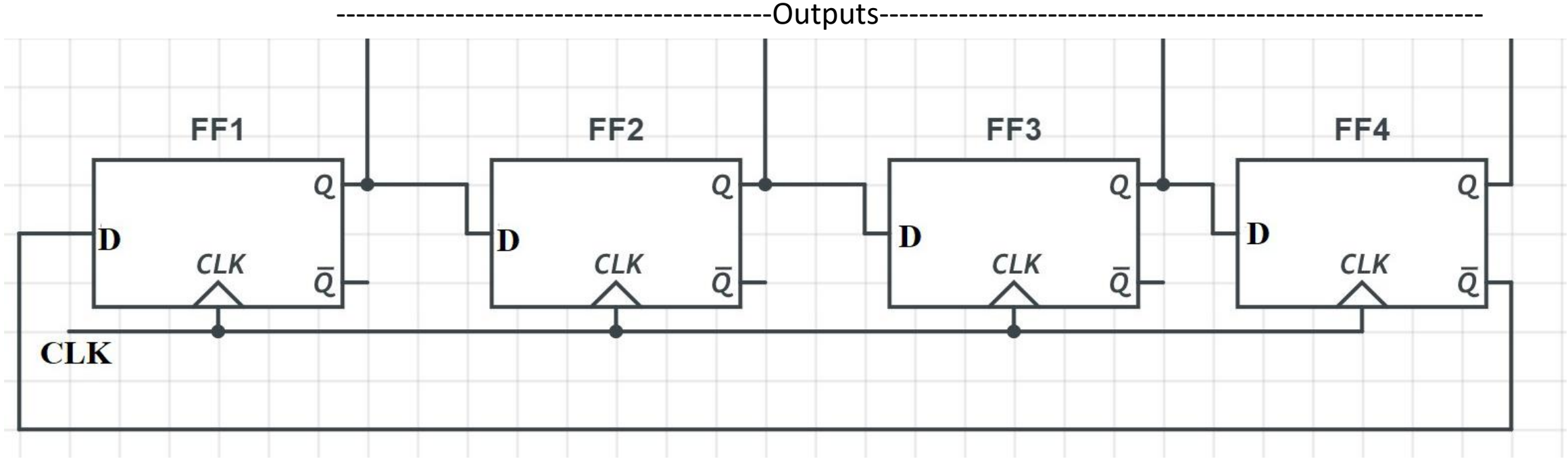
Clock Pulse	Q_1	Q_2	Q_3	Q_4
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0

Assume, initial status of the D flip-flops from leftmost to rightmost is Q_1 Q_2 Q_3 Q_4 = "1000" .

This status repeats for every four(4) clock pulse.

A "mod-n" ring counter will require "n" number of flip-flops connected together to circulate a single data bit providing "n" different output states.
Each state repeats after every "n" clock pulse.

4-bit or MOD-8 Twisted Ring (Johnson) Counter



The 4-bit Johnson counter contains only a 4-bit SIPO shift register.
The complemented output of rightmost D flip-flop(FF4) is connected to serial input of left most D flip-flop(FF1).
A “mod-2n”Johnson counter will require “n” number of flip-flops connected together to circulate a single data bit providing “2n” different output states.

Working of 4-bit or MOD-8 Johnson Counter

Clock Pulse	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Assume, initial status of the D flip-flops from leftmost to rightmost is Q_1 Q_2 Q_3 Q_4 = “0000” .

This status repeats for every four(8) clock pulse.

A “mod-2n” ring counter will require “n” number of flip-flops connected together to circulate a single data bit providing “2n” different output states.

Each state repeats after every “2n” clock pulse.