SPRING END SEMESTER EXAMINATION-2015

6th Semester B.Tech

COMPUTER ORGANIZATION & ARCHITECTURE (CS-605)

(Regular-2012 & Back of Previous Admitted Batches)

Full Marks: 60 **Time: 3 Hours**

Answer any SIX questions including Question No.1 which is compulsory.

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. Answer all the questions. [2 × 10

a) A computer has 64 bit instruction and 12 bit address. If there are 250 three address instruction and 525 two address instruction, how many one address instructions are possible?

b) Execute the following instruction where R_0 is of 8 bit and its content is 11001011.
i) Lshift L #2, R_0
ii) Ashift R #1, R_0

c) Write down the working principle of SRAM cell.

d) What is the hit ratio of a cache memory if cache memory access time is 30ns and main memory access time is 15ns and average access time is 42ns?

e) What are the functions of I/O interface?

f) Draw the space-time diagram for a six-segment pipeline showing the time it takes to process eight number of task. Determine the number of clock cycle that it takes to process 200 tasks.

g) How cycle-stealing mode is different from burst mode data transfer in DMA?

h) One instruction requires 7 clock cycle to complete its execution. How much time is required for that instruction if the processor speed is 5 GHz?

i) Specify the importance of RUN and END control signal in hardwired control unit.

j) Distinguish between temporal and spatial aspect of locality of reference.

2. a) Write the instructions to evaluate the expression [4

X=(A+B/C) *(D-E) in

i) Stack based computer

ii) Accumulator based computer

b) Draw and explain the single bus organisation inside CPU and write the control signal of the given instruction [4

SUB $20(R_1), R_2$

3. a) Explain the following addressing mode with suitable example. [4

i) Relative

ii) Register Indirect

iii) Auto Indexing

iv) Base addressing mode

v) Implied mode

b) Describe the operational principle of hardwired control unit and micro programmed control unit with the help of proper diagram. Specify the advantage and disadvantage of both the control units. [4

4. a) Explain the technique of memory interleaving. [4
Consider a memory of 8 words per block. If 2 clock cycles are required to transfer address from CPU to memory and 6 clock cycles to access 1st word and 3 clock cycle each for consecutive words and 2 clock cycle for transferring the word from memory to cache. Then calculate the total clock cycle required to transfer the block with interleaving and without interleaving if the number of module is four.

b) Define the role of cache memory in memory organisation. [4
Why we use the mapping function? Specify the different mapping function name.
A two-way set associative cache memory uses block of 4 words. The cache can have a total of 2048 words from main memory. The main memory size is 128K X 32.
i) Draw the format of main memory address.
ii) What is the size of cache with tag bits?

5. a) What is parallel processing? Discuss Flynn's Classification with necessary diagram. [4

b) Define pipeline processing system and speed up ratio. Explain any two hazards with its remedy. [4

6. a) Perform Booth's multiplication for the following: [4
(-7) * (+11) = ?

b) Perform division using restoring and non-restoring technique. [4
13 ÷ 4 = ?

7. a) What are the different data transfer schemes present? Explain the programmed I/O briefly. [4

b) Design a 4mX32 memory using 512X8 memory chip. [3

c) How many external connections are required to design 32mX32 memory chip? [1

8. Write short notes on the following (any two): [4 × 2

a) DMA

b) Virtual Memory

c) RISC Vs CISC

d) Memory Mapped I/O Vs I/O mapped I/O

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