DOE
01-9-15

Mid-Semester Examination
School of Computer Engineering
KIIT University, Bhubaneswar-24

Time: 2hrs ***Full Mark:25***

(Answer any five questions including question No.1 which is compulsory.
The figures in the margin indicate full marks.)

Instruction format: Opcode SRC, DEST

1) Short Questions [1 × 5]

a) A computer has 64-bit instructions and 12 bit addresses. If there are 352 three-address instructions, and 2256 no of two-address instructions then how many one-address instructions can be formulated?

b) PC does the same function as MAR, and then justify your answer by keeping two registers instead of one.

c) The content of register R1is 11010110. What will be the decimal value after execution of
AShiftR #2, R1. [Assume the number is represented in 2's complement format]

d) Explain the significant of carry and overflow flag.

e) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. How many bits are there in the operation code, the register code part, and the address part?

2) [2.5 × 2]

a) How does the processor executes an instruction? Explain with suitable example and neat diagram.

b) Explain the following instructions with example.
AND, AShiftR, Compare, Negate, and Branch.

3) [2+2+1]

a) Write the sequence of control steps required for single bus CPU organization of the following instruction
ADD R1, NUM

b) Write the sequence of control steps required for three bus CPU organizations for the above instruction.

c) Design the logic function for WMFC control signal using single bus CPU organization.

4) [2.5 × 2]

a) A two-word instruction is stored in memory at an address designated by the symbol P. The address field of the instruction (stored at P+1) is designated by the symbol Q. The operand used during the execution of the instruction is stored at an address symbolized by EA. An index register contains the value X. State how EA is calculated from the other addresses if the addressing mode of the instruction is direct, indirect, relative, and indexed.

b) Write the number of memory references required for executing the following instructions:
i) ADD R1,(R2)+
ii) SUB #10,R2

iii) MOV R1, 20(R3,R4)
iv) AND R1,R2
v) Increment A

5) [2+3]

a) Explain the working principle of hardwired control unit design with neat diagram. Explain its advantage and disadvantage.

b) The content of the top of the memory stack is 5000. The content of the stack pointer SP is 3000. Assume you want to organize a nested subroutine calls on a computer as follows: the routine Main calls a subroutine SUB1 by executing a two-word call subroutine instruction located in memory at address 1000 followed by the address field of 6000 at location 1001.Again subroutine SUB1 calls another subroutine SUB2 by executing a two-word call subroutine instruction located in memory at address 6050 followed by the address field of 8000 at location 6051 . What are the content of PC, SP, and the top of the stack?

i) After the subroutine call instruction is executed in the main routine?
ii) After the subroutine call instruction is executed in the subroutine SUB1?
iii) After the return from SUB2 subroutine?

6) [2+ 2+1]

Write a program to evaluate the arithmetic statement:

$X = (A-B+C*(D*E-F)) / (G+H*K)$

i) Using a stack organized computer with zero-address operation instructions.
ii) Using an accumulator type computer with one address instructions.
iii) Using a general register computer with two address instructions.