SPECIAL SUPPLEMENTARY EXAMINATION-2023

4th Semester B.Tech

COMPUTER ORGANIZATION AND ARCHITECTURE

CS 2006

(For 2022 (L.E), 2021 & Previous Admitted Batches)

Time: 3 Hours | Full Marks: 50

Answer any SIX questions.
Question paper consists of four SECTIONS i.e. A, B, C and D.
Section A is compulsory.
Attempt minimum one question each from Sections B, C, D.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

SECTION-A

1. Answer the following questions. [1 × 10]

(a) Register R_1 and R_2 of a computer contains the decimal value1000 and 250. What are the effective address of memory operand in each of the following instruction?

i) LOAD 10 (R_1), R_2
ii) MOVE 100, R_7
iii) ADD (R_2), R_1
iv) MUL (R_2)+, R_5

(b) Differentiate between Big Endian and little Endian scheme with suitable example.

(c) The content of register R1 is 10001011. What will be the decimal value of the content of R1 after execution of the following instruction? Assume the number is represented in 2's complement format and carry bit is zero.

RotateRC #2, R1 *//RotateRight through carry.*

(d) A subroutine "**SUB1**" is located at an address **1000** in memory. **After the execution** of the following instruction. what will be the value of PC?

Call SUB1 // The instruction is located at address **2000** and the length of the instruction is **4 bytes**.

(e) Why is refreshing required in a dynamic memory cell?

(f) How many external connections are required to design 128MX32 memory chip?

(g) A CPU has 32 bit memory address and 128KB of cache memory. The cache is organized as a 4-way set associative cache with a block size of 32bytes. How many number of sets are there in the cache memory?

(h) Represent 25.50 into IEEE-754 single precision floating point format.

(i) Give the Booth recoding for the multiplier : 10101

(j) What is vectored interrupt technique?

SECTION-B

2. (a) Write the assembly code to evaluate the following arithmetic expression: [4]

$$X = (A+B-C*D) / (E-F)$$

i) Using an accumulator type computer with one address instructions.

ii) Using RISC computer instruction format.

(b) Explain the following addressing modes with examples: [4]

i. Register Indirect mode ii. Index mode

iii. Relative mode iv. Autodecrement mode.

3. (a) Write the sequence of control steps for the following instructions for single bus CPU organization. Assume second operand is the destination operand. [4]

i) MUL #23, R2

ii) AND (R5), R1

(b) Draw block diagram of the micro-programmed control unit. Explain the following terms related to micro-programmed control unit. [4]

i) Micro Instruction
ii) Micro Program
iii) Micro Routine
iv) Control Store

SECTION-C

4. (a) Discuss the factors that affect the performance of a computer. If a 5GHz computer takes 4 clock cycles for ALU instructions, 10 clock cycles for branch instructions and 3 clock cycles for data transfer instructions. Then Find the total time taken by the computer to execute the program that consists of 15 ALU instructions, 5 branch instructions and 20 data transfer instructions. [4]

(b) Explain the 3-bus architecture inside CPU with neat diagram. Write the control signals for the following instruction. [4]
MUL(R7),R_2 // R_2 is the destination

5. (a) A cache consists of a total of 256 blocks. The main memory contains 2048 blocks, each consisting of 16 words. [4]

(i) What is the size of the cache memory?

(ii) How many bits are there in each of the TAG, BLOCK, and WORD field in case of direct mapping?

(iii) How many bits are there in each of the TAG, and WORD field in case of associative mapping?

(iv) How many bits are there in each of the TAG, SET, and WORD field in case of 8-way set-associative mapping?

(b) A computer uses RAM chips of 128K X 4 capacity. [4]

(b) A computer uses RAM chips of 128K X 4 capacity. Design a memory capacity of 1M X 16 by using available chips. [4]

6. (a) Discuss the technique of virtual memory address translation. What is the importance of TLB in virtual address translation? [4]

(b) Explain the technique of memory interleaving. [4]

Consider a memory of 8 words per block. If 2 clock cycle are required to transfer address from CPU to main memory and 6 clock cycle to access the 1st word and 4 clock cycle each for consecutive words and 1 clock cycle for transferring the word from memory to cache. Then calculate the total clock cycle required to transfer the block with inter leaving and without interleaving if the number of modules is four.

SECTION-D

7. (a) Perform the following division operation using restoring method. $13 \div 4$. [4]

(b) Multiply -14 x 9 using Booth's multiplication algorithm. [4]

8. (a) Explain Program- Controlled I/O technique. Why interrupt driven I/O is more advantageous than Program-Controlled I/O? [4]

(b) Explain the registers used in a DMA operation. Distinguish between cycle stealing and burst mode data transfer in DMA. [4]

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