b) With the help of a neat diagram explain the working of Counter type A/D converter circuit and also discuss the drawbacks of this converter in brief. [4

c) Calculate the storage capacity of a certain memory (in MB) if it has 20 address lines, 8 input data lines and 8 output data lines? [2

8. a) What is Decoder? Explain it with a block diagram and design a **4-16 line decoder using only 2-4 line decoders**. [4

b) Implement the following logic function using a multiplexer having three select lines. [4

$$F(A,B,C,D) = \bar{A}.B + \bar{B}.C + C.\bar{D}$$

c) Find out the resulting output $Q(t)$ of the flip-flop for **next 6 clock pulses** assuming initial condition (Q=1 and $\bar{Q} = 0$) for the following circuit. [2

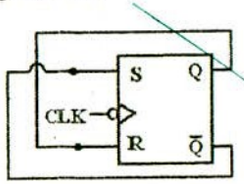

Figure-8(c)

x x x x x

user ID – gautfet@kiit.ac.in
Password – B9V8Q4
http://10.0.2.41/kiitoes.asp

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SPRING END SEMESTER EXAMINATION-2015

4th Semester B.Tech & B.Tech Dual Degree

DIGITAL ELECTRONIC CIRCUITS (EC-2009)

(Regular-2013 Admitted Batch)

Full Marks: 60 **Time: 3 Hours**

Answer any SIX questions including Question No.1 which is compulsory.

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. a) Define 'Positive Logic system' and 'Negative Logic system' [1 × 10 system.

b) Perform following arithmetic :

(i) BCD subtraction (754 – 567)

(ii) (**-13**) - (**-7**) using 2's complement method.

c) Implement 1-bit Magnitude Comparator using **2:4 decoder** (having active HIGH output lines) and **one OR gate**.

d) What is the difference between SRAM and DRAM?

e) Differentiate between the Synchronous and Asynchronous input terminals of flip-flop, explain with the help of J-K flip-flop.

f) Why Asynchronous counters are slow compared with Synchronous counters? Explain in brief.

g) Draw the state diagram of T flip-flop using Moore model.

h) 'Fan-out of CMOS logic is very high compared with TTL and ECL logic families', Justify.

i) What is the difference between PLA & PAL, explain with suitable examples.

j) For a 4-bit successive approximation analog to digital converter if input analog voltage is 7.5V and clock frequency is 5MHz then calculate its conversion time.

2. a) Design a shift register using D-flip flop, which could be used to design MOD-6 Johnson counter. Explain its operation briefly. [4

b) Obtain the minimized expression for the following 4-varible Boolean expression using K-map method and implement the minimized expression using **NAND gates only**. [4

$$F(P,Q,R,S) = \sum m\,(2, 3, 7, 8, 10, 13) + d(9, 11, 15)$$

c) Draw the circuit diagram of a CMOS Inverter and explain its operation in brief. [2

3. a) Simplify the given logic circuit and implement the simplified expression using **only NOR gates**. [4

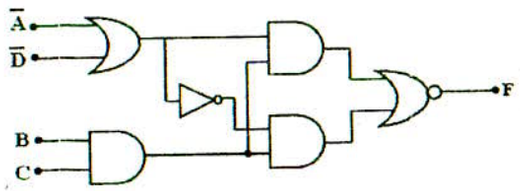


Figure-3(a)

b) Design a Combinational circuit using **only 2-input XOR & OR** gates which takes 4-bit binary data as input and **generates 2's complement of the input data**. [4

c) Define **'Noise-Margin'**. If the noise-margin of 1st logic family is 2.5V and for 2nd it is 1.5V then which one of these logic families is better, explain in brief. [2

4. a) Design a synchronous sequential circuit using T-flip flop which produces an output Z = 1, whenever the following input sequence '0110' occurs. (***Assume overlapping is allowed and use Mealy Model***) [6

b) With the help of a neat diagram, explain the working of a TTL NAND gate with Open-Collector Output and also mention the disadvantages of this configuration. [4

5. a) Using T Flip-Flops design a MOD-6, Asynchronous, Up counter. [4

b) What is Priority Encoder? Design a 4:2 Priority Encoder such that the order of priority of the decimal inputs is given as $D_0 > D_1 > D_2 > D_3$, where all D_i's are inputs to the priority encoder. [4

c) Differentiate between MROM & PROM. [2

6. a) Design a 2-bit Magnitude Comparator using two 1-bit Magnitude Comparator modules and additional basic gates. [4

b) Design a Synchronous counter that goes through states 0, 1, 2, 5, 6, 7, 0, 1… using J-K Flip-Flops. [4

c) For the circuit given, in Figure-6(c), identify the Boolean function **'F'** implemented with the 4x1 MUX and implement the function using minimum number of XOR gates only. [2

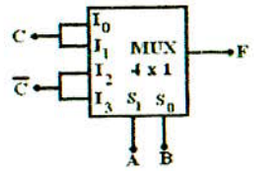


Figure-6(c)

7. a) Design a J-K Flip-Flop using a T Flip-Flop and basic gates. [4

Solutions

Spring End Semester Examination-2015

Digital Electronic Circuits [EC-2009]

B.Tech (Regular)

1)a) **Positive Logic System:** A positive logic system is one in which the higher of the two voltage levels represents Logic '1', and the lower of the two voltage levels represents Logic '0'.
Negative Logic System: A negative logic system is one in which the higher of the two voltage levels represents Logic '0' and the lower of the two voltage levels represents Logic '1'.

b) (i) BCD subtraction (754 – 567)

0111	0101	0100
-0101	0110	0111
0001	1110	1101
	-0110	-0110
0001	1000	0111
1	8	7

(ii) (-13) - (-7) = (-6) using 2's complement method.

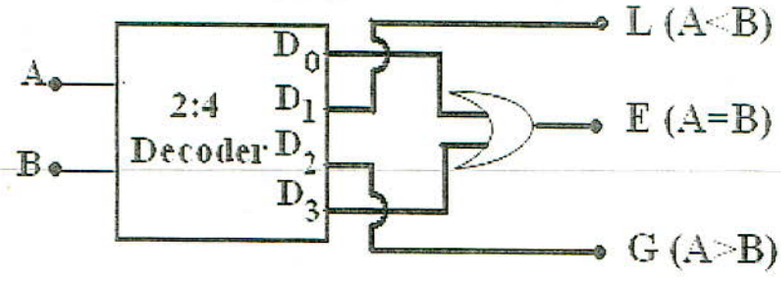
(-13) in 2's complement form = 10011

(-7) in 2's complement form = 11001

2's complement of '11001' = 00111

Now (10011) + (00111) = 11010 = (-6) in 2's complement form

c) **1-bit Magnitude Comparator using 2:4 decoder (having active HIGH output lines) and one OR gate:**



d)

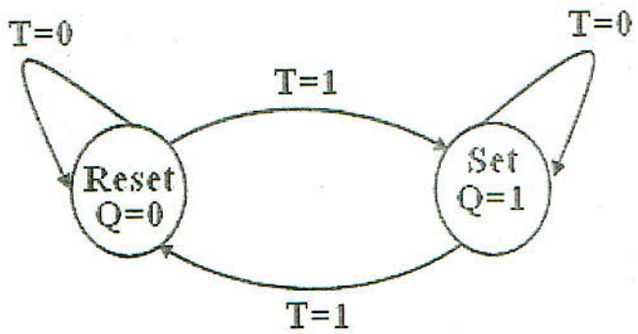
	SRAM	DRAM
(1)	Available in both bipolar and MOS technologies.	Available only in MOS technology.
(2)	Use latches for storage	Use capacitors for storage
(3)	No refreshing is required	Refreshing is required

e) Synchronous input must be used in conjunction with a clock signal to trigger the flip-flop while asynchronous input affect the flip-flop output independently of the clock signal.
For example, In J-K flip-flop,

CLR & PRESET : asynchronous input
J & K : synchronous input

f) Asynchronous counters are slower than synchronous counters because of the delay in the transmission of the pulses from flip-flop to flip-flop. With a synchronous circuit, all the bits in the count change synchronously with the assertion of the clock.

g) **State diagram of T flip-flop using Moore model:**

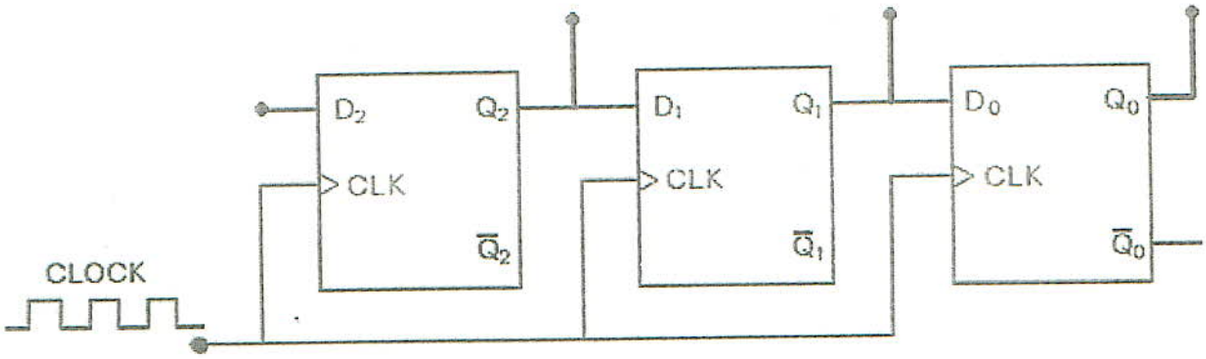


h) **In CMOS** logic family MOSFETs are used which leads to high Fan-Out because MOSFET is voltage controlled device, so required current from the driver gate is very less (theoretically zero).

i) **PLA(Programmable Logic Array):** In Programmable logic array (PLA),both the AND and OR arrays canbe programmed. The product terms in the AND array may be shared by any OR gate to provide the required sum of products implementation.It is the most flexible PLD.
PAL(Programmable Array Logic) : The programmable array logic (PAL) has a fused programmable AND array and a fixed OR array. The AND gates are programmed to provide the product terms for the Boolean functions that are logically summed in each OR gate.

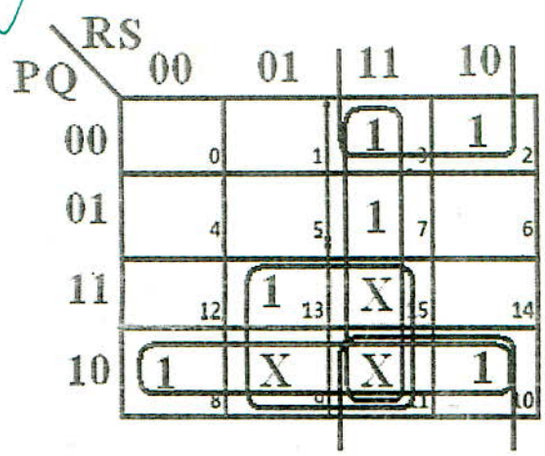
j) Conversion time for a N-bit successive approximation analog to digital converter = N x T_{clk}
where, T_{clk} : Time period of clock
here **N = 4 & $T_{clk} = 1/f_{clk} = 1/5MHz = 0.2\mu s$**
So, Conversion time = 4 x 0.2 μs = **0.8 μs**

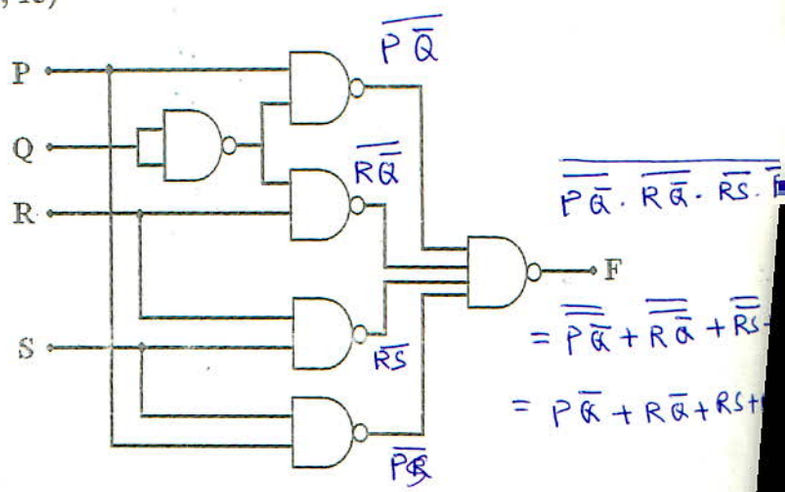
2) a) **Type of Shift Register** : SIPO shift register [1]
No. of bits = Modulus of Johnson counter/2= 6/2= 3 [1]
Explanation: Working in brief [1]
Circuit Diagram: [1]



3-bit SIPO shift register

2) b) $F(P,Q,R,S) = \sum m\,(2, 3, 7, 8, 10, 13) + d(9, 11, 15)$



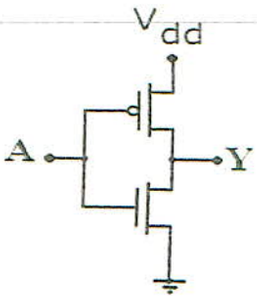


K-map [2] **Circuit diagram** [1]

Expression: $F(P, Q, R, S) = P\overline{Q} + PS + RS + \overline{Q}R$ [1]

2) c) **CMOS Inverter:**

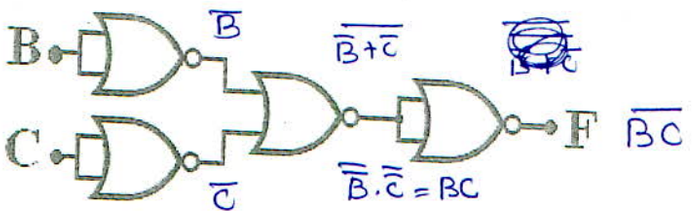
Circuit Diagram: [1]



Explanation: Explanation of working in brief [1]

3) a) Simplified Boolean expression of the given circuit is $F = \overline{BC}$ [2]

Implementation of the simplified expression using only NOR gates [2]



3) b) A: $A_4\ A_3\ A_2 A_1$ (4-bit binary data)
B: $B_4\ B_3\ B_2 B_1$ (2's complement of input binary data)

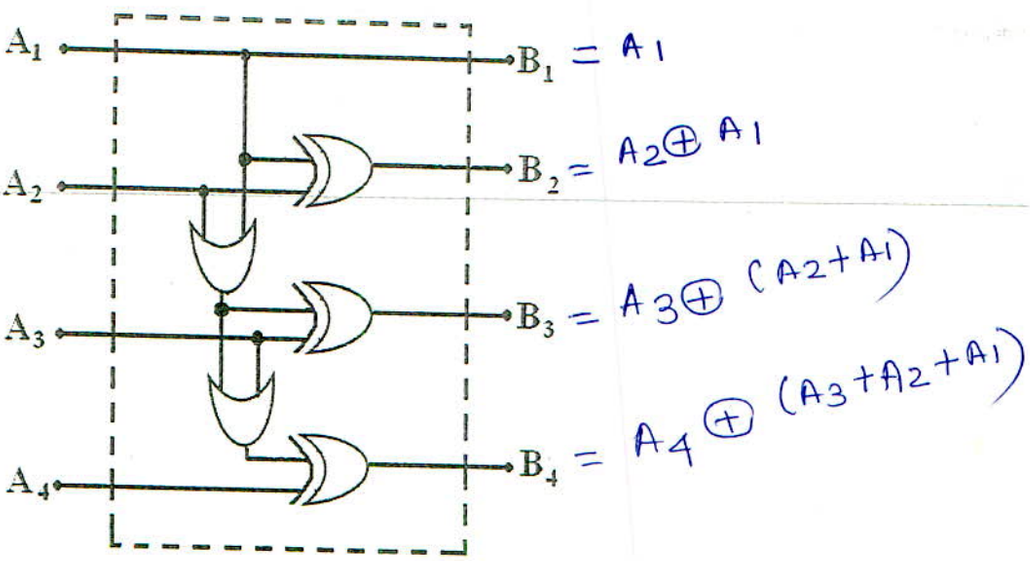
TRUTH TABLE: [1.5]

A_4	A_3	A_2	A_1	B_4	B_3	B_2	B_1
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
0	0	1	1	1	1	0	1
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

From K-map:

$B_4 = A_4 \oplus (A_3 + A_2 + A_1)$ [0.5]
$B_3 = A_3 \oplus (A_2 + A_1)$ [0.25]
$B_2 = A_2 \oplus A_1$ [0.25]
$B_1 = A_1$

Circuit Diagram: [1.5]

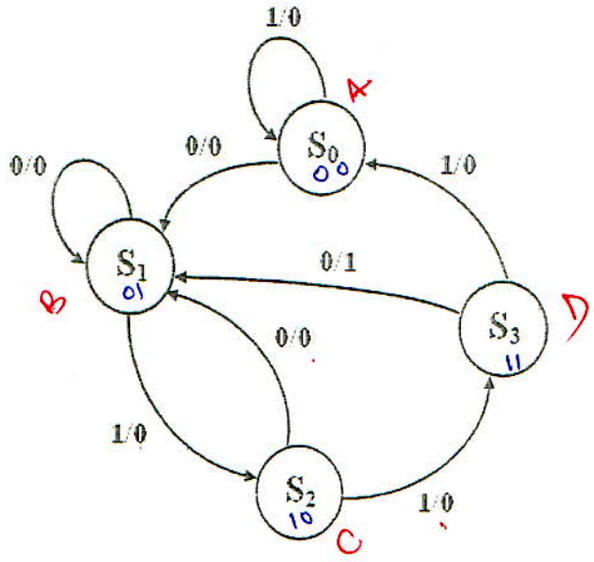


3) c) **Noise Margin** is the maximum noise signal that can be added to the input signal of a digital circuit without causing an undesirable change in the circuit output. [1]

- 1st logic family is better than 2nd logic family (Higher Noise Margin leads to better noise immunity) [1]

4) a) **Synchronous sequential circuit to detect the sequence '0110':**

State Diagram: [1.5]



State Table: As per state diagram [0.25]

State Assignment: S_0 : '00' S_1 : '01' S_2 : '10' S_3 :'11'

Transition & Output Table: As per state table and state assignment [0.25]

Excitation Table: As per Transition & Output Table using T flip-flop. [0.5]

From K-map as per excitation table

$$T_2 = q_1 x + q_2 \bar{x}$$ [1]

$$T_1 = \bar{q}_1 \bar{x} + q_1 x + q_2 \bar{q}_1$$

OR [1]

$$T_1 = \bar{q}_1 \bar{x} + q_1 x + q_2 x$$

$$Z = q_2 q_1 \bar{x}$$ [0.5]

Circuit Diagram: As per the expression [1]

6) b) Synchronous counter that goes through states 0, 1, 2, 5, 6, 7, 0, 1... using J-K Flip-Flops

Excitation Table: [1.5]

Present State $Q_3\ Q_2\ Q_1$	Next state $Q_3\ Q_2\ Q_1$	Required Excitations					
		J_3	K_3	J_2	K_2	J_1	K_1
0 0 0	0 0 1	0	X	0	X	1	X
0 0 1	0 1 0	0	X	1	X	X	1
0 1 0	1 0 1	1	X	X	1	1	X
1 0 1	1 1 0	X	0	1	X	X	1
1 1 0	1 1 1	X	0	X	0	1	X
1 1 1	0 0 0	X	1	X	1	X	1

From K-map:

$J_3 = Q_2$

$K_3 = Q_2 Q_1$ [0.5]

$J_2 = Q_1$

$K_2 = \bar{Q}_3 + Q_1$ [0.5]

$J_1 = 1$

$K_1 = 1$ [0.5]

Circuit: As per the expression. [1]

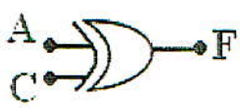
6) c) For 4x1 MUX

$$F = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$ [0.5]

So, $F = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + AB\bar{C}$

$= A \oplus C$ [1]

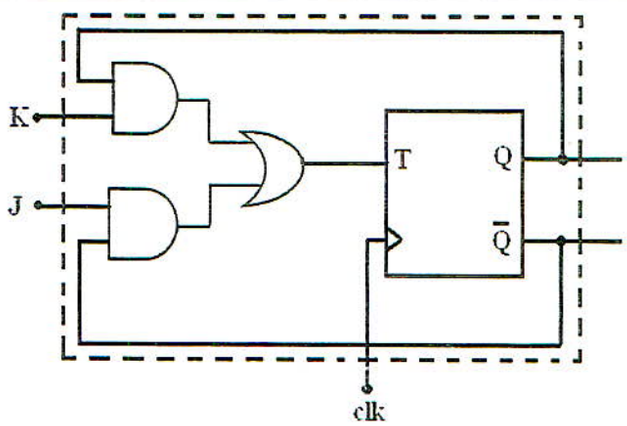
Circuit diagram: [0.5]



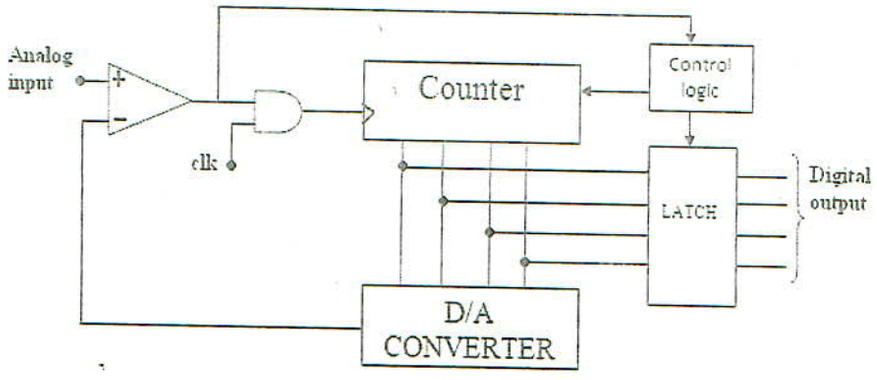
7) a) JK Flip-Flop using a T Flip-Flop and basic gate:

- From excitation table : $T = J\bar{Q} + KQ$ [2]

Circuit diagram: [2]



7) b) **Counter type A/D converter:**



[2]

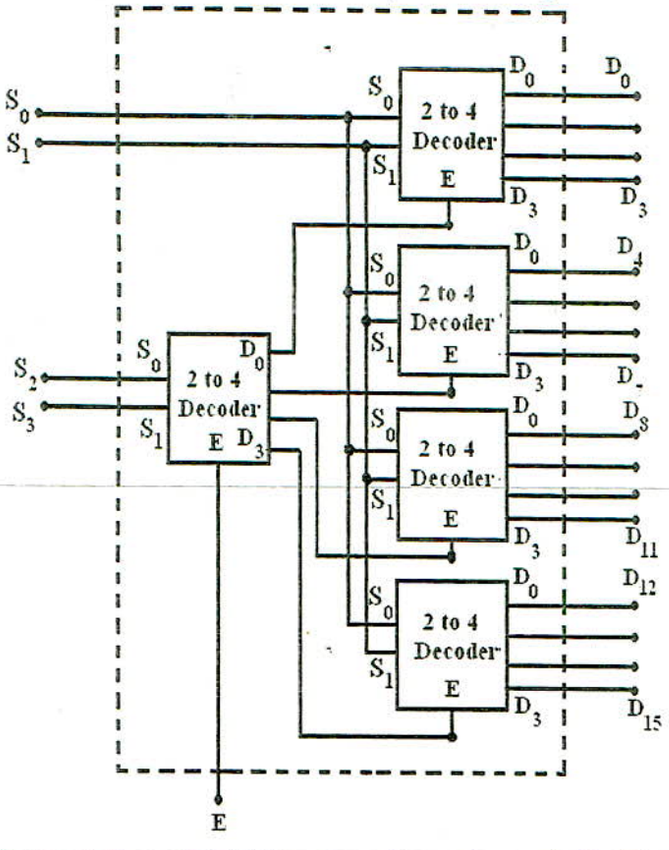
Explanation: Explanation of working in brief [1.5]

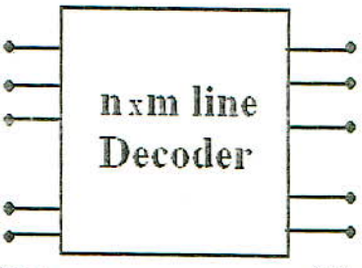
Drawback: [0.5]

- Analog to Digital Conversion time varies with the magnitude of the input analog signal.

7) c) Storage capacity of memory = 2^{20} x 8 bits
= 2^{20} Bytes
= **1MB** [2]

8) a) A decoder is a logic circuit that converts an n-bit binary input code into 2^n output lines, such that each output line will be activated for only one of the possible combinations of inputs. [0.5]





where $m = 2^n$ [0.5]

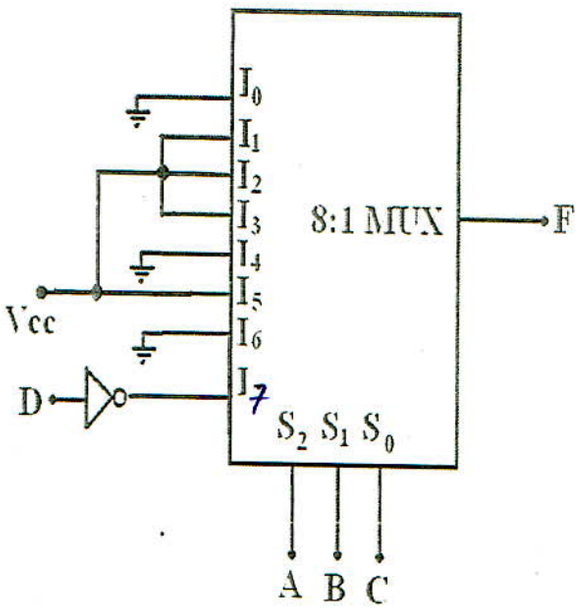
Implementation of 4-16 line decoder using only 2-4 line decoders [3]

8) b) $F(A,B,C,D) = \sum m(2,3,4,5,6,7,10,11,14)$

Truth Table: [2]

A	B	C	D	F	
0	0	0	0	0	F=0
0	0	0	1	0	
0	0	1	0	1	F= 1
0	0	1	1	1	
0	1	0	0	1	F=1
0	1	0	1	1	
0	1	1	0	1	F= 1
0	1	1	1	1	
1	0	0	0	0	F=0
1	0	0	1	0	
1	0	1	0	1	F=1
1	0	1	1	1	
1	1	0	0	0	F=0
1	1	0	1	0	
1	1	1	0	1	$F=\overline{D}$
1	1	1	1	0	

Circuit Diagram: [2]



8) c) Q : 1 0 1 0 1 0 1 0..... [1]

- Flip-flop is in toggle mode [1]