2009 Adm. Batch Onwards
IV-B-Tech(Regular& Back)
DEC EC-402
[E&EE, E&TC, E&I, EE, IT, CSE]

FOURTH SEMESTER EXAMINATION-2012

DIGITAL ELECTRONICS CIRCUITS

EC-402

Full Marks: 60 **Time: 3 Hours**

Answer any six questions including question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and
All parts of a question should be answered at one place only.

Q1. a) What is *don't care term* and how can such term arise in practice? [1x10]
b) Differentiate synchronous and asynchronous input terminals of FFs, explain with the help of J-K FF.
c) 'XOR and XNOR gates can be used as a buffer as well as an inverter', Justify.
d) What is the difference between active LOW and active HIGH terminals?
e) Define (i)Self-complementing code,(ii)Sequential codes. Give examples of both.
f) Define Noise Margin and Fan-out?
g) Perform following arithmetic : (i) BCD addition (749+858),
(ii) (-14) - (-6) using 2's complement method.
h) Calculate the modulus of the counter which counts in **prime numbers** (2, 3, 5…N, 2, 3….) where N < 50.
i) What is the difference between SRAM and DRAM?
j) An 8-bit successive approximation type ADC has a resolution of 15mV.What will its digital output be for an analog input of 2.65V?

Q2. a) Design a synchronous sequential circuit which produces an output Z=1, whenever the following input sequence '10110' occurs. *(Assume overlapping is allowed and use Mealy Model)* [6]
b) Draw the logic diagram of a 4-bit Bi-directional shift register and explain in brief. [4]

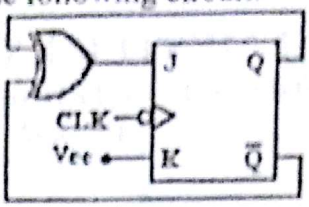
Q3. a) Design a synchronous counter that goes through states 0,2,3,5,6,7,0,2,3…… using J-K FFs. [4]
b) Using 2-4 decoders (having enable input) design **3-8 decoder with enable input** so that the new 3-8 decoder can be used for further expansion. [4]
c) Draw the circuit for 2-input NOR gate using CMOS logic. [2]

Q4. a) Implement 3-bit combined even and odd parity generator using a multiplexer having two select lines and XOR gate.*(Hint: Use XOR gate as a buffer and as an inverter)* [4]
b) With the help of a neat diagram explain the working of a two-input totem-pole TTL NAND gate and also mention some advantages of this configuration. [4]
c) What is the difference between PLA & PAL explain with suitable examples? [2]

Q5. a) With the help of a neat diagram explain the working of Counter type A/D converter circuit and also discuss the drawbacks of this converter in brief. [4]
b) Obtain the minimized expression for the following 4-varible Boolean expression using K-map method and implement the minimized expression using NAND gates only. [4]

$$F(P,Q,R,S) = \Pi M\,(0,1,4,7,10,11,13,14).d(2,7,8,13)$$

c) Find out the resulting output Q(t) of the FF for next 6 clock pulses assuming initial condition (Q=0 and $\bar{Q}$ =1) for the following circuit.

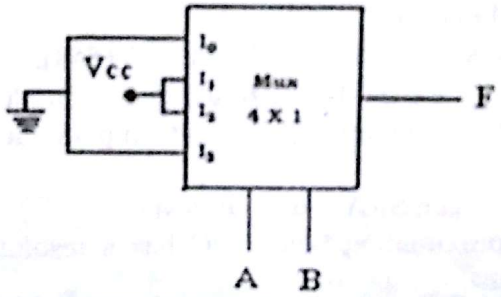


Q6. a) Design a 4:2 priority encoder such that input having least decimal subscript should have highest priority (**Order of priority: D_0>D_1 >D_2>D_3,where all D_i's are inputs to the encoder**) [4]

b) Encode 4-bit data word '1000' into a 7-bit even-parity Hamming code. If we transmitted a 7-bit even parity Hamming code through a noisy channel and at the receiver we obtained '1110110'. [4]

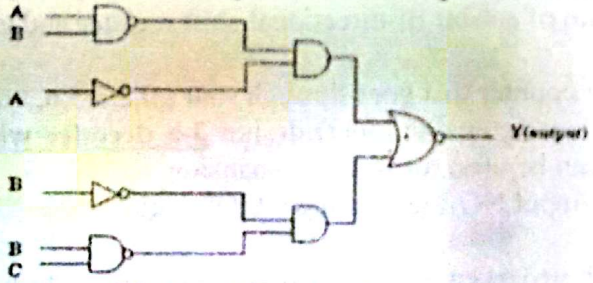
Decode the correct 4-bit data word. (*Assume that at most a single bit error may occur in the code word during transmission)*

c) Identify the Boolean function **F(A,B)** implemented with MUX. [2]



Q7. a) Draw the circuit diagram of (i)MOD-6 Johnson counter (ii)MOD-4 Ring counter and compare N-bit Ring & Johnson counter from modulus and decoding circuit point of view. [4]

b) Simplify the given logic circuit and implement the simplified circuit using only NOR gates. [4]

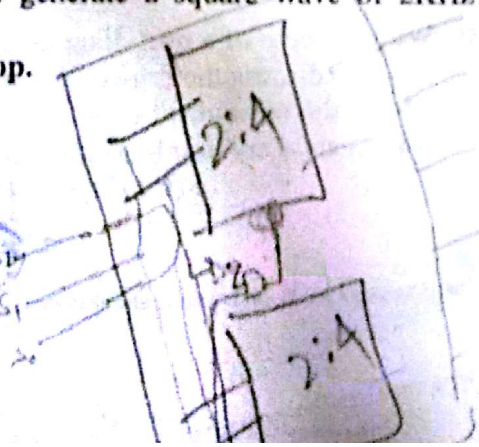


c) **'A decoder circuit having enable input line can be used as a demultiplexer circuit', Justify** this statement with proper circuit diagram. [2]

Q8. a) What is the difference between Astable multivibrator and Monostable multivibrator? Design an Astable Multivibrator using 555 timer to generate a square wave of 2KHz frequency with 60% duty cycle. [4]

b) Design J-K Flip-Flop using **2:1 MUX** and a **T Flip-Flop.** [4]

c) A certain memory has a capacity of 16K x 32. [2]
(i) How many data I/P and O/P lines does it have?
(ii) How many address lines does it have?



Solutions

Fourth Semester Examination 2012

Digital Electronic Circuit (EC-402)

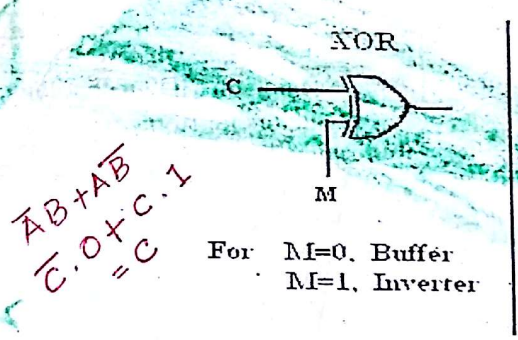
B.Tech (Regular)

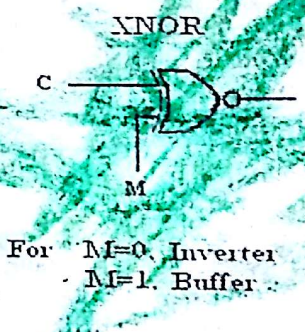
(1) a) The input combinations for which the output values are not specified are called *Don't care* combination. In case of *incompletely specified expressions* Don't care term arises.

b) Synchronous input must be used in conjunction with a clock signal to trigger the flip-flop while asynchronous input affect the flip-flop output independently of the clock signal.
For example, In J-K flip-flop,

CLR & PRESET : asynchronous input
J & K : synchronous input

c) XOR and XNOR gates as a buffer as well as an inverter





$\bar{A}B+A\bar{B}$
$\bar{C}.0+C.1$
$=C$

d) Active LOW terminals are those for which the action represented or initiated by a variable occurs when it is equal to a '0'.Ex: NAND gate output terminal.
Active HIGH terminals are those for which the action represented or initiated by a variable occurs when it is equal to a '1'.Ex: AND gate output terminal.

e) In **Self-complementing codes**, the code word of the 9's complement of 'N' can be obtained from the code word of 'N' by interchanging all the zeros and ones. Ex: XS-3 codes
In **Sequential codes**, each succeeding code word is one binary number greater than its preceding code word. Ex: 8421 BCD codes, XS-3 codes.

f) **Noise Margin** is the maximum noise signal that can be added to the input signal of a digital circuit without causing an undesirable change in the circuit output.
Fan-out is the maximum number of similar gates that the output of the gate can drive without impairing its normal operation.

g) i) BCD addition (749+858) =1607

```
  0111   0100   1001
+1000    0101   1000
------------------
  1111   1001  10001
+0110       1      1
------------------
  10101  1010   0111
+        0110
------------------
  10101 10000   0111
+       1
------------------
 0001   0110   0000   0111
  1      6      0      7
```

ii) (-14) - (-6) =(-8) using 2's complement method.

(-14) in 2's complement form = 10010

(-6) in 2's complement form = 11010

2's complement of '11010' = 00110

Now

$$\begin{array}{r} 10010 \\ +00110 \\ \hline 11000 \end{array}$$

$$-8$$

h) Counter will count in prime numbers ,so 2,3,5,7,11,13,17,19,23,29,31,37,41,43,47,2,3,5.....
Total number of states = 15
So modulus will be '15'(MOD-15 counter).

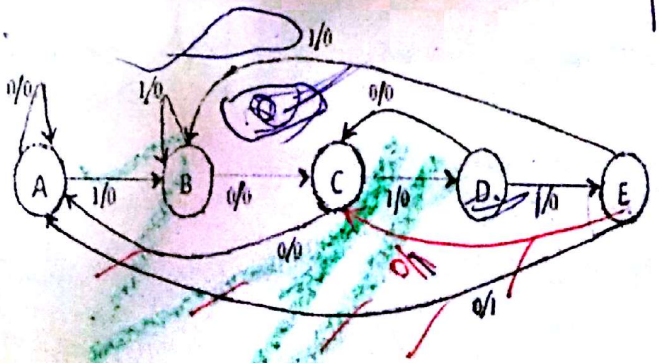
i)

	SRAM	DRAM
(1)	Available in both bipolar and MOS technologies.	Available only in MOS technology.
(2)	Use latches for storage	Use capacitors for storage
(3)	No refreshing is required	Refreshing is required

j) Resolution = 1.5mV
Analog input = 2.65V
Content of register after 1st clock cycle: 10000000
2nd clock cycle: 10000000
3rd clock cycle: 10100000
4th clock cycle: 10110000
5th clock cycle: 10110000
6th clock cycle: 10110000
7th clock cycle: 10110000
8th clock cycle: 10110000

So the final output will be '**10110000**'

2) a) **State diagram** and **State table** for sequence detector for sequence '10110' using Mealy model.



Present state	Next state ,O/P	
	X=0	X=1
A	A,0	B,0
B	C,0	B,0
C	A,0	D,0
D	C,0	E,0
E	A,1	B,0

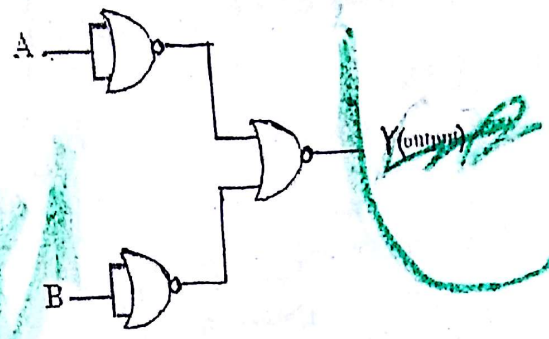
Excitation table: As per the state table and flip-flop used.
Final circuit : As per the final expressions.

:mentation of simplified circuit using only NOR gates

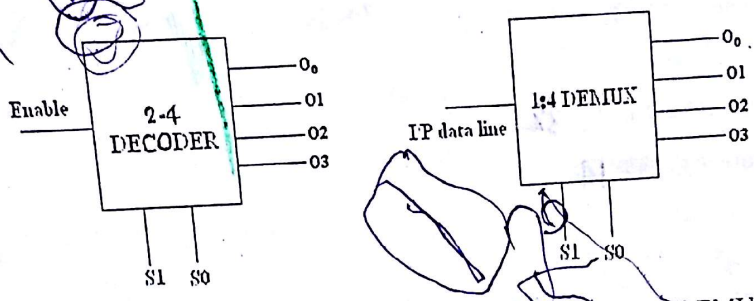
From the circuit

$$Y=(\overline{AB})\,\overline{A}+(\overline{BC})\,\overline{B}$$

$$Y=AB$$



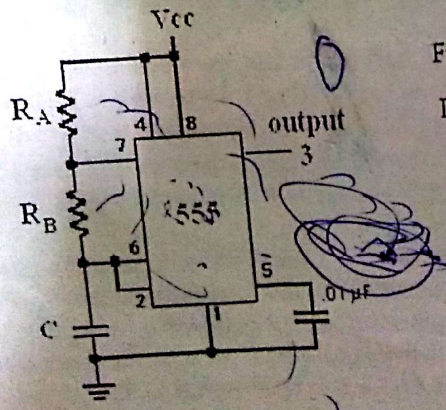
)c)



Enable input of DECODER circuit can be used as input data line of DEMUX circuit.

8)a)

Astable multivibrator	Monostable multivibrator
Circuit is not stable in either state.	One of the states is stable, but the other state is unstable.
It does not require an input such as a clock pulse to change its states, it continually switches from one state to the other.	It requires an input such as a clock pulse to move from stable state to unstable state.



Astable multivibrator using 555 timer

Frequency = 2kHz

Duty cycle = 60%

$t_{on}+t_{off}=T=1/f=0.5\times10^{-3}$ Sec.

$t_{on}=0.6T=0.693(R_A+R_B)C$

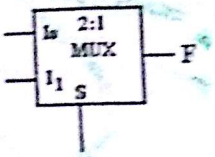
$t_{off}=0.4T=0.693R_BC$

So, $R_AC=0.2T/0.69$

and $R_BC=0.4T/0.69$

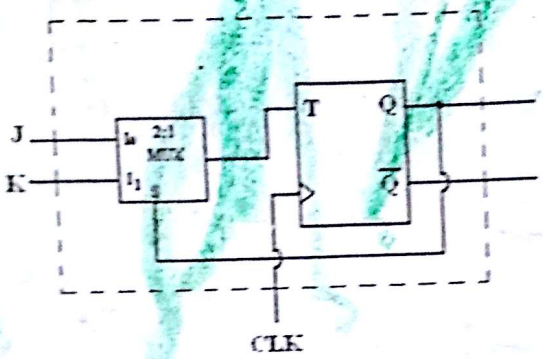
8)b) J-K Flip-Flop using 2:1 MUX and a T Flip-Flop

From excitation table : $T = J\bar{Q} + KQ$.....(a)



For 2:1 MUX : $F = I_0\bar{S} + I_1S$.....(b)

From (a) & (b)



8)c) $16Kx32 = 2^4.2^{10} \times 2^5 = 2^{14} \times 2^5$

i)So number of i/p and o/p lines = 32

ii) number of address lines = 14

Divakar

[D.D.Desired