AUTUMN END SEMESTER EXAMINATION-2017

3rd Semester B.Tech & B.Tech Dual Degree

DEC

EC-2011

(Regular-2016 & Back-2015 Admitted Batch)

Time: 3 Hours | Full Marks: 60

Answer any SIX questions including question No.1 which is compulsory.

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. (a) State De-Morgan's theorem. [1 × 10]

   (b) Draw the circuit diagram of CMOS NAND gate.

   (c) Realize the (i) inverter (ii) OR gate using the NAND gate.

   (d) Define the clock frequency of a Flip-Flop.

   (e) Convert $(597)_{10}$ to BCD code.

   (f) Perform the BCD subtraction of $(532–285)_{10}$.

   (g) What is shift register?

   (h) Define the Resolution of a DAC.

   (i) Define fan-in and fan-out.

   (j) What is priority Encoder?

2. (a) Design a 2 bit magnitude comparator, using required logic gates. [5]

   (b) Reduce to simplest form $Y = ABC + A\overline{BC}\,D + \overline{ABC}\,D$. [3]

(c) State the difference between synchronous and asynchronous counter. [2]

3. (a) Design a full adder using 3:8 decoders having active low output lines. [4]

(b) Give the truth table of S-R and J-K Flip-Flop and write its excitation equations. [4]

(c) Differentiate between error-correcting codes and error-detecting codes. [2]

4. (a) Design a MOD-7 counter using FFs. Draw the table, output waveforms. [5]

(b) Draw and explain the operation of flash type ADC. [5]

5. (a) Draw and explain the working of the totem-pole configuration of NAND gate. [4]

(b) Design a synchronous counter for the following sequence using T-Flip-Flop: 1, 3, 5, 6, 1,..... [4]

(c) State the difference Mealy and Moore Model. [2]

6. (a) Draw the circuit diagram and timing diagram of a 3-bit SIPO shift register. [4]

(b) Design a logic circuit that will allow a signal A to pass to the output only when the control inputs B and C are both HIGH, otherwise the output will stay low. [4]

(c) Subtract binary number 01000111 from 01011000 using 2's complement. [2]

7. (a) Implement a full subtractor using a MUX having two select lines. [4]

(b) Design an asynchronous MOD-10 up counter using D-FF only. [4]

(c) Implement a NOT gate in a 2x1 MUX. [2]

8. (a) Design a synchronous sequential circuit using Mealy Model and D FF which produces an output Z=1, when "1001" is detected. Assume overlapping detection is used. [5]

(b) Draw and explain the operation of Successive Approximation type ADC. [3]

(c) Encode the 4 bit data 1100 into 7 bit Hamming code. Use even parity. [2]

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