6. a) Design a J-K Flip-Flop using a D Flip-Flop and basic gates as required. [4

b) With the help of a neat diagram, explain the working of a 4-bit Successive Approximation type ADC with Analog input of 11.6 V. Find the digital output. What would be its conversion time if clock frequency is 1 MHz? If the analog input voltage is now increased to 14.8 V, what would be the new conversion time? Explain. [4

c) In a T Flip-Flop, the output is initially in SET state. If the input clock frequency is 6 MHz, find the frequency of the output waveform when (i) T = 0, (ii) T = 1. [2

7. a) Design a Combinational circuit **using 2-input basic gates only** which has three inputs A, B & C and three outputs X, Y & Z. When the decimal equivalent of the binary input is 0, 1, 5 or 3, the decimal equivalent of the binary output is one greater than the input and when decimal equivalent of the binary input is 4, 2, 6 or 7, the decimal equivalent of the binary output is one less than the input. [4

b) Design a 3-bit Odd Parity Generator circuit using a Decoder with Active-Low outputs. [4

c) Design a 2-bit Asynchronous UP/DOWN Counter using Negative Edge Triggered JK Flip Flops with Mode (M) as a control input. Given that, when M=0, the counter should count UP and when, M=1, it should count DOWN. [2

8. a) Design a synchronous sequential circuit using D flip-flop, which produces an output Z = 1, whenever the following input sequence '0101' occurs. (***Assume overlapping is allowed and use Mealy Model***) [6

b) With the help of a neat diagram, explain the working of a TTL NAND gate with Totem-pole output and also mention the advantages of this configuration. [4

XXXXX

Spring End Semester Supplementary Examination-2015

4th Semester B.Tech & B.Tech Dual Degree

DIGITAL ELECTRONIC CIRCUITS

(EC-2009)

Full Marks: 60 Time: 3 Hours

Answer any SIX questions including Question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. a) F(A, B) = A ⊕ B, implement this Boolean function using 4x1 MUX. [1 × 10

b) State Noise Margin High (NM_H) and Noise Margin Low (NM_L), with suitable diagram.

c) Show that $PQ + \bar{P}R = (P + R)(\bar{P} + Q)$ where P, Q and R are Boolean variables.

d) What is Asynchronous input of a Flip-Flop? Write down the Table of Operation of **Active Low Asynchronous input** of flip-flop.

e) Draw the state Diagram of S-R Filp-Flop using Moore Model with suitable State Table.

f) What is 'Lock out problem' in case of counters?

g) What is a Carry Look Ahead Adder? What is its advantage over Ripper Carry adder?

h) Implement XNOR gate by using **minimum number of NOR** gates.

i) How many OR gates are there in a 64 × 8 ROM and how many inputs does each OR gate of a 64 × 8 ROM have?

j) The logic levels used in a 4-bit R-2R ladder DAC are: 1 ≡ 5 V and 0 ≡ 0 V. Find the output voltage for digital input of 1010 = 3.125 V.

2. a) Implement the following Boolean function using **minimum number of NAND gates.** [4

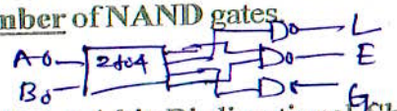
$$F(A,B,C,D) = \prod M(2,3,6,9,12) \cdot d(5,8,15)$$

= $\bar{A}\bar{C} + BD + AC$

b) Design a **4:2 Priority Encoder** such that the order of priority of the decimal inputs is given as $D_3 > D_2 > D_1 > D_0$, where all D_i's are inputs to the priority encoder. [4

$A = D_3 + D_2$
$B = D_3 + \bar{D}_2 D_1$
$V = D_3 + D_2 + D_1 + D_0$

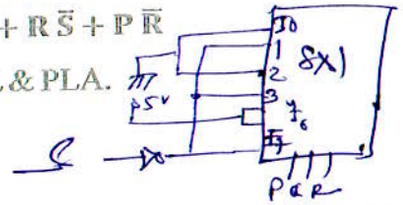
c) Implement a 1-bit Magnitude Comparator using a 2 to 4 Decoder having **ACTIVE LOW** output lines and **minimum number** of NAND gates. [2



3. a) Design a 4-bit Bi-directional Shift register using D-Flip Flops and Four 2x1 MUX. The Shift register should Shift Right when a Control input is **RIGHT/LEFT** = 1, it should shift left when the control input **RIGHT/LEFT** = 0. [4

b) Implement the following logic function using an 8:1 MUX. [4

$$F(P,Q,R,S) = P\bar{Q} + R\bar{S} + P\bar{R}$$



c) Differentiate between PAL & PLA. [2

4. a) Design an Asynchronous, Mod-12 Up-counter using **D Flip-Flops** and a **single NAND** gate. [4

b) What will be the output for L, E & G respectively of the 1-bit magnitude Comparator from the Figure below? Given that, the input at the Hamming Encoder is D3 = 1; D5 = 0; D6 = 1; D7=0 and it's an EVEN Parity Hamming Encoder. [4

The order of Priority of input for 8 to 3 Priority Encoder is **D0 > D1 > D2 > D3 > D4 > D5 > D6 > D7.**

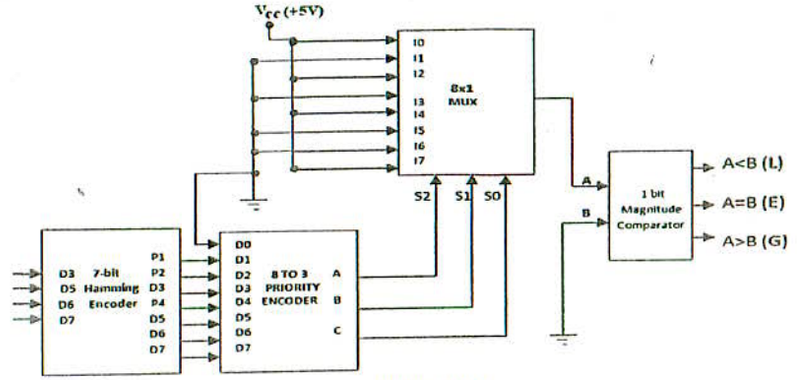


Figure-4(b)

c) Draw the circuit diagram of a 2-input CMOS NOR gate and explain its working in brief. [2

5. a) Design a **Synchronous counter** that goes through states **0, 7, 4, 3, 6, 0, 7, 4...** using J-K Flip-Flops. [4

b) A Cold Storage has three Cooling Fans namely **FAN1, FAN2** and **FAN3.** To maintain the temperature, at least two fans MUST be ON at any instant of time, so there is an ALARM connected with STATUS of The FANs. If, at least two FANs are not ON the ALARM would be triggered. Consider FAN ON as logic '1' and FAN OFF as logic '0' and implement the above ALARM digital logic circuit using **3 to 8 Decoder with ACTIVE LOW output lines** and **minimum number of 2 input AND gates only.** [4

c) A certain memory has a capacity of 128K × 8. [2
(i) How many data input and data output lines does it have? = 8
(ii) How many address lines does it have? = 2^{17}

SPRING END SEMESTER SUPPLEMENTARY EXAM - 2015

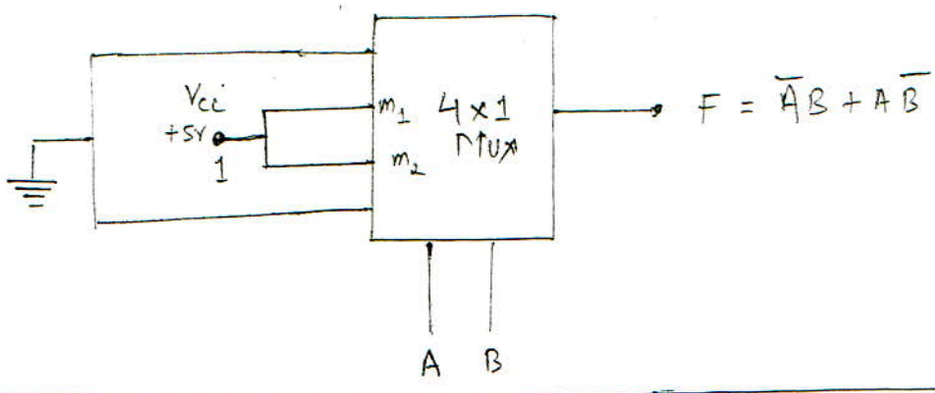
4th SEMESTER B.Tech

DIGITAL ELECTRONICS CIRCUITS.

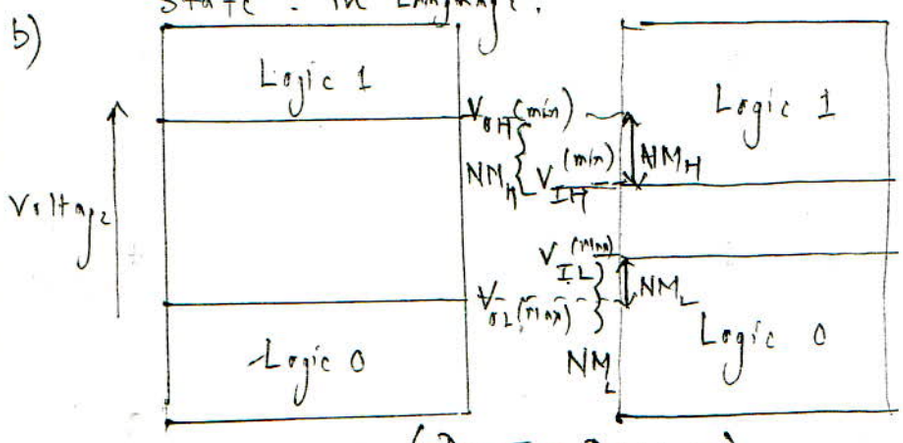
(EC-2009)

"SOLUTION SUBMITTED"

1) a) $F(A,B) = A \oplus B = \bar{A}B + A\bar{B} = \sum m(1,2)$



b) State : in Longmage.



(DRAW THE DIAGRAM)

$NM_H = V_{OH}(min) - V_{IH}(min)$

$NM_L = V_{IL}(max) - V_{OL}(max)$

NM_H = Noise Margin High

NM_L = Noise Margin Low.

c) $PQ + \bar{P}R = (P+R)(\bar{P}+Q)$

RHS = $(P+R)(\bar{P}+Q)$

$= P\cdot\bar{P} + PQ + R\bar{P} + QR$

$= 0 + PQ + \bar{P}R + QR$

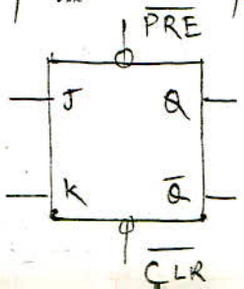
$= PQ + \bar{P}R + QR(P+\bar{P})$

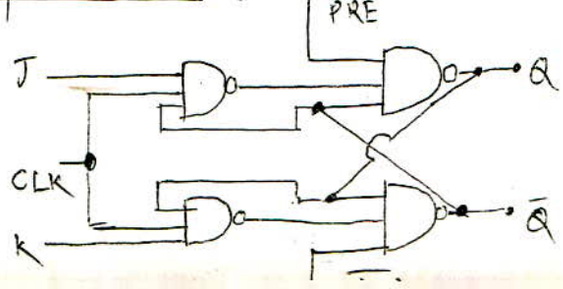
$= PQ + \bar{P}R + PQR + \bar{P}QR$

$= PQ(1+R) + \bar{P}R(1+Q)$

$= PQ + \bar{P}R = RHS.$

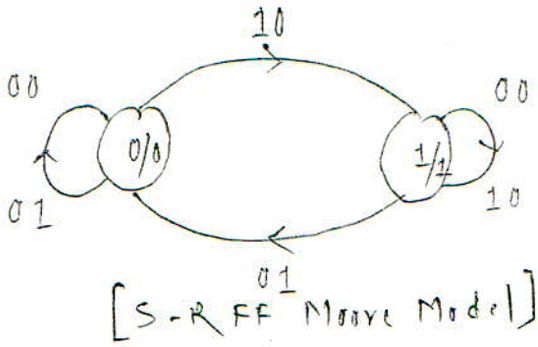
d) Asynchronous input of FLIP-FLOP: (ACTIVE LOW - $\overline{PRESET}$, $\overline{CLEAR}$)





$\overline{PRE}$	$\overline{CLR}$	FF Response
0	0	Not used
1	0	Q = 0
0	1	Q = 1
1	1	CLOCKED OPERATION

e)



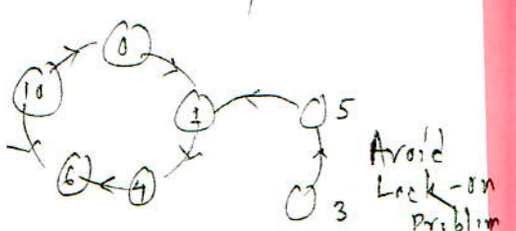
[S-R FF Moore Model]

STATE TABLE

PS	NS, O/P		
	S R = 0 0	S R = 0 1	S R = 1 0
0	0, 0	0, 0	1, 1
1	1, 1	0, 0	1, 1

f) Lock-Out → Moving the Synchronous Sequential Circuit from invalid state to valid state after one or two clock pulses and then continue in the normal way.

If the Synchronous Circuit get stuck inside the invalid state then it is Lock-out problem.



g) CARRY-LOOK-AHEAD ADDER

$P_n = A_n \oplus B_n$ = CARRY PROPAGATION

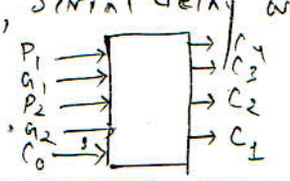
$G_n = A_n \cdot B_n$ = CARRY GENERATION.

$C_1 = P_0 C_0 + G_0$

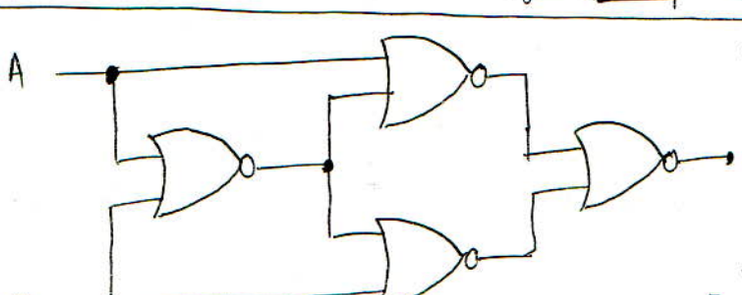
$C_2 = P_1 P_0 C_0 + P_1 G_0 + G_1$

C_3 = So on...

Advantage: Ripple delay, Serial delay will be less.



h)



(XNOR using NOR GATE)

Minimum = 4 NOR gates are required

$A \odot B$

$= \overline{A}\overline{B} + AB$

$= \sum m(0,3)$

i) 8 OR gates are there in 64x8 ROM.

64 inputs each OR gate in 64x8 ROM

j) 1 ≡ 5V ; 0 ≡ 0V. 4 bit R-2R Ladder. Given Number is 1010

Case	MSB			LSB	V_{out}
Case: 1:	1	0	0	0	E/2
Case: 2:	0	1	0	0	E/4
Case: 3:	0	0	1	0	E/8
Case: 4	0	0	0	1	E/16

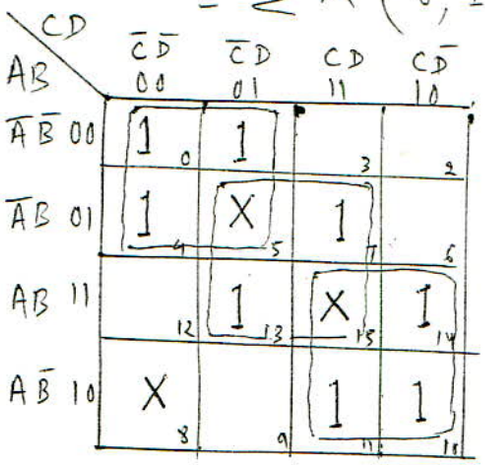
$V_{out} = \frac{E}{2} + \frac{E}{8} = \frac{5E}{8}$

E ≡ 5V.

$V_{out} = \frac{25}{8} V. = 3.125 V$

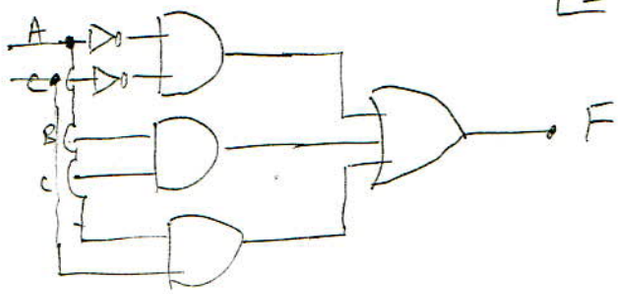
2) a) $F(A,B,C,D) = \prod M(2,3,6,9,12) \cdot d(5,8,15)$

$= \sum m(0,1,4,7,10,11,13,14) + d(5,8,15)$ | 1

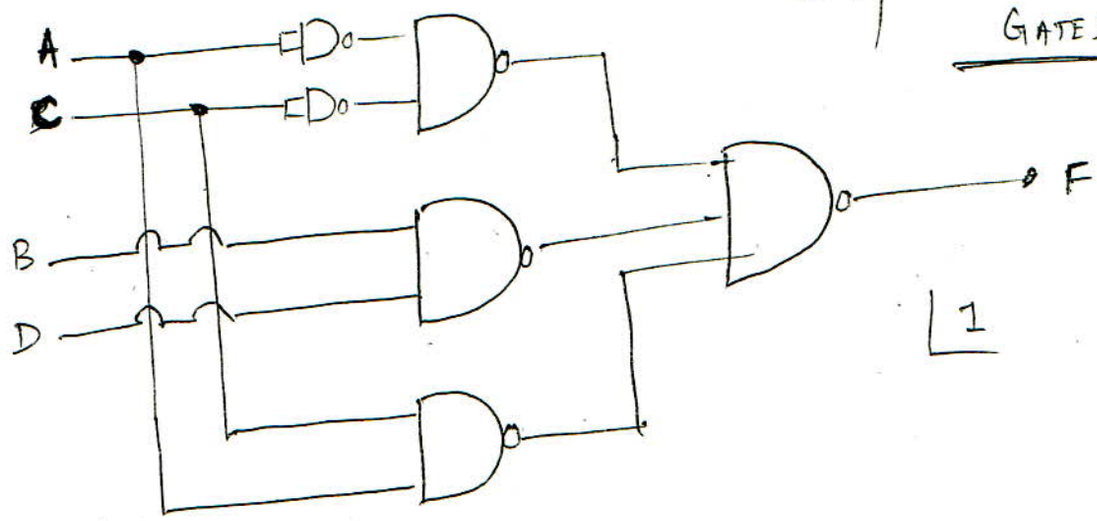


| 1

$F(A,B,C,D) = \bar{A}\bar{C} + BD + AC$ | 1



Two level Logic : "AND-OR" ≡ "NAND-NAND" ONLY - "6 NAND GATES."



| 1

---

b) $D_3 > D_2 > D_1 > D_0$ "PRIORITY ENCODER"

D_3	D_2	D_1	D_0	A	B	V
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

| 1.5

CIRCUIT DIAGRAM.

According to the Boolean Expression. | 1

Solve K-MAP

$A = D_3 + D_2$ | 0.5

$B = D_3 + \bar{D}_2 D_1$ | 0.5

$V = D_3 + D_2 + D_1 + D_0$ | 0.5

c) 1 bit Magnitude Comparator

A_0	B_0	L	E	G
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

1

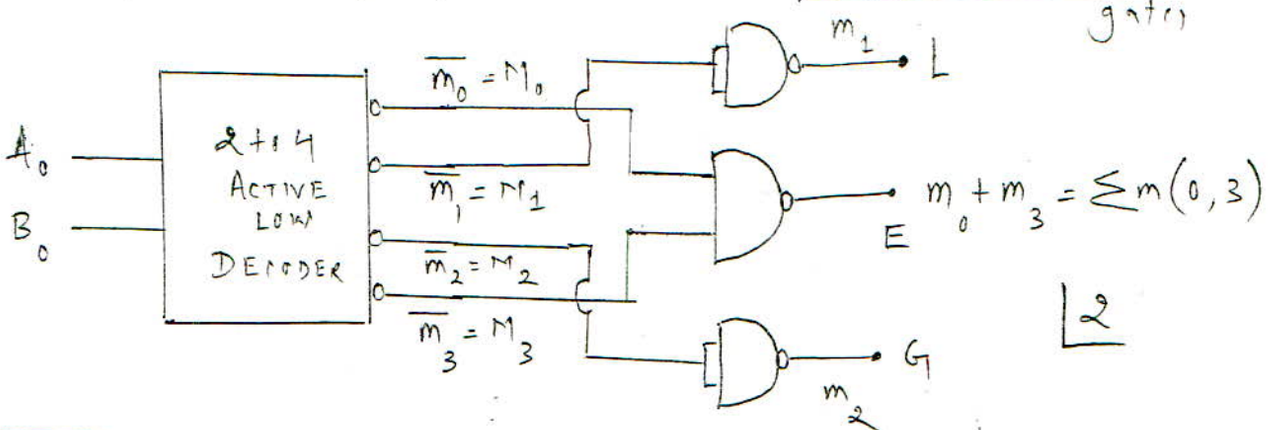
$L = \sum m(1) = \bar{A}B$

$E = \sum m(0,3) = \bar{A}\bar{B} + AB$

$G = \sum m(2) = A\bar{B}$

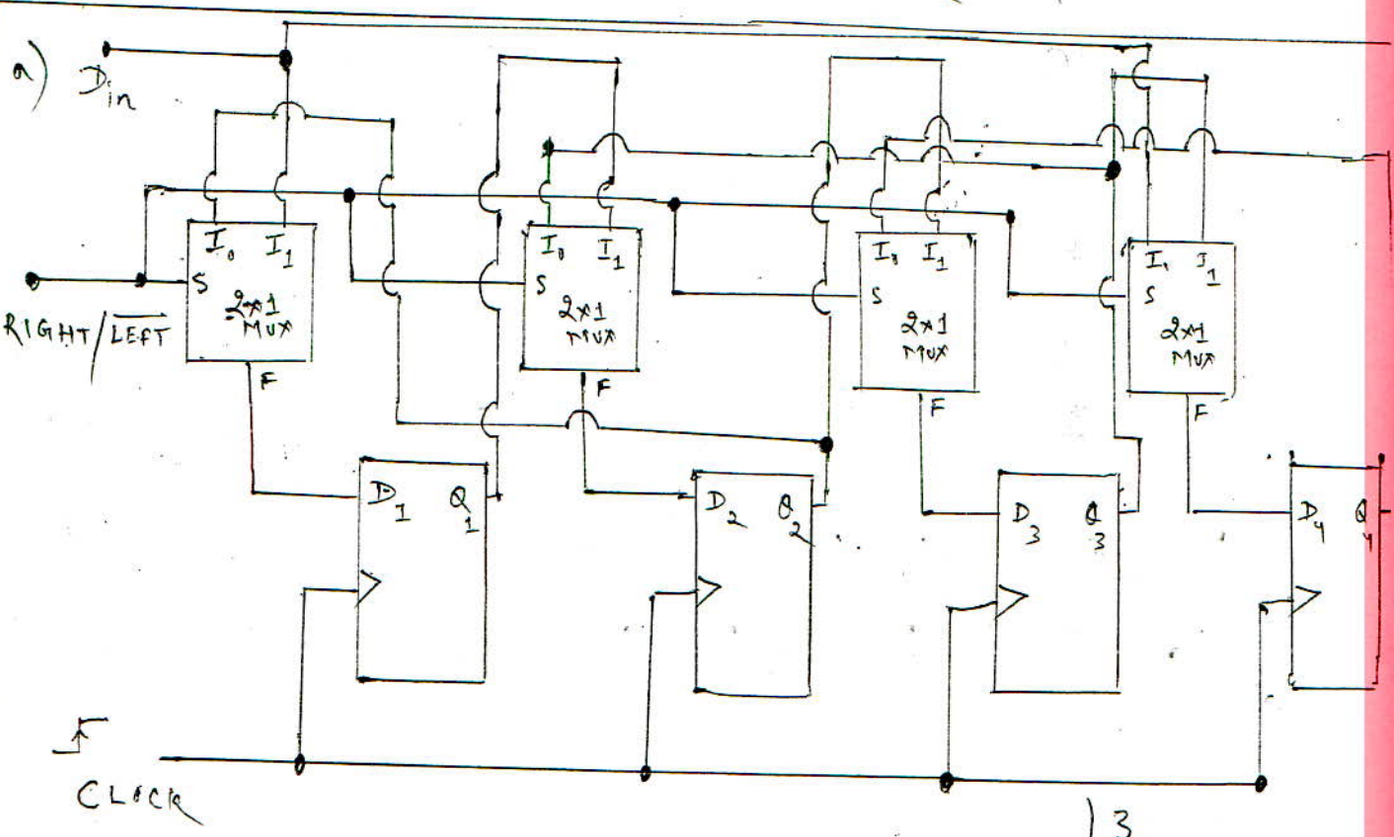
1

"Minimum 3 NAND gates"



2

3) a)



3

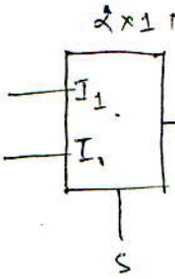
[4 bit - Bi-directional SHIFT REGISTER]

Using D-FF

CONTROL

RIGHT / $\overline{\text{LEFT}}$

When,



$F = \bar{S}I_0 + SI_1$

RIGHT $\equiv I_1$

$\overline{\text{LEFT}} \equiv I_0$

Explanation on working and 2×1 MUX configuration

1

b) $F(P,Q,R,S) = P\bar{Q} + R\bar{S} + P\bar{R}$

$= P\bar{Q}.1.1 + 1.1.R\bar{S} + P.1.\bar{R}.1$

$= P\bar{Q}(R+\bar{R})(S+\bar{S}) + (P+\bar{P})(Q+\bar{Q})R\bar{S} + P(Q+\bar{Q})\bar{R}(S+\bar{S})$

$= P\bar{Q}\bar{S}\bar{R} + P\bar{Q}\bar{R}S + P\bar{Q}R\bar{S} + P\bar{Q}RS + \bar{P}\bar{Q}R\bar{S} + \bar{P}QR\bar{S} + P\bar{Q}R\bar{S} + PQR + P\bar{Q}\bar{R}\bar{S} + P\bar{Q}\bar{R}S + PQR\bar{S} + PQ\bar{R}S$

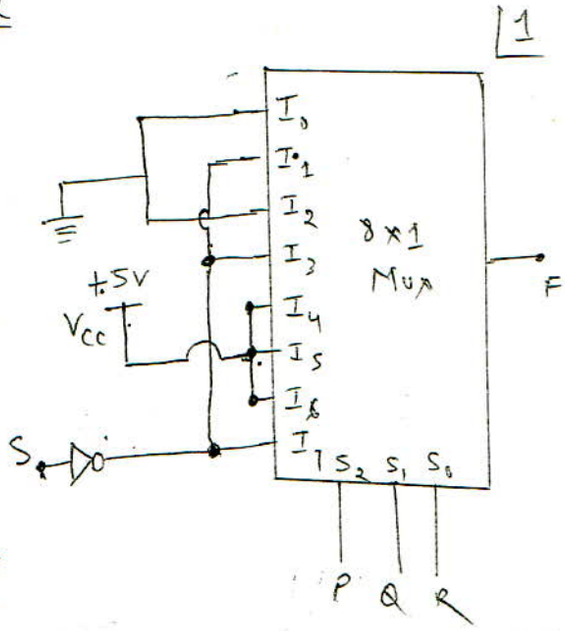
$= m_8 + m_9 + m_{10} + m_{11} + m_2 + m_6 + m_{10} + m_{14} + m_8 + m_9 + m_{12} + m_{13}$

$= m_2 + m_6 + m_8 + m_9 + m_{10} + m_{11} + m_{12} + m_{13} + m_{14}$

$= \sum m(2,6,8,9,10,11,12,13,14)$ [1]

	P	Q	R	S	F	
I_0	0	0	0	0	0	
	0	0	0	1	0	$F=0$
I_1	0	0	1	0	1	
	0	0	1	1	0	$F=\bar{S}$
I_2	0	1	0	0	0	
	0	1	0	1	0	$F=0$
I_3	0	1	1	0	1	
	0	1	1	1	0	$F=\bar{S}$
I_4	1	0	0	0	1	
	1	0	0	1	1	$F=1$
I_5	1	0	1	0	1	
	1	0	1	1	1	$F=1$
I_6	1	1	0	0	1	
	1	1	0	1	1	$F=1$
I_7	1	1	1	0	1	
	1	1	1	1	0	$F=\bar{S}$

[2]



[1]

c)

PAL

1) Programmable Array Logic

2) Programmable "AND" — Fixed "OR"

3) Cheaper / simpler.

4) Any Boolean func^n in SOP form can be implimented.

PLA [2]

1) Programmable Logic Array

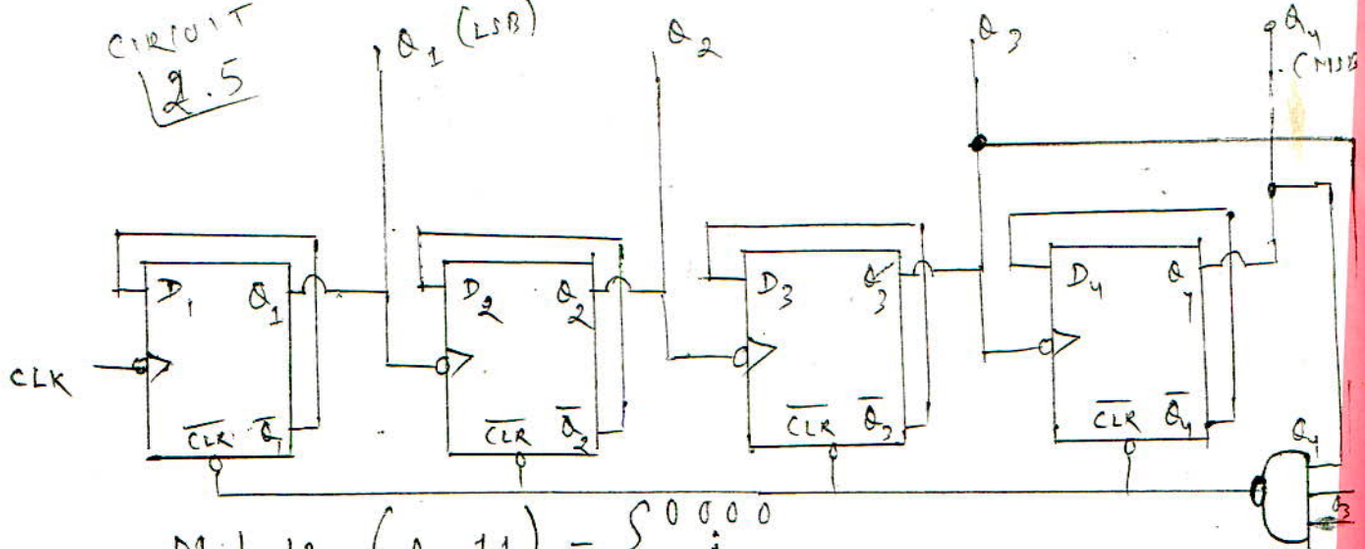
2) Programmable "AND" — Programmable "OR"

3) Costlier / more complex.

4) Any Boolean func^n SOP form can be implimented.

4) a) Asynchronous Mod-12 UP-COUNTER USING D-FF

CIRCUIT 2.5



Mod-12 (0 - 11) - { 0000 : 1011

$\overline{CLR} = \overline{Q_4 \cdot Q_3}$ 0.5

Mod-12

	Q_4 Q_3 Q_2 Q_1
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1
10	1 0 1 0
11	1 0 1 1
Not Right!	1 1 0 0

1

b) "REFER THE CIRCUIT IN QUESTION"

$D_3 = 1$
$D_5 = 0$
$D_6 = 1$
$D_7 = 0$

(EVEN PARITY Hamming Encoder)

$P_1 = D_3 \oplus D_5 \oplus D_7 = 1 \oplus 0 \oplus 0 = 1$

$P_2 = D_3 \oplus D_6 \oplus D_7 = 1 \oplus 1 \oplus 0 = 0$ 1

$P_4 = D_5 \oplus D_6 \oplus D_7 = 0 \oplus 1 \oplus 0 = 1$

PRIORITY ENCODER

Given, $D_0 > D_1 > D_2 > D_3 > D_4 > D_5 > D_6 > D_7$

$D_0 = 0$
$D_1 = P_1 = 1$
$D_2 = P_2 = 0$
$D_3 = D_3 = 1$
$D_4 = P_4 = 1$
$D_5 = D_5 = 0$
$D_6 = D_6 = 1$
$D_7 = D_7 = 0$

A = 1
B = 1
C = 0

These are SELECT LINE for 8×1 MUX

$A = S_2 = 1$
$B = S_1 = 1$
$C = S_0 = 0$

1

8 × 1 Mux

$S_2 = 1$
$S_1 = 1$
$S_0 = 0$

$F = I_6$

$I_6 = 0$ So, $F = 0$ (output of 8×1 Mux)

Which is 'A' for 1 bit Magnitude Comparator. [1]

1-bit Magnitude Comparator

$A = 0$

$A = 0 \quad B = 0$

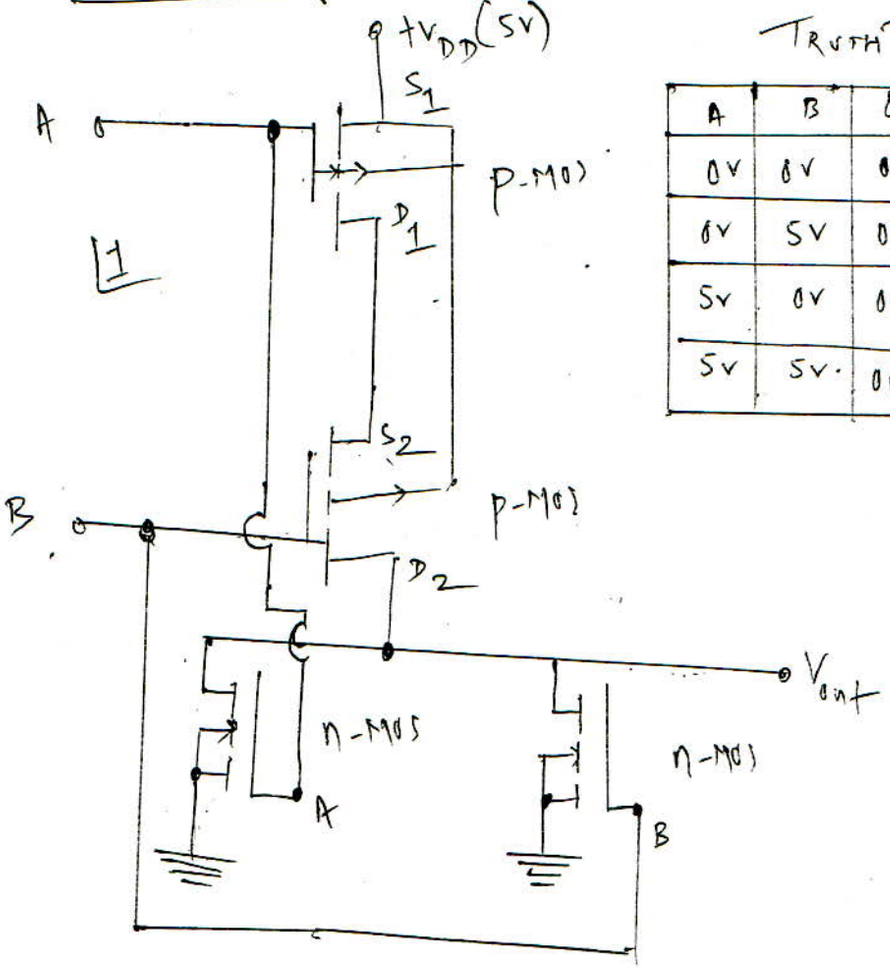
This,

$A < B\ (L) = 0$
$A = B\ (E) = 1$
$A > B\ (G) = 0$

[1]

---

c) CMOS NOR GATE

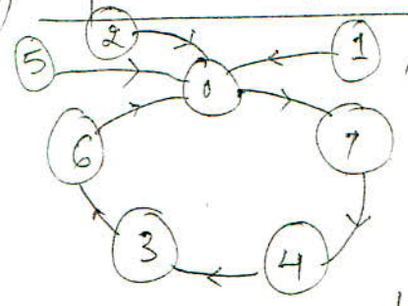


[1]

TRUTH TABLE [1]

A	B	Q_1	Q_2	Q_3	Q_4	V_{out}
0V	0V	ON	ON	OFF	OFF	5V
0V	5V	ON	OFF	OFF	ON	0V
5V	0V	OFF	ON	ON	OFF	0V
5V	5V	OFF	OFF	ON	ON	0V

5) a) Synchronous Counter (0, 7, 4, 3, 6)



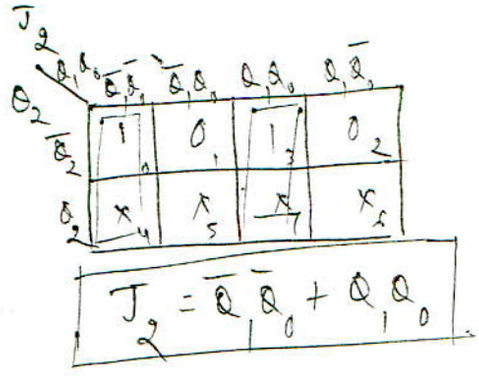
"Avoid Lock-out"

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

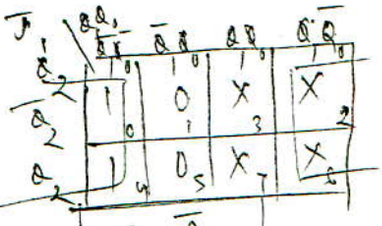
Using J-K FF

PS Q_2	Q_1	Q_0	NS Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	1	1	1	1	X	1	X	1	X
0	0	1	0	0	0	0	X	0	X	X	1
0	1	0	0	0	0	0	X	X	1	0	X
0	1	1	1	1	0	1	X	X	0	X	1
1	0	0	0	1	1	X	1	1	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	1	0	0	X	0	X	1	X	1

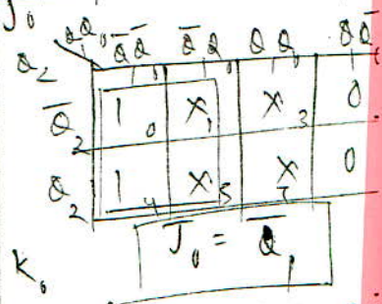
Solve K-MAP [1.5]



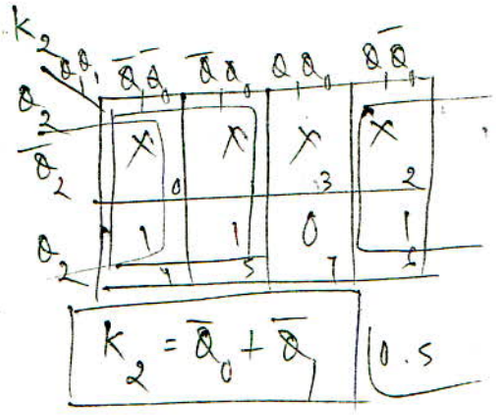
$J_2 = \bar{Q}_1\bar{Q}_0 + Q_1Q_0$



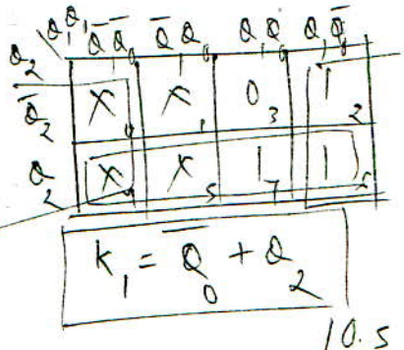
$J_1 = \bar{Q}_0$



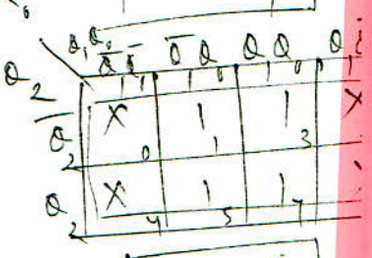
$J_0 = \bar{Q}_1$



$K_2 = \bar{Q}_0 + \bar{Q}_1$ [0.5]



$K_1 = \bar{Q}_0 + Q_2$ [0.5]



$K_0 = 1$ [0.5]

CIRCUIT DIAGRAM [1]

b)

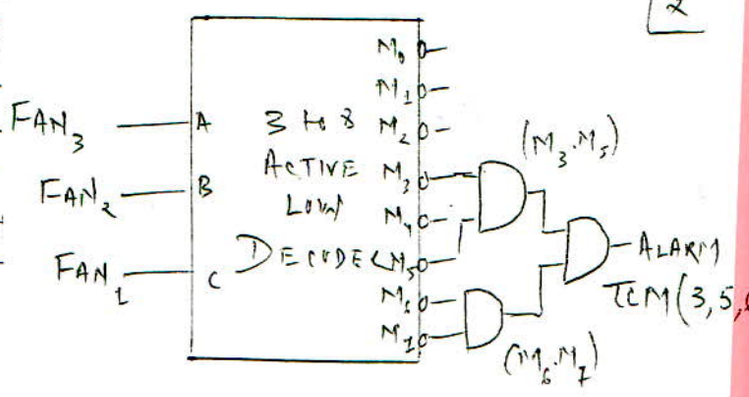
FAN3	FAN 2	FAN 1	ALARM
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

[1.5]

ON - 1
OFF - 0

$ALARM = \sum m(0, 1, 2, 4)$ [0.5]
$= \overline{TCM}(3, 5, 6, 7)$

[2]



c) 128 K × 8

(i) data input and data output lines : 8 [1

(ii) 128 K = 128 × 1024 = $2^7 \times 2^{10} = 2^{17}$ [1

17 Address Lines.

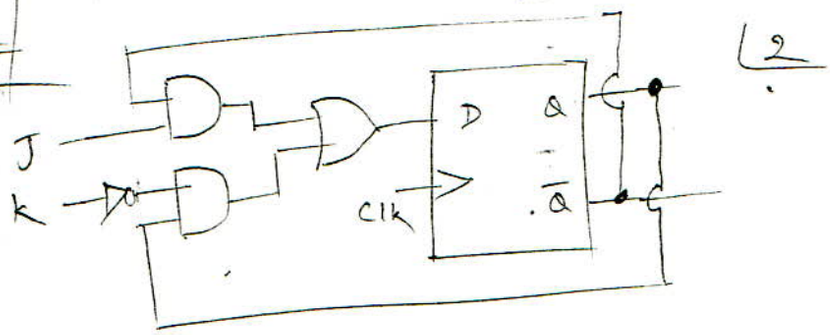
---

6) a) Solve Characteristic Table + Excitation Table [1

Solve K-MAP.

J \ Q_n	$\bar{Q}_n$	$\bar{K}Q_n$	KQ_n	$K\bar{Q}_n$
$\bar{J}$	0	1	0	0
J	1	1	0	1

$D = J\bar{Q}_n + \bar{K}Q_n$ [1



[2

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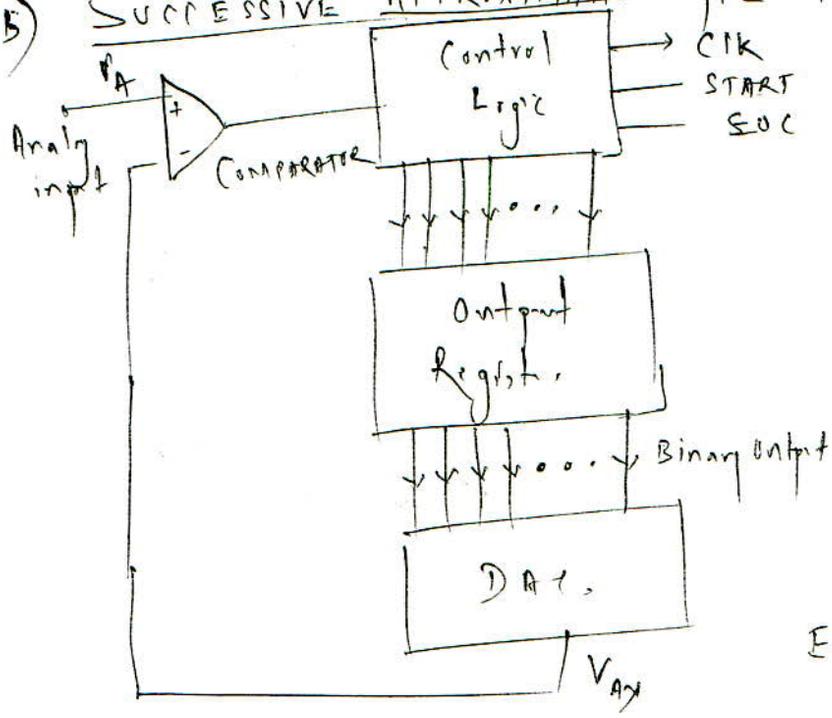
b) SUCCESSIVE APPROXIMATION Type ADC



t_c for SAR = (N × 1) Clk Cycle.

N Clks.

1 clk = $\frac{1}{f} = \frac{1}{1\,MHz}$ = 1 μsec.

N clk. =

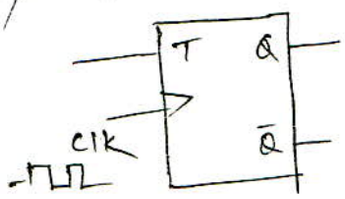
N = 4 4 μsec.

[2

Explanation [2

---

c) T-FF



f_{clk} = 6 MHz = $t_{clk} = \frac{1}{6}$ μsec.

(i) T = 0. ⇒ Q(t+1) = Q(t) (No. change)

[1

Dr. f = 0 Hz.

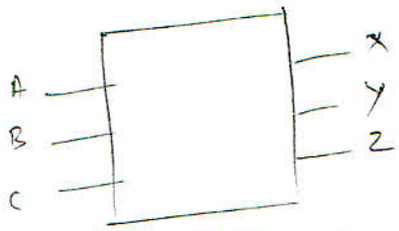
(ii) T = 1 ⇒ $Q(t+1) = \overline{Q(t)}$ (Toggle)

$f_{output} = \frac{1}{2} \times f_{clk}$ = 3 MHz

3 MHz

[1

7) a)



Condition -1

0 → 1

1 → 2

5 → 6

3 → 4

Condition -2

4 → 3

2 → 1

6 → 5

7 → 6

A	B	C	X	Y	Z
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	0

1.5

X

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0 (0)	0 (1)	1 (3)	0 (2)
A	0 (4)	1 (5)	1 (7)	1 (6)

$X = AC + BC + AB$ 0.5

Y

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0 (0)	1 (1)	0 (3)	0 (2)
A	1 (4)	1 (5)	1 (7)	0 (6)

0.5

$Y = A\bar{B} + \bar{B}C + AC$

Z

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1 (0)	0 (1)	0 (3)	1 (2)
A	1 (4)	0 (5)	0 (7)	1 (6)

$Z = \bar{C}$ 0.5

CIRCUIT DIAGRAM 1

---

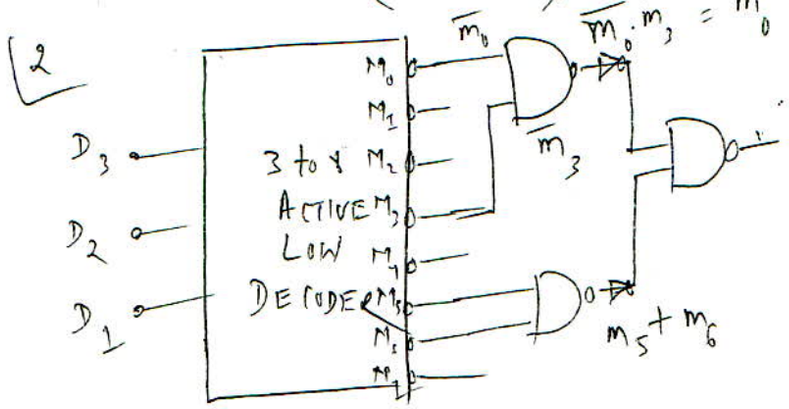
b) 3 bit Odd parity GENERATOR

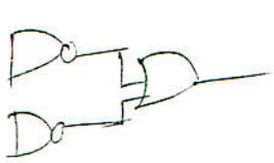
$P_{ODD} = D_1 \oplus D_2 \oplus D_3 = D_1 \odot D_2 \odot D_3$ 1

$= \sum m(0, 3, 5, 6)$

D_3	D_2	D_1	P_{ODD}
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

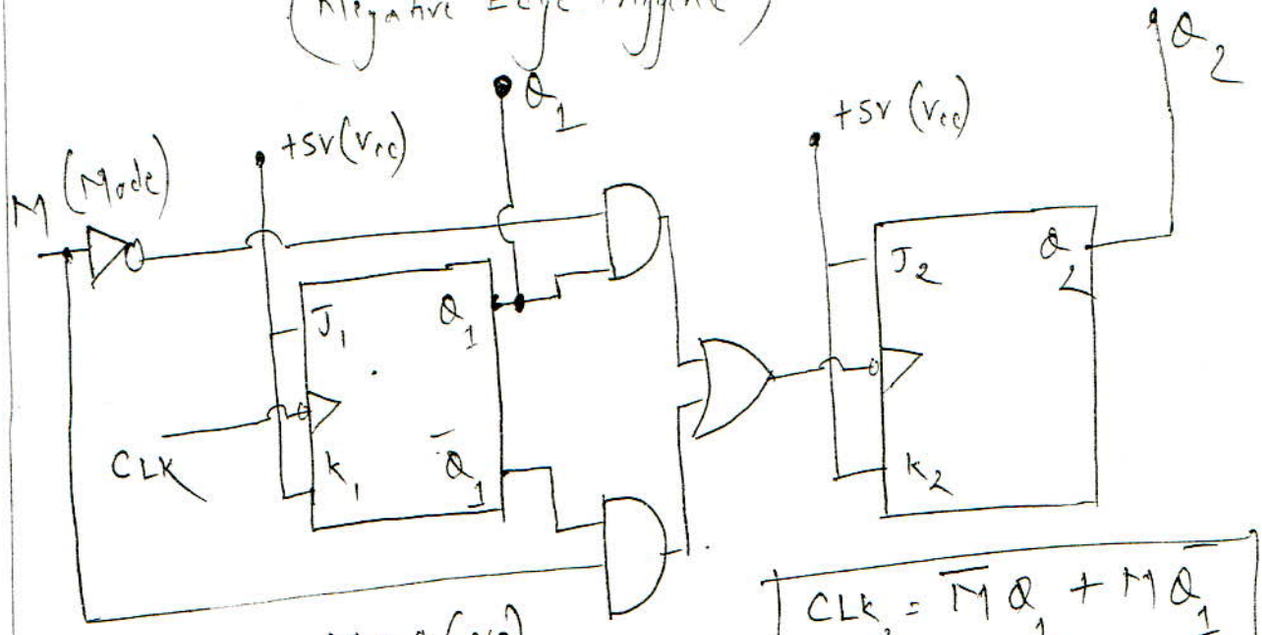
2





e) 2-bit Asynchronous UP/DOWN COUNTER

(Negative Edge Triggered)



L2

$CLK_2 = \overline{M} Q_1 + M \overline{Q_1}$

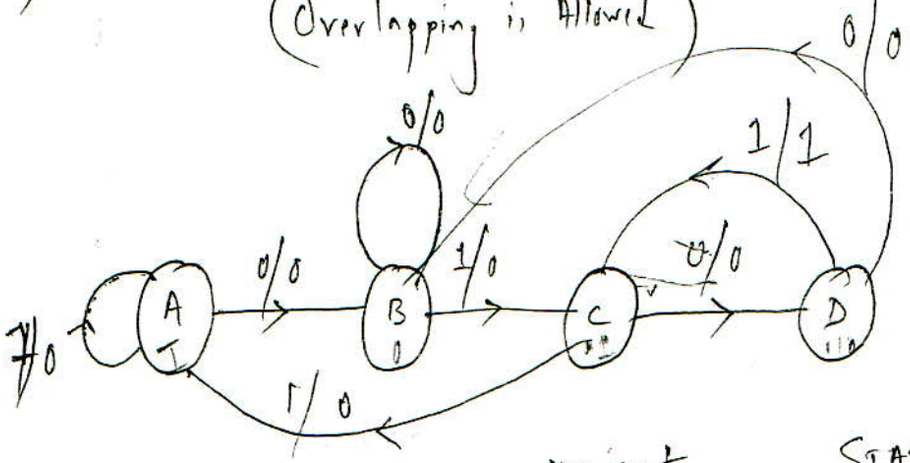
M = 0 (UP)

M = 1 (DOWN)

---

8) a) SEQUENCE DETECTOR (0101) – Mealy Model –

(Overlapping is Allowed)



1

x = input

PS	NS, O/P	
	x = 0	x = 1
A	B, 0	A, 0
B	B, 0	C, 0
C	D, 0	A, 0
D	B, 0	C, 1

1

STATE Assignment

A → 00

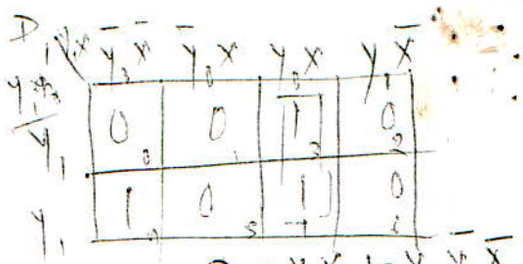
B → 01

C → 10

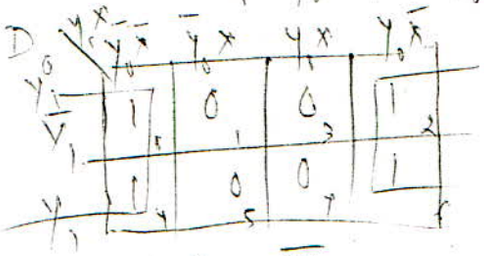
D → 11

PS (Y_1)	PS (Y_0)	Input X	NS (Y_1)	NS (Y_0)	O/P Z	D_1	D_0
0	0	0	0	1	0	0	1
0	0	1	0	0	0	0	0
0	1	0	0	1	0	0	1
0	1	1	1	0	0	1	0
1	0	0	1	1	0	1	1
1	0	1	0	0	0	0	0
1	1	0	0	1	0	0	1
1	1	1	1	0	1	1	0

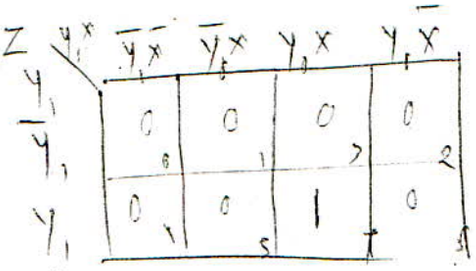
P(S) $Y_1 Y_0$ N(S) $Y_1 Y_0$ — 1.5



$D_1 = y_0 x + y_1 \bar{y}_0 \bar{x}$



$D_0 = \bar{x}$



$Z = Y_1 Y_0 x$

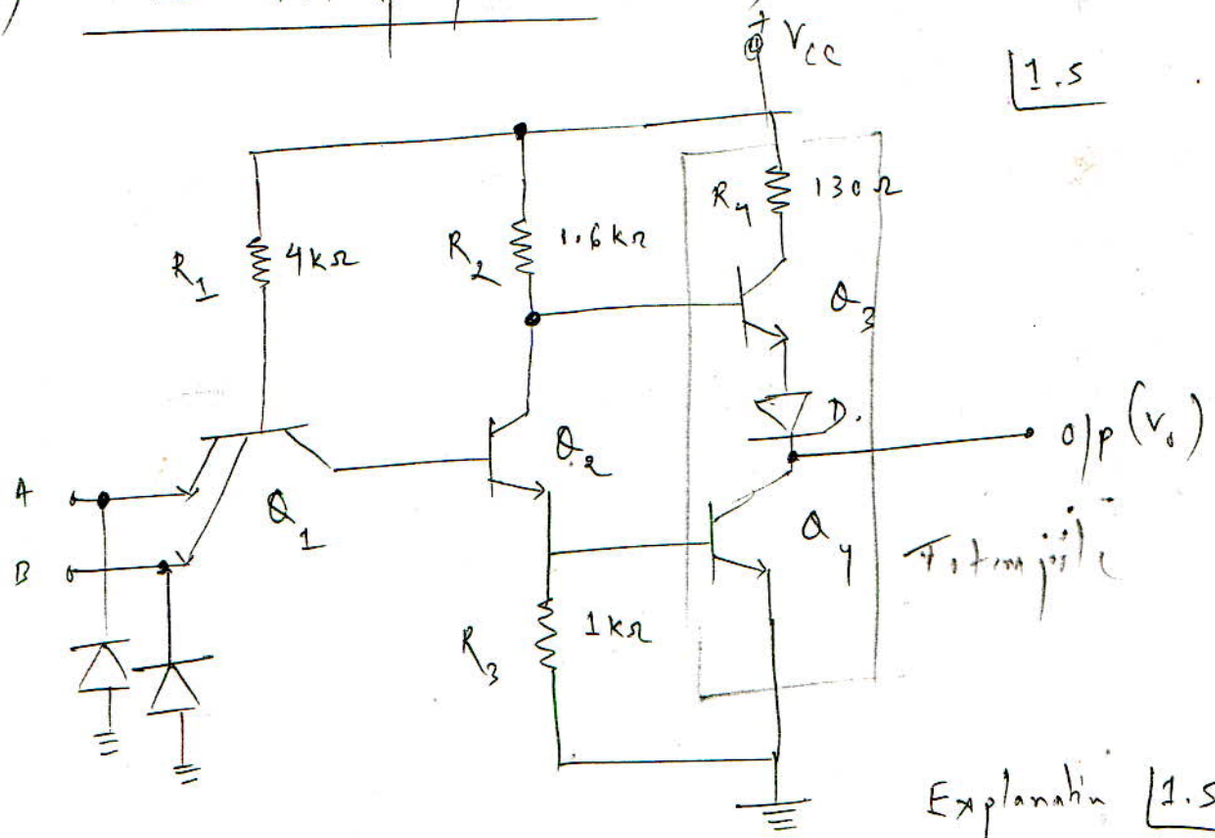
$D_1 = Y_0 x + Y_1 \bar{Y}_0 \bar{x}$ 0.5

$D_0 = \bar{x}$ 0.5

$T = Y_1 Y_0 x$ 0.5

Appropriate Circuit diagram 1

b) TTL - Totimp - pole (NAND)



1.5

Explanation 1.5

Advantage:

1. Pullup Resistance is less, RC ↓ τ = time Constant is less.
2. Circuit is faster.

1