

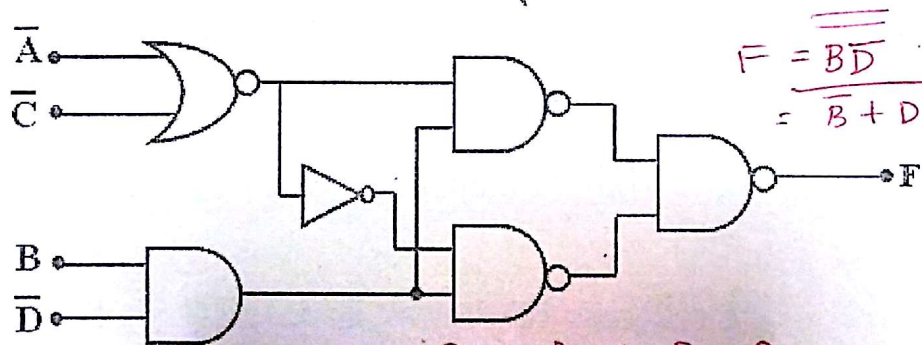
**KIIT UNIVERSITY, BHUBANESWAR**  
**SPRING MID SEMESTER EXAMINATION-2014**  
**DIGITAL ELECTRONIC CIRCUITS [EC- 402]**

Full Marks: 25

Duration: 2Hrs

Answer any FIVE questions including question No.1 which is compulsory.  
 The figures in the margin indicate full marks.  
 Candidates are required to give their answers in their own words as far as practicable and  
all parts of a question should be answered at one place only.

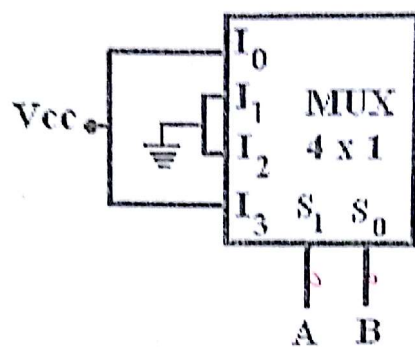
- (1) a) 'XOR and XNOR gates can be used as a buffer as well as an inverter', Justify. [1x5]  
 b) Perform following arithmetic: (i) BCD addition (895+648),  
 (ii)  $(-13) - (-6)$  using 2's complement method.  
 c) Show that,  $V.W + \overline{W}.X + X.Y.Z.V = \overline{W}.X + V.W$ , where V, W, X, Y and Z are Boolean variables.  
 d) What is the difference between active LOW and active HIGH terminals?  
 e) 'XS-3 codes are sequential & self-complementing but not cyclic', Justify.
- (2) Obtain the minimized expression for the following 4-variable Boolean expression using K-map method and implement the minimized expression using only NAND gates. [5]  
 $F(P, Q, R, S) = \Pi M(9, 10, 12, 15) \cdot d(1, 2, 4, 7)$
- (3) a) What is the difference between Ripple carry adder and Look-ahead carry adder explain in brief and draw the circuit diagram of 3-bit Look-ahead carry generator. [4]  
 b) What is 'BCD to Seven Segment Decoder'? [1]
- (4) a) Simplify the given logic circuit and implement the simplified expression using only NOR gates. [4]



- b) Encode 4-bit data word '1000' into a 7-bit even-parity Hamming code. [1]  
 Handwritten:  $P_1=1, P_2=1, P_4=0$   
 1110000

- (5) a) What is Decoder? Explain it with a block diagram and implement the Full-Subtractor circuit using a 3-8 decoder having active-LOW output lines and 2-input AND gates. [4]
- b) Determine the decimal value of the binary string '110011' in  
 (i) Sign-Magnitude form, -19  
 (ii) Sign-1's Complement form, -12  
 (iii) Sign-2's Complement form, -13  
 (iv) Unsigned binary number 51

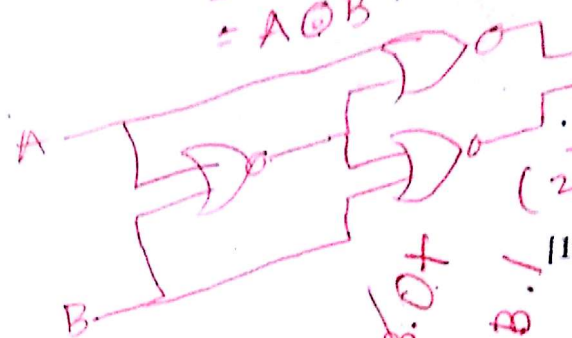
- (6) a) Identify the Boolean function  $F(A, B)$  implemented with 4x1 MUX and then implement the identified Boolean function  $F(A, B)$  using minimum number of NOR gates only.



$$F = \bar{A}\bar{B} + AB \quad (2)$$

$$= (XNOR)$$

$$= A \odot B$$



- b) Design a 8x1 MUX using two 4x1 MUX and one 2x1 MUX.

$$\bar{A}\bar{B}.1 + \bar{A}B.0 + A\bar{B}.1 + AB.0$$

$$= \bar{A}\bar{B} + \bar{A}B + A\bar{B} + AB.0$$

$$= \bar{A}(\bar{B} + B) + A(\bar{B} + B).0$$

$$= \bar{A}.1 + A.0$$

$$= \bar{A} + 0$$

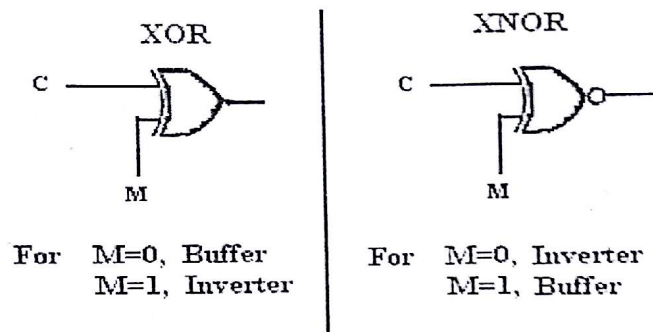
$$= \bar{A}$$



## Solutions

Mid Semester Examination 2014  
Digital Electronic Circuit (EC-402)

(1) a) XOR and XNOR gates as a buffer as well as an inverter



b) i) BCD addition (895+648)

1000	1001	0101
+ 0110	0100	1000
1110	1101	1101
+ 0110	0110	0110
10100	10011	10011
↙ +1	↙ +1	↙ +1
0001	0101	0100
0101	0100	0011

ii)  $(-13) - (-6) = (-7)$  using 2's complement method.

$(-13)$  in 2's complement form = 10011

$(-6)$  in 2's complement form = 11010

2's complement of '11010' = 00110

Now  $(10011) + (00110) = 11001 = (-7)$  in 2's complement form

c)  $V.W + \bar{W}.X + X.Y.Z.V (W+\bar{W})$   
 $= V.W + \bar{W}.X + X.Y.Z.V.W + X.Y.Z.V.\bar{W}$   
 $= VW(1+XYZ) + \bar{W}.X(1+YZV)$   
 $= V.W + \bar{W}.X$

d) Active LOW terminals are those for which the action represented or initiated by a variable occurs when it is equal to a '0'. Ex: NAND gate output terminal. Active HIGH terminals are those for which the action represented or initiated by a variable occurs when it is equal to a '1'. Ex: AND gate output terminal.

e) In **Self-complementing codes**, the code word of the 9's complement of 'N' can be obtained from the code word of 'N' by interchanging all the zeros and ones.

- XS-3 codes satisfy the definition of Self-complementing codes

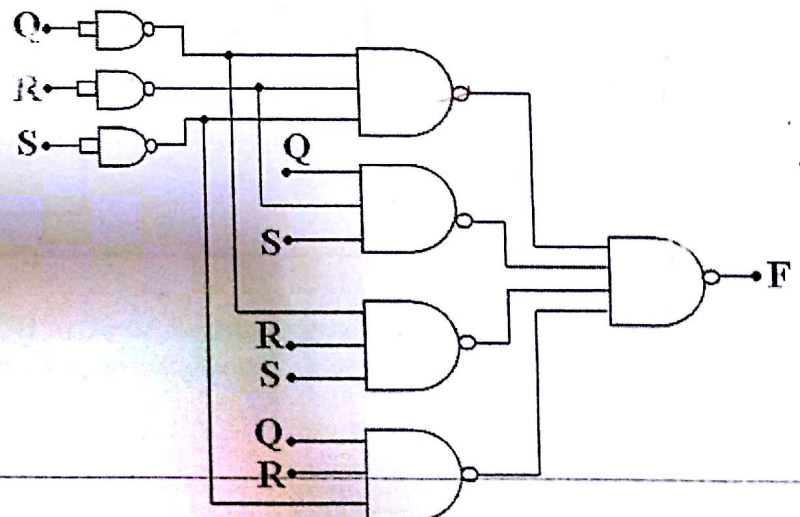
In **Sequential codes**, each succeeding code word is one binary number greater than its preceding code word.

- XS-3 codes satisfy the definition of Sequential codes
- XS-3 codes are not unit distance codes so they are not Cyclic Codes.

(2)  $F(P, Q, R, S) = \prod M(9, 10, 12, 15) \cdot d(1, 2, 4, 7)$   
 $= \sum m(0, 3, 5, 6, 8, 11, 13, 14) + d(1, 2, 4, 7)$

[1]

PQ \ RS	00	01	11	10
00	1 <sub>0</sub>	X <sub>1</sub>	1 <sub>3</sub>	X <sub>2</sub>
01	X <sub>4</sub>	1 <sub>5</sub>	X <sub>7</sub>	1 <sub>6</sub>
11		1 <sub>13</sub>		1 <sub>14</sub>
10	1 <sub>8</sub>		1 <sub>11</sub>	



$F(P, Q, R, S) = \bar{Q}\bar{R}\bar{S} + Q\bar{R}\bar{S} + \bar{Q}R\bar{S} + Q\bar{R}\bar{S}$

[2]

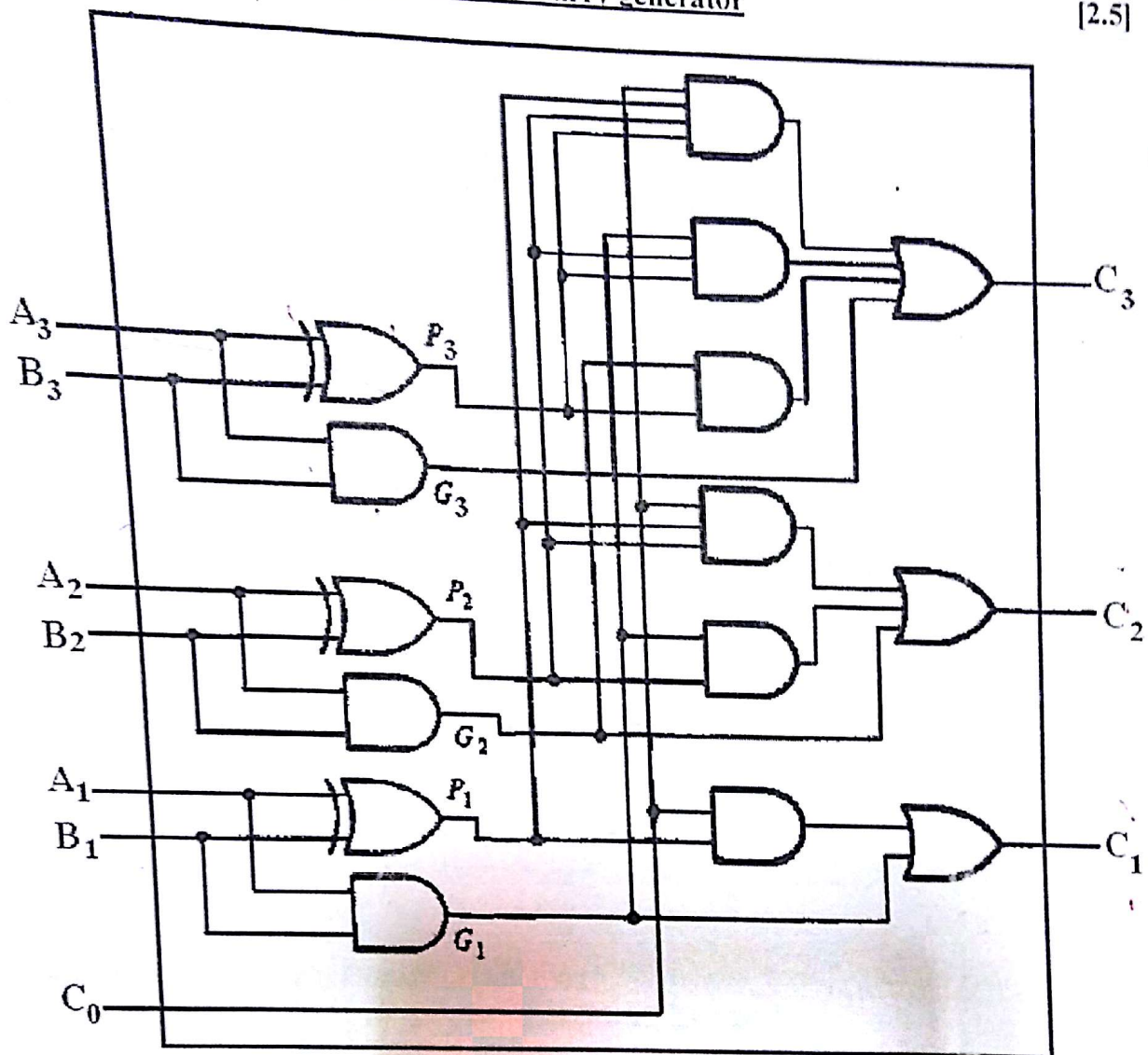
[2]



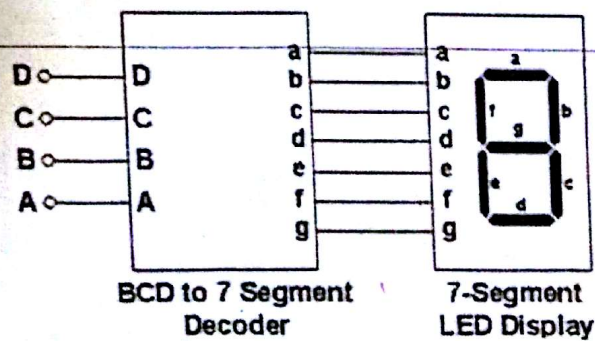
(3) a) Difference between Ripple carry adder and Look- ahead carry adder explanation [1.5]

Circuit diagram of 3-bit Look-ahead carry generator

[2.5]



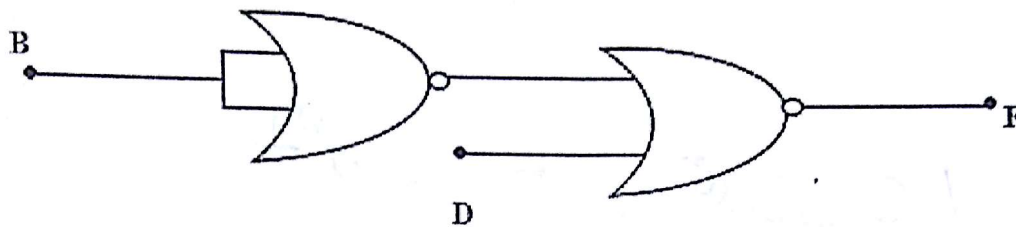
b) **BCD to Seven Segment Decoder:** A BCD to Seven Segment decoder accepts a decimal digit in BCD and generates the corresponding seven-segment code to display the decimal symbol using seven segment display. [0.5]



[0.5]

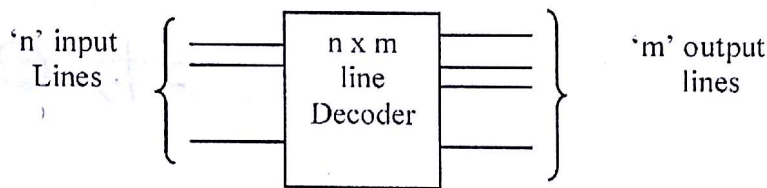
(4) a) Simplified Boolean expression of the given circuit is  $F = B\bar{D}$  [2]

Implementation of the simplified expression using only NOR gates [2]



(b)  $P_1 = 1, P_2 = 1, P_4 = 0$  [0.5]  
So 7-bit Hamming code is '1110000' [0.5]

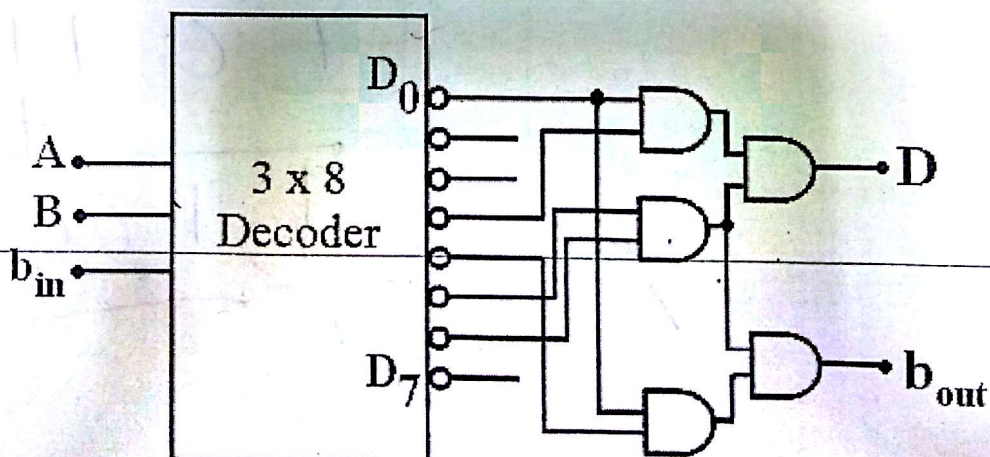
(5) a) A decoder is a logic circuit that converts an  $n$ -bit binary input code into  $2^n$  output lines, such that each output line will be activated for only one of the possible combinations of inputs.



[1]

where  $m = 2^n$

Implementation of Full-Subtractor circuit using a 3-8 decoder having active-LOW output lines and 2-input AND gates



[3]

$$D = \sum m(1, 2, 4, 7) = \prod M(0, 3, 5, 6)$$

$$b_{out} = \sum m(1, 2, 3, 7) = \prod M(0, 4, 5, 6)$$



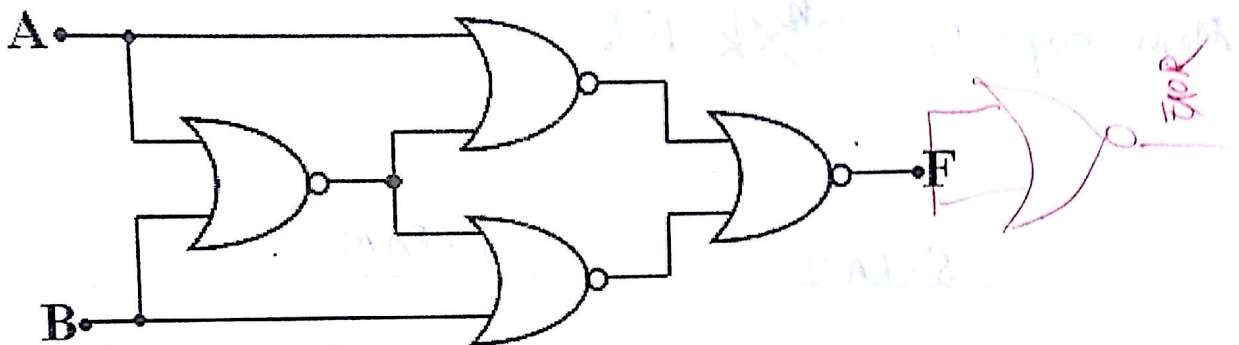
(b) Binary string '110011' in

- |                                |                   |        |
|--------------------------------|-------------------|--------|
| (i) Sign-Magnitude form        | $\Rightarrow -19$ | [0.25] |
| (ii) Sign-1's Complement form  | $\Rightarrow -12$ | [0.25] |
| (iii) Sign-2's Complement form | $\Rightarrow -13$ | [0.25] |
| (iv) Unsigned binary number    | $\Rightarrow 51$  | [0.25] |

(6)a) Function implemented by MUX is  $F(A,B) = AB + \bar{A}\bar{B}$  (XNOR Gate)

[2]

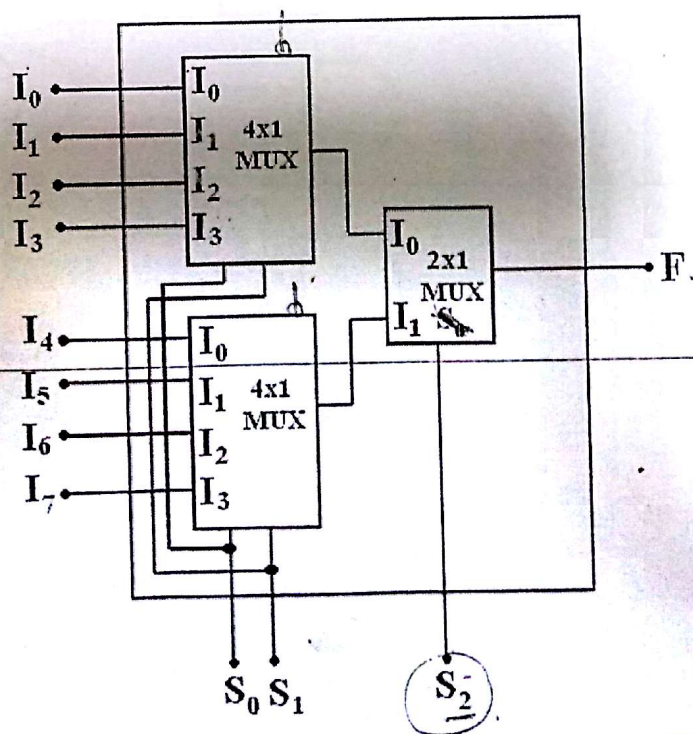
Implementation of the identified Boolean function  $F(A, B)$  using minimum number of NOR gates only

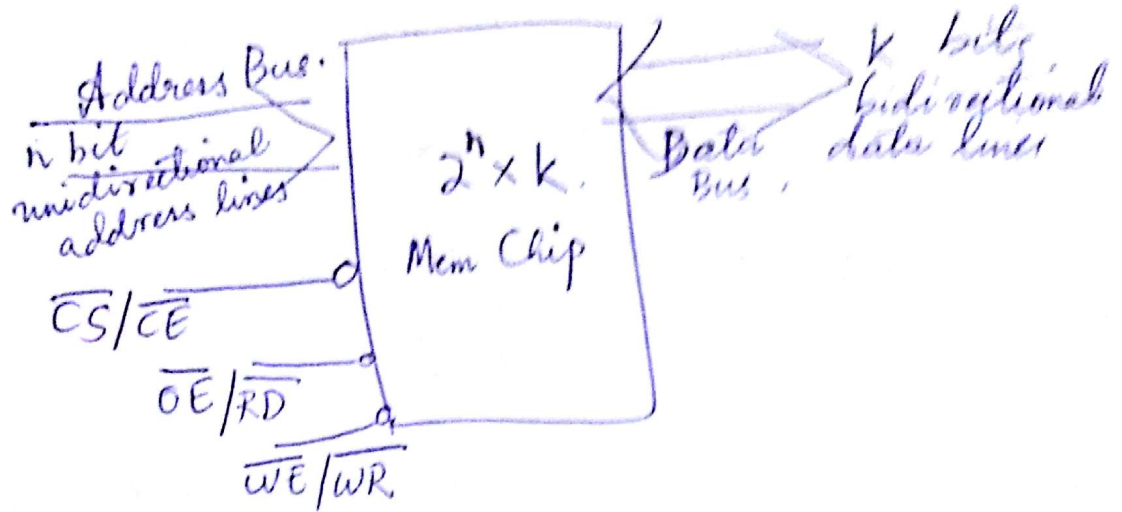


[2]

(b)  $2^3$   
8x1 MUX using two 4x1 MUX and one 2x1 MUX

[1]





Mem. capacity =  $2^n \times k$  bits

S-RAM

D-RAM