Sample Question Format
(For all courses having end semester Full Mark=50)

KIIT Deemed to be University
Online End Semester Examination(Spring Semester-2021)

Subject Name & Code: Computer Architecture (CS- 2006)
Applicable to Courses: B.Tech 4th Semester (CSE, IT, CSSE, CSCE)

Full Marks=50 **Time:2 Hours**

SECTION-A(Answer All Questions. Each question carries 2 Marks)

Time:30 Minutes **(7×2=14 Marks)**

Question No	Question Type (MCQ/SAT)	Question	CO Mapping	Answer Key (For MCQ Questions only)
Q.No:1	mcq	Question -1 Consider a register R1 contains a value 10101010 and R2 contains 11110000.What will be the value of carry , zero and overflow flags after the execution of the instruction **ADD R1,R2**// R2 is the destination a) CF=1, ZF=1, OF=1 b) CF=1, ZF=0, OF=0 c) CF=0, ZF=0, OF=1 d) CF=1, ZF=0, OF=1	CO 1	(b)
	mcq	Question -2 The number of instructions needed to add 15 numbers using **1-operand addressing mode** (including **load and store** instructions) A) 16 B) 31 C) 15 D) 17	CO 1	(A)
	mcq	Question-3 Consider the definition of a structure defined below: struct student{ int rollno; char name[20]; float cgpa;	CO 2	(D)

		} **struct student s1;** Given, the base address of s1 is available in register R5. The data member s1.cgpa can be efficiently accessed using: A) Pre-decrement addressing mode, -(R5) B) Register indirect mode, (R5) C) Relative addressing mode, X(PC),where X represents an offset D) Index addressing mode, X(R5), where X represents an offset		
	mcq	Question -4 **What will be the value in R2 after executing the following sub-program?** Clear R2 Label1 : ADD #3,R2 // *R2 is the destination* CMP #20, R2 // *Compare value in R2 with 20 (immediate value)* JL Label1 // Jump to Label1 if the value in R2 is less than 20. A) 3 B) 21 C) 18 D) 20	CO 2	(B)
Q.No:2	**mcq**	Question -1 In an 21 bit computer instruction format , the size of the address field is 8 bits. The computer have 9 two address instructions and 32 one address instructions. What will be the number of zero-address instructions supported? A) $((2^5 \times 2^8) -32) \times 2^8$ B) $(((2^5 -9) \times 2^8) -32) \times 2^8$ C) $(((2^5 -9) + 2^8) -32) + 2^8$ D) $(2^5 + 2^8) -32) + 2^8$	CO 2	(B)
	mcq	Question -2 A subroutine "**ADD**" is located at an address **9000** in memory. **After the execution** of the following instruction, what will be the value of PC? **Call ADD** // The instruction is located at address **2000** and the length of the instruction is **4 bytes**. A) 9000 B) 2004 C) 11004 D) 9004	CO 2	(A)
	mcq	Question -3 The content of register R1 is 10001011. What will be the decimal value of the content of R1 after execution of the	CO 2	(A)

		following instructions in sequence? Assume the number is represented in 2's complement format and carry bit is zero. **RotateRC #2, R1** //*RotateRight through carry.* A) -94 B) -30 C) +69 D) +94		
	mcq	Question -4 Write the assembly code to evaluate the following arithmetic expression: X = A / (B - C) Using a stack organized computer with zero-address operation instructions. A. PUSH A; PUSH B; PUSH C; SUB; DIV; POP X B. PUSH B; PUSH C; SUB; PUSH A; DIV; POP X C. PUSH A; PUSH C; PUSH B; SUB; DIV; POP X D. PUSH C; PUSH B; SUB; PUSH A; DIV; POP X	CO 2	(A)
Q.No:3	**mcq**	Question -1 Which of the following control steps are required to execute the instruction "mov R1, NUM"? [Where R1 is the source operand]. A) 1. Address_field_of_IRout, MARin 2. R1out, MDRin,Write, 3. WMFC 4. End B) 1. R1out,Addrress_field_of_IRin, end C) 1. WMFC 2.Addrress_field_of_IRout, MARin 3. MDRin, R1out, end D) 1.Address_field_of_IRout, MARin 2.R1out, MDRin,Read 3.WMFC 4. end	CO 3	(A)
	mcq	Question -2 Which of the following control steps are required to execute the instruction "mov #100, R1"? [Where R1 is the destination operand] A) 1. Address_field_of_IRout, MARin,Read 2. WMFC 3. MDRout,R1in,end B) 1.Addrress_field_of_IRout,R1in end C) 1.Addrress_field_of_IRout, MARin 2.MDRin,R1out,Write 3.WMFC 4. end D) 1.Address_field_of_IRout, MARin	CO 3	(B)

<table>
<tr><td></td><td></td><td>2. R1out, MDRin, Read
3. WMFC
4. end</td><td></td><td></td></tr>
<tr><td></td><td><u>mcq</u></td><td>Question -3
A hardwired CPU uses 10 control signals S1 to S10, in various time steps T1 to T4, to
implement 4 instructions I1to I4 as shown below:

<table><tr><td></td><td>T1</td><td>T2</td><td>T3</td><td>T4</td></tr><tr><td>I1</td><td>S1, S3, S5</td><td>S2, S4, S6</td><td>S1, S7</td><td>S10</td></tr><tr><td>I2</td><td>S1, S3, S5</td><td>S8,S9, S10</td><td>S5, S6, S7</td><td>S6</td></tr><tr><td>I3</td><td>S1, S3, S5</td><td>S7, S8,S10</td><td>S2, S6, S9</td><td>S10</td></tr><tr><td>I4</td><td>S1, S3, S5</td><td>S2, S6, S7</td><td>S5, S10</td><td>S6, S9</td></tr></table>
Write the expressions to represent the circuit for generating control signals S1 and S9 respectively?
A) S1=T1, S9=I2.T2+I3.T3+I4.T4
B) S1=T1+T3 S9=I2.T2+I3.T3+T4
C) S1=T1+T3, S9=I2.T2+I3.T3+I4.T4
D) S1=T1+I1.T3, S9=I2.T2+I3.T3+I4.T4</td><td>CO 3</td><td>(D)</td></tr>
<tr><td></td><td><u>mcq</u></td><td>Question -4
The size of Microprogram counter used in microprogrammed control unit depends on
A) The size of Control Memory
B) The number of addressing modes supported
C) The size of main memory
D) The length of an instruction</td><td>CO 3</td><td>(A)</td></tr>
<tr><td><u>Q.No:4</u></td><td><u>mcq</u></td><td>Question -1
What is the value represented in decimal by the following 32-bits IEEE representation?
S=1
E’=1000 0110
M=1001 0000 0000 0000 0000 000
A) +200
B) -200
C) -72
D) +72</td><td>CO 5</td><td>(B)</td></tr>
<tr><td></td><td><u>mcq</u></td><td>Question -2
What is the value represented in decimal by the following 32-bits IEEE representation?
S=0
E’=10000101
M=11000000000000000000000
E) 112
F) -112
G) -48
H) 48</td><td>CO 5</td><td>(A)</td></tr>
</table>

	mcq	Question -3 The representation of $-(18)_{10}$ into IEEE-754 single precision floating point representation is A) S=1 E'=1000 0011 M= 0000 0000 0000 0000 000 0010 B) S=1 E'=1000 0011 M=0010 0000 0000 0000 0000 000 C) S=1 E'=0111 1011 M=0010 0000 0000 0000 0000 000 D) S=1 E'=0111 1011 M=0000 0000 0000 0000 000 0010	CO 5	(B)
	mcq	Question -4 The representation of $-(12.75)_{10}$ into IEEE-754 single precision floating point representation is A) S=1 E'=1000 0010 M= 0000 0000 0000 0000 0010 011 B) S=1 E'=1000 0010 M=1001 1000 0000 0000 0000 000 C) S=1 E'=0111 1100 M=0000 0000 0000 0000 0010 011 D) S=1 E'=0111 1100 M=1001 1000 0000 0000 0000 000	CO 5	(B)
Q.No:5	**mcq**	Question -1 A CPU has 32 bit memory address and 128KB of cache memory. The cache is organized as a 4-way set associative cache with a block size of 32bytes. How many number of sets are there in the cache memory? A) 10 B) 1024 C) 8 D) 256	CO 4	(B)
	mcq	Question -2 Consider a direct mapped cache of size 16MB . In the CPU generated memory address, the higher order 20 bits indicates the tag bits. What will be the number of bits in the memory address? A) 44 bits B) Insufficient data C) 24 bits D) 29 bits	CO 4	(A)
	mcq	Question -3 A computer has a 512KB, 4-way set associative data	Co 4	(A)

		cache with block size of 64B. The processor sends 22-bit addresses to the cache controller. Each cache tag entry contains,in addition to the address tag, 1 valid bit, 1 modified bit and 1 replacement bit. What will be the number of bits stored for each tag entry? A) 8 bits B) 10 bits C) 9 bits D) 11 bits		
	mcq	Question -4 If there are m input lines n output lines for a decoder that is used to uniquely address a byte addressable 4KB RAM, then the minimum value of m+n is a) 4108 b) 4096 c) 12 d) 20	Co 4	(A)
Q.No:6	**mcq**	Question -1 In which of the following mapping function , there is no need of replacement algorithm A) Direct Mapping B) Set-associative Mapping C) Full associative Mapping D) Both (A) and (B)	Co 4	(A)
	mcq	Question -2 A certain processor supports only the immediate and direct addressing modes . Which of the following programming language features cannot be implemented on this processor: A) Pointers B) Arrays C) Structures D) All of these	Co 2	(D)
	mcq	Question -3 Which of the following property allows the processor to execute a number of clustered locations? A) Spatial Locality B) Temporal Locality C) Cache Coherence D) None of the above	Co 4	(A)
	mcq	Question -4 Which of the following is true for a write operation in a write back cache. A) The data is always written simultaneously in the cache and in the main memory. B) The data is modified in the cache memory only. C) The data is written to the main memory only when a dirty cache block is evicted. D) The data is written to the main memory only when an unused cache block is evicted.	Co 4	(C)
Q.No:7	**mcq**	Question -1 Which of the following data transfer schemes requires constant monitoring by the CPU of the peripheral devices? A) Both Interrupt -driven IO and DMA	Co 6	(B)

		B) Programmed IO C) Direct Memory Access D) Interrupt Driven IO		
	mcq	Question -2 Which of the following statement is **wrong** with respect to I/O Mapped IO? A) Separate Address and Data Bus. B) Common Address and Data Bus C) Separate Address Space for IO devices. D) IN and OUT instructions are used for communicating with IO devices.	Co 6	(A)
	mcq	Question -3 The DMA controller indicates the completion of DMA operation to the CPU by generating: A) HLDA signal B) Interrupt Signal C) Read Signal D) Write Signal	Co 6	(B)
	mcq	Question -4 Which of the following statement is **wrong,** with respect to vectored Interrupt technique, A) The interrupting device places the vector code on the data bus along with the INTR request. B) The interrupting device places the vector code along after receiving the INTA signal from the processor C) It eliminates the need of polling the devices. D) It is faster compared to program-controlled IO.	Co 6	(A)

SECTION-B(Answer Any Three Questions. Each Question carries 12 Marks)

Time: 1 Hour and 30 Minutes **(3×12=36 Marks)**

Question No	Question	CO Mapping (Each question should be from the same CO(s))
Q.No: 8	**Q.No:8-1st question** A. Before the following program is executed, assume that the content of	CO2,CO 3

memory location 6000 is 10 and the content of register R5 is 2000. The content of each of the memory locations from 2000 to 2010 is 40. [Here, the 2nd operand is the destination]

INSTRUCTION	Semantics
MOV 6000, R1	R1←Mem[6000]
L1: MOV (R5), R2	R2←Mem[R5]
ADD R1, R2	R2←[R1]+[R2]
MOV R2, (R5)+	Mem[R5]←[R2], R5←[R5]+1
Decrement R1	R1←[R1]-1
Branch≠0 L1	Branch if not zero to L1
HALT	Stop

What will be the content memory locations from 2000 to 2010 **after the program is executed**? Find out the number of memory references required for **each of the instructions** in the above program. Also find the total number of memory references required in the execution of the complete program.

B. Write a program to evaluate an expression X=((A-B)/C)/(D+E*F-G) using **RISC** instructions and also write another program to evaluate the same expression using **0-Addess** instructions . In the expression X,A,B,C,D,E,F, and G are memory addresses.

Answer 8.1

Part A

		Memory reference
	MOV 6000, R1	2
L1 :	MOV (R5), R2	2
	ADD R1, R2	1
	MOV R2, (R5)+	2
	Decrement R1	1
	Branch ≠ 0 L1	1
	HALT	1

[R1] = 10
[R2] = 40, R2 = 50

Total Memory references= 2 +(2+1+2+1+1)x10 + 1 = 73

2000	2001	2002	2003	2004	2005	2006	2
50	49	48	47	46	45	44	4

2010
40

Part B:

Using RISC

X = ((A-B)/C)/(D+E*F-G)

Format : (src1/dst, src2)

Load R1, A
Load R2, B

SUB R1, R2
Load R2, C
DIV R1, R2
Load R2, E
Load R3, F
MUL R2, R3
Load R3, D
ADD R2, R3
Load R3, G
SUB R2, R3
DIV R1, R2
Store X, R1

Using 0 Address

X = ((A-B)/C)/(D+E*F-G)

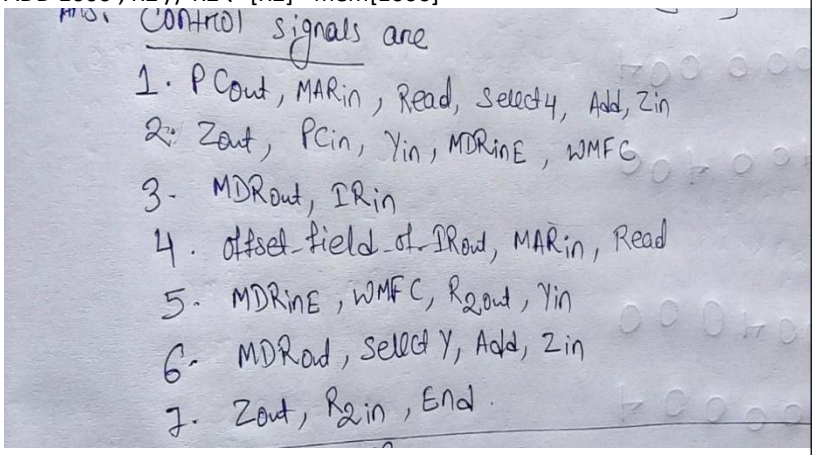
PUSH A
PUSH B
SUB
PUSH C
DIV
PUSH D
PUSH E
PUSH F
MUL
ADD
PUSH G
SUB
DIV
POP X

Q.No:8-2nd question

[6]+[6]

A. Write the micro routine for the following instruction:

ADD 1000 , R2 // R2← [R2]+ mem[1000]



[6]

B. What is the need of Y and Z register in Single bus CPU organization? Explain the need of sending the contents of Control word back to the Starting and branch address generator in the Microprogrammed Control Unit design. State the difference between Program Counter and Micro-Program Counter.

Y and Z register are needed in Single bus CPU organization for temporary storage during the execution of some instructions. These registers are never used for storing data generated by one instruction for later use by another instruction. The programmer cannot access these registers.

To support microprogram branching, starting and branch address generator takes input from control word.

Program Counter: It is a special register which contains the memory address of next instruction.
Micro-Program Counter: To read the control words sequentially from the control store, a micro program counter is used. Micro-program counter is automatically incremented by clock, causing successive microinstructions to be read from the control store. Hence, the control signals are delivered to various parts of the processor in the correct sequence.

[6]

Q.No:8-3rd question

[9+3]

A. Write the sequence of control steps for the following instructions for single bus CPU organization:
[Here, the 2nd operand is the destination]

I.
I1: MOV R1, (R2)
II.
I2: Branch=0 L1
III.
I3: ADD (R5)+, R2

Design the logic function for WMFC and PC_{in} control signal with reference to the above instructions i.e. I1 to I3.

B. "Hardwired control unit is faster compared to microprogrammed control unit" - Justify the statement.

ANSWRES :

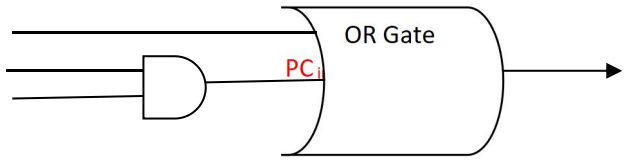
Steps	I1: MOV R1, (R2)	**Steps**	I2: Branch=0 L1	**Steps**		I3: ADD (R5)+, R2
1	PC_{out}, MAR_{in}, Read, Select 4, Add,, Z_{in}	1	PC_{out}, MAR_{in}, Read, Select 4, Add,, Z_{in}	1		PC_{out}, MAR_{in}, Read, Select 4, Add,, Z_{in}
2	Z_{out}, **PC_{in}**, y_{in} ,**WMFC**	2	Z_{out}, **PC_{in}**, y_{in} ,**WMFC**	2		Z_{out}, **PC_{in}**, y_{in} ,**WMFC**
3	MDR_{out} , IR_{in}	3	MDR_{out} , IR_{in}	3		MDR_{out} , IR_{in}

[9]

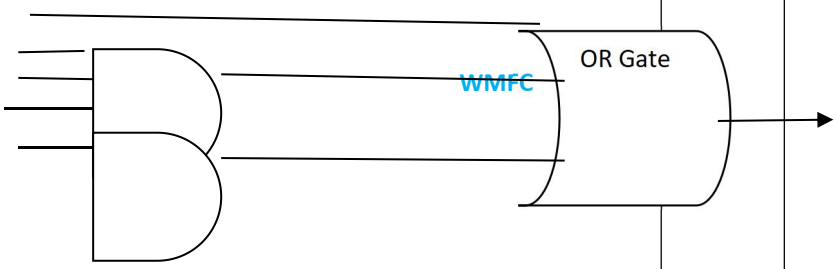
4	R2 $_{out}$, MAR $_{in}$	4	Offset_field_of_IR $_{out}$, Select Y,Add,Z $_{in}$ if Z==0 then End.	4		R5 $_{out}$, MAR $_{in}$, Read	
5	R1 $_{out}$, MDR $_{in}$, Write	5	Z $_{out}$,**PC $_{in}$**,End	5		R2 $_{out}$, Y $_{in}$, WMFC	
6	**WMFC**			6		MDR $_{out}$, Select Y,Add,Z $_{in}$	
7	End			7		Z $_{out}$, R2 $_{in}$	
				8		R5 $_{out}$, Select 4,Add,Z $_{in}$	
				9		Z $_{out}$, R5 $_{in}$, End	

I1 takes 7 control steps which are carried out in time slots T0,T1,T2,T3,T4,T5 and T6.
I2 takes 5 control steps which are carried out in time slots T0,T1,T2,T3 and T4.
I3 takes 9 control steps which are carried out in time slots T0,T1,T2,T3,T4,T5, T6,T7 and T8.

PC $_{in}$ **= T1 + I2.T4**



WMFC= T1+I1.T5+I3.T4



B.
In microprogrammed control unit, to generate the control signals needed for a particular control step, the microinstruction is to be retrieved from the control store , that takes time. And secondly , if the microinstruction follows vertical organization, then some time is needed to decode the microinstruction. But in hardwired control unit , all the control signals are generated with the help of digital logic and the time is related to gate delays only. So the time taken by hardwired control unit is less as compared to microprogrammed unit, Due to these reasons, Hardwired control unit is faster compared to microprogrammed control unit. [3 marks]

[3]

Q.No: 9

Q.No:9-1st question

CO4

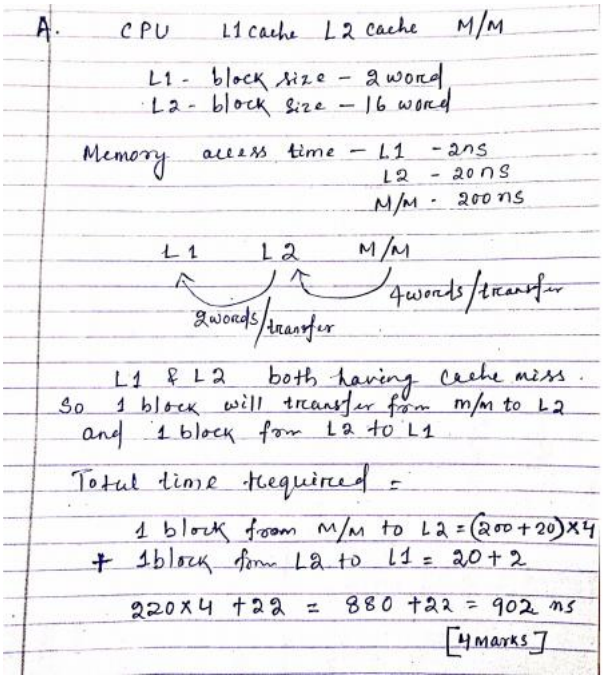
A. A computer system has an L1 cache, an L2 cache, and a main memory unit. The block size in L1 cache is 2 words. The block size in L2 cache is 16 words. The memory access times are 2 nanoseconds. 20 nanoseconds and 200

	nanoseconds for L1 cache, L2 cache and main memory unit respectively. From the **main memory 4 words can be transferred L2 cache** in a single transfer and **2 words can be transferred from L2 to L1** in a single transfer. When there is a miss in both L1 cache and L2 cache, first a block is transferred from main memory to L2 cache, and then a block is transferred from L2 cache to L1 cache. What is the total time taken for these transfers?	[5]

A. CPU L1 cache L2 cache M/M

L1 - block size - 2 word
L2 - block size - 16 word

Memory access time - L1 - 2ns
L2 - 20ns
M/M - 200ns



L1 & L2 both having cache miss.
So 1 block will transfer from m/m to L2 and 1 block from L2 to L1

Total time required =

1 block from M/M to L2 = (200+20)×4
+ 1block from L2 to L1 = 20+2

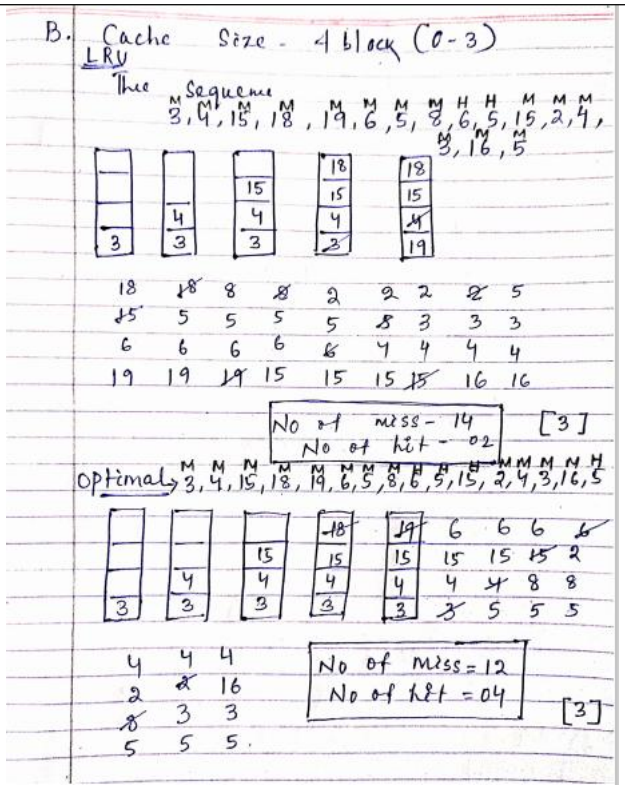
220×4 +22 = 880 +22 = 902 ns

[4marks]

B. Consider a fully associative cache with 4 cache blocks (0-3). The memory **block requests** are in the order-

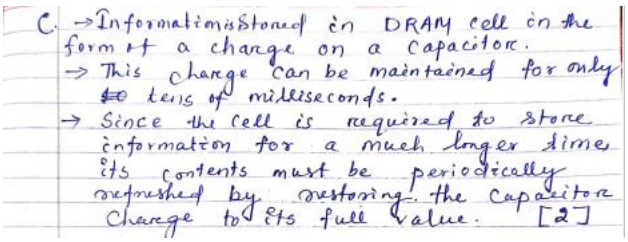
3, 4, 15, 18, 19, 6, 5, 8, 6, 5, 15, 2, 4, 3, 16, 5

Calculate the hit ratio and miss ratio using **LRU** replacement policy and **optimal** replacement policy.



[5]

C. What is the need of periodic refresh operation in DRAM cells?



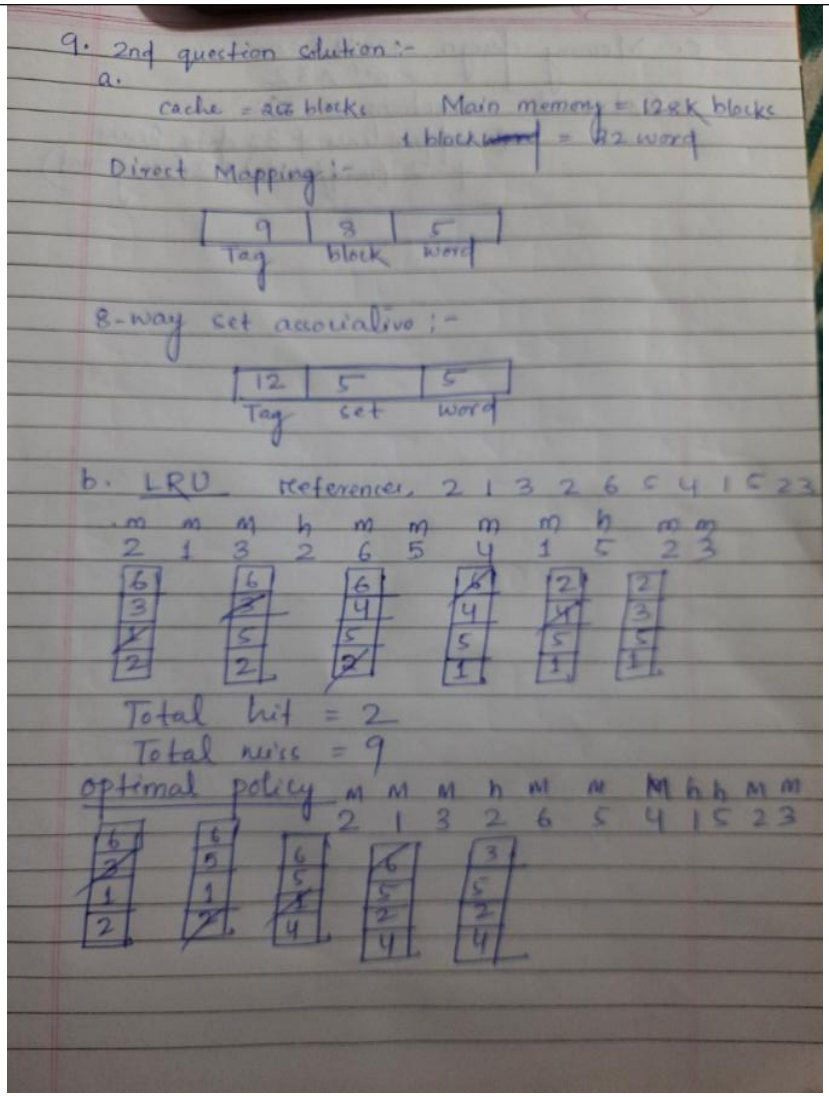
[2]

Q. No:9-2nd question

A. A cache consists of a total of 256 blocks. The main memory contains 128K blocks, each consisting of 32 words. How many bits are there in each of the TAG, BLOCK and WORD field in case of direct mapping? How many bits are there in each of the TAG, SET, and WORD field in case of 8-way set-associative mapping?

B. Calculate the number of hits and misses in a 4-blocked cache for the LRU and optimal policy if the sequence of block reference by CPU is given like; 2,1,3, 2,6,5, 4, 1,5,2,3.

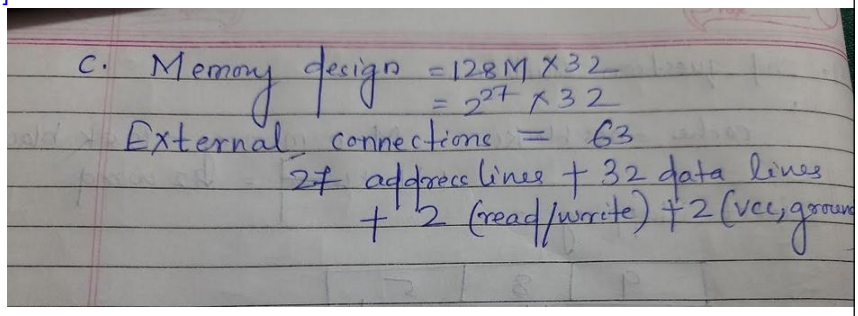
C. How many external connections are required to design 128M X 32 memory chip?



[5]

[5]

[5]



[2]

Q.No:9-3rd question

A. A cache consists of a total of 256 blocks. The main memory contains 2048 blocks, each consisting of 32 words.

(i) What is the size of the main memory?

(ii)What is the size of the cache memory?

(iii)How many bits are there in each of the TAG, BLOCK, and WORD field in case of direct mapping?

(iv) How many bits are there in each of the TAG, and WORD field in case of associative mapping?

(v)How many bits are there in each of the TAG, SET, and WORD field in case of 4-way set-associative mapping?

B.A computer uses RAM chips of 128 X 4 capacity. Design a memory capacity of 1K X 16 by using available chips.

C. A computer has a single cache(L1) (on-chip) with a 2 ns hit time and a 90% hit rate. Main memory has a 100 ns access time. What is the computer's effective access time? If we add an off-chip cache(L2) with a 8ns hit time and a 98% hit rate, what is the computer's effective access time? How much of a speedup does the off-chip cache give the computer?

[5]

A:

Ans: i) size of main memory = No. of blocks in main memory X Size of each block

= 2048 x 32
=2^11 x 2^5
=2^16

64K words

ii) size of cache memory = No. of blocks in cache memory X Size of each block

= 256 x 32
=2^8 x 2^5
=2^13

8K words

iii) Direct Mapping: Total number of bits in the address: 16

Word field: 32 words in each block ;
2^5 words in each block
Therefore 5 bits in word field

Tag field: 2048/256=8=2^3, therefore 3 bits

Block field: 256 blocks in cache : 2^8, therefore 8 bits

iv) Associative mapping:

Word field: 5 bits, same in all mapping
Tag bits: 11 bits

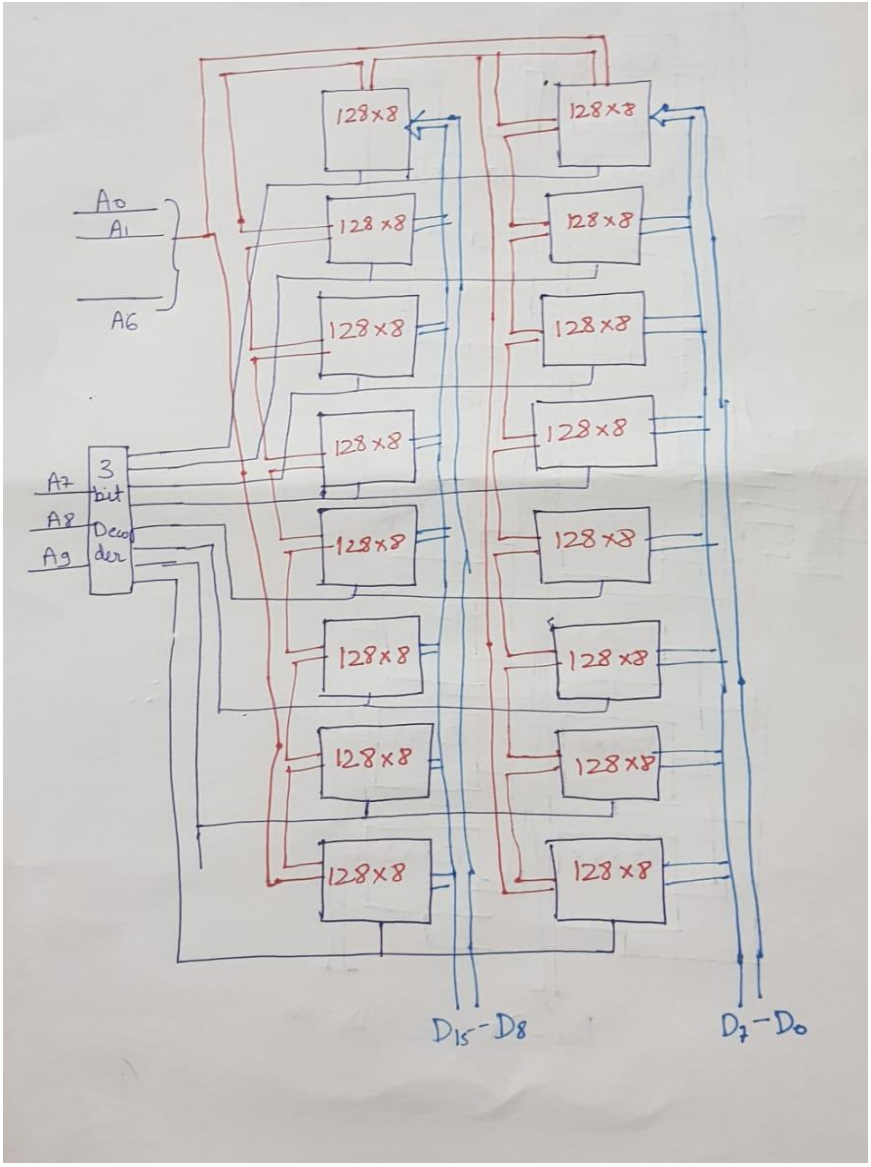
v) Set Associative mapping:

Word field: 5 bits, same in all mapping
Set field: No of sets =256/4=64, therefore 6 bits
Tag bits: No. of blocks in main memory/ No of sets in cache
=2048/64=32, therefore 5 bits

Alternate calculation:16-(5+6)= 5 bits

B:

[5]



C:A computer has a single cache(L1) (on-chip) with a 2 ns hit time and a 90% hit rate. Main memory has a 100 ns access time. What is the computer's effective access time? If we add an off-chip cache(L2) with a 8ns hit time and a 98% hit rate, what is the computer's effective access time? How much of a speedup does the off-chip cache give the computer?

[2]

Ans:

Tavg= hC + (1-h1)M

= 0.9x2 + 0.1x100

=1.8+10=11.8ns

Tavg= h1C1 + (1-h1)h2C2 + (1-h1)(1-h2)M

=0.9x2+0.1x0.98x8 + 0.1x0.02x100

=1.8 + 0.784 + 0.2

=2.784

Speed up=11.8/2.784=4.238

Q.No: 10	**Q.No:10-1st question** A. **Subtract Number 2 from Number 1. (Numbers are represented in IEEE format and give the result in IEEE format.** **Number 1:** S=0 E'= 1000 0101 M=01010000000000000000000 **Number 2:** S=0 E'= 1000 0010 M=00110000000000000000000 B. Multiply (-11 X M) using BOOTH ALGORITHM. Where M= **(your roll number last 3 digits)% 5 + 6.** If your roll no is 1905111, then M= (111%5)+6=1+6=7 C. What is the limitation of ripple carry adder. **Evaluation Scheme** ● Correct answer with proper steps for subtracting a number from another number represented in IEEE format question: 5 Marks (Each) ● Correct answer with proper steps for BOOTH ALGORITHM question: 5 marks ● Correct answer with proper steps for ripple carry adder question: 2 marks ● Step Marks as deemed fit to correct & valid steps only. **Solution** **A. Subtracting a number from another number represented in IEEE format** Given, First Number Biased Exponent=E1'=1000 0101_2=133 => Real Exponent=E1=133-127=6 Second Number Biased Exponent=E2'=1000 0010_2=130 => Real Exponent=E2=130-127=3 First Number=1.0101 x 2^6 Second Number=1.0011 x 2^3 =0.0010011 x 2^6 Subtract 2nd mantissa from first 1.0101000 0.0010011 --- 1.0010101 So the number after subtraction is = 1.0010101 x 2^6 = 1.0010101 x $2^{(6+127)}$ in biased exponent = 1.0010101 x 2^{133} in biased exponent (decimal) = 1.0010101 x $2^{10000101}$ in biased exponent (binary)	CO5 [5]

The result in IEEE format is
S=0, E'=1000 0101, M=0010101 rest 16 zeros.

……..

B.

[5]

Given,
My Roll number is = 1905025
Multiplier=Q=Last three digits of roll%5+6=025%5+6=6 (What is given M in the question)
Multiplicand=M=-11=10101, 2's of M=M^{2s}=01011

To multiply (-11 x 6)

Register	**Multiplier Register**		**Multiplicand Register**	**Operation**
A	**Q**	**Q_{-1}**	**M**	
00000	00110	0	10101	Initial configuration
00000	00110	0		No Add/Sub
00000	00011	0		Shift
01011	00011	0		A=A-M=A+M^{2S}
00101	10001	1		Shift
00101	10001	1		No Add/Sub
00010	11000	1		Shift
10111	11000	1		A=A+M
11011	11100	0		Shift
11011	11100	0		No Add/Sub
11101	11110	0		Shift

Result = Contains of AQ register = 11101 11110 = -66 (Answer of -11 x 6)

As multiplier will vary from (0+6) to (4+6) => from 6 to 10
So the last step (contains of AQ register) will be
-11 x 7 = -77 = 11101 10011
-11 x 8 = -88 = 11101 01000
-11 x 9 = -99 = 11100 11101
-11 x 10 = -110= 11100 10010

……

Limitation of Ripple Carry Adder: The disadvantage of the ripple-carry adder is that it can get very slow when one needs to add many bits. In Ripple Carry Adder, Each full adder has to wait for its carry-in from its previous stage full adder.Thus, nth full adder has to wait until all (n-1) full adders have completed their

[2]

operations. This causes a delay and makes ripple carry adder extremely slow.

Q. No:10- 2nd question

A. Perform the following division operation using restoring and non-restoring method. 14 ÷ d

Where d= **(your roll number last 3 digits)% 5 +3.**

If your roll no is 1905111, then d= (111%5)+3=1+4=4

B. **Perform the addition of the following two numbers represented in IEEE format and give the result in IEEE format.**

Number 1:

S=0

E'= 1000 0101

M=01010000000000000000000

Number 2:

S=0

E'= 1000 0010

M=00110000000000000000000

Evaluation Scheme

- Correct answer with proper steps for Restoring & Non-restoring Question: 3.5 Marks (Each)
- Correct answer with proper steps for Addition of two IEEE Floating point numbers Question: 5 marks
- Step Marks as deemed fit to correct & valid steps only.

Solution

A. Division operation using restoring and non-restoring method. 14 ÷ d [8]

Where d= (your roll number last 3 digits)% 5 +3

=025%5+3=0+3=3 as my roll number is 1905025

Division operation using restoring Method (14 ÷ 3 = ?)

Dividend=Q=14=1110, Divisor=M=3=11

As length of dividend is 4 bit, So length of A and M should be (4+1)=5 bits.

So, A=00000 and M=00011 M^{2s}=11101

Steps	Sub-step	Step/Action	Accumulator (A)	Dividend (Q)	Divisor/Remarks (M)
0	0	Initial values	00000	1110	00011
First Cycle	a)	Shift left A,Q	00001	110_	
	b)	Perform A = A – M (A-Column)	11110	110_	A=A-M=A+M^{2s} A = 00001 M^{2s} = 11101 A = 11110
	c)	Now A is –ve, set q_0 = 0	00001	1100	

			(Q-column) and perform A=A+M (A-Column)			
	Second Cycle	a)	Shift left A,Q	00011	10**0**_	
		b)	Perform A = A – M (A-Column)	00000	10**0**_	A=A-M=A+M^{2s} A = 00011 M^{2s} = 11101 A = 00000
		c)	Now A is +ve, set q_0 = 1 (Q-column)	00000	10**01**	
	Third Cycle	a)	Shift left A,Q	00001	0**01**_	
		b)	Perform A = A – M (A-Column)	11110	0**01**_	A=A-M=A+M^{2s} A = 00001 M^{2s} = 11101 A = 11110
		c)	Now A is –ve, set q_0 = 0 (Q-column) and perform A=A+M (A-Column)	00001	0**010**	
	Fourth Cycle	a)	Shift left A,Q	00010	**010**_	
		b)	Perform A = A – M (A-Column)	11111	**010**_	A=A-M=A+M^{2s} A = 00010 M^{2s} = 11101 A = 11111
		c)	Now A is –ve, set q_0 = 0 (Q-column) and	00010	**0100**	

		perform A=A+M (A-Column)			

So Quotient is the contains of register Q=0100=4

And remainder is the contains of register A=00010=2

Similarly,

Other varieties 14 ÷ 4, 14 ÷ 5, 14 ÷ 6, 14 ÷ 7 can be calculated accordingly bu using restoring method.

……

……

Division operation using Non-Restoring Method (14 ÷ 3 = ?)

Dividend=Q=14=1110, Divisor=M=3=11

As length of dividend is 4 bit, So length of A and M should be (4+1)=5 bits.

So, A=00000 and M=00011 M^{2s}=11101

Steps	Sub-step	Step/Action	Accumulator (A)	Dividend (Q)	Divisor/Remarks (M)
0	0	Initial values	00000	1110	00011
First Cycle	a)	As sign of A is 0, so Shift left A, Q and do	00001	110_	
		Subtract (A=A-M)	11110	110_	A=A-M=A+M^{2s} A = 00001 M^{2s} = 11101 A = 11110
	b)	Set q_0=0 as sign of A is 1	11110	1100	
Second Cycle	a)	As sign of A is 1, so Shift left A, Q and do	11101	100_	
		Add (A=A+M)	00000	100_	A=A+M A = 11101 M = 00011 A = 00000
	b)	Set q_0=1 as sign of A is 0	00000	1001	
Third Cycle	a)	As sign of A is 0,	00001	001_	

		so Shift left A, Q and do			
		Subtract (A=A-M)	11110	0**01**	A=A-M=A+M$_{2s}$ A = 00001 M^{2s} = 11101 A = 11110
	b)	Set q_0=0 as sign of A is 1	11110	0**010**	
Fourth Cycle	a)	As sign of A is 1, so Shift left A, Q and do	11100	**010**	
		Add (A=A+M)	11111	**010**	A=A+M A = 11100 M = 00011 A = 11111
	b)	Set q_0=0 as sign of A is 1	11111	**0100**	

As the sign of A is 1, so do A=A+M=11111+00011=00010=2=Remainder
So Quotient is the contains of register Q=0100=4

Similarly,
Other varieties 14 ÷ 4, 14 ÷ 5, 14 ÷ 6, 14 ÷ 7 can be calculated accordingly bu using non-restoring method.

B. Addition of two numbers represented in IEEE format [4]

Given,
First Number Biased Exponent=E1'=1000 0101$_2$=133 => Real Exponent=E1=133-127=6
Second Number Biased Exponent=E2'=1000 0010$_2$=130 => Real Exponent=E2=130-127=3

First Number=1.0101 x 2^6
Second Number=1.0011 x 2^3 =0.0010011 x 2^6

Add both mantissa

```
  1.0101000
  0.0010011
-------------
  1.0111011
```

So the number after addition is
= 1.0111011 x 2^6
= 1.0111011 x $2^{(6+127)}$ in biased exponent
= 1.0111011 x 2^{133} in biased exponent (decimal)

= $1.0111011 \times 2^{10000101}$ in biased exponent (binary)

The result in IEEE format is

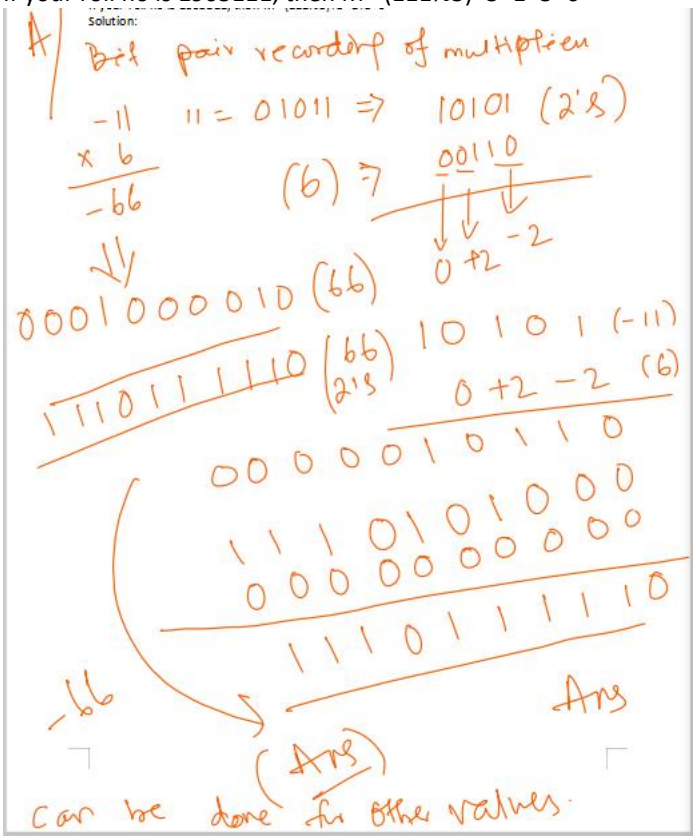
S=0, E'=1000 0101, M=0111011 rest 16 zeros.

Q. No:10- 3rd question [6+6]

A. Multiply (-11 X M) using Bit pair recoding technique.

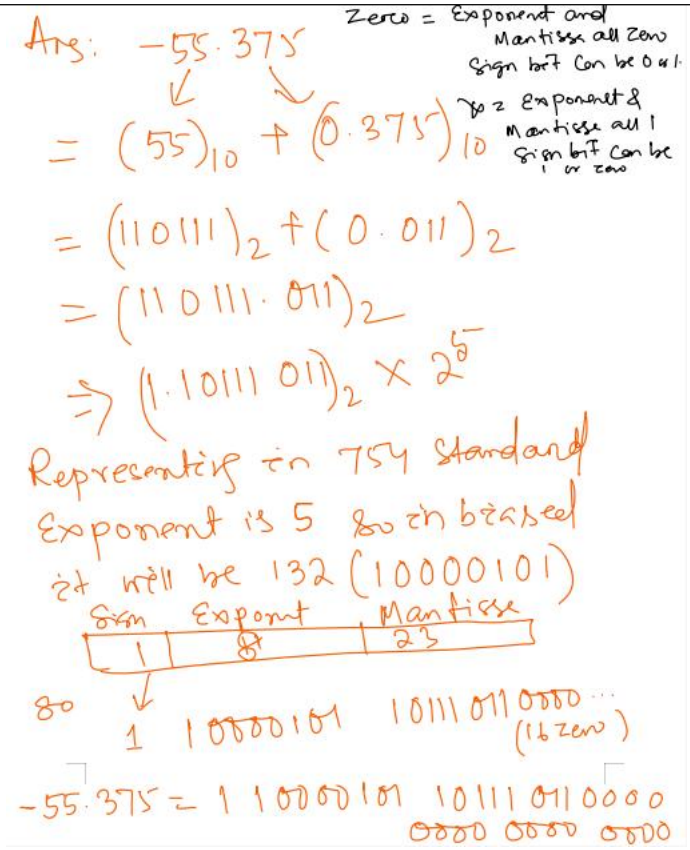
Where M= **(your roll number last 3 digits)% 5 +5.**

If your roll no is 1905111, then M= (111%5)+5=1+5=6



[6]

B. Represent the decimal number -55.375 using IEEE 754 single precision floating point format and double precision format. What is the value of E' and mantissa M to represent the special values 0 and ∞(infinity) in single precision representation?

		[6]
Q.No: 11	**Q.No:11-1st question [4+4+4]** **A.** Explain the disadvantage associated with program-controlled I/O. B. Explain the sequence of events that takes place when an INTR interrupt request (INTR) is received by the processor. C. Explain the registers used in a DMA operation. **A.** Explain the disadvantage associated with program-controlled I/O. Ans: ✓ ties up CPU for long period with no useful work ✓ Unsuitable for high speed data transfer ✓ CPU spends most of its time in a tight loop waiting for the device to become ready(Busy waiting) B. Explain the sequence of events that takes place when an INTR interrupt request (INTR) is received by the processor. Ans: The sequence of events involved in handling an IRQ: ✓ Devices raise an IRQ. ✓ The processor interrupts the program currently being executed. ✓ The device is informed that its request has been recognized and the device deactivates the request signal. ✓ The requested action is performed. ✓ An interrupt is enabled and the interrupted program is	CO6 [4] [4]

resumed.

C. Explain the registers used in a DMA operation.

Ans: The internal registers of a Direct Memory Access (DMA) Controller are:- [4]

1. Base Address Register (16 bit)
2. Base Word Count Register (16 bit)
3. Current Address Register (16 bit)
4. Current Word Count Register (16 bit)
5. Temporary Address Register (16 bit)
6. Temporary Word Count Register (16 bit)
7. Status Register (8 bit)
8. Command Register (8 bit
9. Temporary Register (8 bit)
10. Mode Register (8 bit)
11. Mask Register (4 bit)
12. Request Register (4 bit)

1. **Base Address Register:**
   It is a 16 bit register that stores the initial address from where the data transfer will take place in a DMA Controller. It is used to reload the Current Address Register after every operation.
2. **Base Word Count Register:**
   It is a 16 bit register that stores the number of transfers to be performed during an operation. It is used to reload the Current Word Count Register after every operation.
3. **Current Address Register:**
   It is a 16 bit register that stores the memory address for DMA data transfer. The value automatically increases or decreases after every operation based on how it is programmed. Each channel has its own Current Address Register.
4. **Current Word Count Register:**
   It is a 16 bit register that stores the number of transfers remaining to be performed during an operation. The value automatically decreases after every operation.
5. **Temporary Address Register:**
   It is a 16 bit register that stores the address of data during memory to memory transfer in a DMA Controller.
6. **Temporary Word Count Register:**
   It is a 16 bit register that stores the number of transfers to be performed during a memory to memory transfer in a DMA Controller.
7. **Status Register:**
   It is a 8 bit register that indicates which channel is currently under DMA services or which channels has reached its terminal count. It basically gives the status of the channels. The terminal counts(TC) bits indicates if the channel has reached its terminal count. If terminal count is reached, the transfers are terminated.

8. **Command Register:**
It is a 8 bit register that programs the DMA operation and initializes the channel to be used for data transfer.

9. **Temporary Register:**
It is a 8 bit register that holds data during memory to memory data transfer. It always contain the last byte transferred in previous memory to memory transfer operation

10. **Mode Register:**
It is a 8 bit register that determines the operating mode, i.e., the transfer mode and other transfer parameters, for a channel. Each channel has its own mode register which is selected by bit positions 0 and 1.

11. **Mask Register:**
It is a 4 bit register that is used to mask a channel from requesting the DMA Services. When the mask on a channel is SET, the channel is disabled. It sets or clears all the mask on all the channels with just one command.

12. **Request Register:**
It is a 4 bit register that is used to request DMA data transfer by the software. It determines which channel is requesting for the data transfer.

No:11-2nd question [3+3+6]

A. State how isolated I/O is different from memory mapped I/O.

B. What is the vectored interrupt technique of performing I/O operation?

C. Explain the working principle of Direct Memory Access.

A. State how isolated I/O is different from memory mapped I/O. [3]

In isolated I/O memory and I/O have different address space, but in memory mapped I/O memory and I/O have same address space.
In Isolated I/O Separate instruction control read and write operation in I/O and Memory, but in memory mapped I/O Same instructions can control both I/O and Memory.
Isolated IO is complex due to separate separate logic is used to control both, whereas Memory mapped I/O is simpler logic is used as I/O is also treated as memory only.

Evaluation Scheme- (Three difference contains three marks)

B. What is the vectored interrupt technique of performing I/O operation? [3]

An I/O device requesting an interrupt can identifies itself to the processor by sending a special code to the processor. The special code contains the identification of the device, starting address for the ISR, address of the branch to the ISR. The processor executes the corresponding ISR after receiving the special code. This mechanism is called vectored interrupt.

Evaluation Scheme- (Full marks for correct answer)

C. Explain the working principle of Direct Memory Access.

In DMA approach the I/O module and main memory exchange data directly without the processor involvement. DMA involves an additional module on the system bus i.e. DMA controller, to control the data transfer between i/O module and main memory. The block diagram of DMA controller is shown in fig 7.11.

[6]

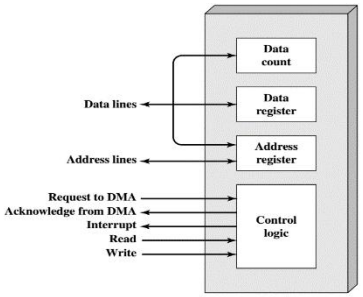


Figure 7.11 Typical DMA Block Diagram

When the processor wishes to read or write a block of data, it issues a command to the DMA controller. The processor sends the read or write request, address of the IO device, the starting memory location and number of words to be read or write. The processor then continue with other work. The MDA controller transfers the entire block of data with out going through the processor. When the transfer is complete, the DMA module sends an interrupt signal to the processor.

Evaluation Scheme- (Marks awarded according to the description)

Q.No:11- 3rd question [4+4+4]

A. What is the need of I/O interface.

B.How does the processor resolve among simultaneous interrupt requests?

C. Distinguish between cycle stealing and burst mode data transfer in DMA.

A. What is the need of I/O interface.

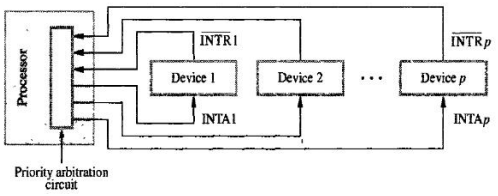
I/O interface co-ordinate the data transfer between the IO devices and system bus. Interface Circuit consists of Address Decoder,Control Circuits,Data registers, Status registers.
Address decoder enables the device to recognize its address when it is available in data line.
The data register holds the data being transfer to or from the processor.
The status register contains the information relevant to the operation of I/O devices.

[4]

B. How does the processor resolve among simultaneous interrupt requests? [4]

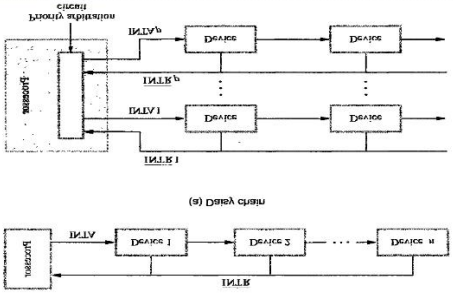
If simultaneous interrupt request arrives to the processor from two or more devices, the processor follows different mechanism to decide which device will service first.

Priority Scheme:
Organizing I/O devices in a prioritized structure. Each of the interrupt-request lines is assigned a
different priority level. The processor is interrupted only by a high priority device.



Daisy-chain:
A widely used scheme is to connect the devices to form a daisy chain, as shown in figure 3a. The interrupt-request line INTR is common to all devices. The interrupt-acknowledge line, INTA, is connected in a daisy-chain fashion, such that the INTA signal propagates serially through the devices. Device that is electrically closest to the processor gets
high priority.

Daisy chain with priority:
The priority and daisy chain schemes may be combined to produce the more general structure in figure 3b. Devices are organized in groups, and each group is connected at a different priority level. Within a group, devices are connected in a daisy chain.



C. Distinguish between cycle stealing and burst mode data transfer in DMA. [4]

Cycle Stealing mode- The DMA module return the system bus to the processor after every data transfer and acquired after every instruction

	cycle. Data transfer rate is slow. CPU utilization is high. Burst mode- The DMA module return the system bus after completion of entire data transfer. Data transfer rate is fast. CPU utilization is low.	