b) With the help of a neat diagram explain the working of Counter type A/D converter circuit and also discuss the drawbacks of this converter in brief. [4

c) Calculate the storage capacity of a certain memory (in MB) if it has 20 address lines, 8 input data lines and 8 output data lines? [2

1MB

8. a) What is Decoder? Explain it with a block diagram and design a **4-16 line decoder using only 2-4 line decoders**. [4

b) Implement the following logic function using a multiplexer having three select lines. [4

$$F(A,B,C,D) = \bar{A}.B + \bar{B}.C + C.\bar{D}$$

c) Find out the resulting output $Q(t)$ of the flip-flop for **next 6 clock pulses** assuming initial condition (Q=1 and $\bar{Q} = 0$) for the following circuit. [2

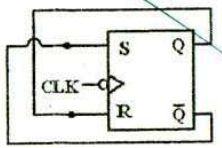

Figure-8(c)

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user ID – gsoutfet@kiit.ac.in
Password – B9V8Q4
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4th Sem (
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SPRING END SEMESTER EXAMINATION-2015

4th Semester B.Tech & B.Tech Dual Degree

DIGITAL ELECTRONIC CIRCUITS (EC-2009)

(Regular-2013 Admitted Batch)

Full Marks: 60 **Time: 3 Hours**

Answer any SIX questions including Question No.1 which is compulsory.

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. a) Define 'Positive Logic system' and 'Negative Logic system' [1 × 10 system.

b) Perform following arithmetic :

(i) BCD subtraction (754 – 567)

(ii) (**-13**) - (**-7**) using 2's complement method.

c) Implement 1-bit Magnitude Comparator using **2:4 decoder** (having active HIGH output lines) and **one OR gate**.

d) What is the difference between SRAM and DRAM?

e) Differentiate between the Synchronous and Asynchronous input terminals of flip-flop, explain with the help of J-K flip-flop.

f) Why Asynchronous counters are slow compared with Synchronous counters? Explain in brief.

g) Draw the state diagram of T flip-flop using Moore model.

h) 'Fan-out of CMOS logic is very high compared with TTL and ECL logic families', Justify.

i) What is the difference between PLA & PAL, explain with suitable examples.

j) For a 4-bit successive approximation analog to digital converter if input analog voltage is 7.5V and clock frequency is 5MHz then calculate its conversion time.

2. a) Design a shift register using D-flip flop, which could be used to design MOD-6 Johnson counter. Explain its operation briefly. [4

b) Obtain the minimized expression for the following 4-varible Boolean expression using K-map method and implement the minimized expression using **NAND gates only**. [4

$$F(P,Q,R,S) = \sum m\,(2, 3, 7, 8, 10, 13) + d(9, 11, 15)$$

c) Draw the circuit diagram of a CMOS Inverter and explain its operation in brief. [2

3. a) Simplify the given logic circuit and implement the simplified expression using **only NOR gates**. [4

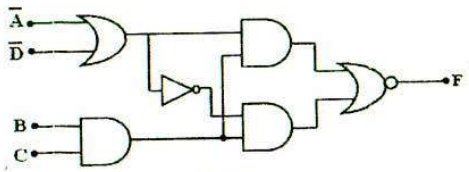

Figure-3(a)

b) Design a Combinational circuit using **only 2-input XOR & OR** gates which takes 4-bit binary data as input and **generates 2's complement of the input data**. [4

c) Define **'Noise-Margin'**. If the noise-margin of 1st logic family is 2.5V and for 2nd it is 1.5V then which one of these logic families is better, explain in brief. [2

4. a) Design a synchronous sequential circuit using T-flip flop which produces an output Z = 1, whenever the following input sequence '0110' occurs. (***Assume overlapping is allowed and use Mealy Model***) [6

b) With the help of a neat diagram, explain the working of a TTL NAND gate with Open-Collector Output and also mention the disadvantages of this configuration. [4

5. a) Using T Flip-Flops design a MOD-6, Asynchronous, Up counter. [4

b) What is Priority Encoder? Design a 4:2 Priority Encoder such that the order of priority of the decimal inputs is given as $D_0 > D_1 > D_2 > D_3$, where all D_i's are inputs to the priority encoder. [4

c) Differentiate between MROM & PROM. [2

6. a) Design a 2-bit Magnitude Comparator using two 1-bit Magnitude Comparator modules and additional basic gates. [4

b) Design a Synchronous counter that goes through states 0, 1, 2, 5, 6, 7, 0, 1… using J-K Flip-Flops. [4

c) For the circuit given, in Figure-6(c), identify the Boolean function **'F'** implemented with the 4x1 MUX and implement the function using minimum number of XOR gates only. [2

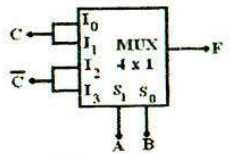

Figure-6(c)

7. a) Design a J-K Flip-Flop using a T Flip-Flop and basic gates. [4