FIFTH SEMESTER EXAMINATION-2012

COMPUTER ORGANIZATION & ARCHITECTURE

[CS 505]

Full Marks: 60 Time: 3 Hours

Answer any SIX questions including Question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. a) The memory unit of a computer has 256K words of 32bits each. The computer has an instruction with four fields: an operation code field, a mode field to specify one of seven addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the number of bits in each field, if an instruction is stored in one memory word. [2 × 10

   b) What is the function of following registers:

   MAR, IR, PC, Y

   c) Differentiate between the *little endian* and the *big endian* address assignment schemes.

   d) Differentiate between DRAM and SRAM.

   e) What is the *vectored interrupt technique* of performing I/O operation?

   f) State how *isolated I/O* is different from *memory mapped I/O*.

g) Explain the importance of *valid bit* associated with cache memory.

h) Represent 9.25 in IEEE single precision format.

i) How many memory references are required for fetching and executing each of the following instructions? [Here the 2nd operand is the destination.]

(a) ADD NUM, R_2 (b) SUB -(R_1), R_2

j) State how *tightly coupled* multiprocessors differ from the *loosely coupled*.

2. Explain, giving examples, different types of instructions depending on [8
(i) the number of operands and (ii) types of operations

3. a) Discuss the concept and utility of the Virtual Memory system. Explain the technique of virtual address to physical address translation with proper block diagram. [4

b) What are the write policies of cache memory? Explain. [4
In a cache organization if the cache memory has an access time of 8nsec and hit rate as 0.98, then find out Average Memory Access time (AMAT) for the whole arrangement. Assume the access time for the main memory is 10msec.

4. a) Explain the 3-bus architecture inside CPU with suitable example. Write the control signals for the following instructions. [4

MUL (R_1),#15 // (R1) ← (R1)*15

b) What is the function of control unit? Explain the following terms related to micro-programmed control unit design: [4

a) Microinstruction b) Micro-program counter
c) Micro routine d) Control Store

5. a) Multiply (15 X –7) using Booth Algorithm. [4

b) State and explain the Flynn's classification of computer with proper diagram. [4

6. a) What is pipeline technique? Why is it used? Give examples of two types of pipelining in a processor. [4

Draw a space-time diagram for a six-segment pipeline to process seven tasks.

b) What is a pipeline hazard? What are the different types of hazards? Explain the data hazard with its remedy. [4

7. a) Explain Program-Controlled I/O technique. Why interrupt driven I/O is more advantageous over it? [4

b) Divide the following using Non-restoring division algorithm. [4

14 ÷ 5

8. Write short notes on any two. [4 × 2

(a) Memory Interleaving
(b) I/O Interface
(c) Associative Memory
(d) Resolving among simultaneous interrupts

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