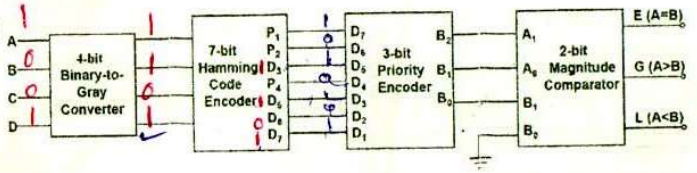
b) With the help of a neat diagram, explain the working of a 4-bit Successive Approximation type ADC with Analog input of 12.6V. Find the digital output. What would be its conversion time if clock frequency is 1 MHz? If the analog input voltage is now increased to 14.8 V, what would be the new conversion time? Explain.

c) A certain memory has a capacity of 64K x 16. [2

(i) How many data input and data output lines does it have?

(ii) How many address lines does it have?

8. a) 

[4

In the figure given above, ABCD=1001 is a 4-bit Binary input data. Find **all three outputs of the 2-bit magnitude comparator**, assuming Odd parity system for Hamming Code Encoder and input line having highest decimal subscript is having the highest priority in the Priority Encoder.

b) Implement the following logic function using an 8:1 MUX. [4

$$F(A,B,C,D) = A\bar{B} + C\bar{D} + A\bar{C}$$

c) Compare N-bit Ring counter, Johnson counter & Ripple counter from modulus and decoding circuit point of view. [2

xxxxx

SPRING END SEMESTER EXAMINATION-2013

4th Semester B.Tech / B.Tech Dual (M.Tech/MBA)

DIGITAL ELECTRONIC CIRCUITS EC-402

[Regular-2011 Admitted Batch & Back]

Full Marks: 60 Time: 3 Hours

Answer any SIX questions including Question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. (a) "Excess-3 codes are non-weighted, sequential & self-complementing." Justify. [1 × 10

(b) Perform the BCD subtraction (476.7 – 297.8).

(c) With the help of a 4:1 MUX, implement a NOT gate.

(d) Show that $AB + \bar{A}C = (A + C)(\bar{A} + B)$ where A, B and C are Boolean variables.

(e) In a T Flip-Flop, the output is initially in SET state. If the input clock frequency is 6.25 MHz, find the frequency of the output waveform when (i) T = 0, (ii) T = 1.

(f) Assume that a 4-bit Ripple counter is holding the count 0110. What will be the count after 31 clock pulses?

(g) Determine the decimal value of the signed binary number '101010' in (i) Sign-Magnitude form (ii) 1's Complement form and (iii) 2's Complement form.

(h) Arrange the following logic families in increasing order of Propagation Delay and Power Dissipation per gate: - TTL, CMOS, ECL.

(i) How many OR gates are there in a 32 x 8 ROM and how many inputs does each OR gate of a 32 x 8 ROM have?

(j) The logic levels used in a 4-bit R-2R ladder DAC are: 1 ≡ 5 V and 0 ≡ 0 V. Find the output voltage for digital input of 1011.

2. a) Design a J-K Flip-Flop using a D Flip-Flop, a 2:1 MUX and a NOT gate. [4

b) Obtain the minimized expression for the following 4-variable Boolean expression using K-map method and implement the minimized expression using NOR gates only. [4

$$F(A,B,C,D) = \sum m(11,12,14) + \sum d(3,4,6)$$

c) Differentiate between PAL & PROM. [2

3. a) Design a 3-bit Even Parity Generator circuit using a Decoder with Active-Low outputs. [4

b) Draw the logic diagram of a 4-bit P-I-S-O Shift Register using J-K Flip-Flops and explain its operation. [4

c) Explain 'High-state Fan-out' and 'High-state Noise Margin' of a logic gate. [2

4. a) Design a synchronous sequential circuit which produces an output Z = 1, whenever the following input sequence '11010' occurs. (*Assume overlapping is allowed and use Mealy Model*) [6

b) With the help of a neat diagram, explain the working of a TTL NAND gate with Open-Collector output and also mention the disadvantages of this configuration. [4

5. a) Design an Asynchronous Mod-5 Up-counter using D Flip-Flops. [4

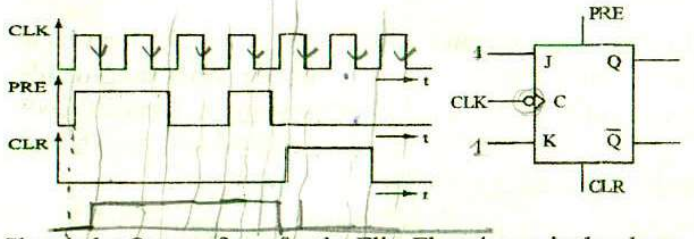
b) Design a 4:2 Priority Encoder such that the order of priority of the decimal inputs is given as $D_2 > D_0 > D_1 > D_3$, where all D_i's are inputs to the priority encoder. [4

c) Draw the circuit diagram of a 2-input CMOS NAND gate. [2

6. a) 'In Astable multivibrator, external trigger input is not required'. Justify. Design an Astable Multivibrator using 555 Timer IC to generate a square wave of 2 KHz frequency with 50 % duty cycle. Given, $R_A = 3\ K\Omega$. [4

b) Design a Synchronous counter that goes through states 0, 5, 3, 2, 6, 0, 5, 3… using S-R Flip-Flops. ***The counter should count only in 3-bit Gray codes.*** [4

c) [2



Sketch the Q waveform for the Flip-Flop shown in the above figure. Assume that Q = 0 initially and the Flip-Flop has *Active-High Asynchronous inputs*.

7. a) Design a Combinational circuit **using 2-input basic gates only** which has three inputs A, B & C and three outputs X, Y & Z. When the decimal equivalent of the binary input is 0, 1, 5 or 3, the decimal equivalent of the binary output is one greater than the input and when decimal equivalent of the binary input is 4, 2, 6 or 7, the decimal equivalent of the binary output is one less than the input. [4