Date 17/08/23

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EXPERIMENT-1

AIM Design and Simulation of boolean functions using Verilog HDL. Hardware implementation of a Boolean function in sum of products and product of sums expressions using Universal gates

COMPONENT / SOFTWARE USED

① ICs - 7400, 7402

② Breadboard, power supply, LED's, Resistors, Switches, Connecting wires

③ Software(s) used - Vivado 2016.1

THEORY

A binary variable may appear either in its normal form (A) or in its complement form ($\bar{A}$). Binary variables combined with an AND operations is called minterms or standard product. Similarly binary variables forming an OR terms called maxterms, or standard sums. For "n" variables with each variable being primed or unprimed, provide "2^n" possible minterms or maxterms.

The eight (2^3) different minterms and maxterms are shown in the table for three (3) variables.

A boolean function can be expressed algebraically from the given truth table by forming a minterm for each combination of the variables that produces a "1" in the boolean function can alternatively be written algebraically by constructing a maxterm for each combination of variables that yeilds a '0' in

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			Minterms		Maxterms	
A	B	C	Term	Designation	Term	Designation
0	0	0	$\bar{A}\bar{B}\bar{C}$	m_0	$A+B+C$	M_0
0	0	1	$\bar{A}\bar{B}C$	m_1	$A+B+\bar{C}$	M_1
0	1	0	$\bar{A}B\bar{C}$	m_2	$A+\bar{B}+C$	M_2
0	1	1	$\bar{A}BC$	m_3	$A+\bar{B}+\bar{C}$	M_3
1	0	0	$A\bar{B}\bar{C}$	m_4	$\bar{A}+B+C$	M_4
1	0	1	$\overline{A\bar{B}C}$	m_5	$\bar{A}+B+\bar{C}$	M_5
1	1	0	$AB\bar{C}$	m_6	$\bar{A}+\bar{B}+C$	M_6
1	1	1	ABC	m_7	$\bar{A}+\bar{B}+\bar{C}$	M_7

Minterms and Maxterms for 3 binary variables

Input			Output
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Truth table of the boolean function

$F(A,B,C) = AB\bar{C} + A\bar{B}C + BC$

the function and then taking the AND of all those terms. Boolean functions expressed as sum of minterms or product of maxterms are said to be in canonical form. The two canonical forms are basic forms of expressing Boolean function which is obtained from reading a given function from the truth table.

Another way to express Boolean functions is in standard forms. In digital logic, the "sum of products" (SOP) and "product of sums" (POS) are two distinct standard forms to describe a Boolean expression. These representations are used to simplify and analyze logic circuits.

Sum of Products (SOP): SOP is a Boolean expression containing AND terms, called product terms, with one or more literals each. The sum denotes the ORing of these terms.

Product of sums (POS): POS is a Boolean expression containing OR terms, called sum terms, with each term having any number of literals. The product denotes the ANDing of these terms.

Consider a Boolean function $F(A,B,C) = AB\bar{C} + A\bar{B}C + BC$ for which the minterms and maxterms can be derived from the truth table shown. The function can be implemented with NAND gates as shown as well as NOR gates by considering POS expression.

NAND or NOR gates are called Universal gates. Digital circuits are frequently constructed with NAND or NOR gates rather than with AND and OR gates.

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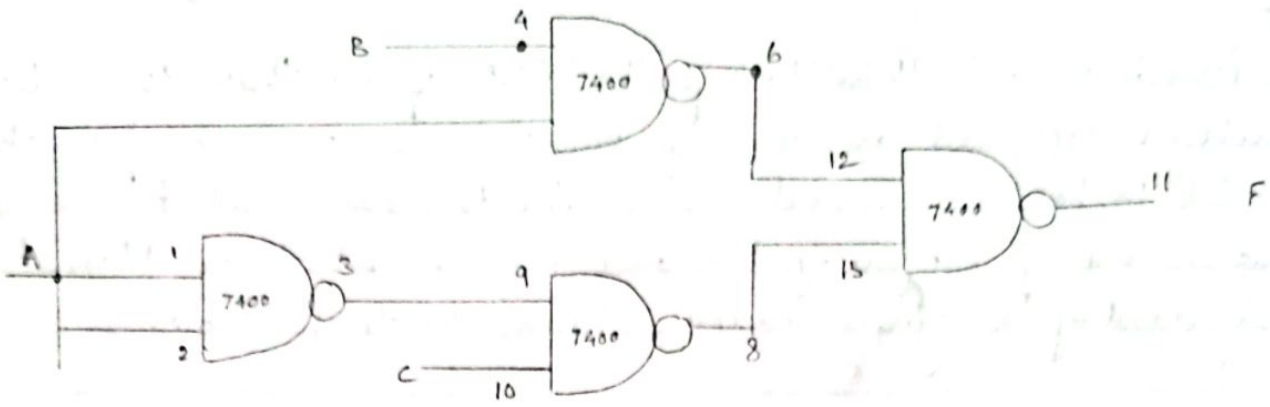

Fig: SOP Implementation of Boolean function using NAND gate

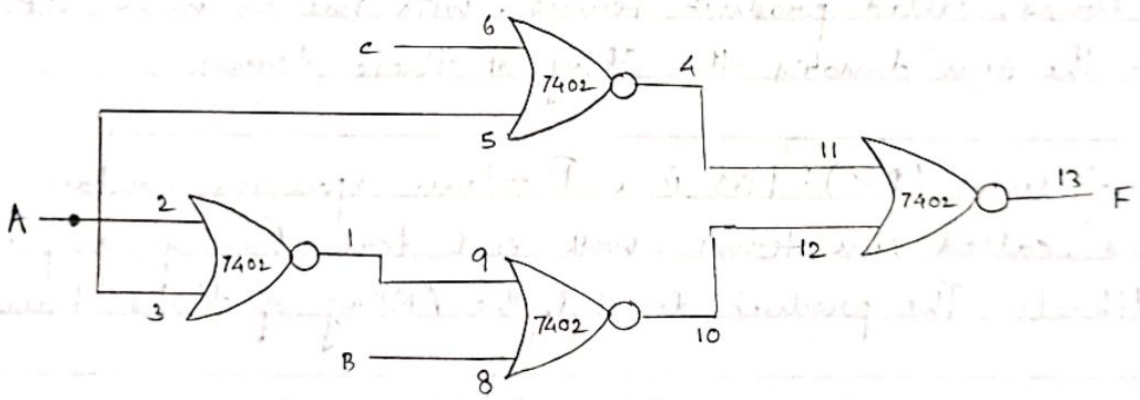

Fig: POS implementation of Boolean function using NOR gate

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SOP: $F(A,B,C) = m_1 + m_3 + m_6 + m_7$

$= \sum (1,3,6,7) = AB + \bar{A}C$

$= \overline{(\overline{AB})(\overline{\bar{A}C})}$

POS: $F(A,B,C) = M_0 M_2 M_4 M_5$

$= \prod (0,2,4,5) = (A+C)(\bar{A}+B)$

$= \overline{(\overline{(A+C)} + \overline{(\bar{A}+B)})}$

PROCEDURE

For software simulation

(a) Create a module with required number of variables and mention its input/output.

(b) Write the description of given Boolean function using operators or by using the built in primitive gates

(c) Synthesize to create RTL schematic

(d) Create another module referred as test bench to verify the functionality and to obtain the waveform of input and output.

(e) Follow the steps required to stimulate the design and compare the obtained output with corresponding truth table.

(f) Take the screenshots of the RTL schematic and

For hardware simulation

(a) Turn off the power of the trainer kit before constructing any circuit.

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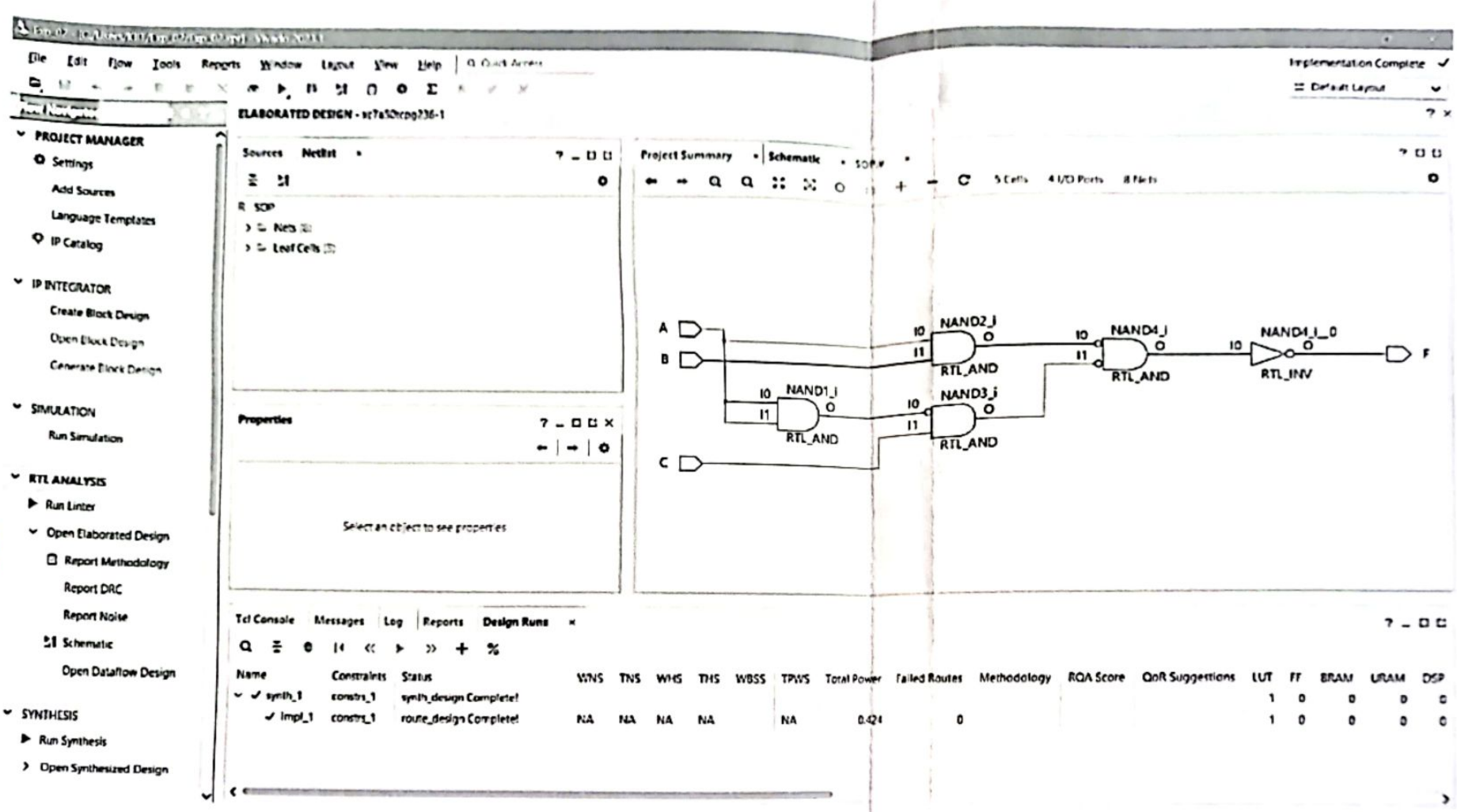

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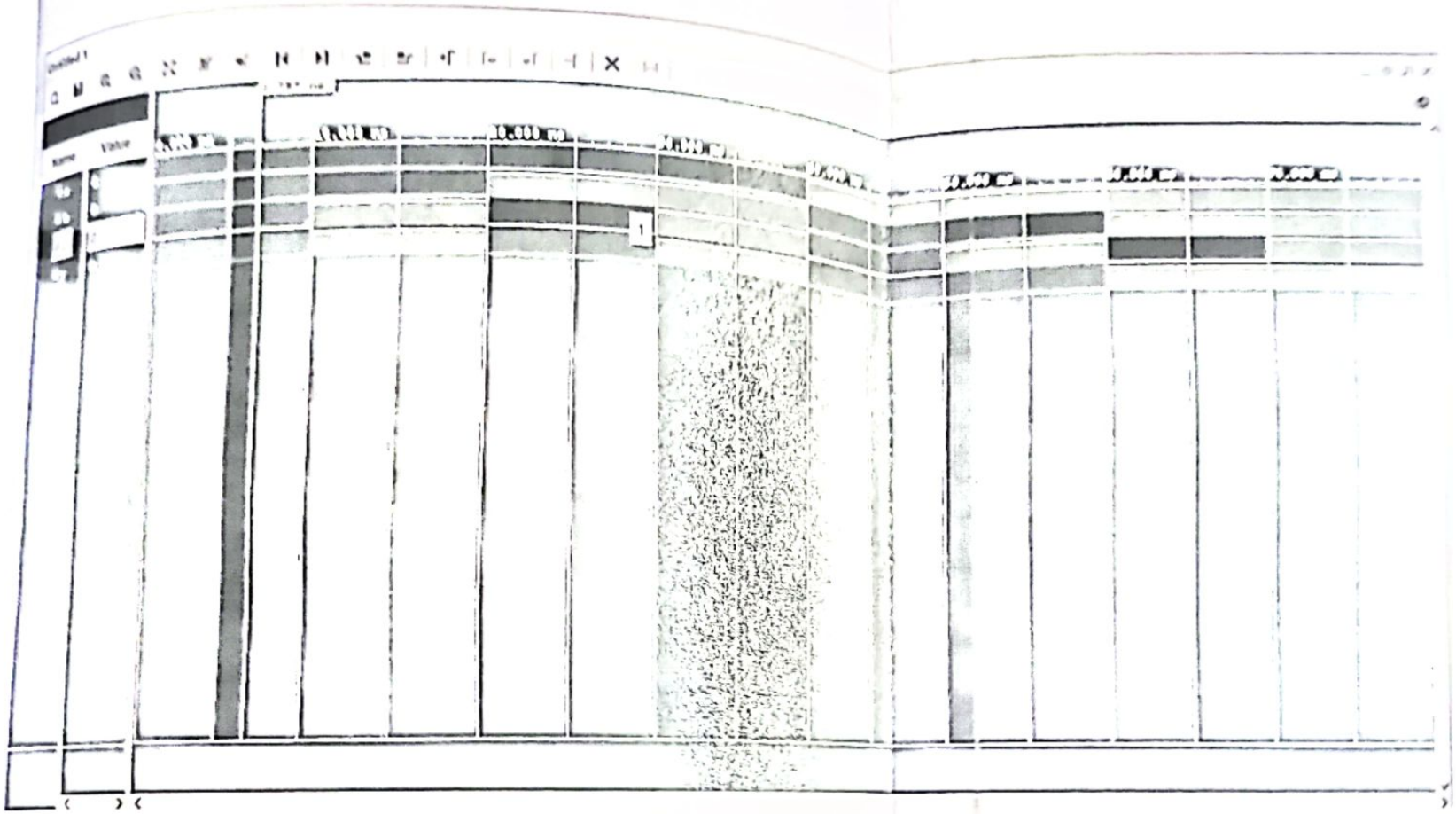

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(b) Connect power supply (+5V DC) pin and ground pin to the respective pins of the trainer kit.
(c) Place the IC's properly on the bread board in the trainer kit.
(d) Connect VCC and GND pins of each chip to the power supply and ground bus strips on the bread board.
(e) Connect the input and output pins of chips to the input switches and output LEDs respectively in the trainer kit.
(f) Check the connections before you turn on the power.
(g) Apply various combinations of inputs according to truth tables and observe outputs of LED's.

HDL Code

- SOP implementation of boolean function using $F(A,B,C) = \sum(1,3,6,7)$ using NAND gates

```
module SOP (output F, input A, input B, input C);
wire w1, w2, w3;
nand NAND1(w1, A, A);
nand NAND2(w2, A, B);
nand NAND3(w3, w1, C);
nand NAND4 (F, w2, w3);
endmodule
```

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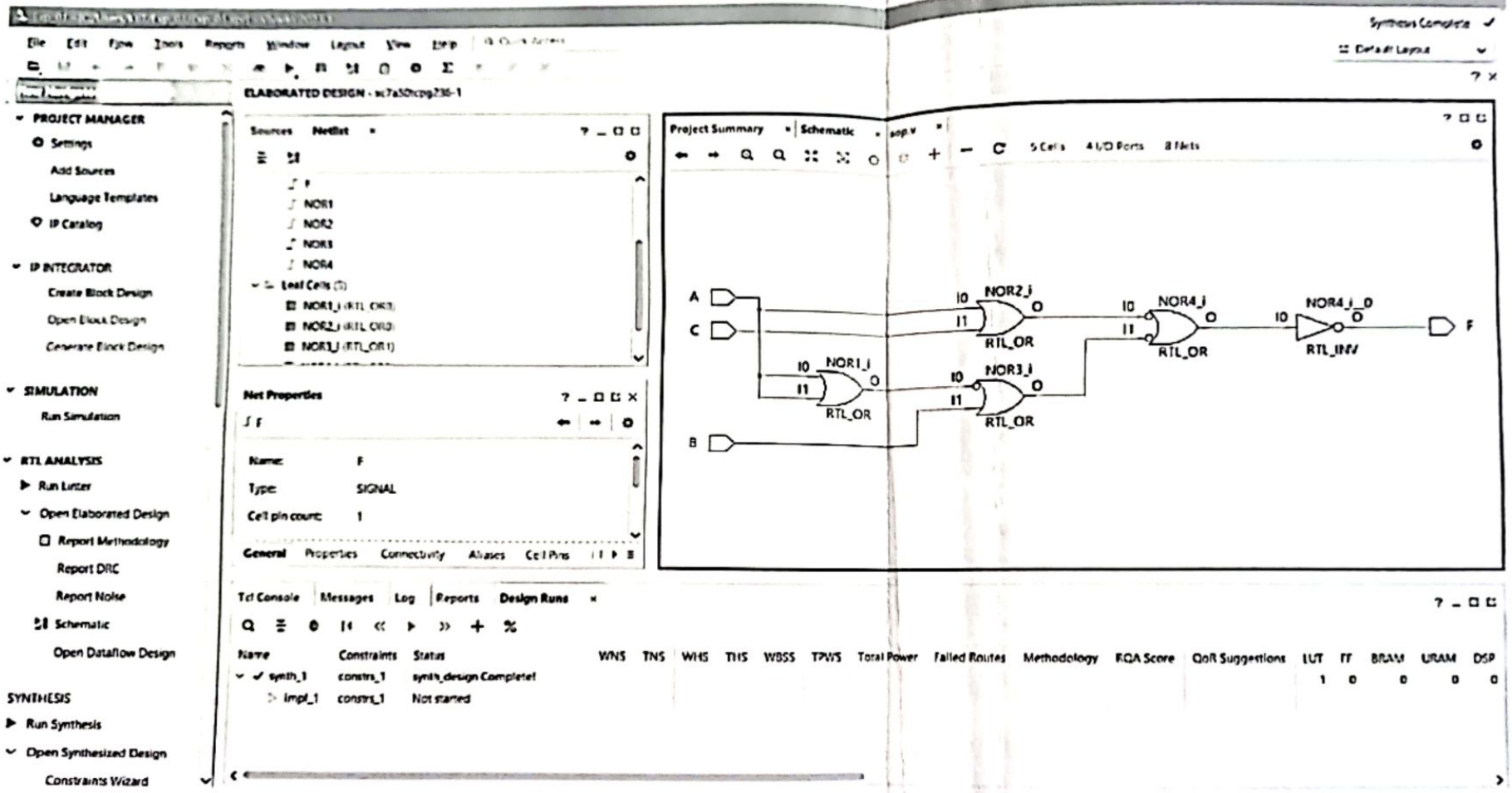

NOR gate and Waveform

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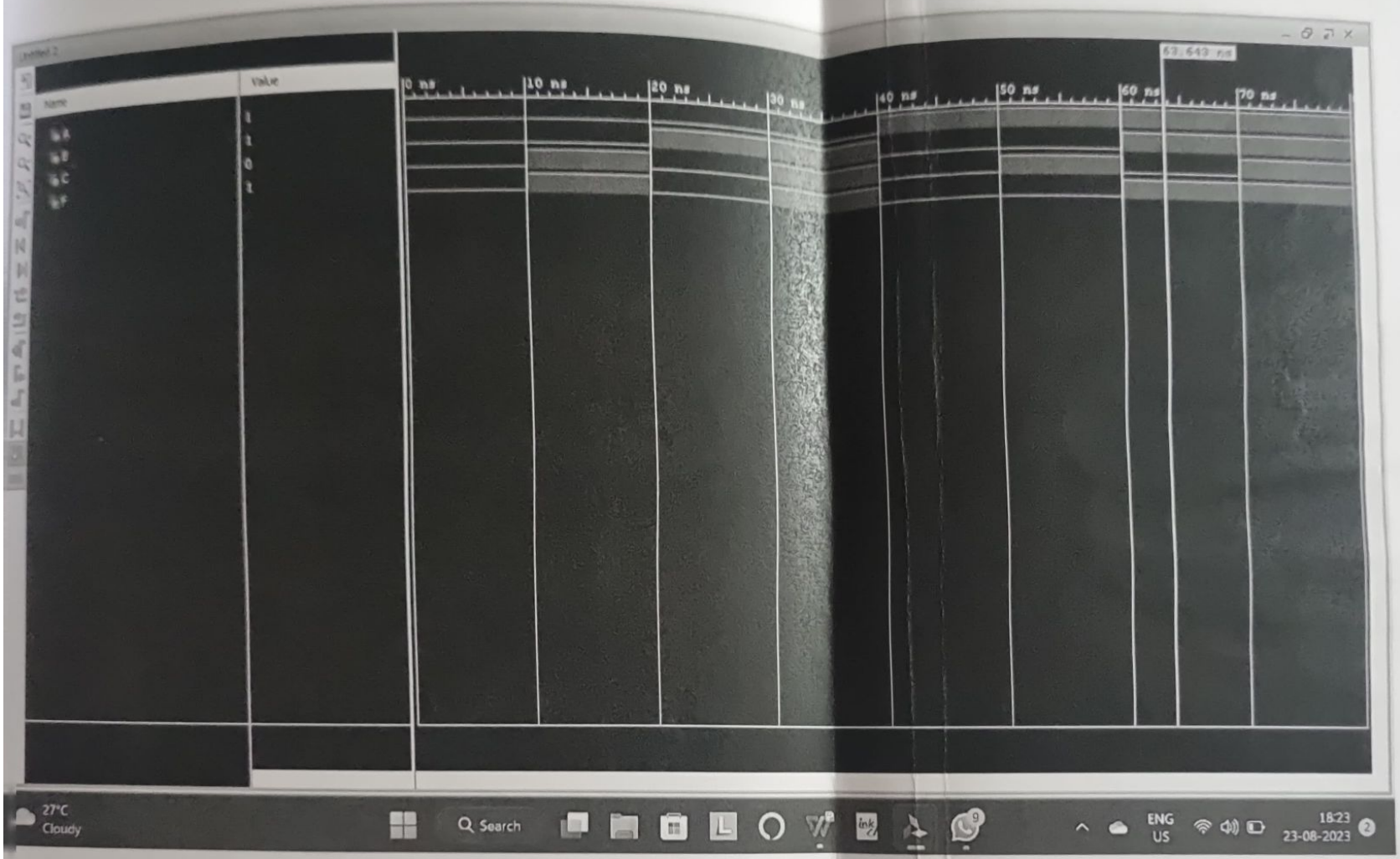

NOR gate and Waveform

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- POS implementation of boolean function using $F(A,B,C) = \prod(0,2,4,5)$ using NOR gates.

```
module POS (output F, input A, input B, input C);
    wire w1, w2, w3;
    nor NOR1 (w1, A, A);
    nor NOR2 (w2, A, C);
    nor NOR3 (w3, w1, B);
    nor NOR4 (F, w2, w3);
endmodule
```

CONCLUSION

Design and simulation of boolean functions using verilog HDL has been done successfully and hardware implementation of boolean functions in sum of products and product of sums using NAND and NOR gates has been done successfully.

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