Qn. Set Code-1

Semester: 4th
Programme: B.Tech
Branch: CSE, IT, CSCE, CSSE, E&CSc

SPRING END SEMESTER EXAMINATION-2023

4th Semester B.Tech

COMPUTER ORGANIZATION AND ARCHITECTURE

CS2006

(For 2022 (L.E), 2021 & Previous Admitted Batches)

Time: 3 Hours | Full Marks: 50

Answer any SIX questions.
Question paper consists of four SECTIONS i.e. A, B, C and D.
Section A is compulsory.
Attempt minimum one question each from Sections B, C, D.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

SECTION-A

1. Answer the following questions. [1 × 10]

(a) Consider a register R1 contains a value 10111000 and R2 contains 10110010. What will be the value of carry , zero and overflow flags after the execution of the instruction

ADD R1, R2 // R2 is the destination

(b) A processor has 48 distinct instructions and 28 general purpose registers. A 32-bit instruction word has an opcode, two register operands and an immediate operand. Assuming that the immediate operand is an signed integer, what is the maximum value of the immediate operand?

(c) What is the use of Y and Z register in single bus CPU organization?

(d) A RAM chip has 8 address lines, 8 data lines and 2 chip select lines. What will be the total number of memory locations?

(e) Explain the role of dirty bit in write-back cache protocol.

(f) There are p input lines q output lines for a decoder that is used to uniquely address a byte addressable 2KB RAM. What is the minimum value of p+q?

(g) The interleaved memory system is divided into 8 number of memory modules. Each module consists of 64 words. The consecutive words are located in consecutive modules. Give the layout of memory address showing the address in module and the module fields.

(h) Represent $-(200)_{10}$ into IEEE-754 single precision floating point format.

(i) Perform 2 times arithmetic shift right operation on : 10101

(j) What is vectored interrupt technique?

SECTION-B

2. (a) Write the assembly code to evaluate the following arithmetic expression: [4]

$$Z = (P - Q + R) * (S / T * U) / V$$

i) Using an accumulator type computer with one address instructions.

ii) Using a stack organized computer with zero-address operation instructions.

iii) Using RISC computer instruction format.

(b) Explain the following addressing modes with examples: [4]

i. Relative mode ii. Immediate mode

iii. Memory indirect mode iv. Autoincrement mode.

3. (a) Write the sequence of control steps for the following instructions for **multi bus** CPU organization [4]

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AND  R2, (R1)     // R2←[R1]+R2
MUL R1, NUM       //R1 the destination
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(b) Explain the following instructions with example: [4]

i. LOAD ii. EI iii. Compare iv. CALL

Explain the working principle of Hardwired control unit design along with neat diagram.

SECTION-C

4. (a) A processor has 32 integer registers and 16 floating point registers. It uses 16-bit instruction format. It has two types of instructions: Type-I and Type-II. Each Type-I instruction contains an opcode, an integer register and a 4-bit immediate value. Each Type-II instruction contains an opcode and two floating point register and one integer register. If there are 48 distinct Type-I opcodes, then what is the maximum number of distinct Type-II opcodes possible? [4]

(b) Write the micro routine for the following instruction. Assume second operand is the destination. (Using Single bus architecture) [4]

I. ADD 50(R1), R2

II. MUL (R3)+, R4

5. (a) Assume a program consists of 64 pages and a computer has 32 frames in memory. A page consists of 4K words and memory is word addressable. Currently, page 0 is in frame 20, page 6 is in frame 12, page 7 is in frame 31 and page 9 is in frame 28. No other pages are in memory, i.e., only page number 0, 6, 7 and 9 are there in the memory. Translate the following logical addresses into the physical addresses. [4]

I. 00 1001 0100 1111 0000

II. 00 0110 0010 0011 0100

(b) A computer uses RAM chips of 128 X 4 capacity. Design a memory capacity of 1K X 16 by using available chips. [4]

6. (a) A computer system uses 16-bit memory addresses. It has a 4K-byte cache organized in a 2-way set associative manner with 32 bytes per cache block. Assume that the size of each memory word is 1 byte. [4]

(I) Calculate the number of bits in each of the Tag, set, and word fields of the memory address.

(II) When a program is executed, the processor reads data sequentially from the following word addresses:

256, 270, 4352, 4365, 256, 4352

All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.

(b) Consider a 4-way set associative mapped cache of size 1MB with block size 1 KB. There are 9 bits in the tag. Find the size of main memory and the size of the tag directory. [4]

What is the importance of valid bit with respect to cache coherence problem?

SECTION-D

7. (a) Perform the following division operation using non-restoring method. 14 ÷ 5. [4]

(b) Multiply (-13) X 12 using Booth's algorithm. [4]

8. (a) Explain the working principle of I/O transfer method that facilitates transfer of bulk data from hard disk to main memory with the highest throughput? [4]

(b) State how isolated I/O is different from memory mapped I/O. Explain nesting of interrupt requests. [4]

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