Semester: 6th
Subject Name:- ...CO...& Code:- CS 3042.....
Branch (s): - CE,ME,EEE,EE

# SPRING MID SEMESTER EXAMINATION-2023

School of Computer Engineering
Kalinga Institute of Industrial Technology, Deemed to be University
Computer Organization
[CS 3042]

**Time: 1 1/2 Hours** **Full Mark: 20**

***Answer any four Questions including Q.No.1 which is Compulsory.***
***The figures in the margin indicate full marks. Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.***

1. Answer all the questions. [ 1 x 5 ]

a) State the difference between Von Neumann Concept and Harvard concept.
b)A 5 Hz machine runs a benchmark program that contains 1000 machine instruction. If each instruction takes 5 cycles (steps) for completion then find out the CPU time to complete the program.

c) Consider a 1 MB (Mega byte) byte addressable memory system, with word size of 64 bits. What is the number of bits in MAR and MDR?

d) Differentiate between byte addressable and word addressable memory.

e) Registers R1 and R2 contain data values 1800 and 3800 respectively in decimal, and the word length of the processor is 4 bytes. What is the effective address of the memory operand for the instruction?
ADD 100 (R2), R6.

2. Difference between computer architecture verses computer organization and describe about the function of different type of register. [ 5 Marks ]

3. .Represent the decimal values 5, −2, 14, −10, , as signed, 7-bit numbers in the following binary formats:

(a) Sign-and-magnitude
(b) 1's-complement [ 5 Marks ]

4. Differentiate between the little endian and the big endian address assignment schemes. Consider a computer that has a byte-addressable memory organized in 32-bit words according to the big-endian scheme. A program reads ASCII characters entered at a keyboard and stores them in successive byte locations, starting at location 1000. Show the contents of the two memory words at locations 1000 and 1004 after the name "Johnson" has been entered. Repeat Problem using little-endian scheme. [ 5 Marks ]

5. What do you mean by

Immediate addressing mode,Direct addressing mode,Register Indirect addressing mode, Memory Indirect addressing mode, Relative addressing mode, Index (R1 as index register) addressing mode. Evaluate the effective address for above addressing modes If an instruction is stored at location 300 with its address field at location 301. The address field has value 500. A processor register R1 contains the number 100. [ 5 Marks ]

*** Best of Luck ***