SPRING MAKEUP MID SEMESTER EXAMINATION-2023

School of Computer Engineering
Kalinga Institute of Industrial Technology, Deemed to be University
Computer Architecture
[CS 2006]

Time: 1 1/2 Hours **Full Mark: 20**

All Questions are compulsory.
The figures in the margin indicate full marks. Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. Answer all the questions. [1 x 5]

a) A Computer has 65 instructions. For executing each instruction maximum control steps required are 20. What will be the specification of instruction and step counter decoder used in hardwired control unit design?

Solution Scheme:
Instruction decoder: 7:128 (0.5 marks)
Step counter decoder: 5:32 (0.5 marks)

b) Write the assembly language code segment to evaluate the arithmetic expression: X=A-B*C, using stack based organization.

Solution Scheme: (1 Mark)
PUSH A
PUSH B
PUSH C
MUL
SUB
POP X

c) Why Y and Z registers are used in the single bus CPU organization?

Solution Scheme: Y and Z is used to hold the temporary result of ALU in single bus CPU organization. (1 mark)

d) Why Microprogram control unit is more flexible than Hardwired control unit?

Solution Scheme: If any changes is needed because of error then the modification is easy in program, however difficulty in Hardwire.

e) There are two 8-bit registers: initially R1= -120, R2= -10. Find the values of Carry and Overflow flags after executing the instruction: ADD R1, R2.

Solution Scheme:
-120 is in binary: 10001000
-10 is in binary: 11110110
Sum:101111110 (result is 9 bit)
Overflow is set 1 (0.5 mark)
Carry flag is set 1 (0.5 mark)

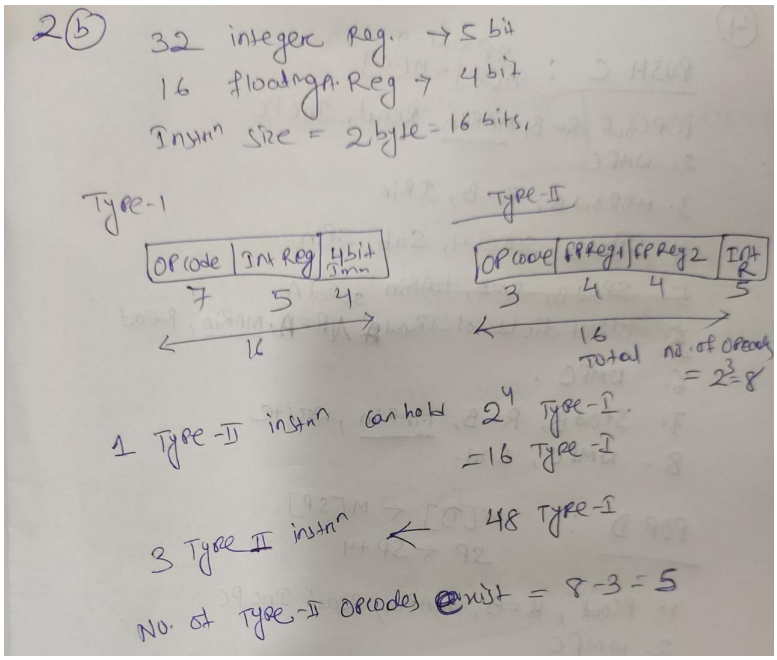
2. Long Answer Type Question [5 Marks]

a) Draw and explain single bus CPU organization in brief. Why Constant 4 is used in single bus CPU organization? [2 Marks]

Solution Scheme: Draw and explain single bus CPU organization in brief. (1.5 mark)
Why Constant 4 is used in single bus CPU organization? (0.5 mark)

b) A processor has 32 integer registers and and 16 floating point registers. It uses 2-byte instruction format. It has two types of instructions: Type-I and Type-II. Each Type-I instruction contains an opcode, an integer register name, and a 4-bit immediate value. Each Type-II instruction contains an opcode, 2 floating point register and one integer register names. If there are 48 distinct Type-I opcodes, then what is the maximum number of distinct Type-II opcodes is possible ? [3 Marks]

Solution Scheme:



3. Long Answer Type Question [5 Marks]

a) Discuss the difference between Von Neumann and Harvard Architecture. [2 Marks]

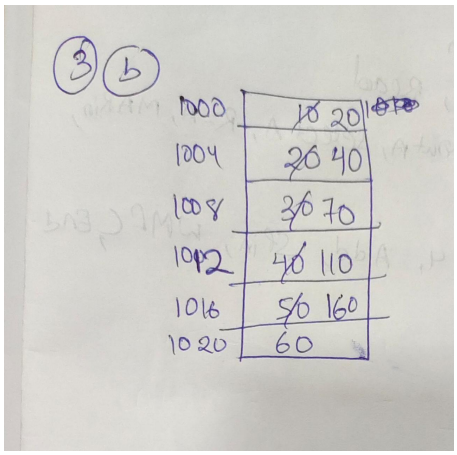
Solution Scheme: Discuss the difference between Von Neumann and Harvard Architecture [2 marks]

b) Assume machine is byte addressable and 1word=32bits. 2nd Operand is the destination operand. Initial content of memory address is given in Table. What will the final content of memory address given in Table, after execution of the following program. [3 Marks]

Address	Content
1000	10
1004	20
1008	30
1012	40
1016	50
1020	60

```
        MOV #5, R0
        MOV #1000, R1
        MOV #10, R2
LOOP:   ADD R2, (R1)
        MOV (R1)+, R2
        DEC R0
        BRANCH  >0 LOOP
```

Solution Scheme:



4. Long Answer Type Question [5 Marks]

Write the control signals for the following instructions using three bus CPU organization. Assume machine is byte addressable and 1 word=32bits.

I1: PUSH C //C is a memory location

I2: POP D //D is a memory location

Design the logic function and circuit diagram for MARin and END control signals.

Solution Scheme:

(4) I_1: PUSH C : $SP \leftarrow SP-4$
$M[SP] \leftarrow M[C]$

1. PC_{out}, R=B, MARin, Read, IncPC
2. WMFC
3. $MDR_{out}B$, R=B, IRin

0.5 marks

4. $SP_{out}B$, Select 4, Sub, SPin
5. offset-field-of-$IR_{out}A$, Select A, R=A, MARin, Read
6. WMFC
7. $SP_{out}B$, R=B, MARin, Write
8. WMFC, End

1 Mark

I_2: POP D : $M[D] \leftarrow M[SP]$
$SP \leftarrow SP+4$

1. PC_{out}, R=B, MARin, Read, IncPC
2. WMFC
3. $MDR_{out}B$, R=B, IRin

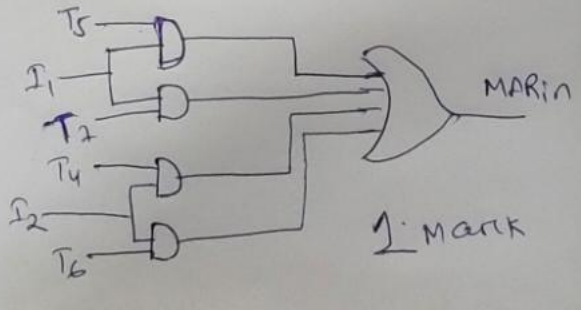
0.5 Mark

4. $SP_{out}B$, R=B, MARin, Read
5. WMFC
6. offset-field-of-$IR_{out}A$, Select A, R=A, MARin, Write
7. $SP_{out}B$, Select 4, Add, SPin, WMFC, End.

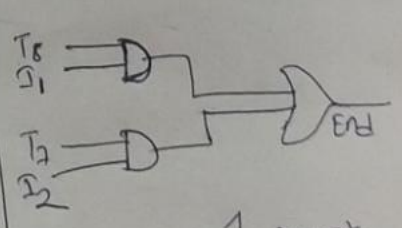
1 Mark

$MARin = T_1 + T_5 \cdot I_1 + T_7 \cdot I_1 + T_4 \cdot I_2 \cdot T_6 \cdot I_2$

$End = T_8 \cdot I_1 + T_7 \cdot I_2$



1 Mark



1 Mark

*** Best of Luck ***