SPRING END SEMESTER EXAMINATION-2014

4th Semester B.Tech/B.Tech Dual

DIGITAL ELECTRONIC CIRCUITS EC-402

(Regular-2012 & Back-2011, 10, 09 Admitted Batch)

Full Marks: 60 **Time: 3 Hours**

Answer any SIX questions including Question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. a) Define 'Positive logic system' and 'Negative logic system'. [1 × 10

   b) Perform following arithmetic :

   (i) BCD addition (854 + 795)

   (ii) **(–15) – (–5)** using 2's complement method.

   c) Implement Half-Adder using **2:4 decoder** (having active HIGH output lines) and one **OR gate**.

   d) What is the difference between SRAM and DRAM?

   e) Differentiate synchronous and asynchronous input terminals of flip-flop, explain with the help of J-K flip-flop.

   f) Find the minimum number of flip-flops required to design a counter which counts in **prime numbers** (2, 3, 5…N, 2, 3….), where N < 50.

   g) Why the row and column values of the K- map are ordered in Gray code rather than binary numerical order, explain in brief.

   h) Define :

   (i) Noise Margin (ii) fan-out

i) What is the difference between PLA & PAL explain with suitable examples?

j) Define the 'Resolution' of a digital to analog converter and calculate the resolution (in %) of a 8-bit digital to analog converter.

2. a) Design a T- Flip-Flop using a D Flip-Flop and a multiplexer having one select line. [4

b) Obtain the minimized expression for the following 4-variable Boolean expression using K-map method and implement the minimized expression using NOR gates only. [4

$$\mathbf{F(P,Q,R,S) = \Pi M\ (1,4,7,8,13,14)\ .d\ (3,5,10,12)}$$

c) Differentiate between PROM & EEPROM. [2

3. a) In the Figure-3(a) X, Y and Z are **7-bit Hamming codes**. A, B and C are **4-bit data** where **X: 1010011** and **Y: 1100101** [4

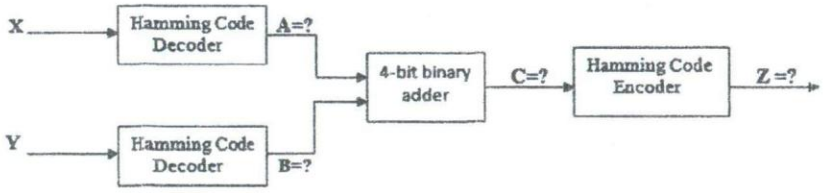

Figure-3(a)

Find **A, B, C** and **Z**.

[Assume (i) even parity system (ii) at most single bit error may take place.]

b) Design a shift register using D-flip flop which takes 4 clock cycles for loading the data and 3 clock cycles for outputting it. Explain its operation briefly. [4

c) Define '**Speed power product**'. If the speed power product of 1st logic family is 40pJ and for 2nd it is 70pJ then which one of these logic families is better, explain in brief. [2

4. a) Design a synchronous sequential circuit using T-flip flop which produces an output Z = 1, whenever the following input sequence '0110' occurs. (***Assume overlapping is allowed and use Mealy Model***) [6

   b) With the help of a neat diagram, explain the working of a TTL NAND gate with Totem-Pole Output and also mention the advantages of this configuration over Open-Collector Output. [4

5. a) Using D Flip-Flops design an Asynchronous counter which generates the output waveform with frequency 1 MHz if the input clock frequency is 5 MHz (*Hint: Use the concept of frequency division by counter*). [4

   b) What is Priority Encoder? Design a 4:2 Priority Encoder such that the order of priority of the decimal inputs is given as $\mathbf{D_1 > D_0 > D_3 > D_2}$, where all $\mathbf{D_i}$**'s** are inputs to the priority encoder. [4

   c) Draw the circuit diagram of a 2-input CMOS NOR gate. [2

6. a) Compare Monostable multivibrator and Astable multivibrator from the external trigger input requirement point of view and calculate the frequency and duty cycle of the 555 astable multivibrator output if $\mathbf{C = 0.02\,\mu F}$, $\mathbf{R_A = 20k\,\Omega}$ **and** $\mathbf{R_B = 40k\,\Omega}$. [4

   b) Design a Synchronous counter that goes through states 0, 1, 3, 2, 4, 5, 0, 1… using J-K Flip-Flops. [4

   c) For the circuit given in Figure-6(c), identify the Boolean function **'F'** implemented with the 4x1 MUX, [2

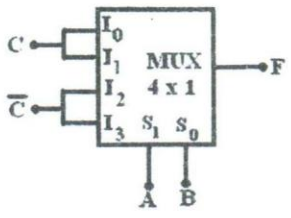

Figure-6(c)

7. a) Realize full subtractor circuit using a multiplexer having 2 select lines. [4

b) With the help of a neat diagram, explain the working of a 3-bit Flash type analog to digital converter and compare the conversion time of Counter type, Succesive Approximation type and Flash type analog to digital converter. [4

c) Calculate the storage capacity of a certain memory (in KB) if it has 18 address lines, 16 input data lines and 16 output data lines? [2

8. a) Design 4-bit combined adder/subtractor circuit using **full adders & XNOR gates only** and explain the working in brief. [4

b) In a room there are three electric lamps. For sufficient light intensity, at least two lamps must be ON at the same time. Design a circuit using a multiplexer having two select lines which enables an alarm when light intensity in the room is not sufficient. [4

c) For the circuit given, in Figure-8(c) calculate the time period of output (Q) waveform if clock signal frequency is 2 MHz.(Assume initially Q = 0) [2

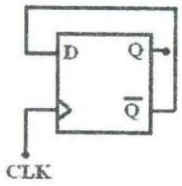

Figure-8(c)

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