Mid-Semester Examination
School of Computer Engineering
KIIT University, Bhubaneswar-24

Time: 2Hrs. FullMark:40

(Answer any 4 **questions** including **question no.1**)

(Instruction format: Opcode src2, src1/dest)

[2X5=10]

Q1 .(a) A general purpose register organization computer has a 16 bit instruction consisting of opcode, source register and a destination register. It supports 7 no of arithmetic operations and 6 no of logical operations. Find the total number of maximum registers present in the system.

(b)

i. A processor is connected to a 128G X 32 memory module. What is the width of its MAR and MDR register ?

ii. An instruction takes 9 clock cycles to execute it on a 1.5GHz processor. How much time is taken by that instruction to complete its execution?

(c) Both of the following statements cause the value 150 to be stored in location 2000.

```
ORIGIN 2000
DATAWORD 150
```

And

```
Move #150, 2000
```

Explain the difference.

(d) How many memory references are required for fetching and executing the following instructions:

i. MUL #100, 80(R_1)

ii. ADD (R_2)+,R_1

(e) The content of a register R_1 is 10001010.What will be the decimal value in R_1 after the execution of

ASHR #1,R_1

[Assume the numbers are represented in 2's complement form]

2 (a) Write the equivalent instructions for Zero Address Organization and One Address Organization of the following instructions: [5]

MOV P, R_1

SUB Q, R_1

DIV R, R_1
MUL S, R_1
MOV R_1, X

(b) Register R_1 and R_2 of a computer contain the decimal value 1540 and 1290. What is the effective address of the memory operand in each of the following instructions? [1X5=5]

i. LOAD $18(R_1),R_5$
ii. STORE $R_5,25(R_1,R_2)$
iii. ADD $-(R_1),R_3$
iv. SUB $(R_2)+,R_5$
v. MOV #1235,R_3

3. (a) The content of the top of memory stack is 2452.The content of SP is 1258. A two byte call subroutine instruction is located in memory address 1456 followed by address field of 5490 at location 1457.What are the content of PC, SP and top of stack. i) Before Call instruction execution, ii) After Call instruction execution, iii) After Return from subroutine. [5]
(b) Explain the working of hardwired control unit with a block diagram. [5]

4. (a) Draw and explain the single-bus CPU organization. [5]
(b) Write the micro routine for the following instruction: [5]
ADD (R1)+, R2

5. (a) Draw and explain the 3-bus CPU organization. Write the sequence of control signals to execute the following instruction using the same organization. [5]
ADD (R5), R1, R2
(b) Write short notes on: [2½ x 2=5]
i. Condition Codes.
ii. Von-Neumann Vs. Harvard Architecture.