KIIT, Deemed to be University
School of Electronics Engineering
Digital System Design Laboratory [EC 29005]

EXPERIMENT - 7

Aim:

Design and simulation of a pseudo random sequence generator in Verilog.

Implementation of pseudo random sequence generator using shift register.

Component/Software Used:

Component/Software	Specification
ICs	7495,7486
Bread Board, Power supply, LEDs, Resistors,Switches, Connecting wires	As per requirement
Software(s) Used	Vivado 2016.1

Theory:

A register is a device capable of storing a number of bits. We know that a flip-flop has a memory element. Thus, flip-flop can be connected together to form a register. A register capable of shifting the binary information held in each cell to its neighboring cell, in a selected direction is called a shift register.

Shift registers are synchronous sequential circuits consists of a group of flip-flops connected so that each flip-flop transfers its bit of data to the next flip-flop of the register when a clock pulse arrives. Data may have to be shifted left or shifted right. We have shifted left and shifted right registers.

An n - bit register consists of a group of n flip-flops capable of storing n bits of binary information. In addition to the flip-flops, a register may have combinational gates that perform certain data-processing tasks. The flip-flops hold the binary information. and the gates determine how the information is transferred into the register.

Serial in - Serial out:

The data is loaded into and read from the shift register serially. Fig.7.1 shows the circuit of a 4-bit serial in-serial out (SISO) shifts right register using four D flip-flops. The Q outputs of one state (FF) are connected to the D input of the next state(FF). Thus, the inputs to second, third and fourth flip-flop are conditioned by their preceding flip-flops. The data in each flip-flop is shifted to the next flip-flop on the arrival of a positive edge of clock pulse. Since it is a 4 bit register, 4 clock pulses are required to shift the data through this register.

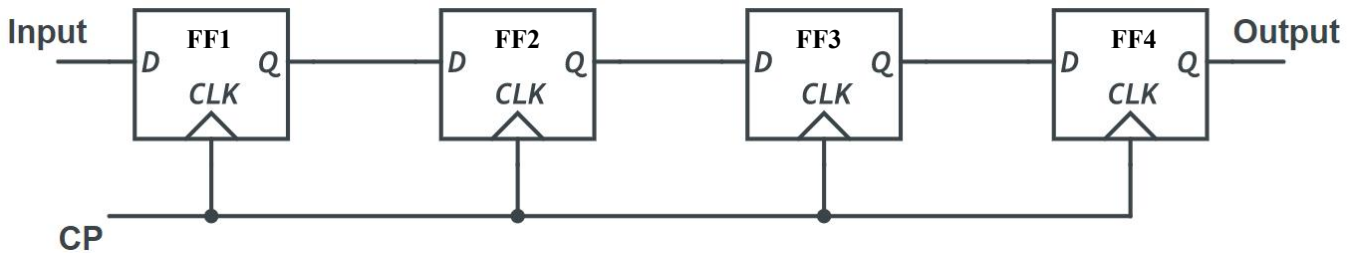


Figure 7.1: Logic diagram of 4 bit serial-in serial-out shift register

The data shifting in the 4-bit SISO is summarized below in the Table.7.1 with an example of 4 bit data "1110". Load the shift register with a 4-bit data '$B_3B_2B_1B_0$'one by one serially. In the 1st clock pulse, B_0 is shifted to Q_1 (FF1). In the 2nd clock pulse,B_0 is shifted to Q_2 (FF2) and B_1 is shifted to Q_1(FF1). In the 3rd clock pulse,B_0 is shifted to Q_3(FF3), B_1 is shifted to Q_2(FF2) and B_3 is shifted to Q_1(FF1). At the end of 4th clock pulse, $B_0$is shifted to Q_4(FF4), B_1 is shifted to Q_3(FF3), B_2 is shifted to Q_2 (FF2) and B_3 is shifted to Q_1(FF1). In the next clock pulse, the second data 'B_1'will appear at Q_4 (FF4). In the next clock pulse, the third data 'B_3' will appear at Q_4 (FF4).Application of next clock pulse will enable the 4th data 'B_3' to appear at Q_4(FF4).Thus the data applied serially at the input comes out serially at Q_4(FF4).

Clock	Serial I/P	Q_1	Q_2	Q_3	Q_4
1	$B_0 = 0$	0	X	X	X
2	$B_1 = 1$	1	0	X	X
3	$B_2 = 1$	1	1	0	X
4	$B_3 = 1$	1	1	1	0
5	X	X	1	1	1
6	X	X	X	1	1
7	X	X	X	X	1

Table 7.1: Truth table of 4-bit SISO shift register

Parallel in-Parallel out:

The data is loaded in parallel and read from the register in parallel, i.e., all bits are loaded simultaneously and read simultaneously. Figure 7.2 shows the circuit of a 4-bit parallel in-parallel out (PIPO) shifts right register using four D flip-flops. The data in each flip-flop is shifted to the output the arrival of a positive edge of clock pulse. Output terminals and data are available at all of them together. The parallel data bits are $B_0B_1B_2B_3$ and Q1, Q2, Q3, and Q4 are parallel data outputs. After one clock pulse, all the input data is available in the outputs.

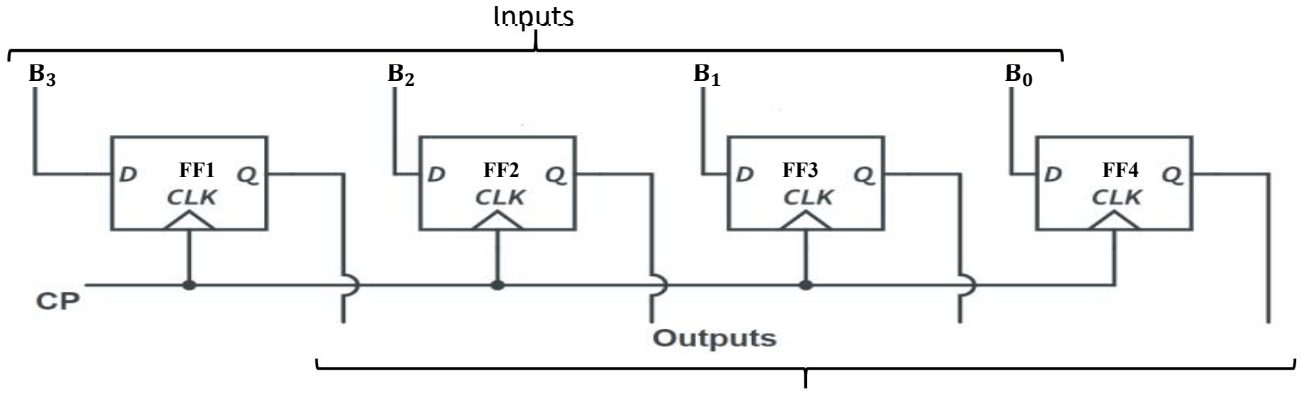


Figure 7.2: Logic diagram of PIPO shift register

Serial in-Parallel out: The data is loaded into the register serially but read in parallel mode, i.e., data is available from all flip-flops simultaneously. Figure 7.3 shows the circuit of a 4-bit serial in-parallel out (SIPO) shifts right register using four D flip-flops. The Q outputs of one state are connected to the D input of the next state. Thus, the inputs to second, to the third and fourth flip-flop are conditioned by their preceding flip-flops. The data in each flip-flop is shifted to the next flip-flop on the arrival of a positive edge of the clock pulse. Output terminals and data are available atall of them together. Since it is a 4 bit register, after 4 clock pulses we see all the datais available in the outputs of this register.

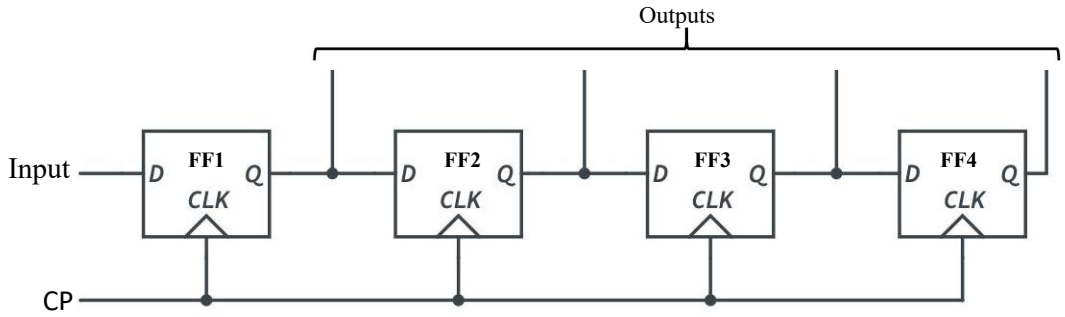


Figure 7.3: Logic diagram of PIPO shift register

The data shifting in the 4-bit SIPO is summarized below in the Table.7.2 with an example of 4 bit data ”1110”. Load the shift register with a 4-bit data ‘$B_3B_2B_1B_0$’one by one serially. In the 1st clock pulse,B_0 is shifted to Q_1(FF1). In the 2nd clock pulse,B_0 is shifted to Q_2 (FF2) and B_1 is shifted to Q_1(FF1). In the 3rd clock pulse,B_0 is shifted to Q_3(FF3), B_1 is shifted to Q_2(FF2) and B_3 is shifted to Q_1(FF1). At the end of 4th clock pulse, $B_0$is shifted to Q_4(FF4), B_1 is shifted to Q_3(FF3), B_2 is shifted to Q_2 (FF2) and B_3 is shifted to Q_1(FF1). Thus after 4th clock pulse all the outputs are available.

Clock	Serial I/P	Q_1	Q_2	Q_3	Q_4
1	$B_0 = 0$	0	X	X	X
2	$B_1 = 1$	1	0	X	X
3	$B_2 = 1$	1	1	0	X
4	$B_3 = 1$	1	1	1	0

Table 7.2: Truth table of 4-bit SIPO shift register

Parallel in-Serial out: The data is loaded in parallel form and read serially. Figure 7.4 shows the circuit of a 4-bit parallel in-serial out (PISO) shifts right with four bits. It uses D flip-flops and four data input lines: B_0 (LSB), B_1, B_2, and B_3 (MSB).

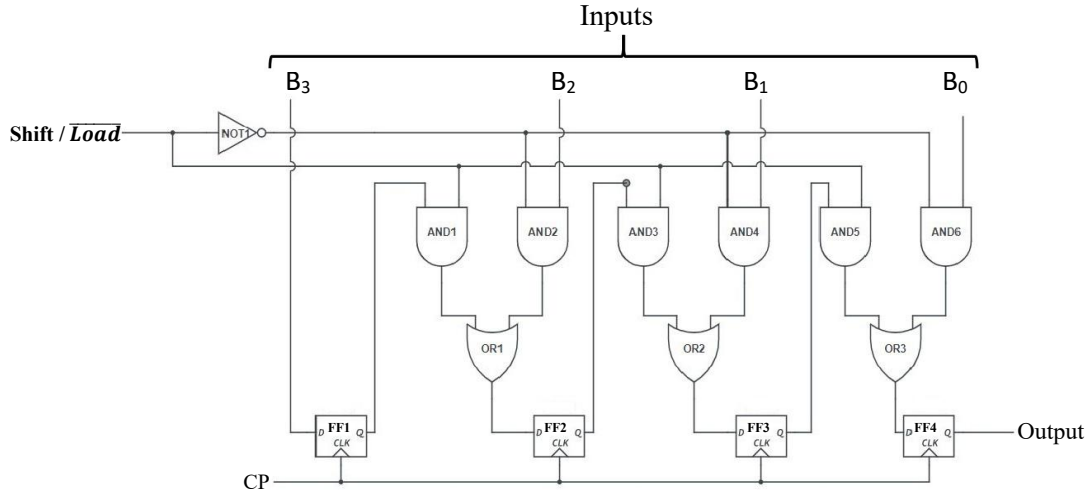


Figure 7.4: Logic diagram of PISO shift register

The data shifting in the 4-bit PISO is summarized below in the Table 7.3 with an example of 4 bit data "1110". Load the shift register with a 4-bit data '$B_3B_2B_1B_0$' simultaneously in the 1st clock pulse. In the 2nd clock pulse, B_3 is shifted to Q_2 (FF2), B_2 is shifted to Q_3(FF3) and B_1 is shifted to Q_4 (FF4) . In the 3rd clock pulse, B_3 is shifted to Q_3 (FF3) and B_2 is shifted to Q_4(FF4). At the end of 4th clock pulse B_3 is shifted to Q_4(FF4).

Clock	Parallel I/P	Q_1	Q_2	Q_3	Q_4
1	$B_3B_2B_1B_0$ = 1110	1	1	1	0
2		X	1	1	1
3		X	X	1	1
4		X	X	X	1

Table 7.3: Truth table of 4-bit PISO shift register

IC7495:

The IC-7495 is a 4-Bit Shift Register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH to LOW transition of the appropriate clock input. It has a Serial (D_S) and four Parallel ($P_0 - P_3$) Data inputs and four Parallel Data outputs ($Q_0 - Q_3$). The serial or parallel mode of operation is controlled by a Mode Control input (S) and two Clock Inputs ($\overline{CP}_1$) and ($\overline{CP}_2$). The serial (right-shift) or parallel data transfers occur synchronous with the HIGH to LOW transition of the selected clock input.

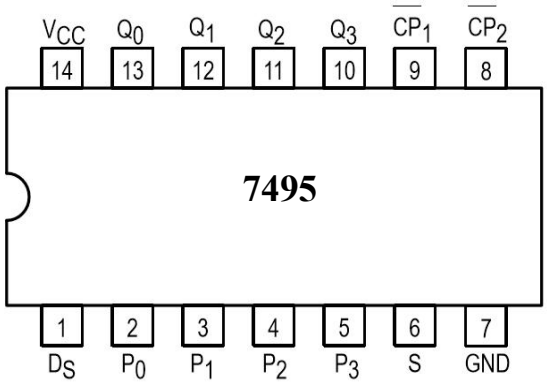


Figure 7.5: Pin diagram of IC 7495

Pin No	Pin Name	Pin Description
1	D_S	Serial Data Input
2 to 5	P_0 to P_3	Parallel Data Inputs 0 to 3
6	S	Mode Control Input
7	GND	Ground Pin
8	$\overline{CP}_2$	Negative edge Parallel Clock input
9	$\overline{CP}_1$	Negative edge Serial Clock input
10 to 13	Q_3 to Q_0	Parallel Outputs 3 to 0
14	Vcc	Supply Voltage

Table 7.4: Pin description of IC 7495

When the Mode Control input (S = 1) is HIGH, $\overline{CP}_2$ is enabled. A HIGH to LOW transition on enabled $\overline{CP}_2$ transfers parallel data from the $P_0 – P_3$ inputs to the $Q_0 – Q_3$ outputs.

When the Mode Control input (S = 0) is LOW, $\overline{CP}_1$ is enabled. A HIGH to LOW transition on enabled $\overline{CP}_1$ transfers the data from Serial input (D_S) to Q_0 and shifts the data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3 respectively (right-shift).

A left-shift is accomplished by externally connecting Q_3 to P_2, Q_2 to P_1 & Q_1 to P_0 and operating the IC7495 in the parallel mode (S = 1) HIGH.

For normal operation, S should only change states when both Clock inputs are LOW. However, changing S from LOW to HIGH while $\overline{CP}_2$ is HIGH, or changing S from HIGH to LOW while $\overline{CP}_1$ is HIGH and CP_2 is LOW will not cause any changes on the register outputs.

Implementation of various shift registers using IC 7495 has been show below.

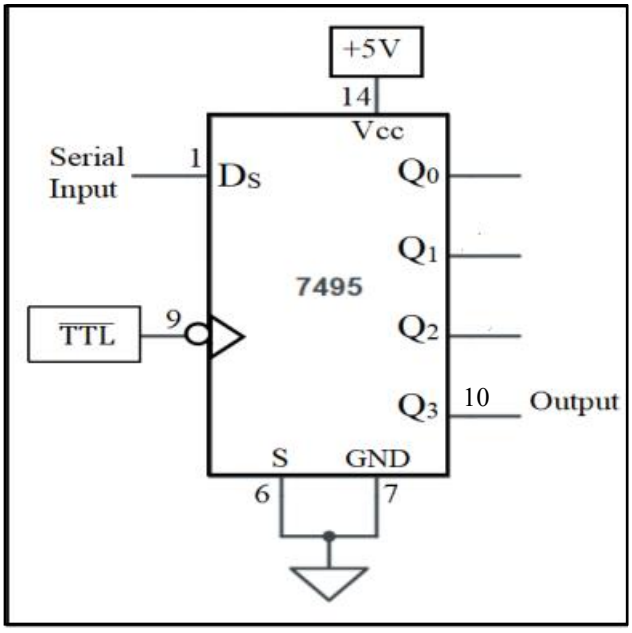


Figure 7.6: Logic diagram of 4 bit SISO shift register using IC 7495

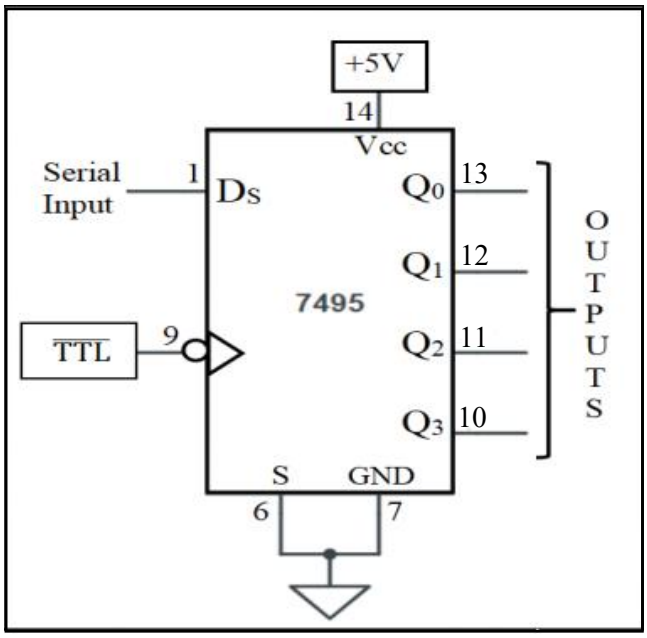


Figure 7.7: Logic diagram of 4 bit SIPO shift register using IC 7495

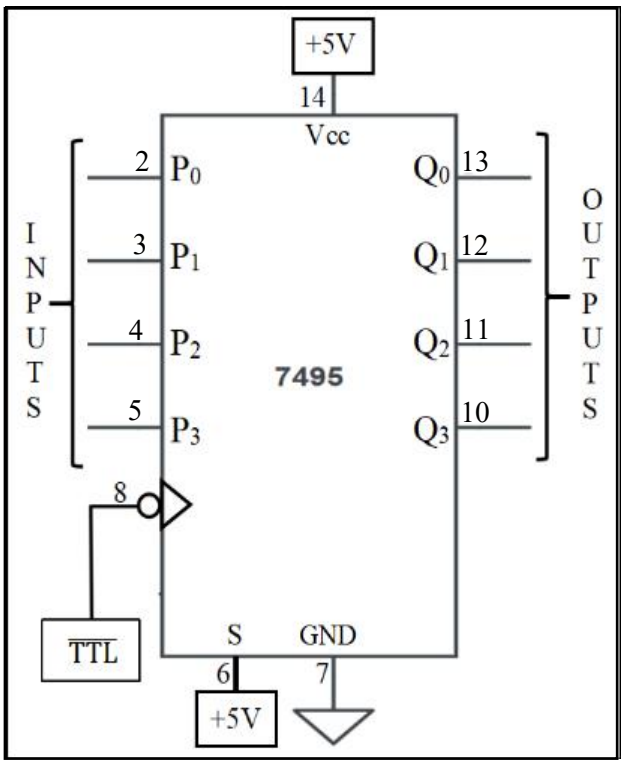


Figure 7.8: Logic diagram of 4 bit PIPO shift register using IC 7495

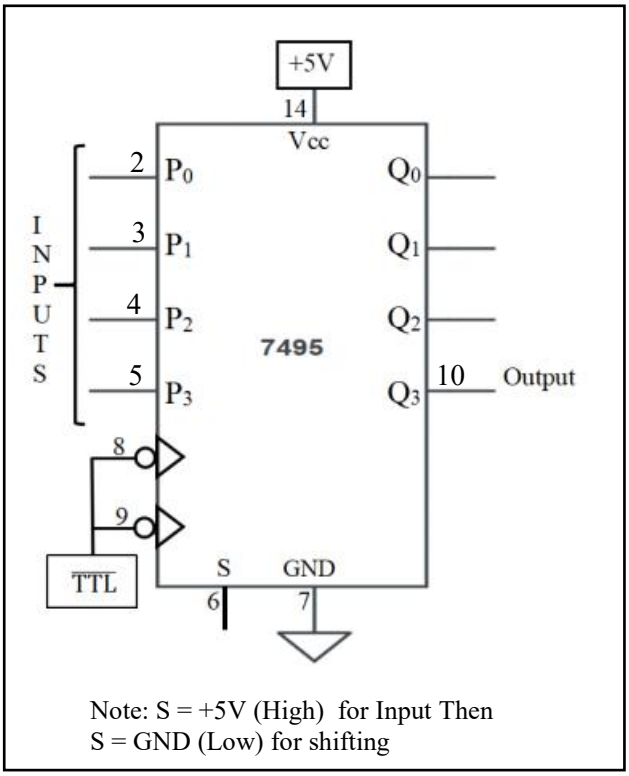


Figure 7.9: Logic diagram of 4 bit PISO shift register using IC 7495

Pseudo Random Sequence generator:

The sequence generator digital circuit which generates a set of outputs. This is a shift register where the input is a combinational logic function of the outputs of the flip-flops of the shift register. The sequence generator generates a sequence of binary bits. Thus, the length of the sequence is related to the number of flip-flops that are required to design a sequence generator. These generators are utilized in a wide variety of applications like coding and control. The length of the sequence is related to the number of flip-flops that are required to produce a sequence generator.

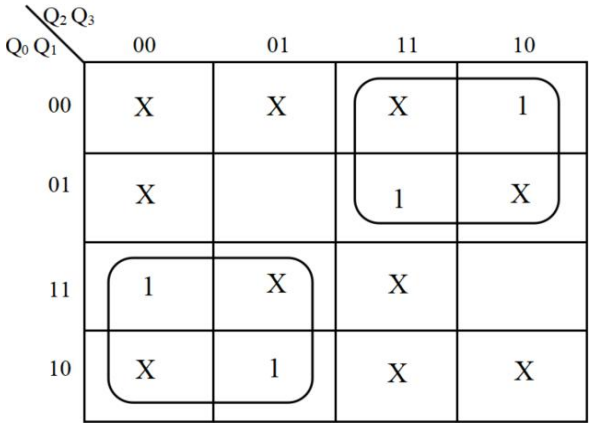
$$\mathbf{L \leq 2^n - 1}$$

where **L** is the length of the sequence and **n** is the minimum number of flip-flops required.

Designing of a sequence generator is shown using IC7495 for the sequence "**1101001**" .

Q_0	Q_1	Q_2	Q_3	D_S
1	1	0	0	1
1	1	1	0	0
0	1	1	1	1
1	0	1	1	0
0	1	0	1	0
0	0	1	0	1
1	0	0	1	1

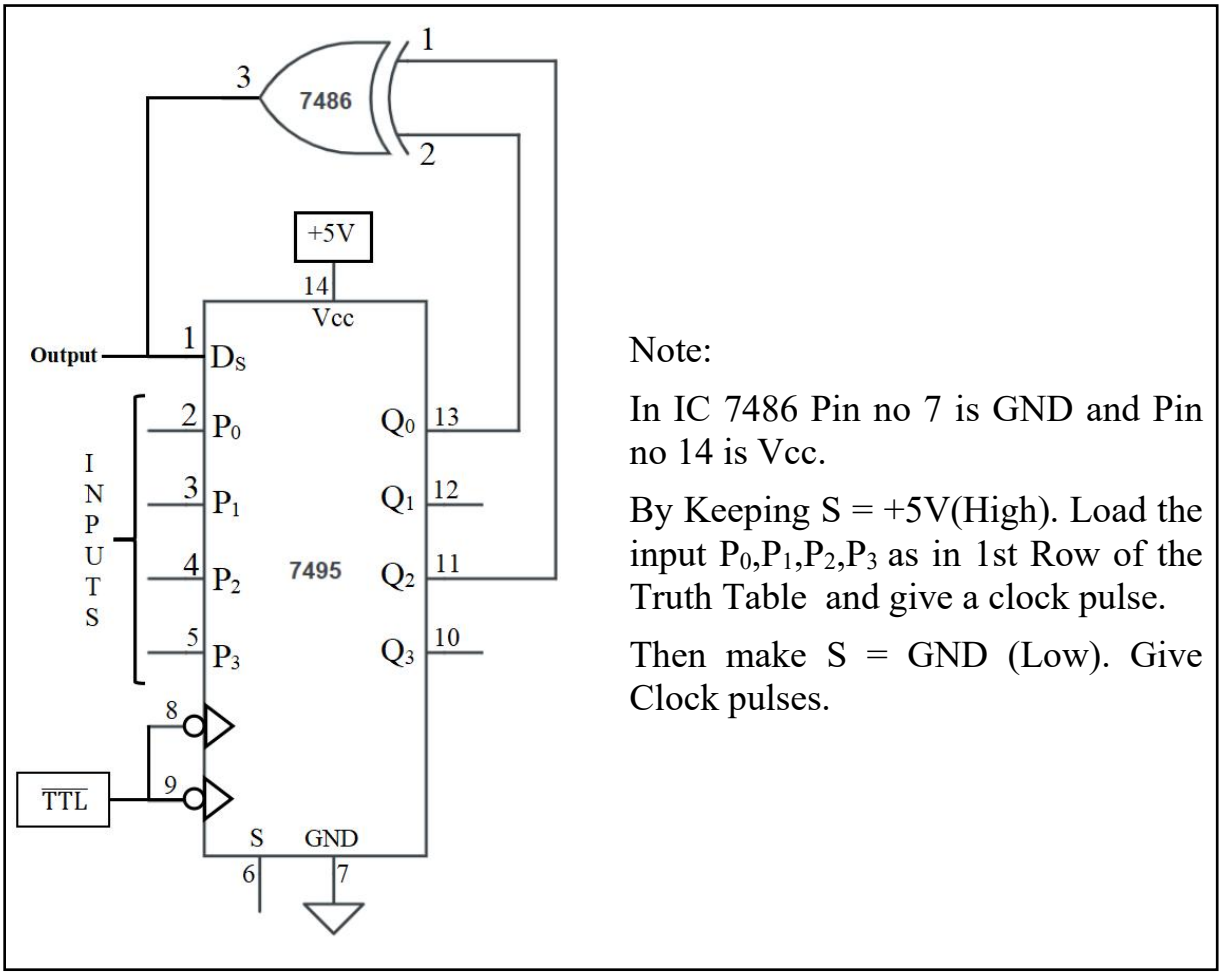
Table 7.5: Truth Table of the Sequence Generator



K-Map for the Input(D_S) of the shift register

$$D_S(Q_0, Q_1, Q_2, Q_3) = \sum (2,7,9,12) + d(0,1,3,4,6,8,10,13,15) = Q_2 \oplus Q_0$$

Boolean expression for the input D_s



Note:

In IC 7486 Pin no 7 is GND and Pin no 14 is Vcc.

By Keeping S = +5V(High). Load the input P_0,P_1,P_2,P_3 as in 1st Row of the Truth Table and give a clock pulse.

Then make S = GND (Low). Give Clock pulses.

Figure 7.10: Logic diagram of "1101001" sequence generator using IC 7495

Procedure

For Software Simulation:

a) Create a module with required number of variables and mention it's input / output.
b) Write the description of given Boolean function using operators or by using the built in primitive gates.
c) Synthesize to create RTL Schematic.
d) Create another module referred as test bench to verify the functionality and to obtain the waveform of input and output.
e) Follow the steps required to simulate the design and compare the obtained output with the corresponding truth table.
f) Take the screenshots of the RTL schematic and simulated waveforms.

Note: Students need to write the Verilog HDL code by their own for which they can refer Appendix - A if required.

For Hardware implementation:

a) Turn off the power of the Trainer Kit before constructing any circuit.
b) Connect **power supply (+ 5 V DC)** pin and **ground** pin to the respective pins of the trainer kit.
c) Place the ICs properly on the bread board in the Trainer Kit.
d) Connect VCC and GND pins of each chip to the power supply and ground bus strips on the bread board.
e) Connect the input and output pins of chips to the input switches and output LEDs respectively in the Trainer Kit.
f) Check the connections before you turn on the power.
g) Apply various combinations of inputs according to truth tables and observe outputs of LEDs.

Observation:

To be written by students

Design Problem

Design and Simulation of 4 bit Ring counter and 4 bit Johnson counter using Verilog HDL.

Hardware implementation of 4 bit Ring counter and 4 bit Johnson counter.

Solution:

Ring Counter:

Ring counter is a sequential logic circuit that is constructed using shift register. Same data recirculates in the counter depending on the clock pulse.It consists of a group of flip-flops connected in a circular chain or "ring" formation, where the output of one flip-flop is connected to the input of the next, and the last flip-flop is connected back to the first.

When a clock pulse is applied to the ring counter, the data is shifted from one flip-flop to the next, with each flip-flop in the ring taking turns being in the "high" or "low" state. The output of each flip-flop represents a different bit of the counter's binary value, with the least significant bit (LSB) being the first flip-flop in the ring, and the most significant bit (MSB) being the last flip-flop.

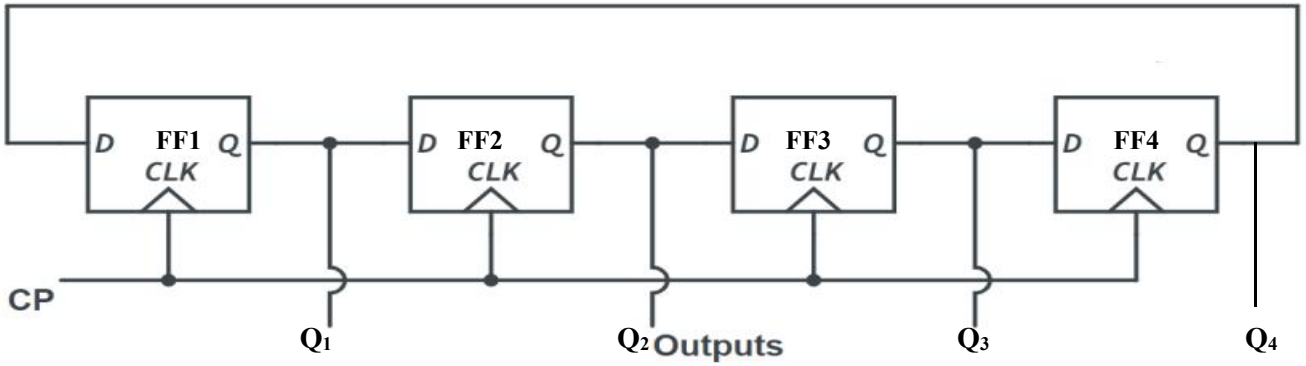


Figure 7.11: Logic diagram of 4 bit Ring Counter

Assume, initial status of the D flip-flops from leftmost to rightmost is Q_1 Q_2 Q_3 Q_4 = "1000" .This status repeats for every four(4) clock pulse. which is shown in below Table 7.6. A "mod-n" ring counter will require "n" number of flip-flops connected together to circulate a single data bit providing "n" different output states.Each state repeats after every "n" clock pulse.

Clock Pulse	Q_1	Q_2	Q_3	Q_4
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0

Table 7.6: Truth table of 4-bit Ring Counter

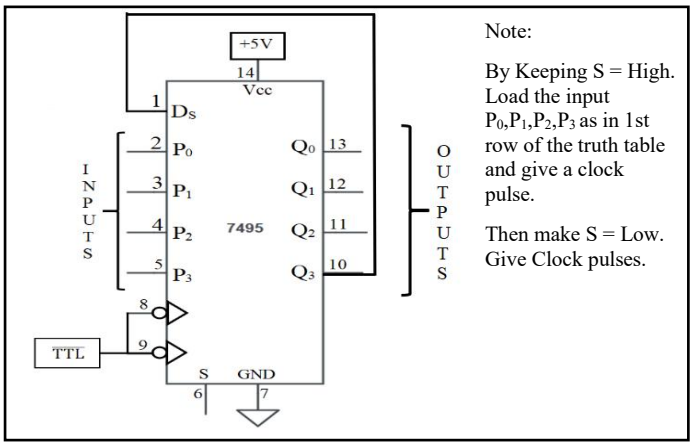


Figure 7.12: Logic diagram of Ring Counter using IC 7495

Johnson Counter:

A Johnson counter is a type of shift register that is similar to a ring counter, but with an additional invert stage. It is sometimes also called a "twisted ring counter" counter". The operation of a Johnson counter is similar to that of a ring counter, with each flip-flop output changing state on each clock pulse. However, in a Johnson counter, the output of the last flip-flop is inverted and fed back into the first flip-flop. This causes the counter to cycle through a sequence of states that includes both ascending and descending binary values.

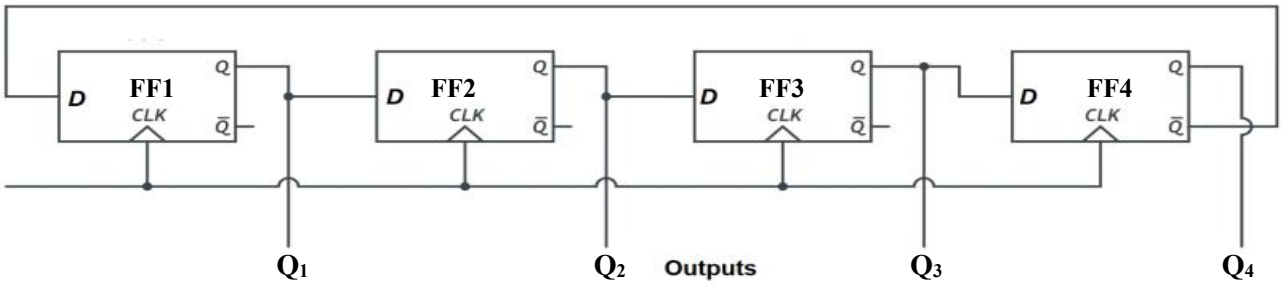


Figure 7.13: Logic diagram of Johnson Counter

Assume, initial status of the D flip-flops from leftmost to rightmost is Q1 Q2 Q3 Q4 = "0000" .This status repeats for every Eight (8) clock pulse which is shown in below Table 7.7.

A "mod-2n" ring counter will require "n" number of flip-flops connected together to circulate a single data bit providing "2n" different output states.Each state repeats after every "2n" clock pulse.

Clock Pulse	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Table 7.7: Truth table of 4-bit Johnson Counter

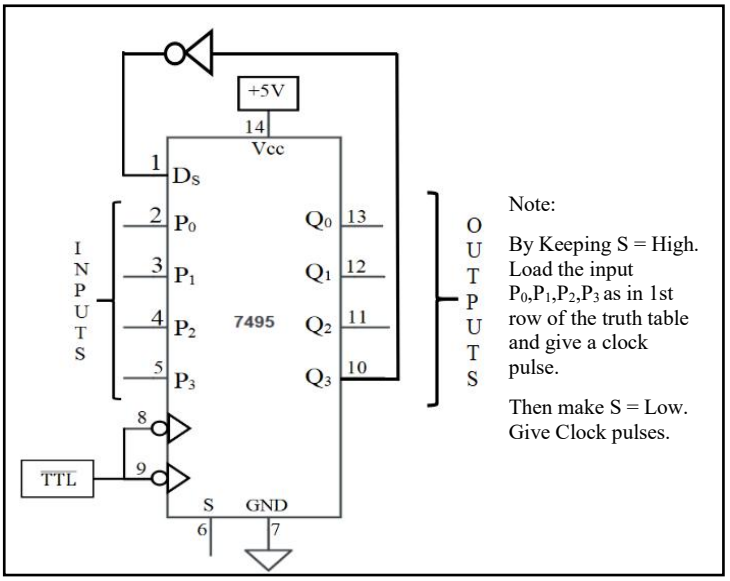


Figure 7.14: Logic diagram of 4-bit Johnson Counter using IC 7495

Conclusion:

To be written by students.

Sample viva-voice questions

1. What do you mean by serial and parallel data?
2. What is a register?
3. What are the types of loading the registers?
4. What is the basic difference between a shift register and a counter?
5. What are the applications of shift registers?
6. How will you use a shift register to multiply or divide a binary number by 2?
7. What are the basic types of shift registers?
8. What is a bi-directional shift register?
9. What is a universal shift register?
10. What is the advantage and disadvantage of ring counter?