Condition Code Register / Status Register.

- It is a special purpose CPU register. This register is used to keep track of information about the results of various operations.
  ↓
  (may be addition, subtraction etc)

- These information is used by the following (subsequent) conditional branch instruction to decide whether to take a branch or not.

- Like after an arithmatic operation is performed, whether the result is zero / negative / carry is generated / overflow occured, these various conditions are trapped inside the flag register. And looking at the content of flag register, branch has to be taken or not can be decided.

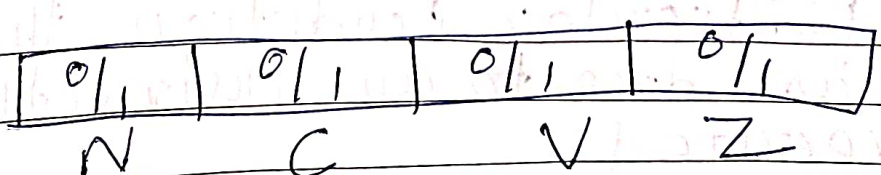
- Basically, a flag resister contains a collection of bits, where each bit position is an indication of a particular condition that may occur due to an instruction is executed.

Four commonly used Flags are

- N (negative): set to a 1 if the result is negative, else cleared to 0.
- Z (zero): set to 1 if the result is 0, else cleared to 0
- V (overflow): set to 1 if arithmetic overflow occurs, else cleared to 0.
- C (carry): set to 1 if carry-out results from the operation else cleared to 0.

Note: overflow occurs when the result of an arithmetic operation is outside the range of values that can be represented by the number.

- overflow can occur only when adding two numbers of same sign.
- The carry out signal from the signbit position is not a sufficient indicator of overflow when adding signed number.



overflow condition can be detected by examining the signs of the two summands X and Y and the sign of the result.

- When both operands X and Y have the same sign, an overflow occurs when the sign of S is not matching with the signs of X and Y.

Example, add +7 and +4

+ve

+7 = 0111

+4 = 0100

+ve

-ve (1) 0 1 1

1 1 0 1 = -5

-2^{n-1} → $2^{n-1} - 1$

range of 2's complement.

How to interpret the result?

As the numbers are represented in 2's complement form and the sign bit is 1, hence the result is -ve quantity. To get the magnitude, find the 2's complement of the result (1011)

2's complement of 1011

= 1 0 0 1 = -5

i.e. (+7) + (+4) = -5 an incorrect result.

As (+7) + (+4) = +11, and to represent +11 we need 5 bits, 1 for the sign and 4 bits for the magnitude.

So the addition of +7 and +4 is generating overflow condition, as the result is outside the range of values that can be represented using 4 bit.
Here there is no carry but overflow is there.

Example - 2:
add -4 + -6
4 = 0100 , 2's complement =
-4 = 1100 ⇒ 1011+1 = 1100
2's complement of -6:
0110 = +6
1001+1 = 1010

1100 +1010 10110 1 carry discarded.	Result = 0110 (Result is +ve) 0110 = +6

As the number are represented in 2's complement form and the sign bit is zero (0), hence the result is a positive quantity. To get the magnitude, just write the decimal equivalent of resultant bits.
$(0110)_2 = (6)_{10}$
So the result is +ve.

i.e. $(-4)+(-6) = +6$, an incorrect result.
As $(-4)+(-6) = -10$, and to represent -10 we need 5 bits.
So the addition of -4 & -6 is generating overflow condition.
In this case:

$Cf = 1$ $\quad Z = 0$
$OF = 1$ $\quad S(NF) = 0$

Example-3

Consider a register R_1 containing a value 10101010 and R_2 contains 11110000. What will be the value of carry, zero and overflow flags after the execution of the instruction:
ADD R_1, R_2 // R_2 is the destination

R_1 : 1 0 1 0 1 0 1 0
+ R_2 : 1 1 1 1 0 0 0 0
1 0 0 1 1 0 1 0

$C = 1$ $\quad Z = 0$

$N = 1$ $\quad V = 0$

Consider a Register R_1 containing a value 11110000 and R_2 containing 00010100

What will be the value of carry, zero, negative(sign) and overflow flags after the execution of the instruction SUB R_2, R_1 // R_1 is the destination

Ans $R_1 \leftarrow [R_1] - [R_2]$

$R_1 \leftarrow [R_1] + (-[R_2])$

We will take the 2's complement of (00010100)

The 2's complement of (00010100): 11101100

$R_1 = 11110000$

$+(-R_2) = 11101100$

carry discarded $\rightarrow$ 1 | 11011100

$C = 1$

$Z = 0$

NF or SF = 1

VF or OF = 0

2's complement

10100011

$+\ 1$

10100100

Result = -36

Example-4.

There are two eight bit registers 'R1' and R_2 containing the values -5 and -125 respectively. Find out the values of the status bits of V (overflow), S (sign), Z (zero) C carry flags when the following instruction is executed.

ADD R_1, R_2.

Ans $-5 = 10000101$

2's complement $= 11111011$

$-125 = 11111101$

2's complement $= 10000011$

$R_1 = 11111011$ (-ve)

$+(R_2) = 10000011$ (+ve)

carry $1\ 1\ 11111100$ → +ve (126)

	-125
+	-5
	-130

CF = 1

ZF = 0

SF = 0

OF = 1

Range

$-2^7 - 2^7 - 1$

$-128 \rightarrow +127$

here result is -130

Hence overflow