(R) 29-4-17

4th Sem (Regular)
DE EC-2011
(E&EE, E&TC, E&IE, EE)

SPRING END SEMESTER EXAMINATION-2017

4th Semester B.Tech & B.Tech Dual Degree

DIGITAL ELECTRONICS
EC-2011

(Regular-2015 Admitted Batch)

Time: 3 Hours | Full Marks: 60

Answer any Six questions including question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. Answer the following questions. [1 × 10]

   (a) Define Fan in and Fan out.

   (b) Add (-39 and +27) using 2's complement method.

   (c) State Demorgan's theorem.

   (d) Differentiate between Synchronous and Asynchronous counter.

   (e) What are the standard forms of logic expression?

   (f) How a SR Flip-flop can be converted to a JK, D and T flip-flop?

   (g) What are the drawback of binary weighted resistor type D/A converter?

   (h) Implement an XOR gate using a 4x1 MUX.

   (i) Implement the following functions using NAND only Y= B'D+A'D+BD.

   (j) Explain duality principle of Boolean Algebra.

2. (a) What do you mean by Universal gates? Verify the universal properties of NAND gate. [4]

(b) Add 647 and 482 in BCD Code. [4]

(c) What do you understand by +ve logic and -ve logic? [2]

3. (a) Design a BCD to 7 segment decoder. [4]

(b) Implement the following expression by using a 8:1 MUX. [4]
$F(A,B,C,D) = \sum m(1,3,4,11,12,13,14,15)$

(c) Determine the complement of : $F(A,B,C) = \sum m(2,4,5,7)$ [2]

4. (a) Briefly describes the operation of CMOS NAND logic circuits with Circuit diagrams. [4]

(b) A seven bit error correcting code is received as 0010100. Check whether it is a correct code or not. If there is any error then what was the code transmitted. [4]

(c) Implement the function: $F(x,y,z) = x'yz' + x'y'z + xy'z'$ using 3 to 8 line decoder. [2]

5. (a) Give the comparison between Ring counter & Ripple counter. [4]

(b) Design a sequential circuit that detects the sequence '1101' using Mealy model. Assume overlapping is permitted. [4]

(c) What is the function of clear and preset in flip-flop? [2]

6. (a) Design 4 bit Ring counter & twisted ring counter using DFF. Write the count table also. [4]

(b) Design a Decade counter in Synchronous mode. [4]

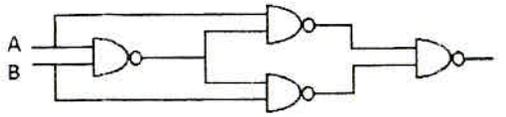
(c) Convert J-K flip flop to D flip flop and J-K to T flip flop. [2]

7. (a) Simplify the Boolean expressions using K-map and draw its simplified logic diagram: [4]

$F(A,B,C,D) = \Pi M(4,5,6,7,8,12,13) \cdot \Pi d(1,2,3,9,11,14)$.

(b) Let the input equation of a JK flip flop is specified as $J_A=B$, $K_A=Bx'$, $J_B=x'$, $K_B=A'x+Ax'$ then form the circuit diagram, state table and State diagram. [4]

(c) Show that the following circuit produced an Ex-OR operation. [2]



8. (a) Explain the operation of a JK flip-flop with suitable logic diagram. Also derive the Excitation Table for JK flip-flop. [4]

(b) Explain R-2R Ladder type D/A converter. [4]

(c) Show the difference between Moore Model and Mealy model. Draw the state diagram of D-FF (Mealy model). [2]

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