SPRING END SEMESTER EXAMINATION-2020

4th Semester B.Tech & B.Tech Dual Degree

DIGITAL ELECTRONICS

EC 2011

(For 2018 & Previous Admitted Batches)

Time: 3 Hours Full Marks: 50/60

Answer any SIX questions.
Question paper consists of four sections-A, B, C, D.
Section A is compulsory.
Attempt minimum one question each from Sections B, C, D.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

SECTION-A			
1.			[1×10]
	(a)	Define error detecting and error correcting codes.	
	(b)	Find the decimal representation of 16 bit number whose 2 complement representation is FFFF (1 bit sign and 15 bit magnitude)	
	(c)	Implement the Boolean expression $(A \odot \bar{B}) \odot (A \odot \bar{B})$ using minimum no. of gates.	
	(d)	Evaluate $(AD)_{16} - (BE)_{16}$ using 1's complement method.	
	(e)	Implement a NAND gate using 2:1 Multiplexer.	
	(f)	Define Noise Margin and Fan out.	
	(g)	Differentiate between Synchronous and Asynchronous input w.r.t JK flip flop.	

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	(h)	Calculate the percentage resolution of a 8 bit ADC.	
	(i)	Draw the circuit diagram of a CMOS NAND gate.	
	(j)	Distinguish between Mealy and Moore model.	
SECTION-B			
2.	(a)	Obtain a minimized expression for the following Boolean expression using K Map and implement the same using minimum number of NAND gate. $F(A,B,C,D) = \sum m(2,3,6,9,12) \cdot \sum d(5,8,15)$	[4]
	(b)	Explain the working of Flash type analog to digital converter.	[4]
3.	(a)	Design a 4:2 Priority Encoder such that order of priority of the decimal inputs is given as $D_1 > D_3 > D_0 > D_1$ where all $D_i's$ are inputs to the encoder.	[4]
	(b)	With the help of a neat diagram, explain the working of two input TTL NAND gate. State the advantages and disadvantages of Totem pole output configuration in the circuit of TTL NAND gate.	[4]
SECTION-C			
4.	(a)	Design a 4 bit bidirectional Shift Register using D flip flop and multiplexer.	[4]
	(b)	Implement the following logic function using a 4:1 Multiplexer $F(A,B,C,D) = \sum m(0,1,3,4,8,9,15)$ and logic gates.	[4]
5.	(a)	Convert S-R Flip Flop to J-K Flip Flop and vice versa.	[4]
	(b)	Distinguish between parallel adder and carry look ahead adder. Explain with equation how carry look ahead adder speed up the addition process.	[4]
6.	(a)	Design a synchronous mod 10 counter using J-K Flip Flops.	[4]
	(b)	Distinguish between Ring counter and Johnson counter.	[4]
SECTION-D			
7.	(a)	Design a synchronous sequential circuit using Mealy model and D Flip flops which produces an output Z=1, when "1001" is detected .Assume Overlapping Detection is used.	[4]
	(b)	Implement the function $F(A,B,C) = B + \bar{A}C + A\bar{B}C$ using 3:8 active low decoder.	[4]
8.	(a)	Develop a synchronous 3 bit Up/Down counter with a gray code sequence. The counter should count up when an UP/DOWN control input is 1 and count down when the control input is 0.	[5]
	(b)	Define "Speed- power product". If the speed power product of 1^{st} logic family is 40 pJ and 2^{nd} its 70 pJ then which one of these logic families is better . Explain in brief.	[3]
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MAPPING OF QUESTIONS WITH COURSE OUTCOMES AND LEARNING LEVELS

The paper setter /Moderator will provide mapping of Question with Course Outcomes and learning levels in the following format:

Course Name:
Course code:
Examination:

CO1	*Simplify and realize Boolean expression*
CO2	*Design various combinational circuits using logic gates*
CO3	*Design various asynchronous & synchronous sequential circuits using flip-flops*
CO4	*Design & implement Mealy and Moore model FSM for different synchronous sequential circuits*
CO5	*Differentiate between different logic families such as TTL & CMOS chips*
CO6	*Differentiate different type of Analog-to-Digital converters and Digital- to- Analog converters*

Rows may be added or deleted as necessary

Question number	Course Outcome number				Learning Level (Blooms taxonomy)
	CO No:-	Tick Any One (√)			
		Low(2)	Medium(3)	High(5)	
Section A					
Q1a	1,2	✓			1
1b	1,2		✓		2
1c	2		✓		2
1d	1		✓		2
1e	2			✓	3
1f	5		✓		2
1g	3			✓	4
1h	6			✓	3
1i	5		✓		5
1j	4		✓		3
Section B					
Q2a	1,2			✓	4
2b	6		✓		1,2,3
Q3a	2			✓	1,2,3
3b	5			✓	1,2,3
Section C					
Q4a	3			✓	4
4b	1,2			✓	3,4
Q5a	4		✓		4
5b	2			✓	4
Q6a	3,4			✓	3,4
6b	4		✓		3,4
Section D					
Q7a	4			✓	4,5,6
7b	2			✓	4
Q8a	3,4			✓	4,5,6
8b	5		✓		4,5

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Signature of Paper Setter/Moderator

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