7. (a) With the help of a neat diagram, explain the working of a counter-type ADC. [4]

(b) What is a multiplexer? Draw a 4:1 MUX using 2:1 MUX. [4]

(c) Decode the message 1110110 and 1001001. Assume that at most a single error has occurred and the message was coded in 7-bit Hamming code before transmitted. [2]

8. (a) Design a BCD to excess 3 code converter using minimum number of NAND gates. [4]

(b) How many 32K X 8 RAM chips are needed to provide a memory capacity of 256KB. How many lines of address must be used to access 256KB? How many of these lines are connected to the address inputs of all chips? [4]

(c) Reduce the expression F = **C(B + C)(A + B + C)**. [2]

– ***** –

AUTUMN END SEMESTER EXAMINATION-2017

3rd Semester B.Tech & B.Tech Dual Degree

DIGITAL ELECTRONICS CIRCUITS

EC-2009

(Back-2014 & 2013 Admitted Batch)

Time: 3 Hours Full Marks: 60

Answer any SIX questions including question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. (a) Differentiate between Mealy State Machine and Moore state Machine. [1 × 10]

(b) Perform following binary arithmetic -
(i) BCD Subtraction 476.7–258.9
(ii) (–13)– (–6) using 2's complement method.

(c) Encode a 4 bit data word '1001' into 7-bit even parity Hamming code.

(d) Design a 8:1 MUX using two 4:1 MUX and one 2:1 MUX.

(e) Find the minimum number of NAND gates required to realize a half subs- tractor circuit.

(f) Draw a 4-bit odd parity generator circuit.

(g) Find the Gray code and BCD code for the decimal value $(29)_{10}$.

(h) A 8-bit DAC has a step size of 50mV. Determine the full scale output voltage and percentage resolution.

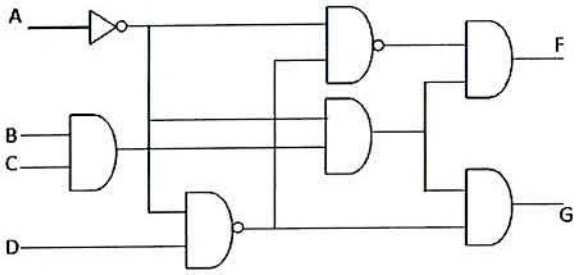
(i) Draw the circuit diagram of a 2-input CMOS NAND gate.

(j) Find the minimum number of Flip-Flops required to design a counter that counts in prime number (2, 3, 5.....N, 2, 3, ...) Where N<50.

2. (a) Obtain a minimized expression for the following Boolean expression using K-map and implement the minimized expression using minimum number of NOR gates only. [4]

$$F(A,B,C,D) = \bar{C}D + AB\bar{C} + A\bar{B}D + \bar{A}\bar{B}D$$

(b) Obtain simplified Boolean expressions for the outputs F and G [3]



(c) Design a 4:2 Priority Encoder circuit such that the order of priority of inputs is given as **D2>D0>D1>D3**, where all Di's are inputs to the encoder. [3]

3. (a) Design a combinational circuit with 3 inputs **X,Y,Z** and 3 outputs **A,B,C**. When the binary input is less than or equal to 3, the binary output is one greater than the input. When the binary input is greater than 3, the binary output is one less than the input. [4]

(b) Draw and explain a combined 4-bit adder-subs tractor block using full adders and XNOR gates only. [3]

(c) Implement the following Boolean function with a MUX having 3 select lines [3]

F(A,B,C,D) = $\sum$ m (0,1,3,4,8,9,15)

4. (a) Draw the logic diagram of a 4-bit PISO shift register using J-K Flip-Flops. Explain its operation. [4]

(b) Design a synchronous counter that goes through the states 0,3,2,6,4,0,3..... using S-R FFs [4]

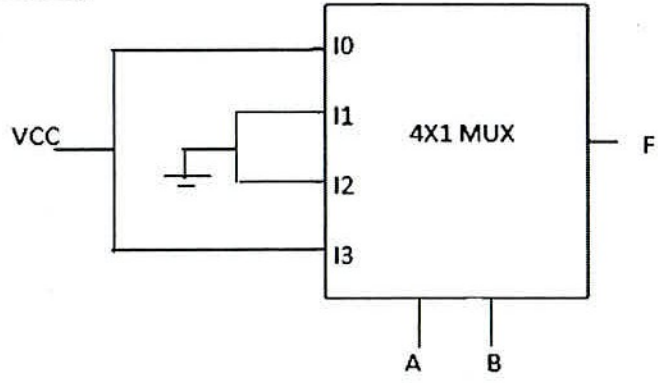
(c) Implement a full-subs tractor using a decoder circuit and two input logic gates. [2]

5. (a) Design a Synchronous sequential circuit which produces an output Z=1, whenever the following input sequence "1011" occurs. Use Mealy Model and assume overlapping is allowed. [6]

(b) Construct a J-K FF using D FF, a 2:1 MUX and an inverter. [4]

6. (a) Explain the working of a TTL NAND gate with Totem-Pole output with proper diagram. [4]

(b) Identify the Boolean function **F(A,B)** in the given figure and implement the function **F** using minimum number of NAND gates only [4]



(c) Differentiate between error-correcting and error-detecting codes. [2]