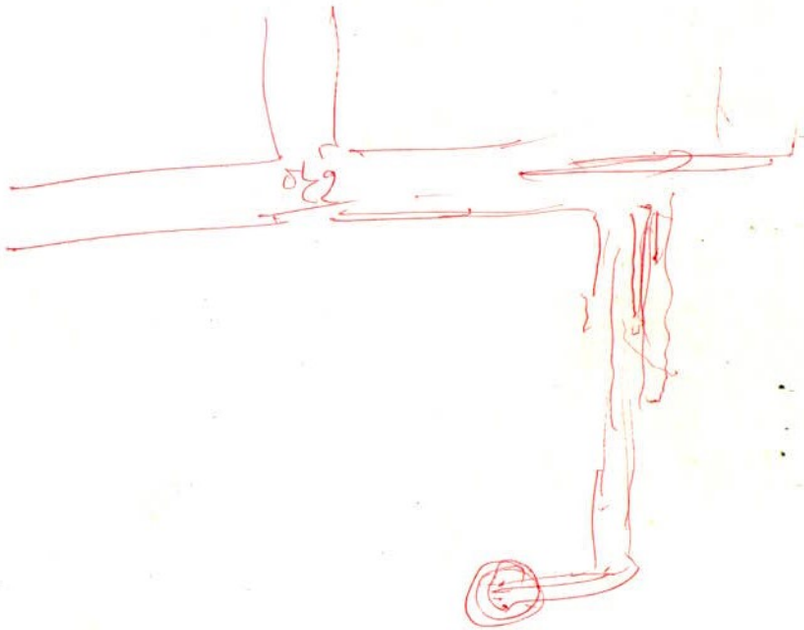


Ghanashyam Rout

IV [illegible] Regular)

DE[illegible]EC 402

(CSE, [illegible] E&TC, EE)

FOURTH SEMESTER EXAMINATION-2011

DIGITAL ELECTRONIC CIRCUITS

[EC 402]

Full Marks: 60 Time: 3 Hours

Answer any SIX questions including Question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. a) Show that NAND and NOR operations are not associative. [1 × 10
   b) What is the range of signed decimal numbers that can be represented by 6 bit binary number in 1's compliment form? Justify.
   c) What is the difference between positive and negative logic?
   d) What is the number of 4 × 16 decoders required to design a 8 × 256 decoder? Justify.
   e) What is the difference between SRAM and DRAM?
   f) Why is the fan-out of CMOS very high?
   g) Design a two-input n-mos NOR gate (only n-mos).
   h) In a 4-bit weighted resistor D/A converter, the resistance value corresponding to LSB is 32 KΩ. Find the resistance value corresponding to the MSB.
   i) A 4-bit synchronous counter uses Flip-Flop with overall propagation delay time of 15ns each. What will be the maximum possible time required for the change of state?

KIIT-U/2011/Spring End Semester Examination-2011

j) Find out the resulting output (Q(t)) of the FF for next 6 clock pulses assuming initial condition (Q=0 and $\overline{Q}$=1) for the following circuit in Figure-1(J).

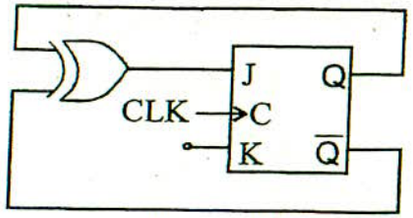


Figure-1(j)

2. a) Design a Johnson counter using D-FF to generate 8 timing signals. Make sure that the counter will be initialized with count value 0 (all FFs in reset state) when it is turned ON. Determine the count sequence for this counter and draw the decoding circuit needed to decode each state. [5

b) Find out all the states and the modulus of the counter shown in Figure-2(b). (Assume initially $Q_2\ Q_1\ Q_0$=111). [3

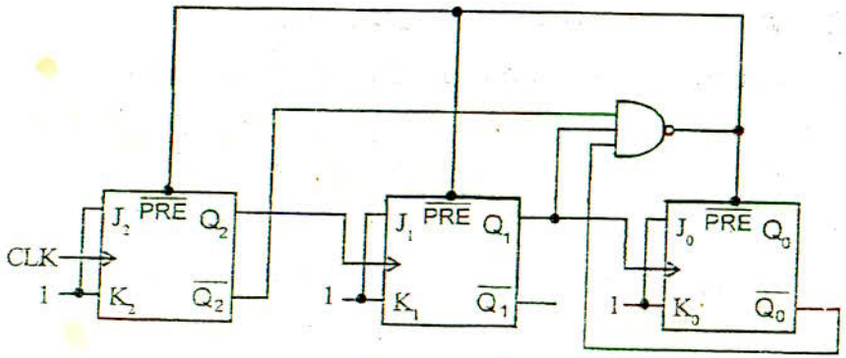


Figure-2(B)

recognized as logic-1 output is 4.5V. A negative noise voltage signal of 0.5V is added in the interconnecting wire between A and B. The noise margin is given as 0.3V. Find out the output of inverter B. Justify.

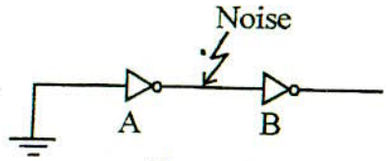


Figure-8(c)

d) Derive the Boolean expression f for the circuit implemented in Figure-8(d) using 2-input multiplexers. [2

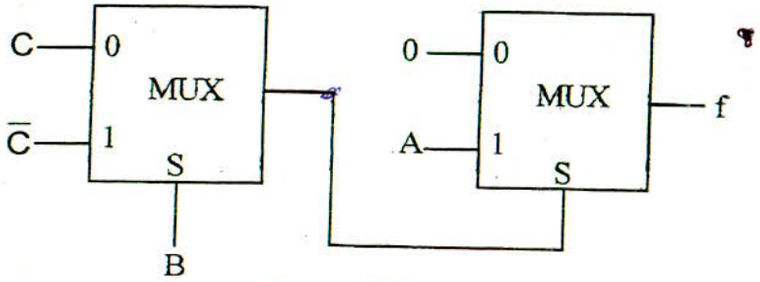


Figure-8(d)

xxxxx

8. a) Reduce the number of states in the state diagram given in the Figure-8(a). [4

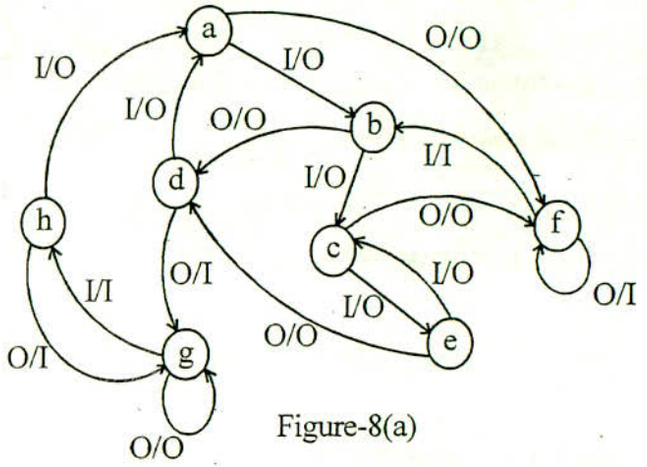


Figure-8(a)

b) The waveform shown in the Figure-8(b) are applied to a positive edge-triggered JK-FF with active low $\overline{PRESET}$ and $\overline{CLEAR}$. Draw the output waveform (Assume initially Q(t)=0). [2

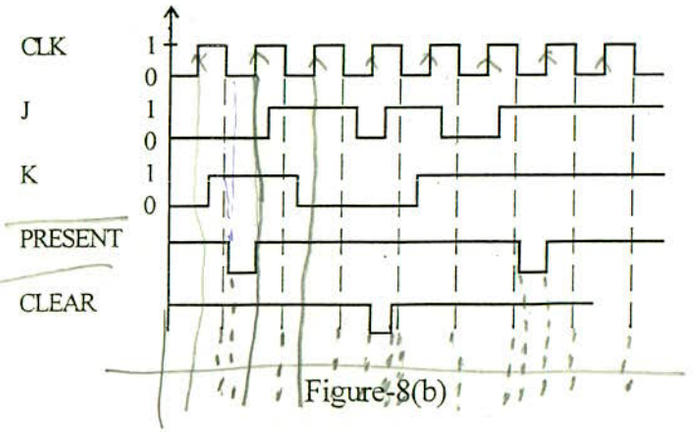


Figure-8(b)

c) In the circuit given in Figure-8(c), inverter A is driving inverter B. The minimum output voltage that can be [2

c) For the ring oscillator circuit shown below. Draw the output waveform $v_0(t)$ and find out the fundamental frequency of the oscillator if the propagation delay of each inverter is 100 pico sec. (Assume $v_0(t)=0$ for t=0). Figure-2(c). [2

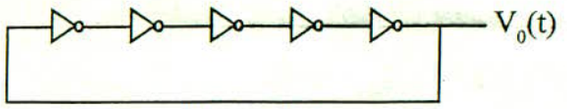


Figure-2(c)

3. a) Give the PLA realization of the following functions using PLA with 3 inputs (A, B, C) and 4 outputs. [4

$F_1(A, B, C) = \sum m(0, 1, 2, 4, 6)$
$F_2(A, B, C) = \sum m(0, 2, 6, 7)$
$F_3(A, B, C) = \sum m(3, 6)$
$F_4(A, B, C) = \sum m(1, 3, 5, 7)$

b) Design a complex CMOS function as given below [3

$$F = \overline{(A.B + C.D).E}$$

c) A 4-bit DAC circuit (Resolution=IV) is connected to a 3-bit up counter, as shown in the following figure. Draw the output waveform $v_0(t)$. (Assume Q_2 Q_1 Q_0=000 at t=0) {Figure-3(c)}. [3

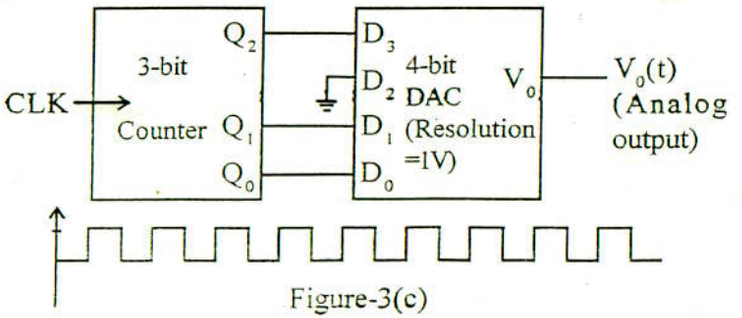


Figure-3(c)

4. a) Design an Astable multivibrator using 555 timer to generate a square wave of 2KHz frequency with 50% duty cycle. [3

b) With the help of a neat diagram explain the working of a two-input open-collector TTL NAND gate. [4

c) A certain memory has a capacity of 8K × 16. [1

(i) How many data I/P and O/P lines does it have?

(ii) How many address lines does it have?

d) Design a 4K RAM using 1K RAM chip with chip select input. [2

5. a) Design a synchronous sequential circuit which produces an output z=1, whenever any of the following input sequences 1101 or 1001 occurs. The circuit resets to the initial state after a 1 output is generated. [6

b) Draw the logic symbol and logic diagram of a 4-bit PISO shift Register using D-FF. [3

c) Determine the number of Flip-Flops and decoding gates required to design MOD-10 counter for the following topology: [1

(i) Ring Counter (ii) Johnson Counter

6. a) With the help of a neat diagram and suitable example explain the working of successive approximation type [4

A/D converter circuit. Compare its conversion time with the counter type A/D for a clock speed of 500 KHz.

b) Implement the following Boolean function using one 4:1 MUX and external gates [4

$$F(A\,B\,C\,D) = \sum(1, 3, 4, 11, 12, 13, 14, 15)$$

c) (i) Add $(-31.5)_{10}$ and $(-93.125)_{10}$ using 2's compliment arithmatic. [2

(ii) What is the Radix of the numbers if the solution to the quadratic equation $x^2-10x+31=0$ is x=5 and z=8?

7. a) Design a MOD-6 Ripple down counter using negative edge triggered JK-FF. [3

b) Design an alarm circuit using logic gates for which the specification is given as following: [3

"The ALARM output is 1 if the PANIC input is 1, or if the ENABLE input is 1, the EXITING input is 0 and the house is not SECURE; the house is SECURE if WINDOW, DOOR and GARAGE inputs are all 1".

c) State the differences between Mealy and Moore model for the following: [2

(i) Output (ii) Speed (iii) No. of states

d) What is the main problem associated with Binary parallel adder circuit and how is that overcome by using the look-ahead-carry adder circuit? [2

(2) (1)

(1)

Ghanashyam Rout 9861096193 (1)

Solution

Fourth Semester Examination 2011

Digital Electronic Circuits (EC 402)

B Tech (Regular)

---

1) (a) NAND is not associative $(A \uparrow B) \uparrow C \neq A \uparrow (B \uparrow C)$

$\{A \uparrow (B \uparrow C) = f(A, B, C) = \sum m(0, 1, 2, 3, 7)$

$(A \uparrow \{B) \uparrow C\} = f(A, B, C) = \sum m(0, 2, 4, 6, 7)$

NOR is not associative $A \downarrow (B \downarrow C) \neq (A \downarrow B) \downarrow C$

L.H.S $= f(A, B, C) = \sum m(1, 2, 3)$

R.H.S $= f(A, B, C) = \sum m(3, 5, 7)$

(b) Range $\Rightarrow (-31)$ to $(+31)$ including $+0$ & -0 (3)

for a n-bit binary no. in 1's compliment form

range $= [-(2^{n-1} - 1)$ to $(2^{n-1} - 1)]$

(c) If the voltage level assigned to logic 1 is more positive than the voltage level assigned to logic 0 such logics are called positive logic. While reverse of the +ve logic is called negative logic.

(d) Seventeen $(16 + 1)$

16 to get the output and one to select one out of 16 decoders.

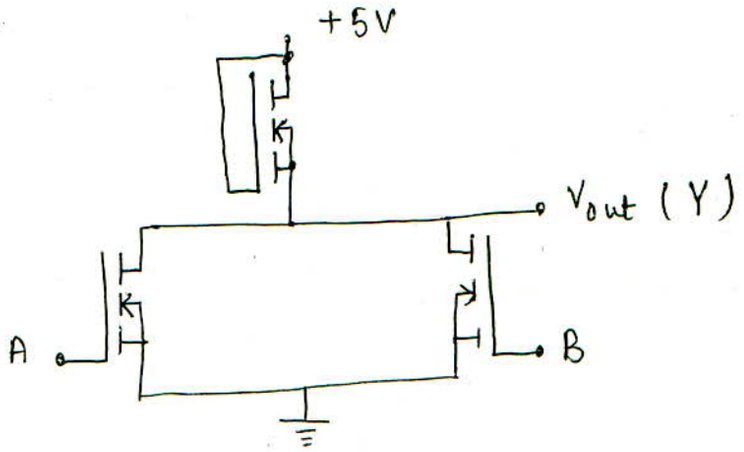
(e)

SRAM	DRAM
Binary info. is stored in the latches	Binary information is stored in the form of charges on mos capacitors which needs to be refreshed periodically.

(f) CMOS has a higher input impedance so it draws almost zero current from the driving gate so it has a high fan-out value.

(g) n-MOS NOR gate

$Y = \overline{(A + B)}$



(h) $(R)_{LSB} = 32\ k\Omega$ (4 bit weighted resistor DAC)

$(R)_{MSB} = 4\ k\Omega$.

(i) In case of synchronous counter all the FFs change their states simultaneously. So max. possible time for change of state will be 15 ns (overall propagation delay of any FF).

(j) $J = Q \oplus \bar{Q} = 1$ $\quad J = Q \oplus \bar{Q} = 1$

$K = 0$ $\quad$ or $\quad K = 1$

$Q(t) = 1\ 1\ 1\ 1\ 1 \ldots$ $\quad Q(t) = 1\ 0\ 1\ 0\ 1\ 0 \ldots$

③

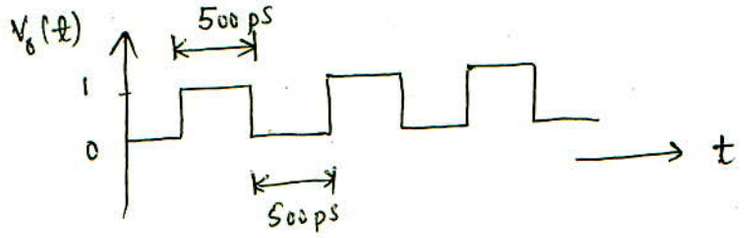
2)(b) The counter resets to count $Q_2 Q_1 Q_0 = 111$ if the state of the counter reaches $Q_2 Q_1 Q_0 = 010$

From the circuit, counter goes through following states with the application of clock pulses.

Clock Pulse	Q_2	Q_1	Q_0	
0	1	1	1	← Resets to 111
1	0	1	1	
2	1	0	1	
3	0	0	1	
4	1	1	0	
5	0	1	0	
⋮	⋮	⋮	⋮	

Finally Modulus of the counter = 6

2)(c) Plot of $V_0(t)$ with time will be as following

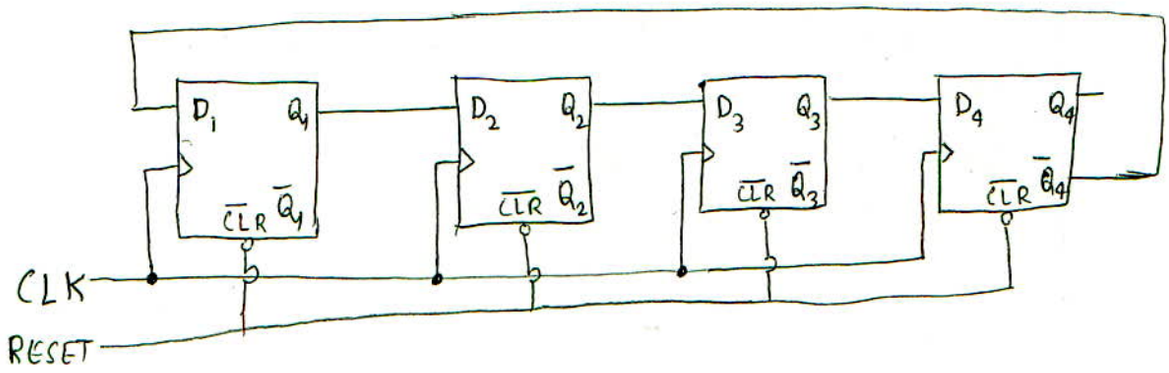


Time Period $T = 1000\ pS = 10^{-9}$ sec.

Fundamental freq. $f = 1/T = 10^9$ Hz.

④

2) a) 4-bit Johnson Counter go through 8 different states (1000 → 1100 → 1110 → 1111 → 0111 → 0011 → 0001 → 0000)



Initially RESET = 0 ⇒ count value = 0

Then RESET = 1 and applying clock pulses.

Clock Pulse	Q_1	Q_2	Q_3	Q_4	Count value	AND-gate inputs
0	0	0	0	0	0	$\bar{Q}_1 \bar{Q}_4$
1	1	0	0	0	8	$Q_1 \bar{Q}_2$
2	1	1	0	0	12	$Q_2 \bar{Q}_3$
3	1	1	1	0	14	$Q_3 \bar{Q}_4$
4	1	1	1	1	15	$Q_1 Q_4$
5	0	1	1	1	7	$\bar{Q}_1 Q_2$
6	0	0	1	1	3	$\bar{Q}_2 Q_3$
7	0	0	0	1	1	$\bar{Q}_3 Q_4$
8	0	0	0	0	0	

3) a) On simplification using K-map,

$F_1(A, B, C) = \sum m(0, 1, 2, 4, 6)$

$= \bar{C} + \bar{A}.\bar{B} = \overline{BC + AC}$

$F_2(A, B, C) = \sum m(0, 2, 6, 7) = AB + \bar{A}\bar{C}$

$F_3(A, B, C) = \sum m(3, 6) = \bar{A}BC + AB\bar{C}$

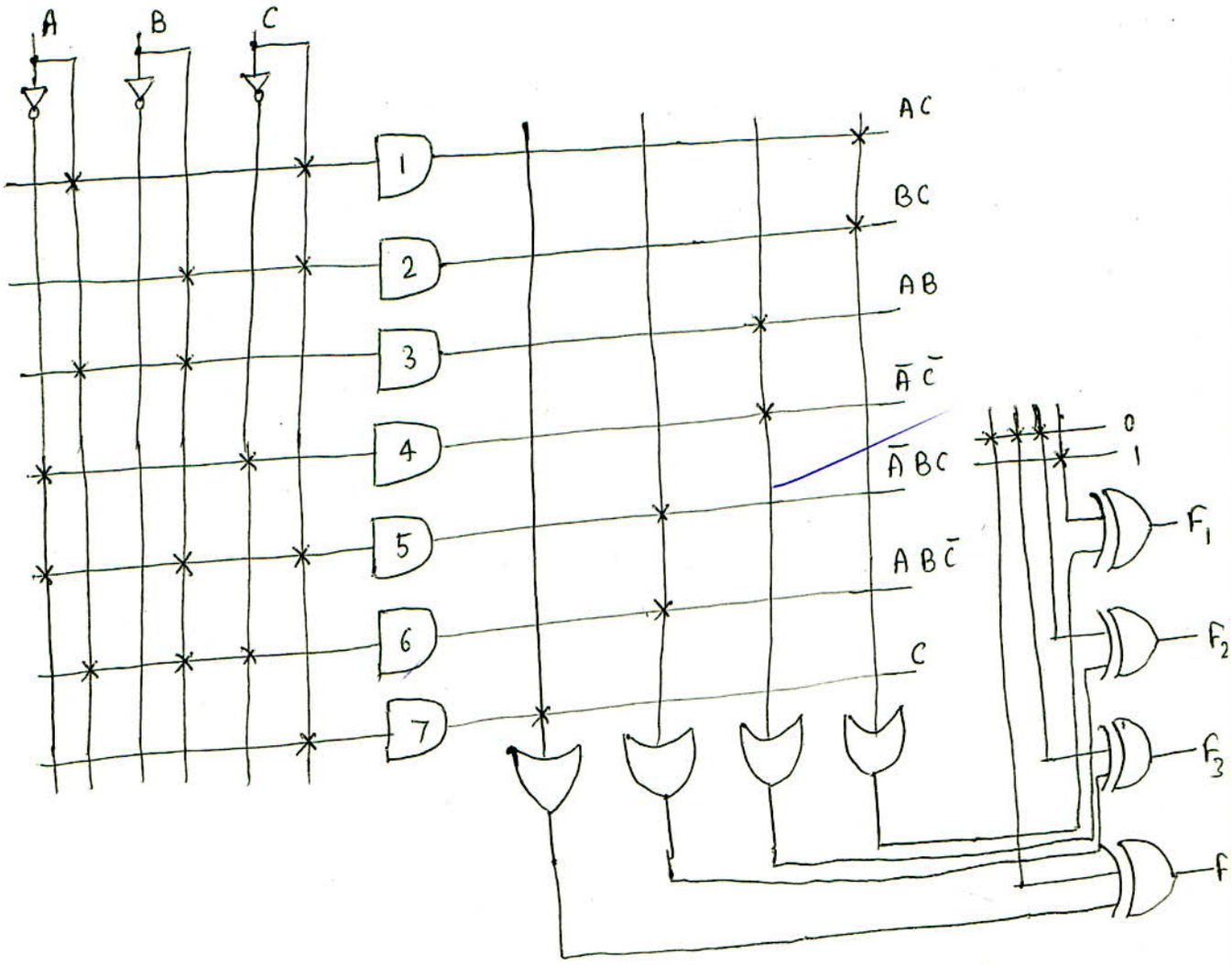
$F_4(A, B, C) = \sum m(1, 3, 5, 7) = C$

(5)

(5)

PLA programming table,

	Product term	Inputs			Outputs			
		A	B	C	$(C)'(T)$ F_1	(T) F_2	$(T)'$ F_3	$(\bar{T})$ F_4
1	AC	1	-	1	1	-	-	-
2	BC	-	1	1	1	-	-	-
3	AB	1	1	-	-	1	-	-
4	$\bar{A}\bar{C}$	0	-	0	-	1	-	-
5	$\bar{A}BC$	0	1	1	-	-	1	-
6	$AB\bar{C}$	1	1	0	-	-	1	-
7	C	-	-	1	-	-	-	1

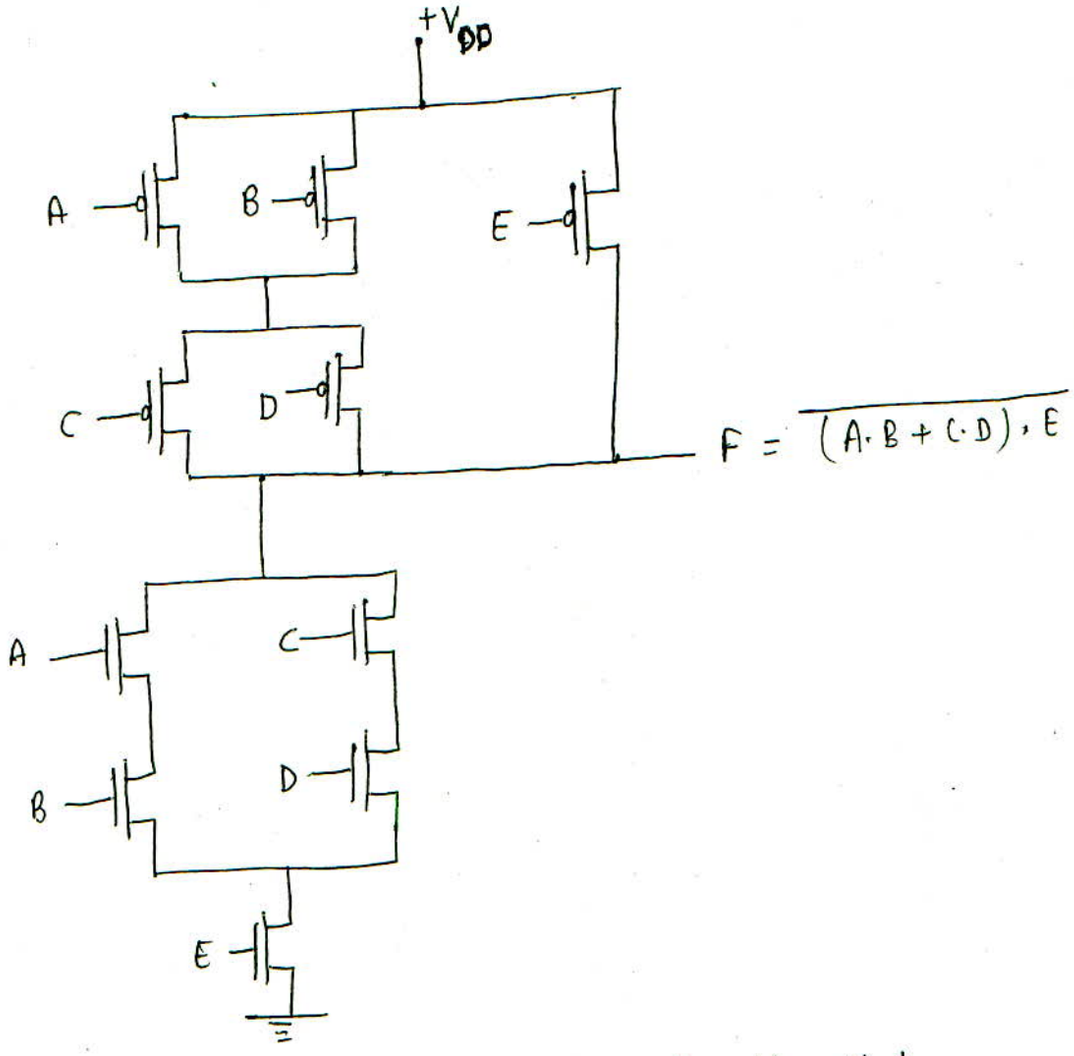


PLA realization of the functions.

(6)

(6)

3) (b) $F = \overline{(A \cdot B + C \cdot D) \cdot E}$

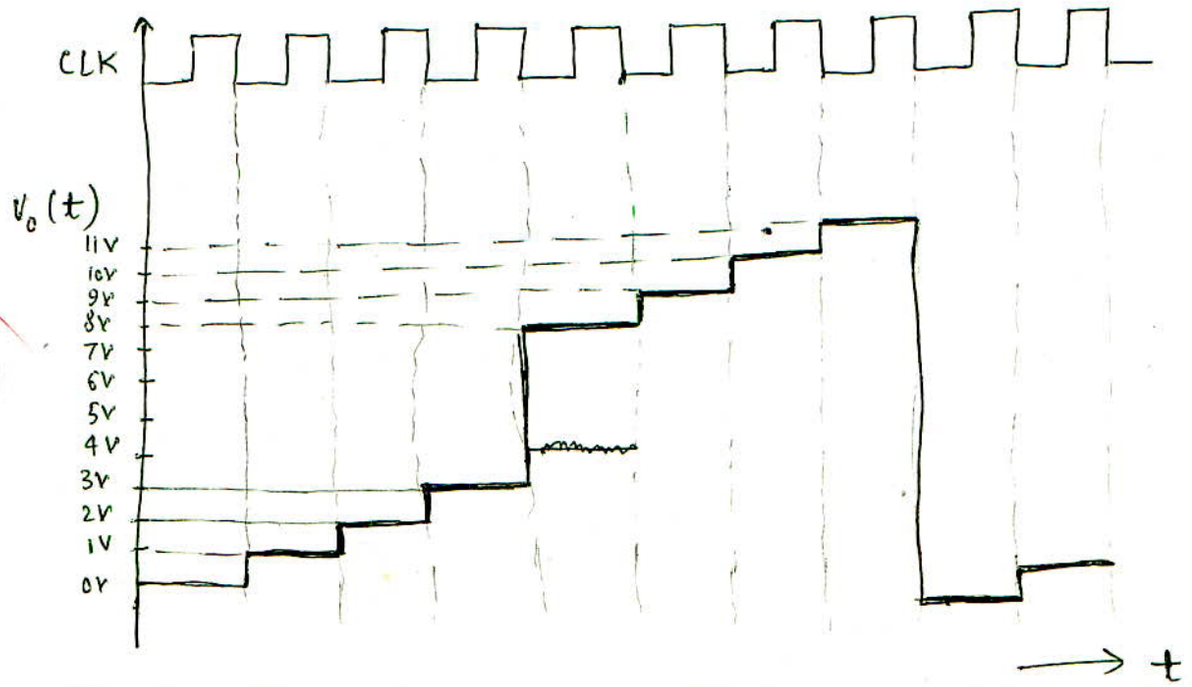


(03)

3) (c) 3 bit counter goes through the states

0, 1, 2, 3, 4, 5, 6, 7

Input to the DAC ⇒ 0, 1, 2, 3, 8, 9, 10, 11, 0, 1, 2..



(03)

7

4) (a) In an astable multivibrator using 555

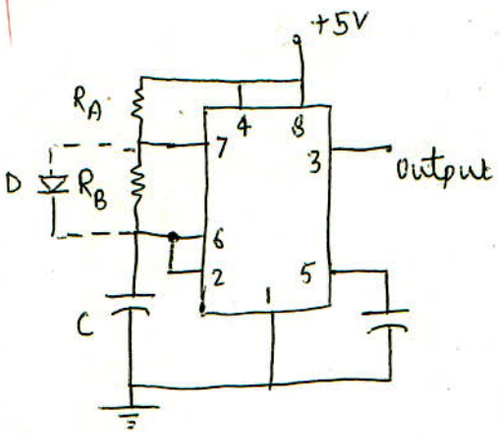
$t_1 = 0.693 (R_A + R_B) C$

$t_2 = 0.693 R_B C$

$t_1 = 0.693 R_B C$

To get 50% duty cycle (i) $R_A << R_B$

or (ii) A diode can be connected across R_B to get a perfect square wave.



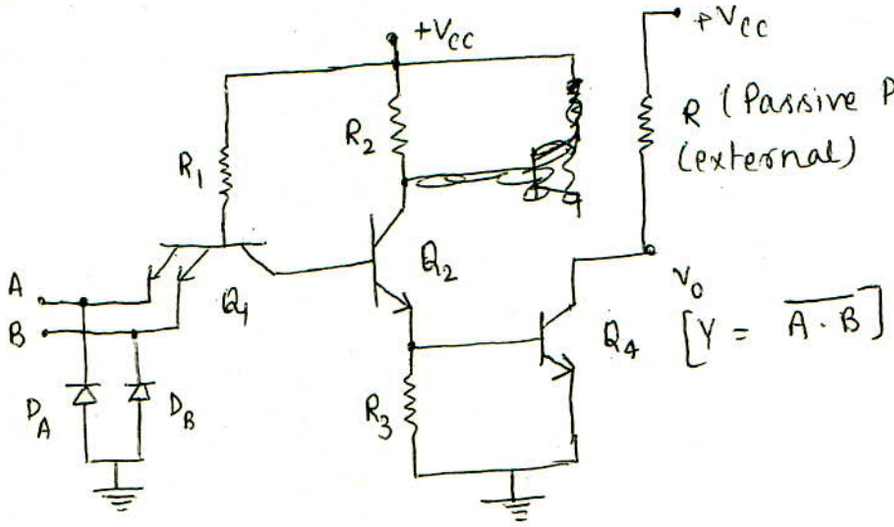
(i) $t_1 = t_2 = 0.693 R_B C = \frac{1}{2f}$

~~Take $R_B = 2k\Omega$ (Assume)~~

$R_B C = \frac{0.25 \times 10^{-3}}{0.693}$

or (ii) $R_A C = R_B C = \frac{0.25 \times 10^{-3}}{0.693}$

4(b) Two input open-collector TTL-NAND gate



(8)

(8)

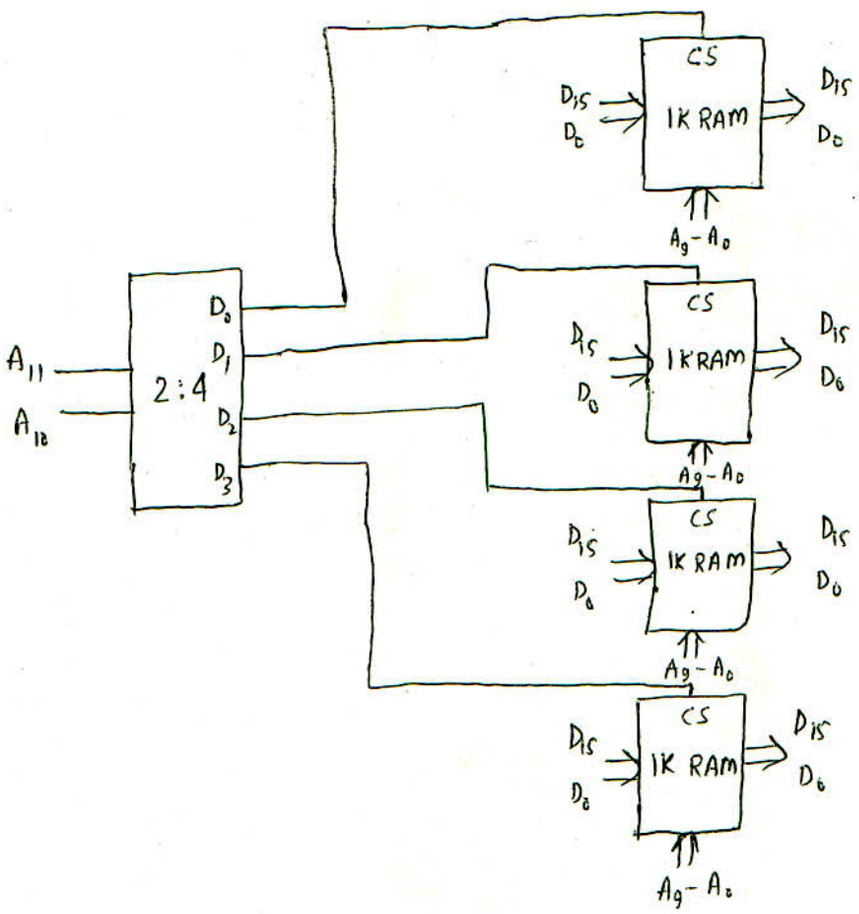
4 (c) (i) Data input = 16 lines } word length
" output = 18 lines }

01

(ii) Address lines ⇒ 8K words
= 13 2^{13} words

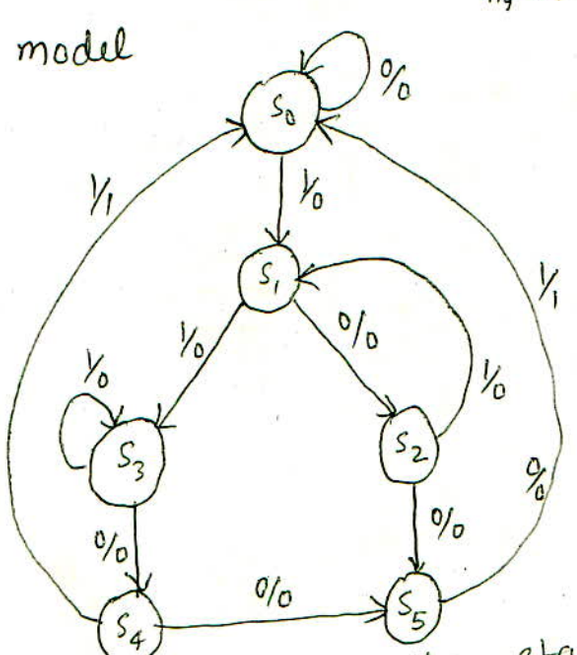
4 (d)

02



5) (a) Mealy model

06

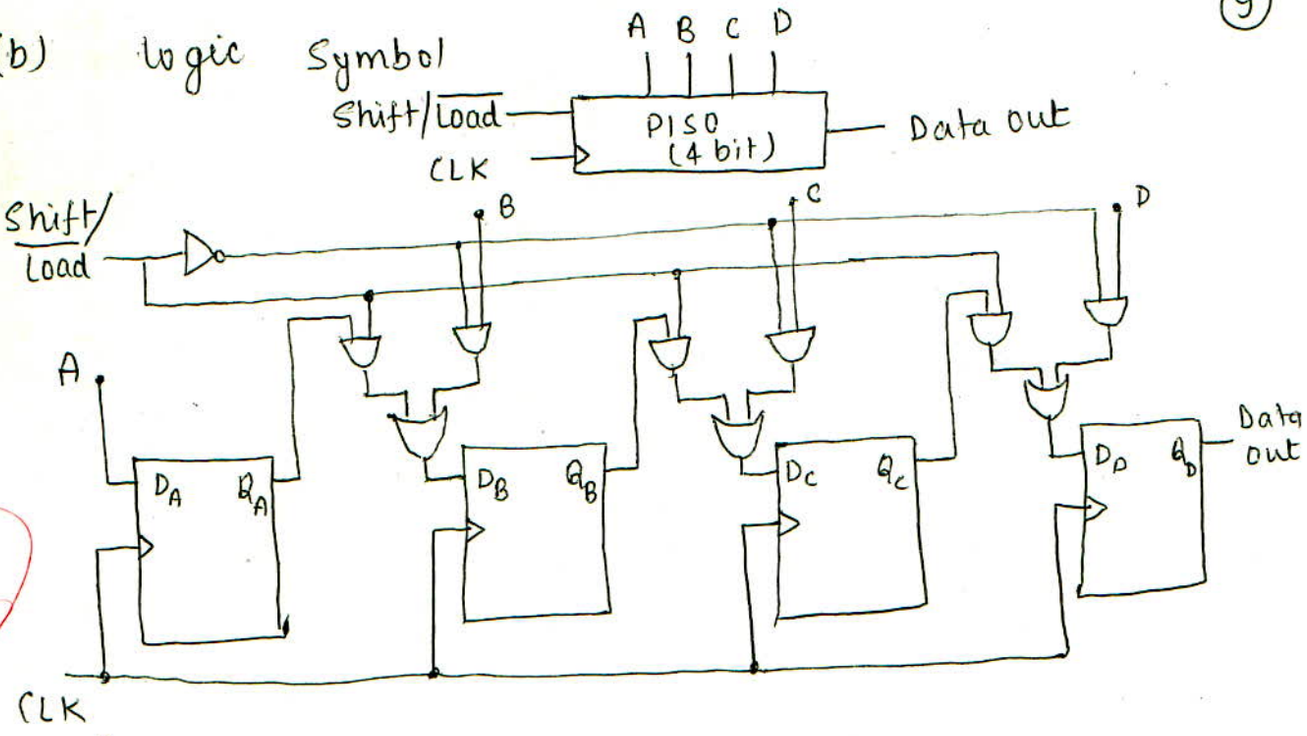


S_0 - Reset
S_1 - "1"
S_2 - "10"
S_3 - "11"
S_4 - "110"
S_5 - "100"

State table - As per the state diagram
Final circuit → As per the final expression.

9

5) (b) logic Symbol



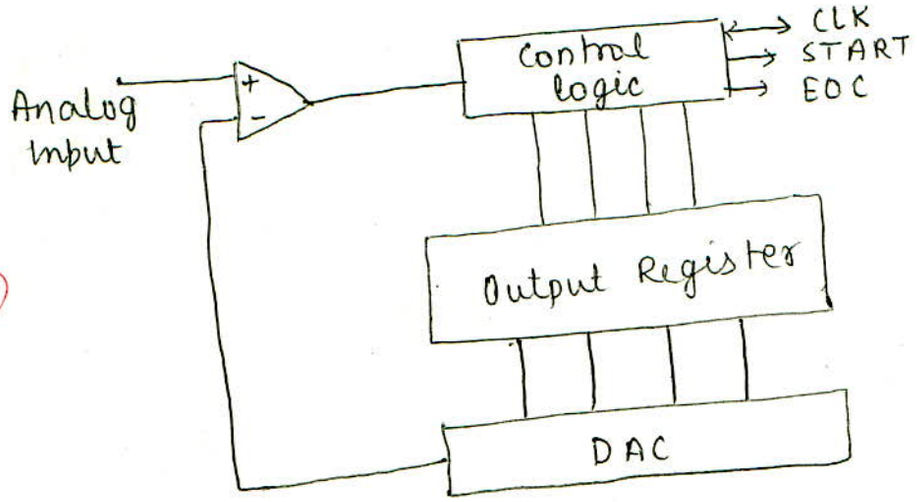
03

5) (c)

Topology	No. of FF required	No of decoding gates
i) Ring	10	0
ii) Johnson	5	10

01

6) (a) 4-bit Successive Approximation type ADC



04

Conversion time (4 bit Successive approximation type ADC)

$= 4 \times 2\,\mu s = 8\,\mu s$

While for 4-bit counter type ADC will have max possible conversion time $= 2^4 \times 2\,\mu s = 32\,\mu s$

(10)

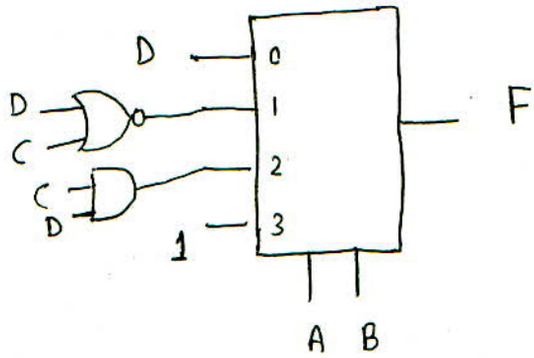
(10)

6)(b) $F(A,B,C,D) = \sum m(1,3,4,11,12,13,14,15)$

A	B	C	D	F	
0	0	0	0	0	
0	0	0	1	1	$f = D$
0	0	1	0	0	
0	0	1	1	1	
0	1	0	0	1	
0	1	0	1	0	$f = \overline{C+D}$
0	1	1	0	0	
0	1	1	1	0	
1	0	0	0	0	
1	0	0	1	0	$f = C \cdot D$
1	0	1	0	0	
1	0	1	1	1	
1	1	0	0	1	
1	1	0	1	1	$f = 1$
1	1	1	0	1	
1	1	1	1	1	

07

Implementation



6(c)(i) -31.500 -93.125 -124.625

11100000.100
10100010.111
110000011.011

02

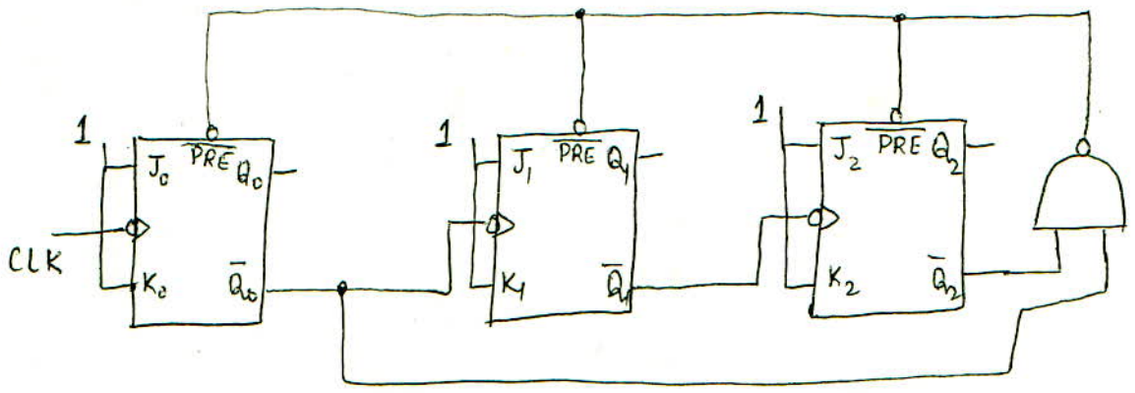
(ii) Base of the number system = 13

$x^2 - 10x + 31 = 0$ $\quad x^2 - 13x + 40 = 0$

$(10)_b = (13)_{10}$ & $(31)_b = (40)_{10} \Rightarrow b = 13$

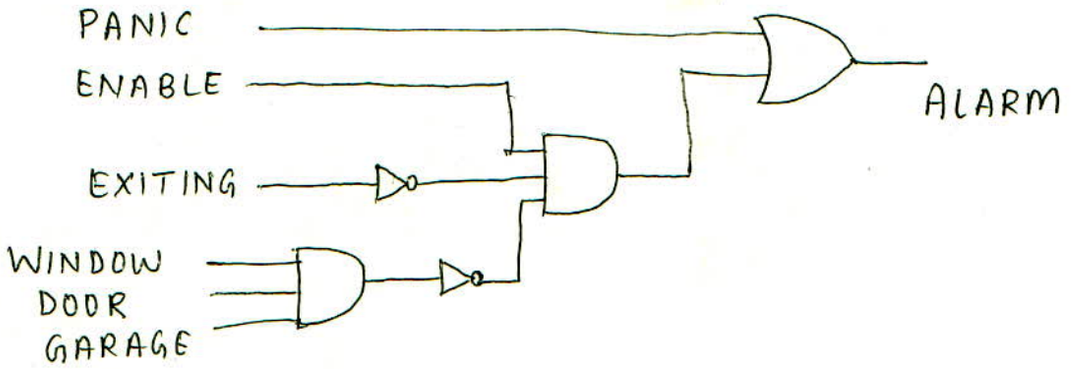
11

7)(a) MOD - 6 Ripple down counter
(using -ve edge triggered JK-FF)



03

7)(b)



03

7(c)(i) Output ⇒ o/p depends on I/p & P.S. in Mealy machine
o/p depends on the present state in Moore "

02 (ii) Speed ⇒ Mealy has higher speed than Moore

(iii) No. of states ⇒ No. of states is more in Moore machine.

7(d) In the case of binary parallel adder, the speed with which an addition can be performed is governed by the time required for the carries to propagate or ripple through all the stages of the adder.

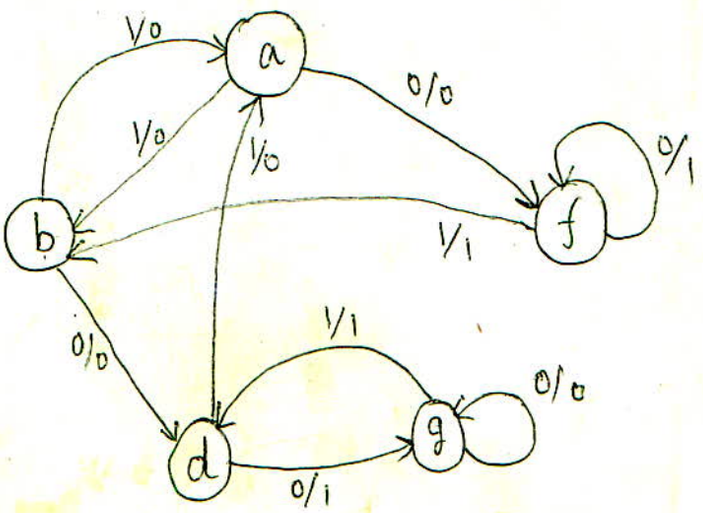
01 The look ahead carry adder speeds up process by eliminating this ripple carry delay. It examines all the I/p bits simultaneously also generates the carry-in bits for all the stages simultaneously.

12

12

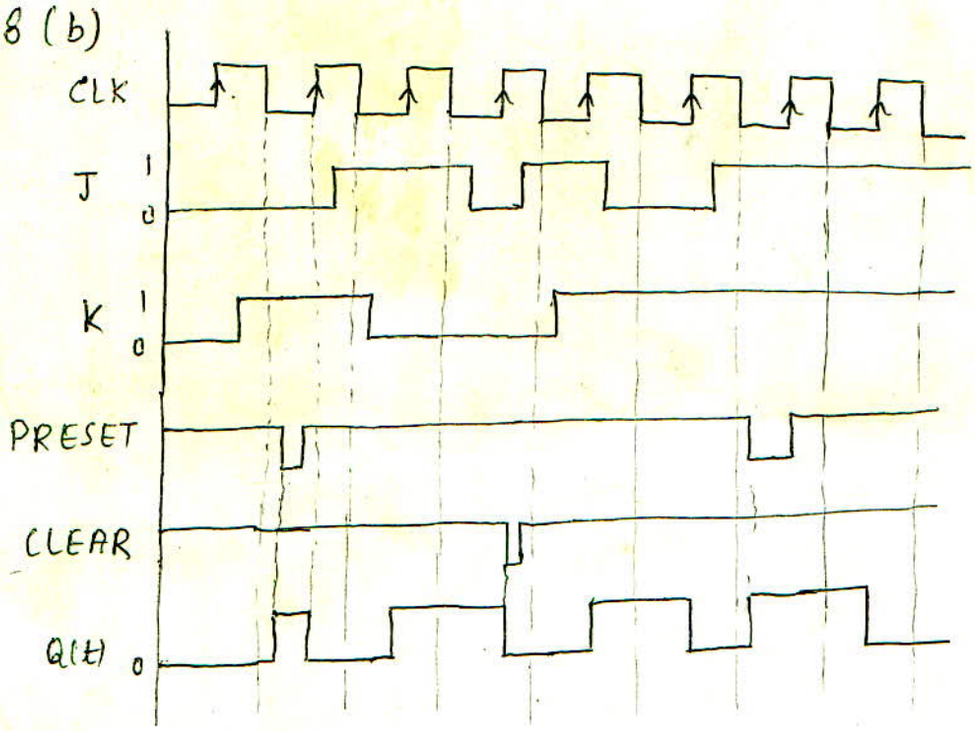
8) (a) Identical States = (d, h)
(b, e)
(a, c)

Reduced state diagram



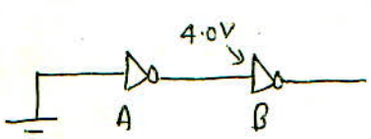
04

8 (b)



02

8 (c)



V_{O_A} = 4.5 V
V_{iB} = 4.0 V (Noise voltage = 0 - 0.5 V)

V_{IH} at B = 4.5 - 0.3
= 4.2 V

Since input to Inverter B is not logic 1 so the final output will be undetermine

02

8 (d) $f = (\bar{B}C + B\bar{C}) \cdot A$

03