Ghanashyam Roul — (2)

KIIT UNIVERSITY, BHUBANESWAR

Re-Mid Semester Examination-Spring'2014

DIGITAL ELECTRONIC CIRCUITS

[EC-402]

Full Marks: 25 **Duration: 2Hrs**

Answer all five questions.

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

(1) a) For what minimum value of propagation delay in each flip-flop will a 10 bit ripple counter skip a count when it is clocked at 10 MHz? [1x5]

b) Differentiate synchronous and asynchronous input terminals of flip-flop, explain with the help of J-K FF.

c) What is *don't care term* and how can such term arise in practice?

d) Define (i)Self-complementing code,(ii)Sequential codes. Give examples of both.

e) Show that, $AB+\bar{A}C+BCDE = AB+\bar{A}C$

(2) a) Design a MOD-6 synchronous up-counter using JK-FFs. [2.5]

b) Using 2-4 decoders (having enable input) design 3-8 decoder with enable input so that the new 3-8 decoder can be used for further expansion. [2.5]

(3) a) Implement 4-bit odd parity generator using a multiplexer having three select lines. [2.5]

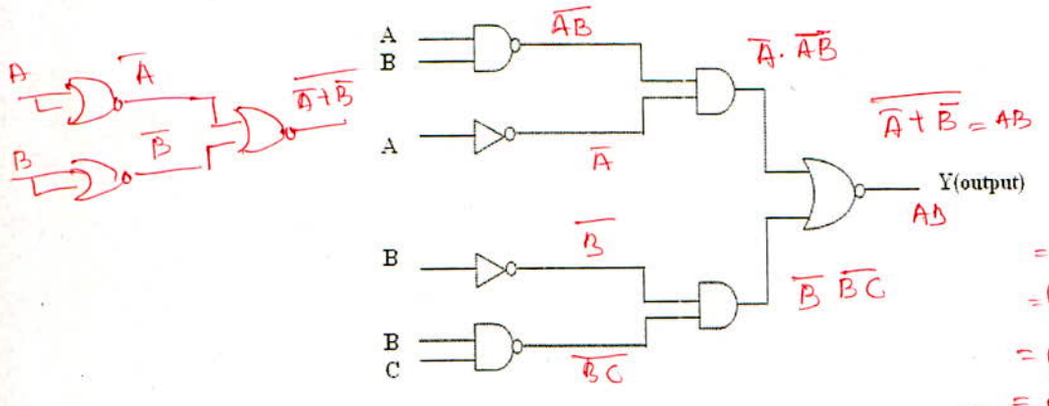
b) Design J-K Flip-Flop using **2:1 MUX** and a **T Flip-Flop.** [2.5]

(4) a) Obtain the minimized expression for the following 4-varible Boolean expression using K-map method and implement the minimized expression using NAND gates only. [2.5]

$$F(P,Q,R,S) = \Pi M(0,1,4,10,11,14).d(2,7,8,13)$$

b) Design a 4:2 priority encoder using given priority order **priority order : $D_2 > D_1 > D_3 > D_0$.** [2.5]
where D_3, D_2, D_1 *and* D_0 are input lines of encoder.

(5) a) Simplify the given logic circuit and implement the simplified circuit using only NOR gates. [2.5]



$\overline{A+\bar{B}} = AB$

$\bar{A}\cdot\overline{AB} + \bar{B}\cdot\overline{BC}$

$= \overline{\bar{A}\cdot\overline{AB}} \cdot \overline{\bar{B}\cdot\overline{BC}}$

$= (\bar{\bar{A}} + \overline{AB})(\bar{\bar{B}} + \overline{BC})$

$= (A + AB)(B + BC)$

$= A(1+B)B(1+C) = AB.$

b) Draw the circuit diagram of (i)MOD-6 Johnson counter (ii)MOD-4 Ring counter and compare N-bit Ring & Johnson counter from modulus and decoding circuit point of view. [2.5]

$\overline{AB} = AB$

$\overline{A+B}$

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1. (a) Prime numbers till 50 → 2, 3, 5, 7, 11, 13, 17, 19, 23, 29, 31, 37, 43, 47.

total → 14

modules of counter → 14.

(b).

Synchronous input Terminals.	Non-synchronous input terminals
(i) Memory elements are clocked FFs	(i) Memory elements are either unclocked FFs or time delay elements.
(ii) The change in input signal can affect memory elements upon actuation of clock signal	(ii) change in input signal can affect memory elements at any instant of time.

(c) 'Don't care term' are the combinations for B which the values of the expression are not specified.

It often occurs when for certain input combinations, output is not determined or unspecified because either the input is invalid or the precise value of output is of no consequence.

(d). A code is said to be self-complementing, if the code word of 9's compliment of N i.e; of 9-N can be obtained from the code word of N by interchanging all the 0s and 1s.

XS-3 codes are self-complementing.

Sequential code is one in which each successive code binary number greater than its preceding code word. eg → XS-3 codes.

e. LHS = $AB + \bar{A}C + BCDE$.

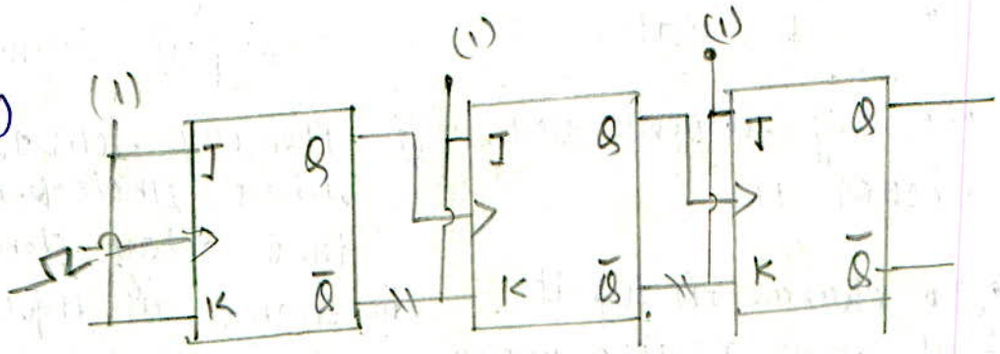
$= AB + \bar{A}C + BCDE(A+\bar{A})$

$= AB + \bar{A}C + ABCDE + \bar{A}BCDE$

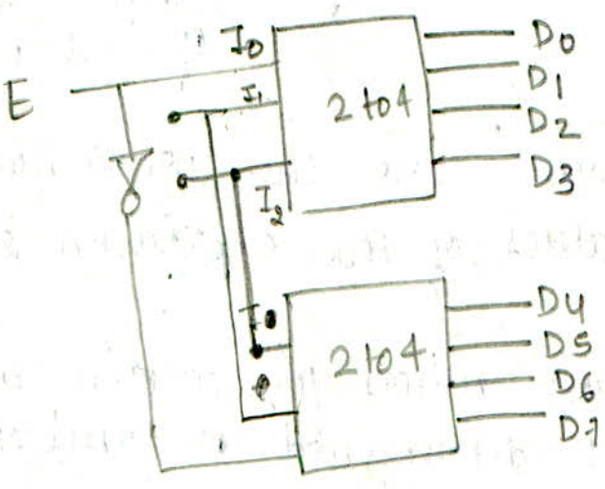
$= AB(1+CDE) + \bar{A}C(1+BDE)$

$= AB + \bar{A}C$ = RHS

2. (a)



(b)

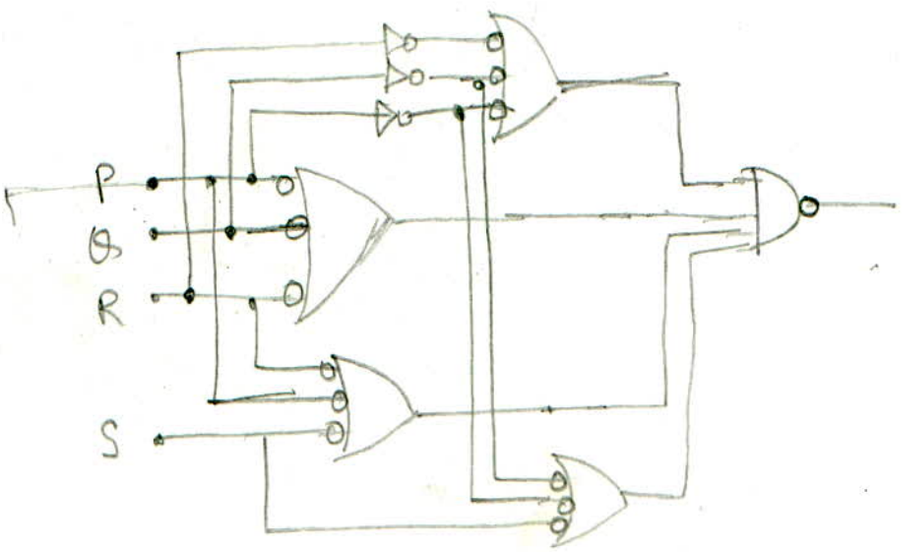


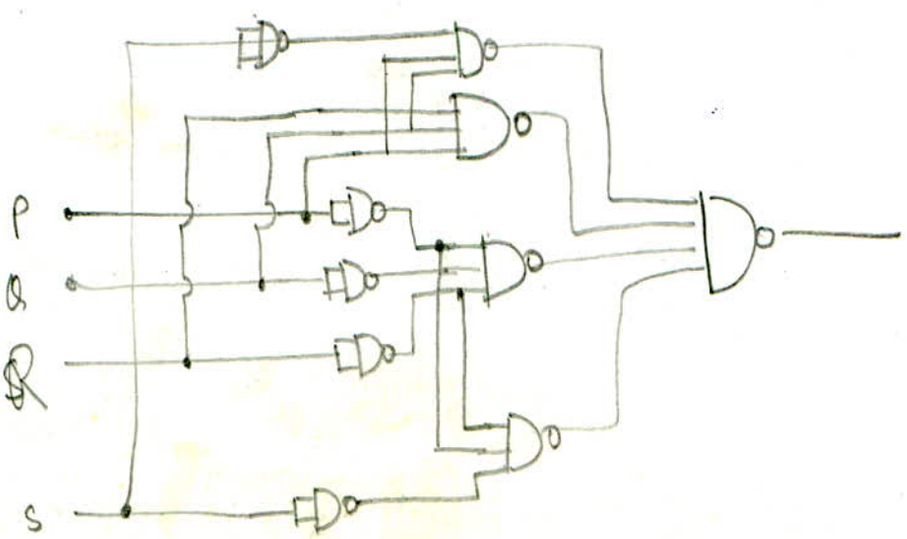
3 to 8 decoder

4 a.

PQ \ RS	00	01	11	10
00	0	0		X
01	0		X	
11	X		0	0
10		X		0

$$F = (P+Q+R)(P+R+S)(\bar{P}+\bar{Q}+\bar{R})(\bar{P}+\bar{R}+S)$$





15. (a) data word → '1000'

_	_	1	_	0	0	0
P_1	P_2	D_1	P_3	D_2	D_3	D_4

P_1, D_1, D_2, D_4 should for even parity system

$\therefore P_1 = 1$.

P_2, D_1, D_3, D_4 should form even parity

$\therefore P_2 = 1$

Now, $P_3 D_2, D_3, D_4$ should be even parity

$P_3 = 0$.

~~Now, $C_2 C_1 C_0 = 011$~~

~~$\uparrow \quad = 3$~~

Hamming code → 1110000.

II error code → 1110110

even parity → $P_1 D_1 D_2 D_4$ should be even parity

$\therefore$ 1110 is not even parity

$\therefore C_0 = 0$.

Now, P_2, D_1, D_3, D_4 should be even parity.

$\therefore$ 1110 is not even parity

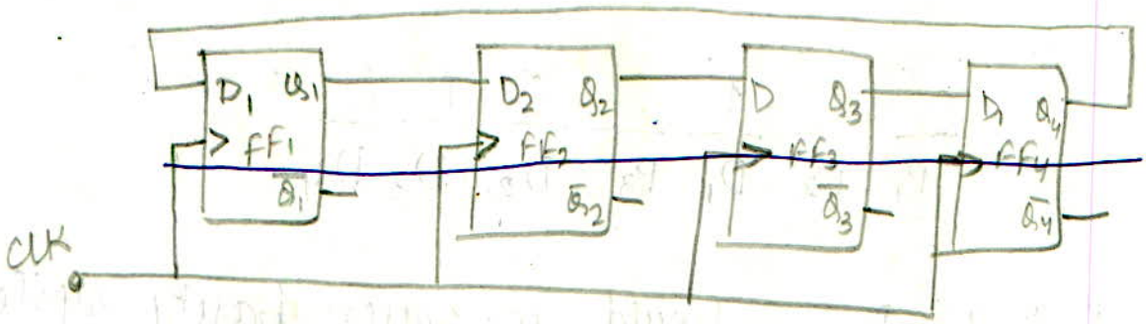
$\therefore C_1 = 1$

again, $P_3 D_2 D_3 D_4 \rightarrow 0110 \rightarrow$ even parity $\therefore C_2 = 0$

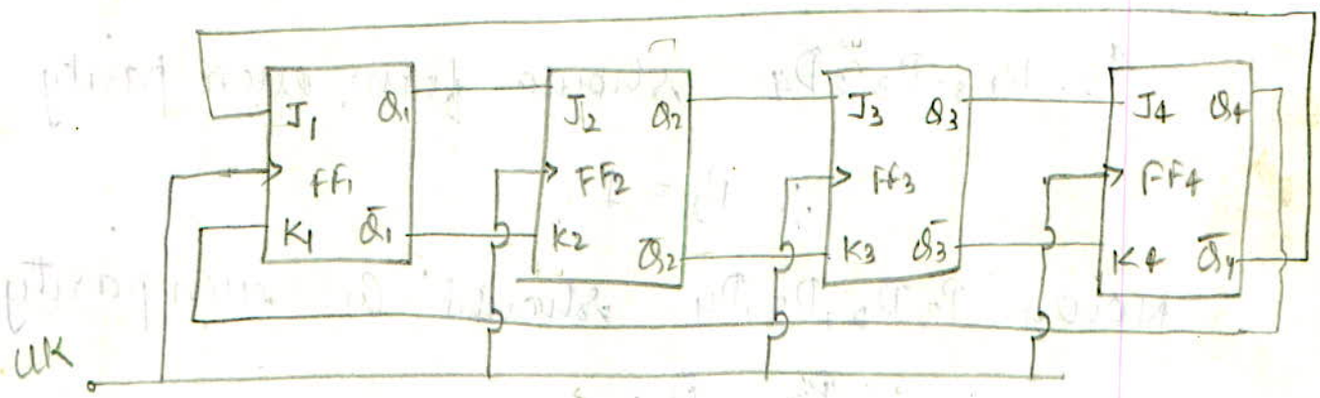
so, $C_2 C_1 C_0 = 011 = 3$

so, correct 4-bit data = 0110.

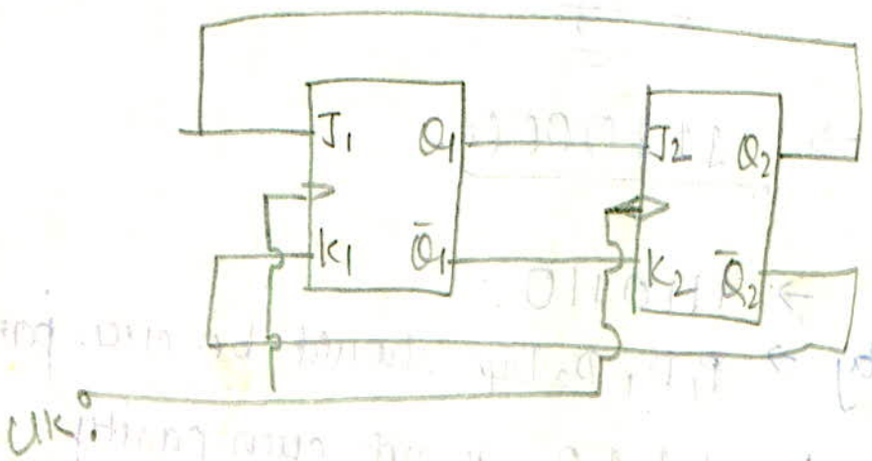
(b) MOD-6 Johnson counter.



~~MOD-4 John~~



MOD-4 RING COUNTER.



MOD-2^N Johnson counter

(i)

N BIT Ring counter.

(i)