2010 Adm. Batch
VI-B-Tech Supplementary Examination
DEC EC-402
[E&EE, E&TC, AE&I, CSE, IT, EE]

FOURTH SEMESTER EXAMINATION-2012

DIGITAL ELECTRONICS CIRCUITS

[EC-402]

Full Marks: 60 **Time: 3 Hours**

Answer any six questions including question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and All parts of a question should be answered at one place only.

1. a) $(11010110110)_2 = (\ ?\ )_{16}$ (1x10)
   b) What do you mean by non-weighted code? Give examples.
   c) How can an X-NOR gate be used as an inverter?
   d) State Demorgan's Theorem.
   e) Write the truth table and draw the circuit diagram of a 2:1 multiplexer.
   f) What is bidirectional shift register?
   g) Determine the percentage resolution of a 8-bit DAC.
   h) Explain the term Fan-in and fan-out as applicable to gates.
   i) What do you mean by state reduction and what is it's advantage?
   j) Draw the circuit of a CMOS inverter.

2. a) Implement 3-bit combined even and odd parity generator using a multiplexer having two select lines and X or gate. (hint: use X or gate as a buffer and as an inverter) (4)

   b) Minimize the following (4)
   $F(A, B, C, D) = \sum m(1, 3, 7, 11, 15) + \sum d(0, 2, 5)$
   And realize it using minimum number of NAND gates.

   c) Perform the following decimal additions in the 8421 code. (2)
   i) 23.2 + 88.4

3. a) Design a 4 bit look-ahead carry adder and explain how does the look-ahead carry adder speed up the addition process. (5)

   b) Design a 1 line to 4 line Demultiplexer and write it's truth table. What is it's application. (5)

4. a) Design a 4 bit parallel-in serial-out (PISO) shift register using D FFs. (4)

   b) Design a Mod-6 synchronous counter using T FFs. (4)
   c) Design a 3 bit Ring counter. (2)

5. a) Convert D FF to T FF and J-K FF to D FF. (5)

b) Describe the operation of the 555 astable multivibrator with proper logic diagram. (5)
Calculate the frequency and duty cycle of the astable multivibrator output for C=0.01 μF, R_A = 10 KΩ, R_B = 50kΩ.

6. a) Explain the working of two-input TTL NAND gate with totem-pole out put. Write it's advantage and disadvantage. (5)

b) With the help of a neat diagram explain the working of a flash-type ADC. (5)

7. a) Show the difference between Moore circuit and Mealy circuit. Draw the state diagram and the state table for a Mealy type sequence detector to detect the sequence 1011 and also draw the logic diagram of the sequence detector using D FFs. (6)

b) Design a full subtractor using (4)
i) Decoder
ii) Multiplexer

8. Write short notes on any TWO (2x5)

a) PAL and PLA

b) RAM & ROM

c) State diagram and State table

d) 3 bit ripple up counter

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