

Question 1 [1 x10]

(a)	Consider a register R1 contains a value 10111000 and R2 contains 10110010. What will be the value of carry , zero and overflow flags after the execution of the instruction ADD R1, R2 // R2 is the destination
(b)	A processor has 48 distinct instructions and 28 general purpose registers. A 32-bit instruction word has an opcode, two register operands and an immediate operand. Assuming that the immediate operand is an signed integer, what is the maximum value of the immediate operand?
(c)	What is the use of Y and Z register in single bus CPU organization?
(d)	A RAM chip has 8 address lines, 8 data lines and 2 chip select lines.What will be the total number of memory locations?
(e)	Explain the role of dirty bit in write-back cache protocol.
(f)	There are p input lines q output lines for a decoder that is used to uniquely address a byte addressable 2KB RAM. What is the minimum value of p+q?
(g)	The interleaved memory system is divided into 8 number of memory modules. Each module consists of 64 words. The consecutive words are located in consecutive modules. Give the layout of memory address showing the address in module and the module fields.
(h)	Represent $-(200)_{10}$ into IEEE-754 single precision floating point format.
(i)	Performs two time arithmetic shift right operation on: 10101
(j)	What is vectored interrupt technique?

QUESTION 1 ANSWER

Date: _____

① @ $R_1 = 10111000$
 $R_2 = 10110010$
 Add $R_1, R_2: R_2 \leftarrow R_2 + R_1$

$$\begin{array}{r} 10110010 \\ + 10111000 \\ \hline 101101010 \end{array}$$

carry = 1
 zero = 0
 overflow = 1

②

OPCode	R ₁	R ₂	Imm
6	5	5	16

maximum value
 $= 2^{15} - 1$
 $= 32767$

$48 \leq 2^6$
 $28 \leq 2^5$

Imm = $32 - 16 = 16$

-2^{n-1} to $2^{n-1} - 1$
 -2^{15} to $2^{15} - 1$

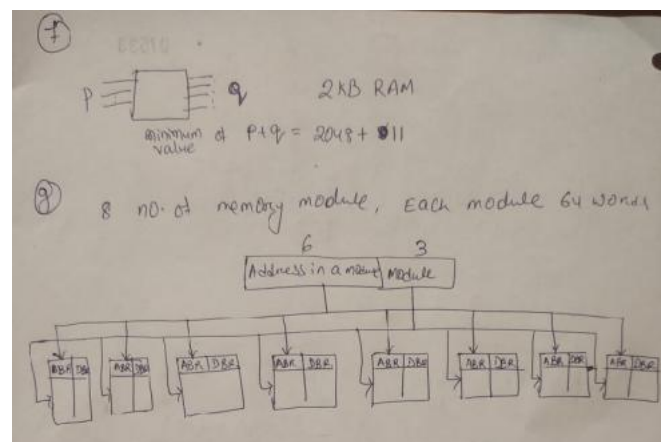
③ Y is used to store temporary value that will be input to ALU. Z is used to store temporary value that will be output of ALU.

④ RAM chip $\begin{cases} 8 \text{ Address lines} \\ 8 \text{ data lines} \end{cases}$ RAM size = 2^8 memory loc.

2 chip select lines \Rightarrow that means two RAM are there

$2 \times 2^8 = 2^9 = 512$ memory locations.

⑤ Dirty bit $\begin{cases} 1 \text{ when code block is updated} \\ \text{(MM block content \& CM block content are inconsistent)} \\ 0 \text{ when cache block is not updated} \\ \text{(MM block content \& CM block content)} \end{cases}$



H) S = 1, E' = 1000 0110, M = 100 10000 (23 bits)

(i) 10101
 $\rightarrow 11010$
 $\rightarrow 11101$

(j) vector interrupt is a processing technique in which the interrupting device directs the processor to the appropriate interrupt service routine.

⑦

2KB RAM

minimum of $P+Q = 2048 + 11$

⑧ 8 no. of memory module, Each module 64 words

Address in a module

6 3

⑨

$-200 = 100111000$
 $= 1.00111100 \times 2^8$
 $E = 8$
 $E' = 127 + E = 127 + 8 = 135 = 10000111$

$S = 1$
 $E' = 10000111$
 $M = 00111$

$-256 + 56 = -200$
 -256
 $+56$
 -200

(i) 10101
 $\rightarrow 11010$
 $\rightarrow 11101$

(j) Vector interrupt is a processing technique in which the interrupting device directs the processor to the appropriate interrupt service routine.

2.	<p>(a) Write the assembly code to evaluate the following arithmetic expression:</p> $Z = (P - Q + R) * (S / T * U) / V$ <p>i) Using an accumulator type computer with one address instructions. ii) Using a stack organized computer with zero-address operation instructions. iii) Using RISC computer instruction format.</p> <p>Evaluation Scheme: If one part is correct then give two marks. If two parts are correct then give three marks. If all parts are correct then full marks(4) will be awarded.</p>	[4]
	<p>(b) Explain the following addressing modes with examples:</p> <p>i. Relative mode ii. Immediate mode ii. Memory indirect mode iv. Autoincrement mode.</p> <p>Evaluation Scheme: Each part carries one mark.</p>	[4]

QUESTION 2 ANSWER

section-B

$$② Z = (P - Q + R) \div (S / T * U) / V$$

$$= \frac{PQ - R + ST / U * V}{V}$$

(i) using Accumulator

Load P
Sub Q
Add R
Store R1
Load S
Div T
Mul U
Mul R1
Div V
Store Z

(ii) using stack

Push P
Push Q
Sub
Push R
Add
Push S
Push T
Div
Push U
Mul
Mul
Push V
Div
POP Z

(iii) RISC

Load P, R1
Load Q, R2
Load R, R3
Load S, R4
Load T, R5
Load U, R6
Load V, R7
Sub R1, R2, R3
Add R5, R3, R4
Div R4, R5, R10
Mul R10, R6, R11
Mul R9, R11, R12
Div R12, R7, R13
Store R13, Z

③ (i) Relative mode

$$X(PC) \Rightarrow E \cdot A = X + PC$$

This mode is used to specify the target address in branch instruction.

1000: Branch > 0 100
1004: Next instr

$$PC = 1004 + 100 = 1104$$

(ii) Immediate mode

→ In this mode, operand is given explicitly.

MOV #100, R1 : R1 ← 100

(iii) Memory indirect mode

→ In this mode, the effective address of the operand is the content of a memory location.

MOV (1000), R0

$$E \cdot A = M[1000]$$

$$R0 \leftarrow M[M[1000]]$$

(iv) Autoincrement mode

→ In this mode, the effective address of the operand is the content of a register in the instruction.

(Ri) + EX: MOV (R1) +, R2 : EA = R1

$$: R2 \leftarrow M[R1]$$

$$R1 \leftarrow R1 + 4$$

3.	(a)	Write the sequence of control steps for the following instructions for multi bus CPU organization AND R2, (R1) // $R_2 \leftarrow [R_1] + R_2$ MUL R1, NUM // R1 the destination Evaluation Scheme: Each part carries two marks. Here step marks may be awarded appropriately.	[4]
	(b)	Explain the following instructions with example: i. LOAD ii. EI iii. Compare iv. CALL Evaluation Scheme: Each part carries 0.5 mark. [0.5 x 4] Explain the working principle of Hardwired control unit design along with neat diagram. [2 mark] Evaluation Scheme: Diagram [1 mark], theory[1 mark]	[4]

QUESTION 3 ANSWER

③ (a) AND $R_2, (R_1) : R_2 \leftarrow [R_1] + R_2$

(i) PCout, R=B, MARin, Read, IncPC
(ii) WMFC
(iii) MDRowdB, R=B, IRin
(iv) R_1 outB, R=B, MARin, Read
(v) WMFC
(vi) MDRowdB, R2 outA, select A, Add, R2 in, End.

MUL R_1, NUM // R_1 is the destination
 $R_1 \leftarrow M[NUM]$

(i) PCout, R=B, MARin, Read, IncPC
(ii) WMFC
(iii) MDRowdB, R=B, IRin
(iv) offset-field-of-IRoutA, select A, R=A, MARin, Read
(v) WMFC
(vi) MDRowdB, R=B, R1 in, End.

③ ⑥

(i) Load R_1 : ~~Accumulator content~~ will be loaded by the content of R_1
 $ACC \leftarrow R_1$

(ii) EI : Enable Interrupt

(iii) Compare SRC, dest : $\frac{dest - SRC}{}$
 According to its value the flag will set.

(iv) CALL 1000 : It is an ~~unconditional~~ branch instr.
 Relative: $PC = PC + 1000$
 Absolute: $PC = 1000$

4.	(a)	A processor has 32 integer registers and 16 floating point registers. It uses 16-bit instruction format. It has two types of instructions: Type-I and Type-II. Each Type-I instruction contains an opcode, an integer register and a 4-bit immediate value. Each Type-II instruction contains an opcode and two floating point register and one integer register. If there are 48 distinct Type-I opcodes, then what is the maximum number of distinct Type-II opcodes possible?	[4]
	(b)	Write the micro routine for the following instruction. Assume second operand is the destination. I. ADD 50(R1), R2 II. MUL (R3)+, R4 Evaluation Scheme: Each part carries two marks. Here step marks may be awarded appropriately.	[4]

QUESTION 4 ANSWER

④ ⑥

32 integer Reg $\rightarrow 5$ bits.
 16 float pt. Reg $\rightarrow 4$ bit
 Instrⁿ Size = 2 byte = 16 bits

Type-I

Opcode	Int. Reg	4 bit imm
7	5	4

Type-II

Opcode	FP Reg ₁	FP Reg ₂	Int Reg
3	4	4	5

1 Type-II instrⁿ contains 2^4 Type-I
 $= 16$ Type-I

3 Type-II instrⁿ contains \leftarrow 48 Type-I

Total ~~max~~ max no. of instrⁿ in Type-II = $2^3 = 8$
 NO. of Type-II instrⁿ Exist = $8 - 3 = 5$

46) Micro routine using single bus

(I) Add 50(R₁), R₂ : $R_2 \leftarrow R_2 + M[50 + R_1]$

(i) PCout, MARin, Read, select 4, Add, Zin

(ii) Zout, PCin, WMFC

(iii) MDRow, IRin

(iv) offset-field-of-IRow, Yin

(v) R₁out, select Y, Add, Zin

(vi) Zout, MARin, Read

(vii) R₂out, Yin, WMFC

(viii) MDRow, select Y, Add, Zin

(ix) Zout, R₂in, End.

	PCout	PCin	MARin	Read	MDRow	IRin	Yin	Select	Add	Zin	Zout	R ₁ out	R ₂ out	R ₂ in	WMFC	Read	End	offset-Row
I	1	0	1	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0
II	0	1	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0
III	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1
IV	0	0	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0
V	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
VI	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
VII	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
VIII	0	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	1	0
IX	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0

II. MUL (R₃)t, R₄ : $R_4 \leftarrow R_4 \times M[R_3]$
 $R_3 \leftarrow R_3 + 4$

(i) PCout, MARin, Read, select 4, Add, Zin

(ii) Zout, PCin, Yin, WMFC

(iii) MDRow, IRin

(iv) R₃out, MARin, Read

(v) R₄out, Yin, WMFC

(vi) MDRow, select Y, Mult, Zin

(vii) Zout, R₄in

(viii) R₃out, select 4, Add, Zin

(ix) Zout, R₃in, End.

	PCout	PCin	MARin	Read	MDRow	IRin	Yin	Select	Add	Zin	Zout	R ₃ out	R ₄ out	R ₄ in	WMFC	Read	End	offset-Row
I	1	0	1	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0
II	0	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
III	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
IV	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
V	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
VI	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
VII	0	0	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0
VIII	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
IX	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0

5.	(a)	<p>Assume a program consists of 64 pages and a computer has 32 frames in memory. A page consists of 4K words and memory is word addressable. Currently, page 0 is in frame 20, page 6 is in frame 12, page 7 is in frame 31 and page 9 is in frame 28. No other pages are in memory, i.e., only page number 0, 6, 7 and 9 are there in the memory. Translate the following logical addresses into the physical addresses.</p> <p>I. 00 1001 0100 1111 0000</p> <p>II. 00 0110 0010 0011 0100</p> <p>Evaluation Scheme: Each part carries two marks.</p>	[4]
	(b)	<p>A computer uses RAM chips of 128 X 4 capacity. Design a memory capacity of 1K X 16 by using available chips.</p> <p>Evaluation Scheme: Here step marks may be awarded appropriately.</p>	[4]

QUESTION 5 ANSWER

⑤ ② program 4 pages, 32 frames in memory. , Page size = 4K words = 2^{12}

0	20
6	12
7	31
8	
9	28

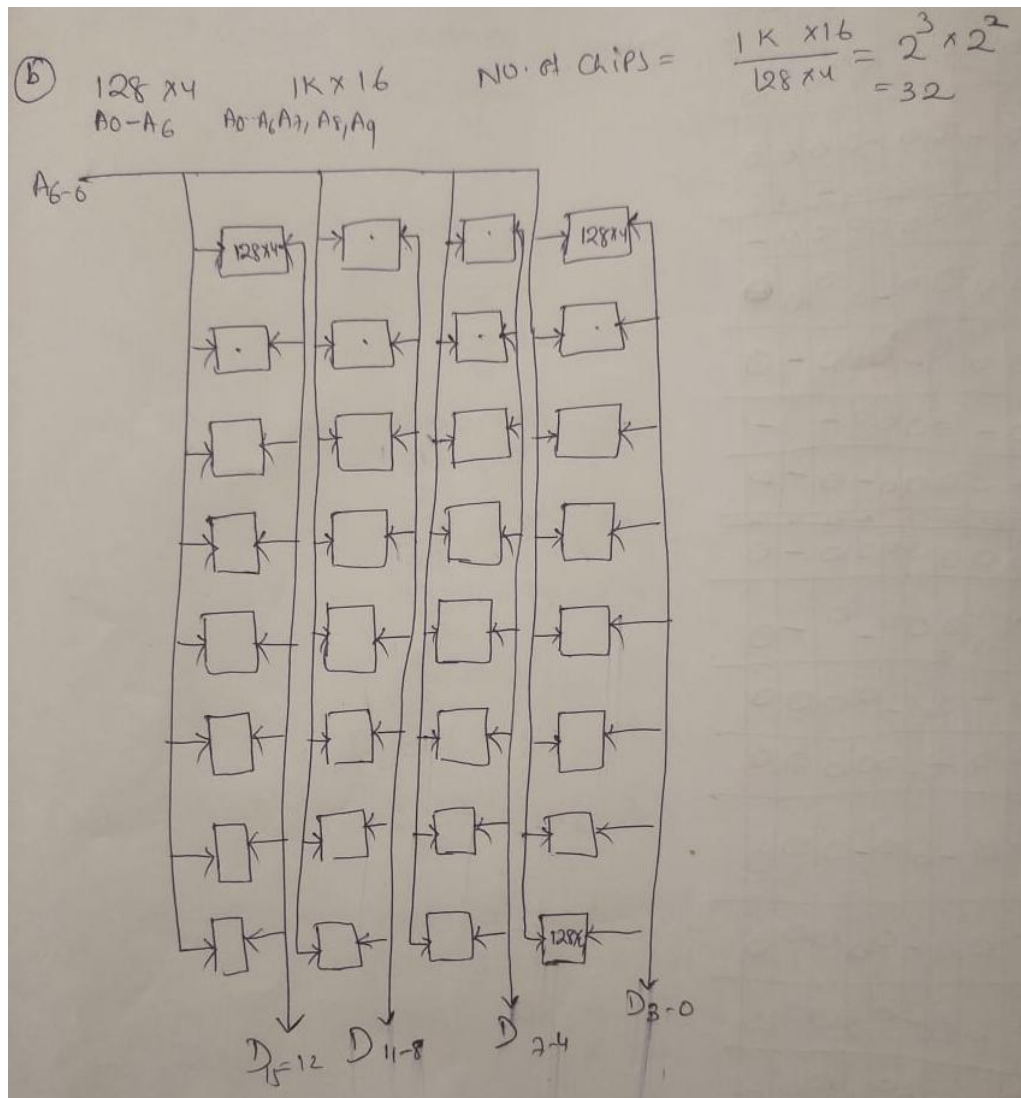
Translate logical address to physical address

I. $\boxed{00\ 1001\ 0100\ 1111\ 0000} \Rightarrow \begin{array}{c|c} 28 & \\ \hline 11100 & 0100\ 1111\ 0000 \\ \hline \text{Frame no.} & \text{offset} \end{array}$

Page 20 = 9 $\Rightarrow 28$

II. $\boxed{00\ 0110\ 0010\ 0011\ 0100} \Rightarrow \begin{array}{c|c} & \\ \hline 01100 & 0010\ 0011\ 0100 \\ \hline 12 & \end{array}$

6



6.	<p>(a) A computer system uses 16-bit memory addresses. It has a 4K-byte cache organized in a 2-way set associative manner with 32 bytes per cache block. Assume that the size of each memory word is 1 byte.</p> <p>(I) Calculate the number of bits in each of the Tag, set, and word fields of the memory address.</p> <p>(II) When a program is executed, the processor reads data sequentially from the following word addresses:</p> <p style="text-align: center;">256, 270, 4352, 4365, 256, 4352</p> <p>All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.</p> <p>Evaluation Scheme: Here first part is 1 mark and second part is 3 marks. For each memory reference 0.5 will be awarded.</p> <p>[1+3]</p>	[4]
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	<p>(b) Consider a 4-way set associative mapped cache of size 1MB with block size 1 KB. There are 9 bits in the tag. Find the size of main memory and the size of the tag directory.</p> <p>What is the importance of valid bit with respect to cache coherence problem.</p> <p>Evaluation Scheme: Size of MM [1 mark] Size of tag directory [2 Marks] Valid bit [1 mark]</p>	[4]
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QUESTION 6 ANSWER

⑥

② 16 bit memory address. \Rightarrow MM size = $2^{16} = 64 \text{ K byte}$.
 cache size = 4K byte
 2 way set Association.
 1 block size = 32 bytes.
 1 word = 1 byte.

(I)

Tag	set	word
5	6	5

$\log_2(2^4) \quad \log_2 64 \quad \log_2 32$

(II)

MM word no.	MM block NO	
M 256 \rightarrow	$\frac{256}{32} = 8$	(M)
H 270 \rightarrow	$\frac{270}{32} = 8$	(H)
M 4352 \rightarrow	$\frac{4352}{32} = 136$	(M)
H 4365 \rightarrow	$\frac{4365}{32} = 136$	(H)
H 256 \rightarrow	$\frac{256}{32} = 8$	(H)
H 4352 \rightarrow	$\frac{4352}{32} = 136$	(H)

MAPS TO SET NO.
 $8 \% 64 = 8$
 fill one cache block

$136 \% 64 = 8$
 fill another cache block exist in that set

(b) 4 way set Associative mapped cache of size 1MB with block size 1 KB. 9 bits are Tag.
 CM size = 1MB, No. of cache blocks = $\frac{1 \text{ M}}{1 \text{ K}} = 2^{10}$
 No. of set = $\frac{2^{10}}{4} = 2^8$

Tag	set	word
9	8	10

MM size = $2^{(9+8+10)} = 2^{27} \text{ Byte} = 128 \text{ MB}$
 Size of tag directory = $9 \times 2^{10} = 9 \text{ K bits}$

Valid bit:

when cache contain a block of information but that content is not exist in main memory in that case valid bit will be set to 0.

7.	(a)	Perform the following division operation using non-restoring method. $14 \div 5$. Evaluation Scheme: Here step marks may be awarded appropriately.	[4]
	(b)	Multiply $(-13) \times 12$ using Booth's algorithm. Evaluation Scheme: Here step marks may be awarded appropriately.	[4]

QUESTION 7 ANSWER

⑦ @ $14 \div 5$ by Non restoring

$M = 5 = 0101$ $-M = -5 = 1011$, $Q = 1110$

Initialization	A	Q
	0000	1110
Left shift	0001	110□
Sub M	$+ 1011$ 1100	110□
Left shift	1001	100□
Add M	$+ 0101$ 1110	100□
Left shift	1101	000□
Add M	$+ 0101$ 0010	000□
Left shift	0100	001□
Sub M	$+ 1011$ 1111	001□

Reminder = 1111
 $+ 0101$
~~0010~~
 = 4

Quotient = 0010
 = 2

⑦ ⑤ Multiply -13×12 using Booth's Algorithm
 $M = -13 = 10011$ $Q = 12 = 01100$
 $-M = +13 = 01101$

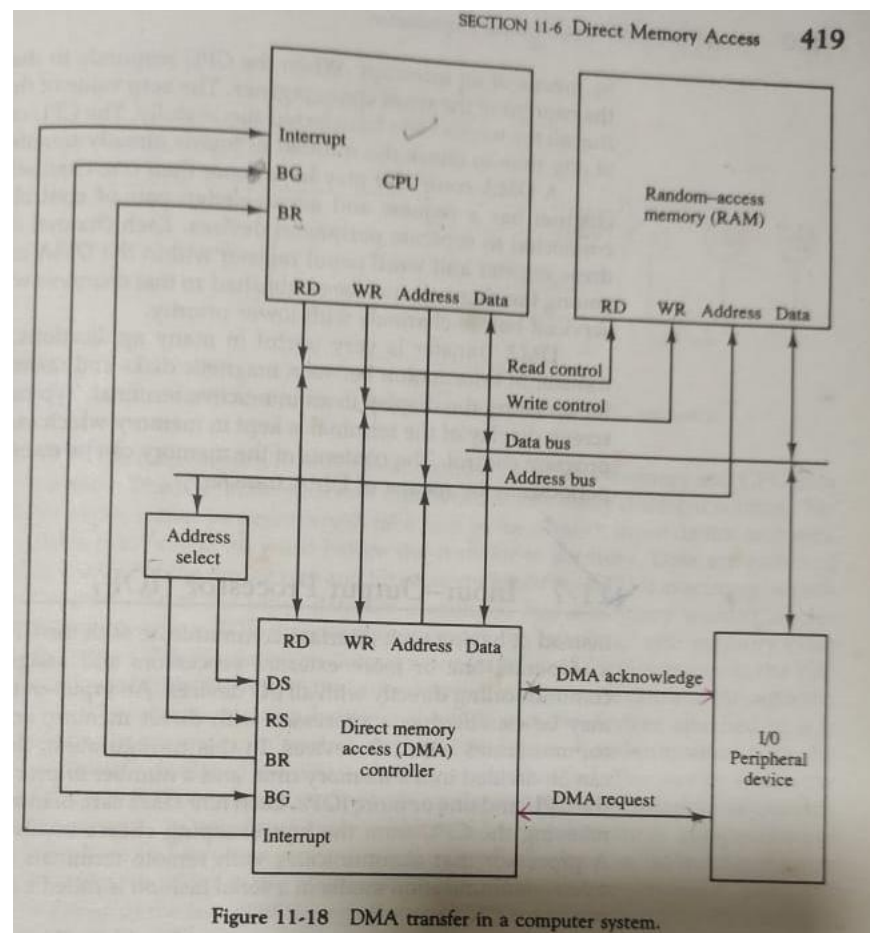
	A	Q	C
Initialization	00000	01100	0
NO OP A shift R	00000	00110	0 $\rightarrow C-1$
NO OP A shift R	00000	00011	0 $\rightarrow C-2$
Subm A + (-M)	+01101 01101	00011	0 $\rightarrow C-3$
A shift R	00110	10001	1
NO OP A shift R	00011	01000	1 $\rightarrow C-4$
Addm	+10011 10110	01000	1 $\rightarrow C-5$
A shift R	11011	00100	0
Result = 1101100100			
$= -256 + 64 + 32 + 4 = -156$			

8.	(a)	Explain the working principle of I/O transfer method that facilitates transfer of bulk data from hard disk to main memory with the highest throughput? Evaluation Scheme: Diagram [2 marks] Theory [2Marks]	[4]
	(b)	State how isolated I/O is different from memory mapped I/O. Explain nesting of interrupt requests. Evaluation Scheme: Difference [2 Marks] Nesting of interrupt request [2 Marks]	[4]

QUESTION 8 ANSWER

(a) DMA Transfer Technique

DMA controller can transfer a block of data from an external device to the processor, without any intervention from the processor. However, the operation of the DMA controller must be under the control of a program executed by the processor. That is, the processor must initiate the DMA transfer. To initiate the DMA transfer, the processor informs the DMA controller of: Starting address, Number of words in the block, Direction of transfer (I/O device to the memory, or memory to the I/O device). Once the DMA controller completes the DMA transfer, it informs the processor by raising an interrupt signal.



(b)

I/O Mapped I/O

Memory Mapped I/O

I/O Mapped I/O	Memory Mapped I/O
I/O device is treated as an I/O device and hence given an I/O address.	I/O device is treated like a memory device and hence given a memory address.
I/O device has an 8 or 16 bit I/O address.	I/O device has a 20 bit Memory address.
Decoding is easier due to lesser address lines	Decoding is more complex due to more address lines
Decoding is cheaper	Decoding is more expensive
Works faster due to less delays	More gates add more delays hence slower
Allows max $2^{16} = 65536$ I/O devices	Allows many more I/O devices as I/O addresses are now 20 bits.
I/O devices can only be accessed by IN and OUT instructions.	I/O devices can now be accessed using any memory instruction.