KIIT UNIVERSITY, BHUBANESWAR
AUTUMN MID SEMESTER EXAMINATION-2015
DIGITAL ELECTRONICS CIRCUITS
[EC-2009]

Full Mark: 25 **Duration: 2 Hrs.**

Answer any FIVE questions including question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. **[1x5]**

a) Perform the **BCD subtraction** (**476.7 – 297.8**)

b) Determine the decimal value of the signed binary number '101010' in i) Sign-Magnitude form ii) 1's Complement form and iii) 2's Complement form.

c) Show that, $\mathbf{U\,\overline{V} + U\,W + V\,\overline{W} = U + V\,\overline{W}}$ where U, V and W are Boolean variables

d) What is the Advantage of ***Look-Ahead Carry Adder***? Write the expression of $\mathbf{C_1, C_2, C_3, C_4}$ in terms of $\mathbf{C_0}$ and with proper $\mathbf{P_i}$ and $\mathbf{G_i}$.

e) Implement Half-Subtractor using 2:4 decoder (having active HIGH output lines) and one OR gate.

2. Obtain the minimized expression for the following 4-variable Boolean expression using **[5]** K-map method. Implement the minimized expression using ***minimum numbers of only NAND gates.***

$$\mathbf{F(P,Q,R,S) = \prod M\,(4,6,8,9,12,13,14)\,.\,d(1,3,7)}$$

3. a) Implement the below given Boolean function using a ***MULTIPLEXER having 3 Select lines.*** Given that, Apart from the given MUX, ***only NOT gate should be used*** (if required). No other Gates are allowed to be used. **[4]**

$$\mathbf{F(A,B,C,D)} = \bar{A}B + BC + B\bar{D}$$

b) Implement $F(A,B) = \overline{A \oplus B}$ ***using a single 4x1 MULTIPLEXER*.** **[1]**

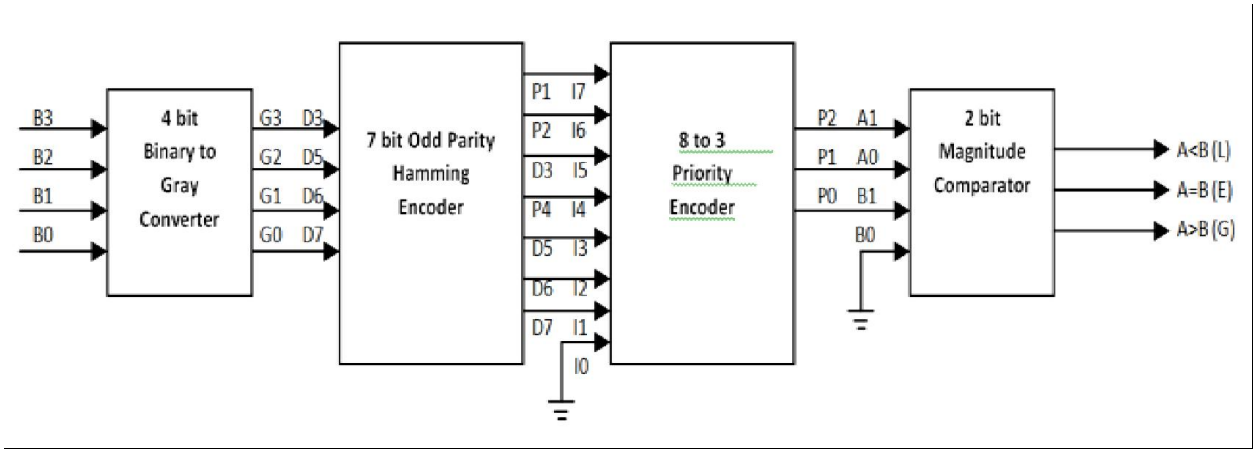
4. a) A nuclear reactor has 3 cooling FANS, The Reactor core is stable and temperature remain under control, if ***at least 2 FANs are ON***. Design a ALARM Digital Circuit , where ALARM will be triggered when less than 2 FANs are ON. Given that, inputs are ***FAN_1, FAN_2,FAN_3*** and Output is "***ALARM"*** using ***3-to-8 DECODER (ACTIVE LOW) and minimum number of 2-inputs UNIVERSAL GATES ONLY***. **[3]**

b) What is 1-bit Magnitude Comparator? Write down the input and output table and Boolean function of each outputs. Draw the 1-bit Magnitude comparator circuit ***using minimum number of 2 inputs NAND gates only.*** **[2]**

5. a) Design a ***2 bit Priority Encoder***; where the given order of the priorities for 4 inputs are ***D3 > D2 > D1 > D0.*** Draw the required table, solve the required K-Map and Obtain the Minimized Expression for Output ***A, B and V*** (VALID) and ***implement the circuit using required basic gates***. **[4]**

b) If the received ***7-bit Hamming code*** is '***1110100***' then find the 4-bit data word. **[1]**
[Assume ***(i) Even parity system, (ii) At most single bit error may take place***]

6. a) What will be the output for **L, E & G** respectively of the 2 bit magnitude Comparator from the Figure below ? Given that, **B3 = 1**; **B2 = 0**; **B1 = 1**; **B0 = 0** (***Given that, B3 MSB and B0 LSB***) and ***I7 > I6 > I5 > I4 > I3 > I2 > I1 > I0*** is the order of Priority of input for ***8 to 3 Priority Encoder*** and It's a ***ODD Parity Hamming Encoder***. ***(Explain Each Stage with proper input/output)*** **[4]**



b) Draw a ***2-bit ADDER/SUBTRACTOR*** using **2 FULL ADDER BLOCKS** and **2 XNOR gates**.*(Given that, Full Adder Block inputs are* $A_i B_i C_i$ *and Outputs are* $\sum_i , C_{i+1}$*; where "i" represents the number of FULL ADDER BLOCK.* ***Here 2 Full Adders So use i=0 ; i=1)***

(i) ONLY Draw the Circuit (No Explanation required) **[0.5]**

(ii) Condition of Control input (When it will work as an ADDER/ SUBTRACTOR) **[0.5]**

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