SPRING END SEMESTER EXAMINATION - 2019

COMPUTER ORGANIZATION AND ARCHITECTURE

1. (a) Defination of von-Neuman architecture. 1/2

Difference between von-Neuman and Harvard architecture 1/2

(b) R1 = 1200, R2 = 1300

(i) EA = 20 + 1300 = 1320 1/4

(ii) EA = 300 1/4

(iii) EA = 1200 1/4

(iv) EA = 1200 1/4

(c) Comparison between static RAM and Dynamic RAM

(Minimum two comparision) 1/2 + 1/2

(d) Difference between memory mapped I/O and I/O mapped I/O

(Minimum two difference) 1/2 + 1/2

(e) Instruction Decoder : 5 : 32 1/2

Step Decoder : 3 : 8 1/2

(f) c = 30 ns

m = 15 ns 1

Tavg = 42 ns

$T_{avg} = h * c + (1-h) * (c+m)$

$\Rightarrow 42 = h * 30 + (1-h) * 45$

$\Rightarrow h = 0.2$

(g) Register Name : Instruction pointer (IP) 1/2

Explanation 1/2

(h) Advantage of stack over link register — 1

(i)

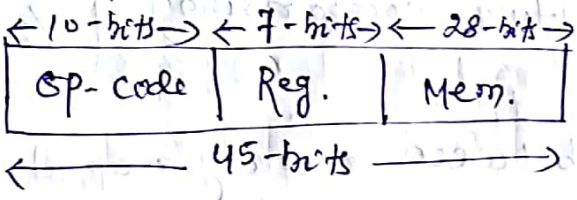
TAG	SET	BLOCK
19	5	6

1

(j) problem of polling process — 1½
vectored interrupt as solution — ½

SECTION - B

2. (a) Explanation of Relative Add. Mode — 1
Explanation of Auto Add. Mode — 1



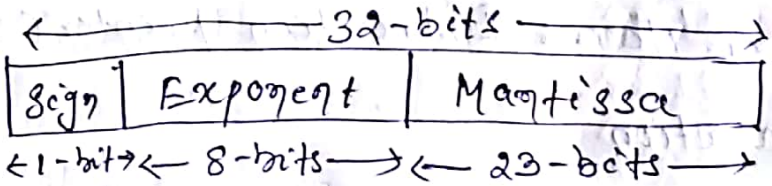
2

Total opcode possible = 2^{10}
No. of one Add. Inst^n. possible = $(2^{10} - 450) \times 2^7$

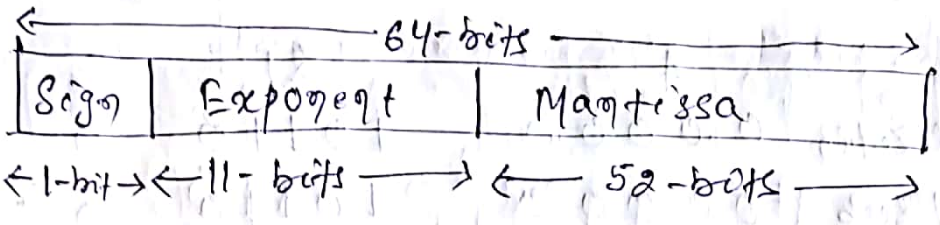
(b) RISC Instructions — 2
Stack Organization — 2

3. (a) Difference between RISC vs CISC — 4
Mention four comparisions. Each comparision carries one mark

(b) Single precision IEEE floating point number — 1



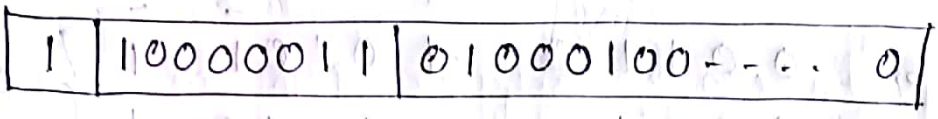
Double precision IEEE floating point number is 1



The binary value of −20.25 is 10100.01 2

The corresponding normalized value is 1.010001×2^4

The single precision floating point representation is



$E' - 127 = 4$

$\Rightarrow E' = 131 = 10000011$

SECTION-C

4.(a) Explanation of multi-bus CPU organization (including diagram) 2

The control sequence for the instruction 2
ADD #50, R1, R2 is

1. PCout, R=B, MARin, Read, IncPc
2. WMFC
3. MDRoutB, R=B, IRin
4. Offset-field-of-IRout, R1outB, SelectA, Add, R2in, End

(b) Definition of parallel processing 1

Flynn's classification (Explanation with diagram) 3

1. SISD
2. SIMD
3. MISD
4. MIMD

5. (a) $M = 10011$, $\bar{M}+1 = 01101$, $Q = 10110$ | 4

	A	Q	Q_0	
Initialization	00000	10110	0	
NO Add/Sub	00000	10110	0	} cycle-1
AshR	00000	01011	0	
SUB M	01101			
	01101	01011	0	} cycle-2
AshR	00110	10101	1	
NO Add/Sub	00110	10101	1	} cycle-3
AshR	00011	01010	1	
ADD M	10011			
	10110	01010	1	} cycle-4
AshR	11011	00101	0	
SUB M	01101			
	01000	00101	0	} cycle-5
AshR	00100	00010	1	

so, product = AQ = 10000010

5. (b) Defination of virtual memory | 1

Address translation mechanism with diagram | 3

6. (a) The control sequence for the instruction ADD (R1)+, R2 is as follows | 2

1. PCout, MARin, Read, Select 4, Add, Zin
2. Zout, PCin, Yin, WMFC
3. MDRout, IRin

4. $R1_{out}$, MAR_{in}, Read, Select 4, Add, Z_{in}

5. Z_{out}, $R1_{in}$, WMFC

6. $R2_{out}$, Y_{in}

7. MDR_{out}, Select Y, Add, Z_{in}

8. Z_{out}, $R2_{in}$, End

The corresponding microroutine for the aforesaid control sequence [2]

8 (b) Types of data transfer techniques [1]

Explanation of DMA (working principle) [3]

7 (a) Role of cache memory [1]

Use and types of mapping function [1]

Main memory size is 128K × 32 [2]

No. of Address line = 17.

Total cache has 2048 words

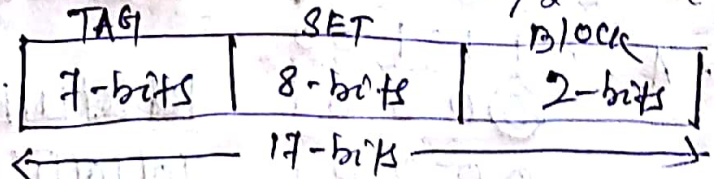
and a block size = 4 words

No. of blocks in cache = $\frac{2048}{4} = 512 = 2^9$

Two-way set-associative,

so, no. of sets = $2^9/2^1 = 2^8$

(i)



(ii) Tag = 7-bits

Size of cache with tag bits = 2048 × 32 + 512 × 7

= 69120 bits

where, cache size is 2048 words, each word is 32-bits, no. of blocks in cache is 512 and each block having tag of 7-bits.

7. (b) **Restoring Division** 2

Dividend = Q = 13 = 01101

Divisor = M = 4 = 00100 , $\bar{M}+1$ = 11100

operations	A	Q	
Initialization	00000	1101	
Left shift	00001	101	cycle-1
sub M from A	11100		
	(1)1101		
Restore	00100		
	00001	1010	
Left shift	00011	010	cycle-2
sub M from A	11100		
	(1)1111		
Restore	00100		
	00011	0100	
Left shift	00110	100	cycle-3
sub M from A	11100		
set q_0 = 1	(0)0010		
	00010	1001	
Left shift	00100	001	
sub M from A	11100		
	(0)0001		
	00001	0011	
	Remainder	Quotient	

Non-Restoring Division

[2]

Dividend = Q = 13 = 1101

Divisor = M = 4 = 00100, M+1 = 11100

operations	A	Q	
Initialization	00000	1101	
Left shift	00001	101□	cycle-1
Sub M from A	11100		
set q_0	11101	1010	
Left shift	11011	010□	cycle-2
Add M to A	00100		
set q_0	11111	0100	
Left shift	11110	100□	cycle-3
Add M to A	00100		
set q_0	00010	1001	
Left shift	00101	001□	
Sub M from A	11100		
	00001	0011	

Remainder Quotient

8. (a) $T_{avg} = [0.9 \times 1 + 0.1 \times 5] \times 160 + [0.9 \times 2 + 0.1 \times 10] \times 40$ [4]

$= 336$ ns

(b) No. of chips $= \frac{2M \times 32}{512K \times 8} = \frac{2^{21} \times 2^5}{2^{19} \times 2^3} = \frac{2^{26}}{2^{22}} = 2^4$ [4]

$= 16$ chips

No. of columns $= 32/8 = 4$

No. of rows $= 16/4 = 4$