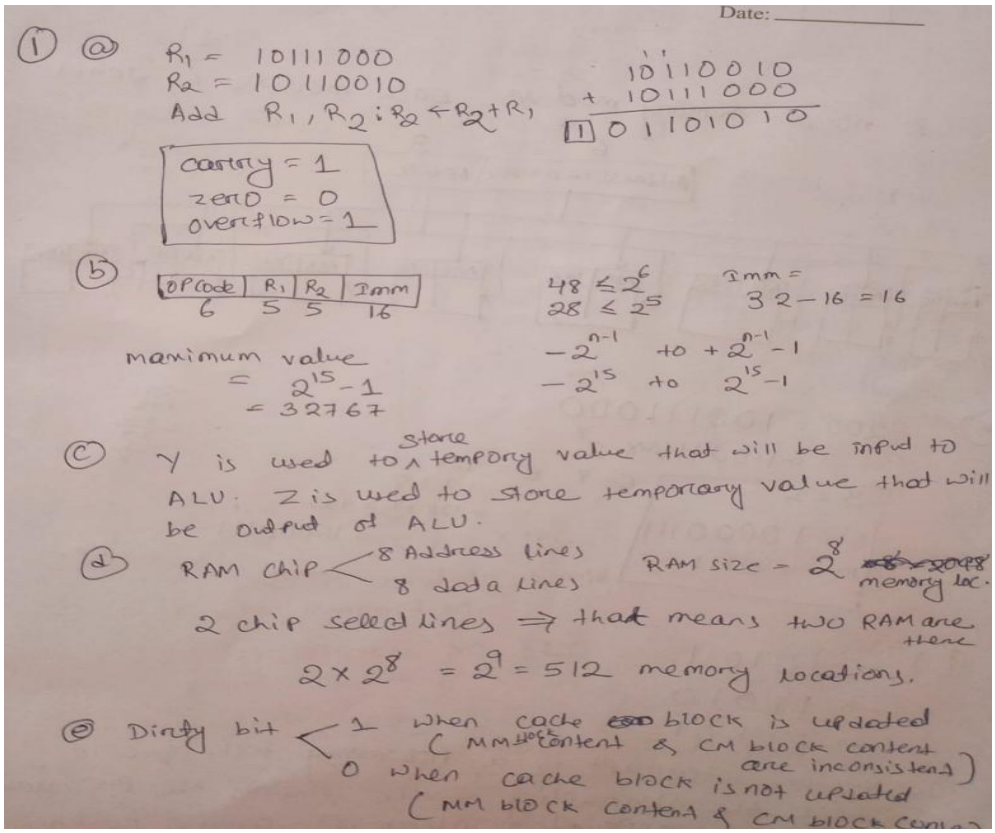
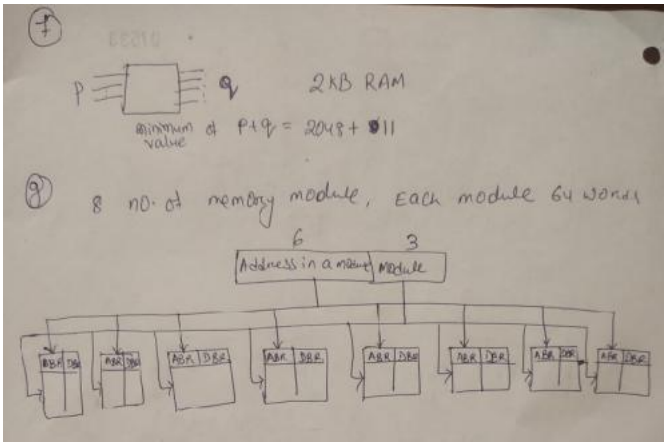
Question 1 [1 x10]

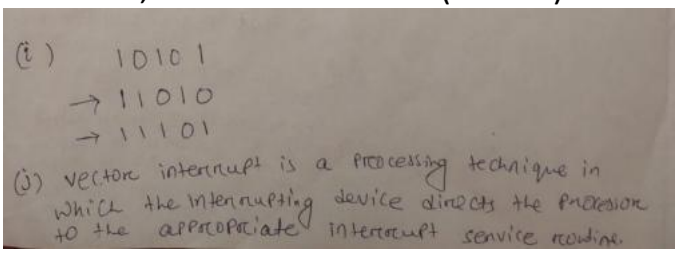
(a)	Consider a register R1 contains a value 10111000 and R2 contains 10110010. What will be the value of carry , zero and overflow flags after the execution of the instruction **ADD R1, R2** // R2 is the destination
(b)	A processor has 48 distinct instructions and 28 general purpose registers. A 32-bit instruction word has an opcode, two register operands and an immediate operand. Assuming that the immediate operand is an signed integer, what is the maximum value of the immediate operand?
(c)	What is the use of Y and Z register in single bus CPU organization?
(d)	A RAM chip has 8 address lines, 8 data lines and 2 chip select lines.What will be the total number of memory locations?
(e)	Explain the role of dirty bit in write-back cache protocol.
(f)	There are p input lines q output lines for a decoder that is used to uniquely address a byte addressable 2KB RAM. What is the minimum value of p+q?
(g)	The interleaved memory system is divided into 8 number of memory modules. Each module consists of 64 words. The consecutive words are located in consecutive modules. Give the layout of memory address showing the address in module and the module fields.
(h)	Represent $-(200)_{10}$ into IEEE-754 single precision floating point format.
(i)	Performs two time arithmetic shift right operation on: 10101
(j)	What is vectored interrupt technique?

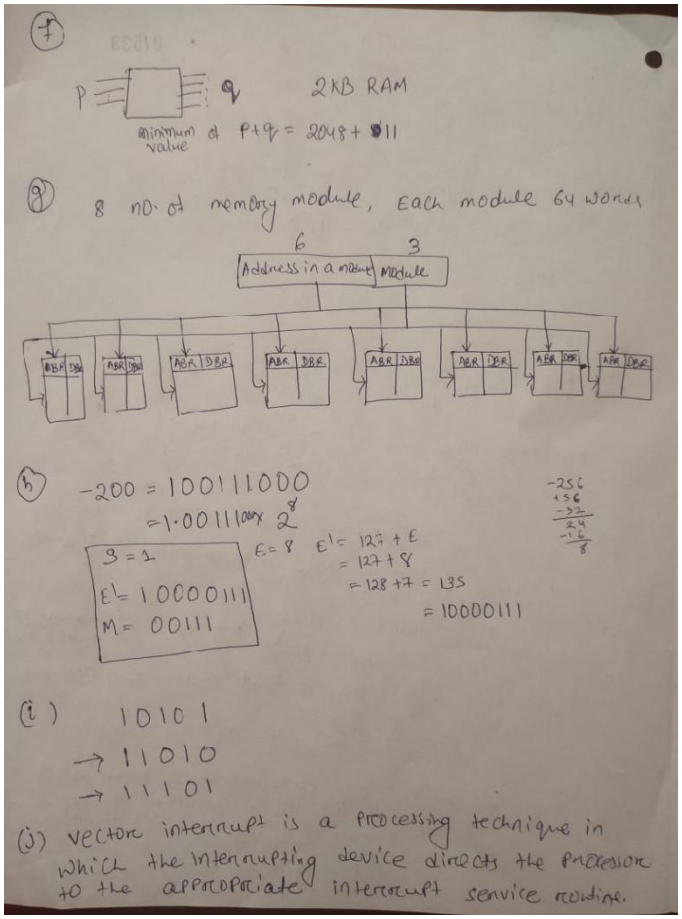
QUESTION 1 ANSWER





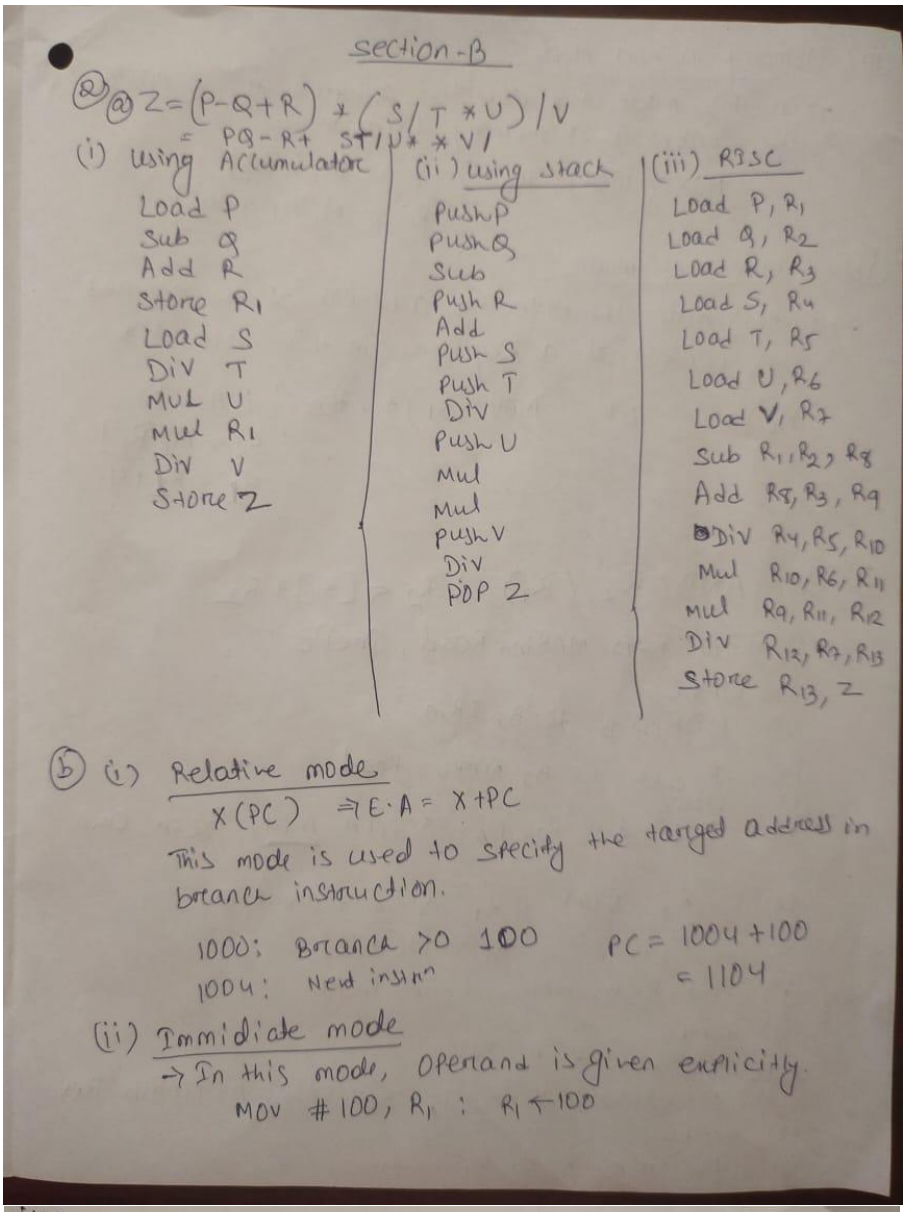
H) S = 1, E' = 1000 0110, M = 100 1000 ....0 (23 bits)





2.	(a)	Write the assembly code to evaluate the following arithmetic expression: $Z = (P - Q + R) * (S / T * U) / V$ i) Using an accumulator type computer with one address instructions. ii) Using a stack organized computer with zero-address operation instructions. iii) Using RISC computer instruction format. Evaluation Scheme: If one part is correct then give two marks. If two parts are correct then give three marks. If all parts are correct then full marks(4) will be awarded.	[4]
	(b)	Explain the following addressing modes with examples: i. Relative mode ii. Immediate mode ii. Memory indirect mode iv. Autoincrement mode. Evaluation Scheme: Each part carries one mark.	[4]

QUESTION 2 ANSWER



Section-B

(2) (a) $Z=(P-Q+R)*(S/T*U)/V$

$= PQ-R+ ST/U**V/$

(i) Using Accumulator

```
Load P
Sub Q
Add R
Store R1
Load S
Div T
MUL U
Mul R1
Div V
Store Z
```

(ii) using stack

```
Push P
Push Q
Sub
Push R
Add
Push S
Push T
Div
Push U
Mul
Mul
Push V
Div
POP Z
```

(iii) RISC

```
Load P, R1
Load Q, R2
Load R, R3
Load S, R4
Load T, R5
Load U, R6
Load V, R7
Sub R1, R2, R8
Add R8, R3, R9
Div R4, R5, R10
Mul R10, R6, R11
Mul R9, R11, R12
Div R12, R7, R13
Store R13, Z
```

(b) (i) Relative mode

$X(PC) \Rightarrow E.A = X+PC$

This mode is used to specify the targeted address in branch instruction.

1000: Branch >0 100 PC = 1004 + 100

1004: Next instn = 1104

(ii) Immidiate mode

→ In this mode, Operand is given explicitly.

MOV #100, R_1 : $R_1 \leftarrow 100$

(iii) Memory indirect mode

→ In this mode, the effective address of the operand is the content of a memory location.

MOV (1000), R_0 $E.A = M[1000]$

$R_0 \leftarrow M[M[1000]]$

(iv) Autoincrement mode

→ In this mode, the effective address of the operand is the content of a Register in the instruction.

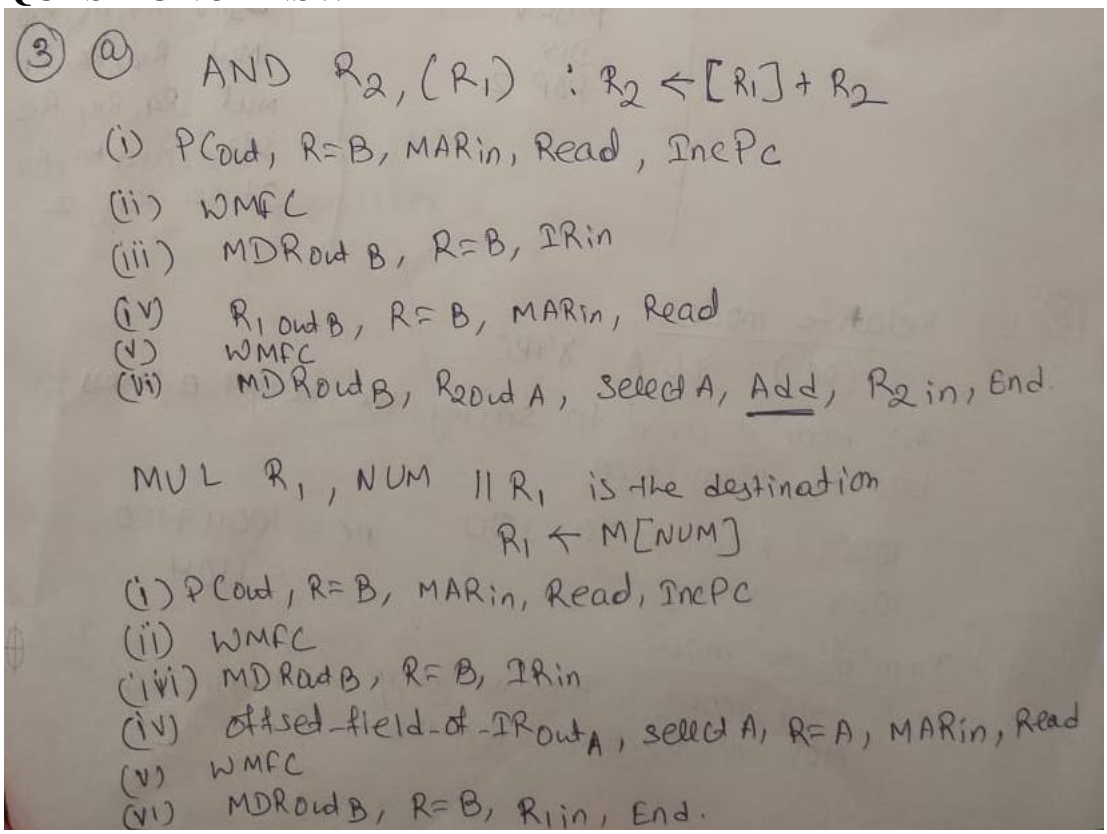
$(R_i)+$ Ex: MOV $(R_1)+, R_2$: $EA = R_1$

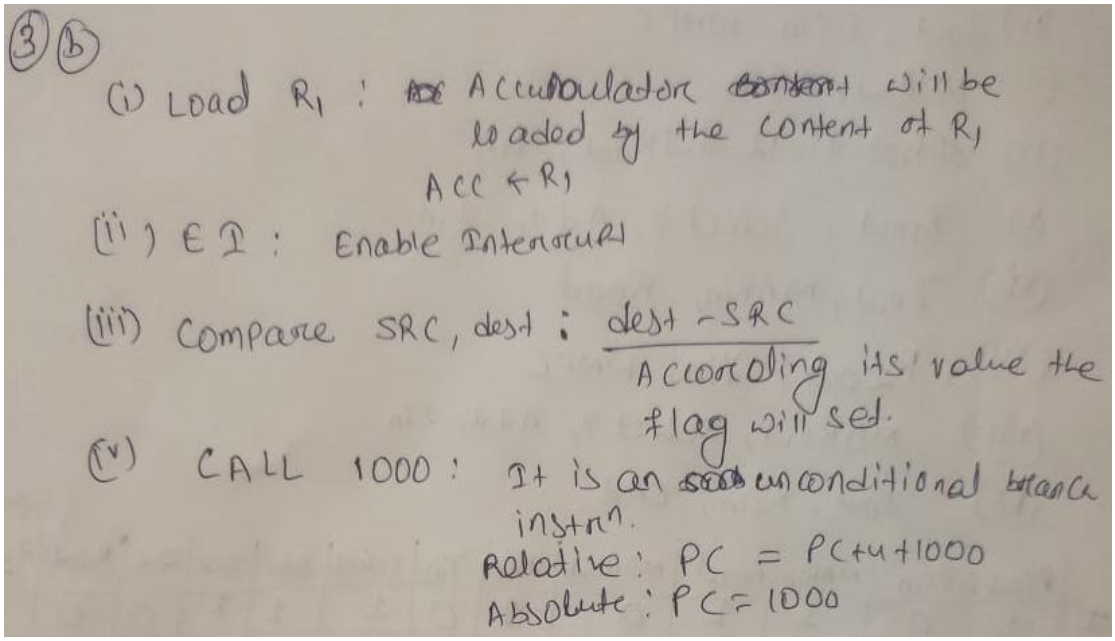
: $R_2 \leftarrow M[R_1]$

$R_1 \leftarrow R_1 + 4$

3.	(a)	Write the sequence of control steps for the following instructions for **multi bus** CPU organization AND R2, (R1) // R2←[R1]+R2 MUL R1, NUM //R1 the destination Evaluation Scheme: Each part carries two marks. Here step marks may be awarded appropriately.	[4]
	(b)	Explain the following instructions with example: i. LOAD ii. EI iii. Compare iv. CALL Evaluation Scheme: Each part carries 0.5 mark. [0.5 x 4] Explain the working principle of Hardwired control unit design along with neat diagram. [2 mark] Evaluation Scheme: Diagram [1 mark], theory[1 mark]	[4]

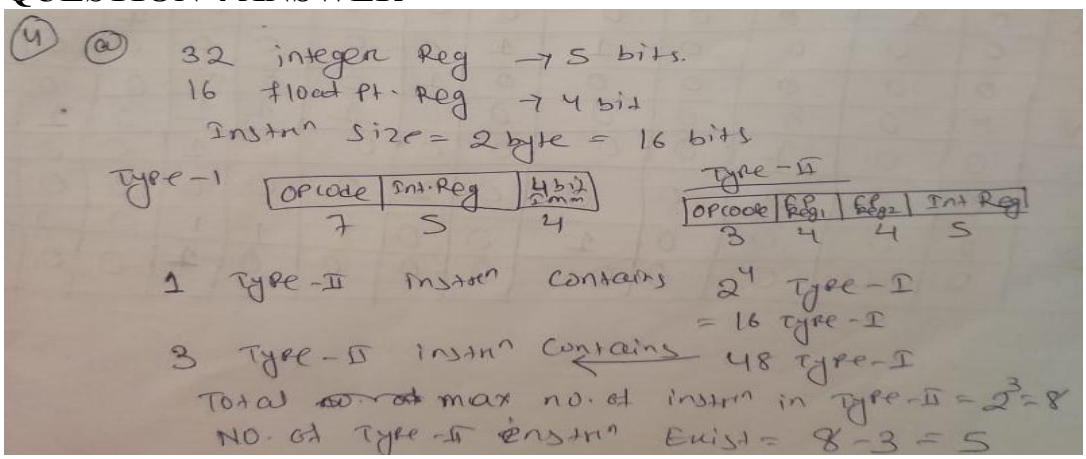
QUESTION 3 ANSWER





4.	(a)	A processor has 32 integer registers and 16 floating point registers. It uses 16-bit instruction format. It has two types of instructions: Type-I and Type-II. Each Type-I instruction contains an opcode, an integer register and a 4-bit immediate value. Each Type-II instruction contains an opcode and two floating point register and one integer register. If there are 48 distinct Type-I opcodes, then what is the maximum number of distinct Type-II opcodes possible?	[4]
	(b)	Write the micro routine for the following instruction. Assume second operand is the destination. I. ADD 50(R1), R2 II. MUL (R3)+, R4 Evaluation Scheme: Each part carries two marks. Here step marks may be awarded appropriately.	[4]

QUESTION 4 ANSWER



(4b) Micro routine using single bus

(I) Add 50(R1), R2 : R2 ← R2 + M[50+R1]

(i) PCout, MARin, Read, Select 4, Add, Zin

(ii) Zout, PCin, WMFC

(iii) MDRout, IRin

(iv) offset-field-of-IRout, Yin

(v) R1out, Select Y, Add, Zin

(vi) Zout, MARin, Read

(vii) R2out, Yin, WMFC

(viii) MDRout, Select Y, Add, Zin

(ix) Zout, R2in, End.

	PCout	PCin	MARin	Read	MDRout	IRin	Yin	Select	Add	Zin	Zout	R1out	R2out	R2in	WMFC	Read	End	offset-field
I	1	0	1	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0
II	0	1	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0
III	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
IV	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1
V	0	0	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0
VI	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
VII	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0
VIII	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0
IX	0	0	0	0	1	0	0	1	0	0	1	0	0	0	1	0	1	0

II. MUL (R3)+, R4 : R4 ← R4 * M[R3]
R3 ← R3 + 4

(i) PCout, MARin, Read, Select 4, Add, Zin

(ii) Zout, PCin, Yin, WMFC

(iii) MDRout, IRin

(iv) R3out, MARin, Read

(v) R4out, Yin, WMFC

(vi) MDRout, Select Y, Mult, Zin

(vii) Zout, R4in

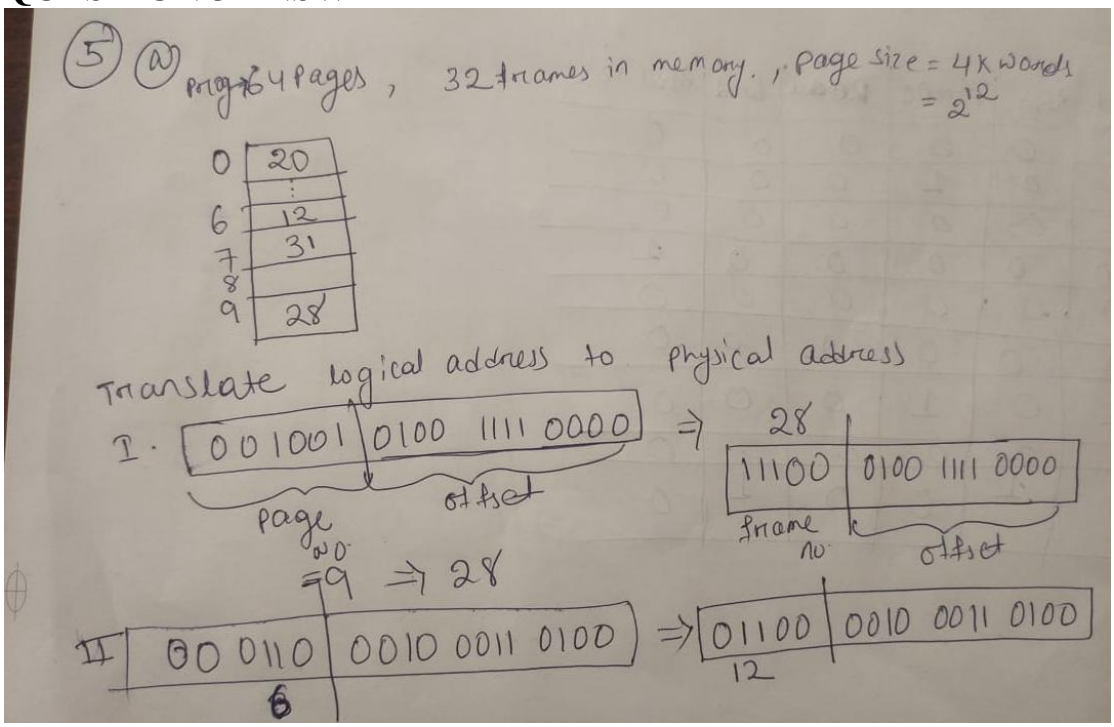
(viii) R3out, Select 4, Add, Zin

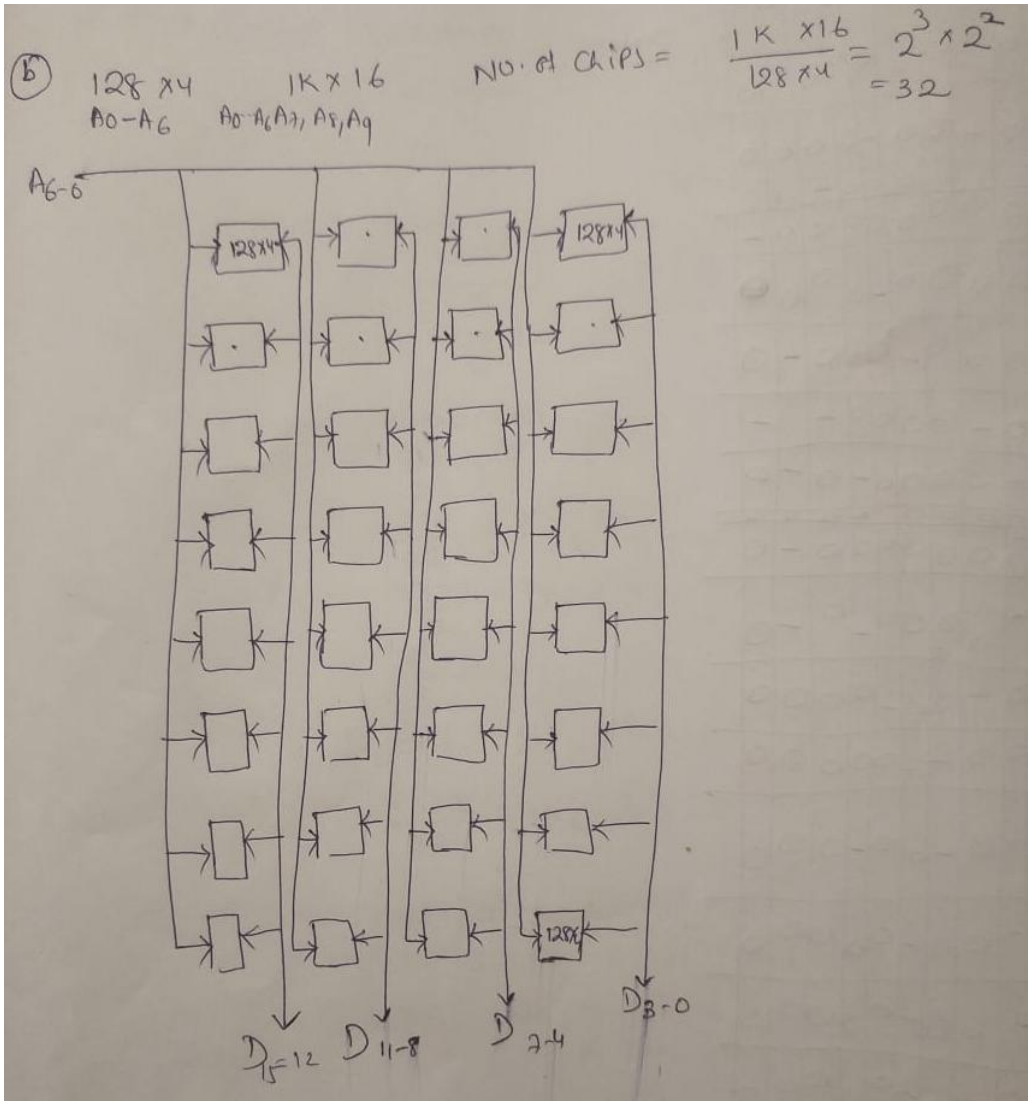
(ix) Zout, R3in, End.

	PCout	PCin	MARin	Read	MDRout	IRin	Yin	Select	Add	Zin	Zout	R3out	R4out	R3in	WMFC	Read	End	offset-field
I	1	0	1	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0
II	0	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
III	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
IV	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
V	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0
VI	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	0	0
VII	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0
VIII	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0
IX	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0

5.	(a)	Assume a program consists of 64 pages and a computer has 32 frames in memory. A page consists of 4K words and memory is word addressable. Currently, page 0 is in frame 20, page 6 is in frame 12 , page 7 is in frame 31 and page 9 is in frame 28. No other pages are in memory, i.e., only page number 0, 6, 7 and 9 are there in the memory. Translate the following logical addresses into the physical addresses. I. 00 1001 0100 1111 0000 II. 00 0110 0010 0011 0100 Evaluation Scheme: Each part carries two marks.	[4]
	(b)	A computer uses RAM chips of 128 X 4 capacity. Design a memory capacity of 1K X 16 by using available chips. Evaluation Scheme: Here step marks may be awarded appropriately.	[4]

QUESTION 5 ANSWER

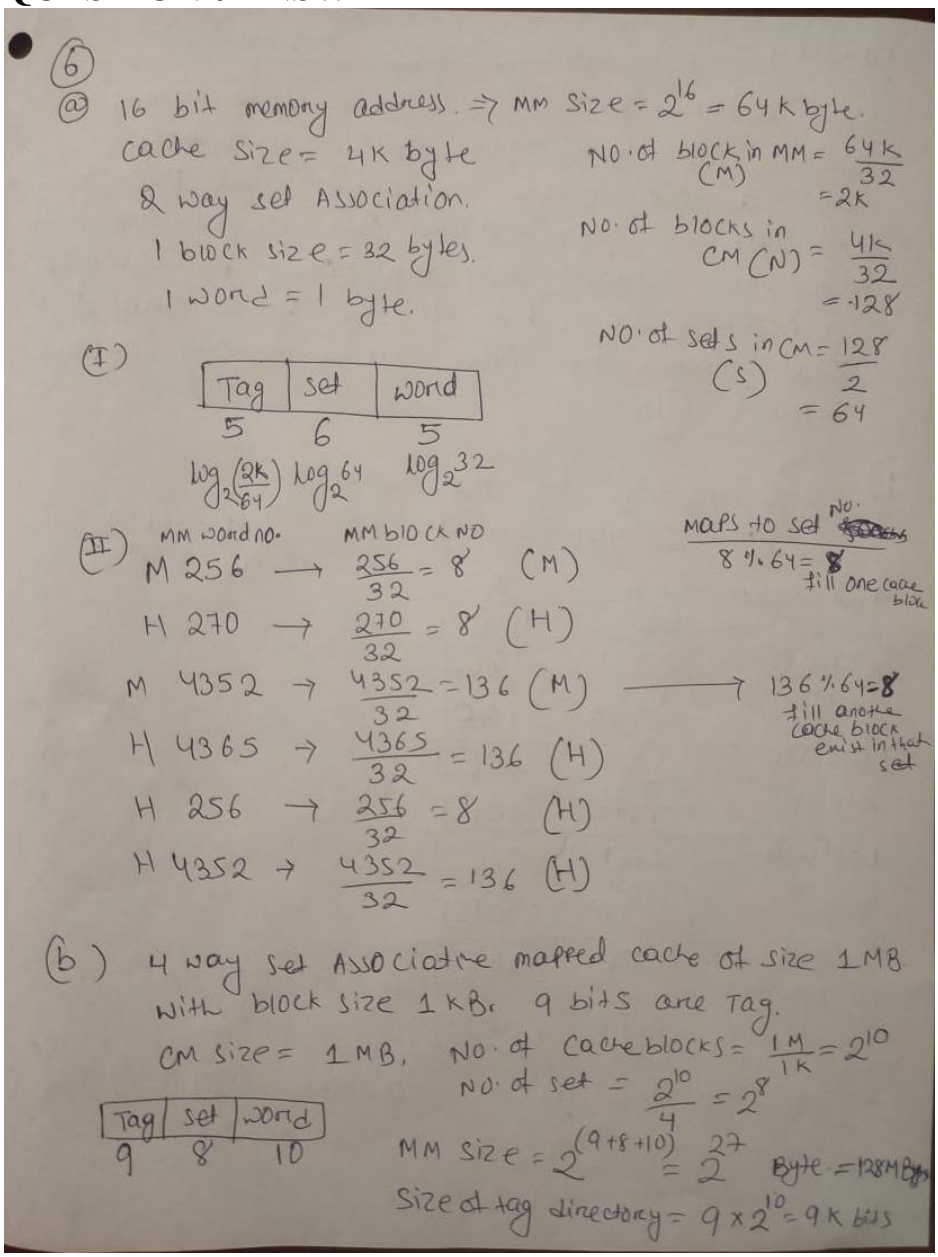




6.	(a)	A computer system uses 16-bit memory addresses. It has a 4K-byte cache organized in a 2-way set associative manner with 32 bytes per cache block. Assume that the size of each memory word is 1 byte. (I) Calculate the number of bits in each of the Tag, set, and word fields of the memory address. (II) When a program is executed, the processor reads data sequentially from the following word addresses: 256, 270, 4352, 4365, 256, 4352 All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss. Evaluation Scheme: Here first part is 1 mark and second part is 3 marks. For each memory reference 0.5 will be awarded. [1+3]	[4]

	(b)	Consider a 4-way set associative mapped cache of size 1MB with block size 1 KB. There are 9 bits in the tag. Find the size of main memory and the size of the tag directory. What is the importance of valid bit with respect to cache coherence problem. Evaluation Scheme: Size of MM [1 mark] Size of tag directory [2 Marks] Valid bit [1 mark]	[4]

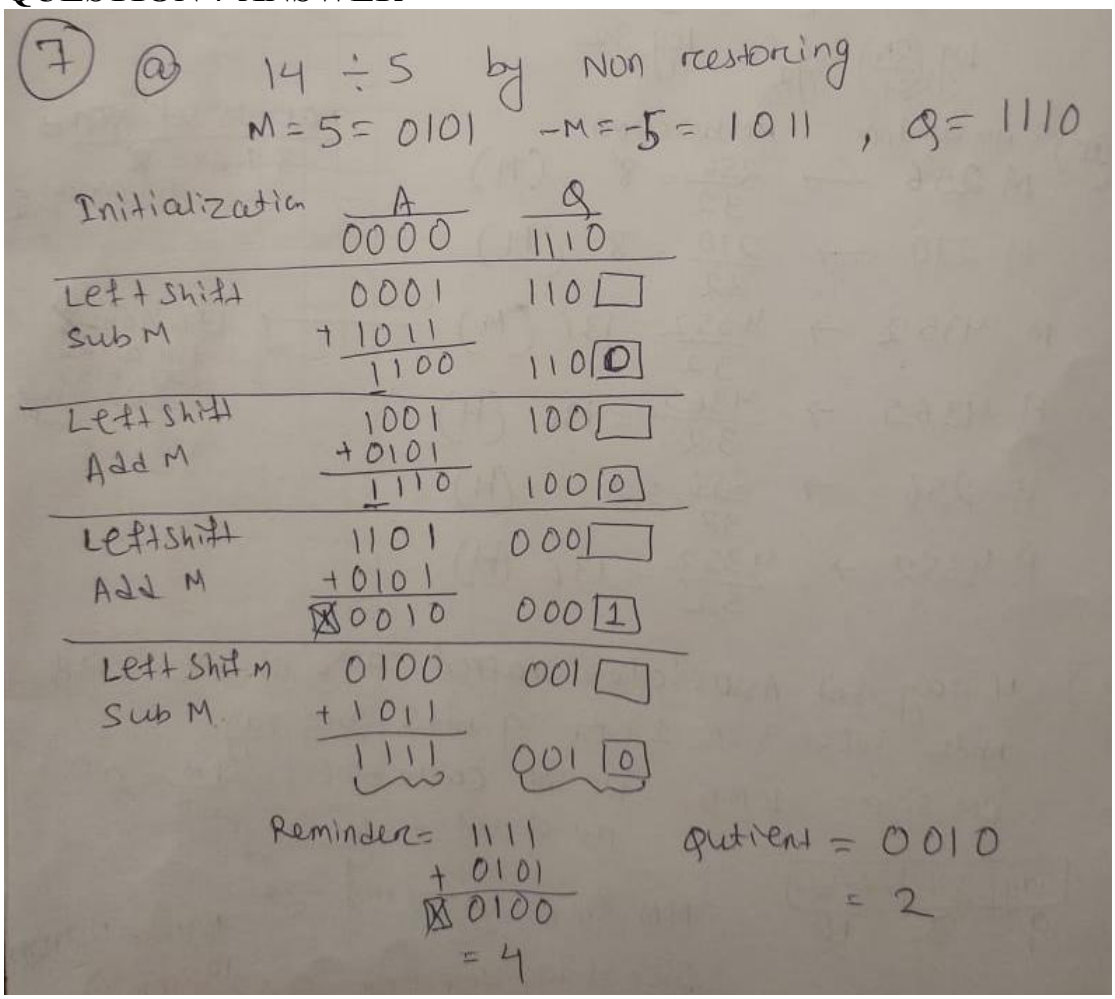
QUESTION 6 ANSWER

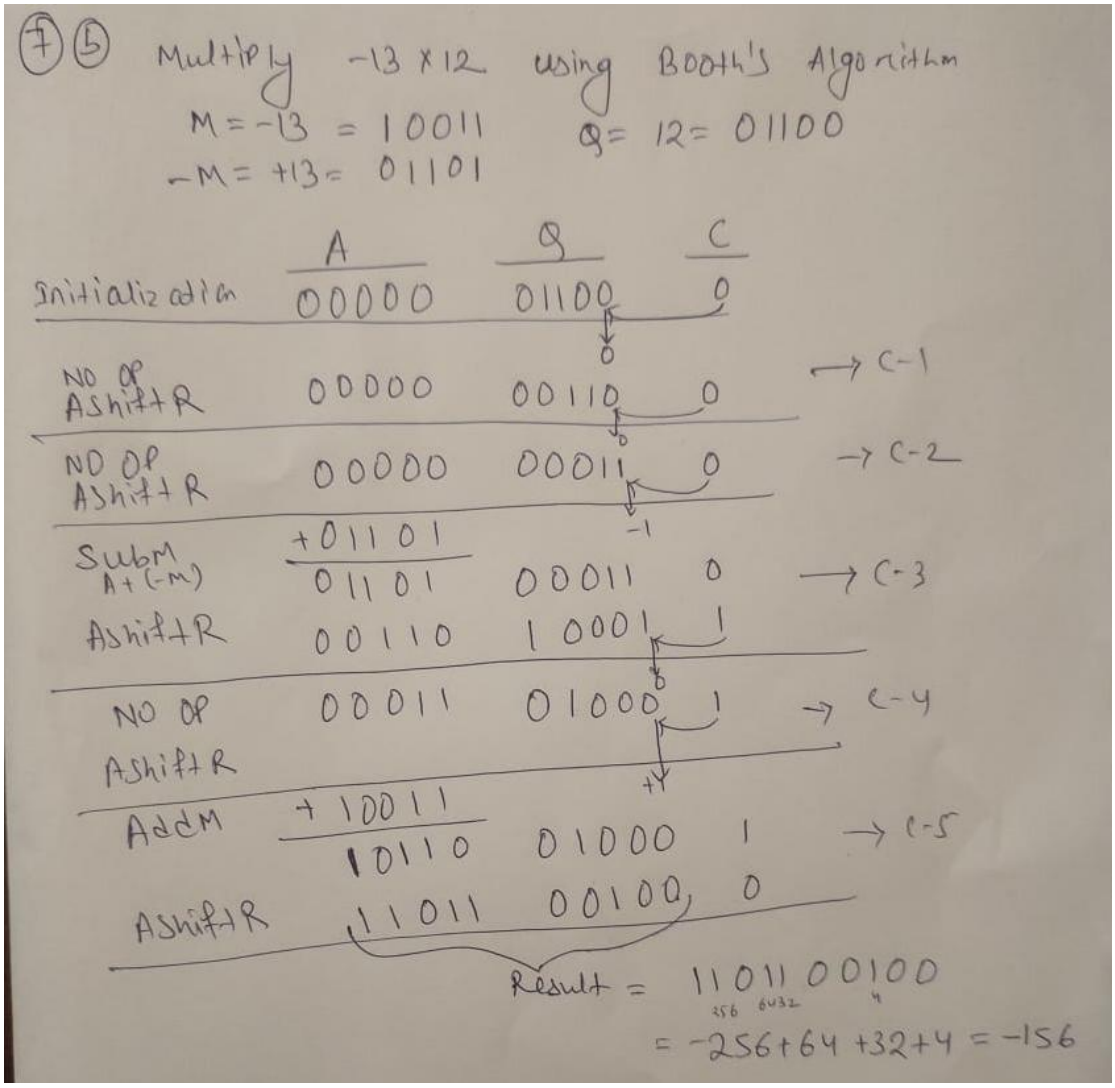


Valid bit:
when cache contain a block of information but that content is not exist in main memory in that case valid bit will be set to 0.

7.	(a)	Perform the following division operation using non-restoring method. 14 ÷ 5. Evaluation Scheme: Here step marks may be awarded appropriately.	[4]
	(b)	Multiply (-13) X 12 using Booth's algorithm. Evaluation Scheme: Here step marks may be awarded appropriately.	[4]

QUESTION 7 ANSWER





8.	(a)	Explain the working principle of I/O transfer method that facilitates transfer of bulk data from hard disk to main memory with the highest throughput? Evaluation Scheme: Diagram [2 marks] Theory [2Marks]	[4]
	(b)	State how isolated I/O is different from memory mapped I/O. Explain nesting of interrupt requests. Evaluation Scheme: Difference [2 Marks] Nesting of interrupt request [2 Marks]	[4]

QUESTION 8 ANSWER

(a) DMA Transfer Technique

DMA controller can transfer a block of data from an external device to the processor, without any intervention from the processor. However, the operation of the DMA controller must be under the control of a program executed by the processor. That is, the processor must initiate the DMA transfer. To initiate the DMA transfer, the processor informs the DMA controller of: Starting address, Number of words in the block, Direction of transfer (I/O device to the memory, or memory to the I/O device).
Once the DMA controller completes the DMA transfer, it informs the processor by raising an interrupt signal.

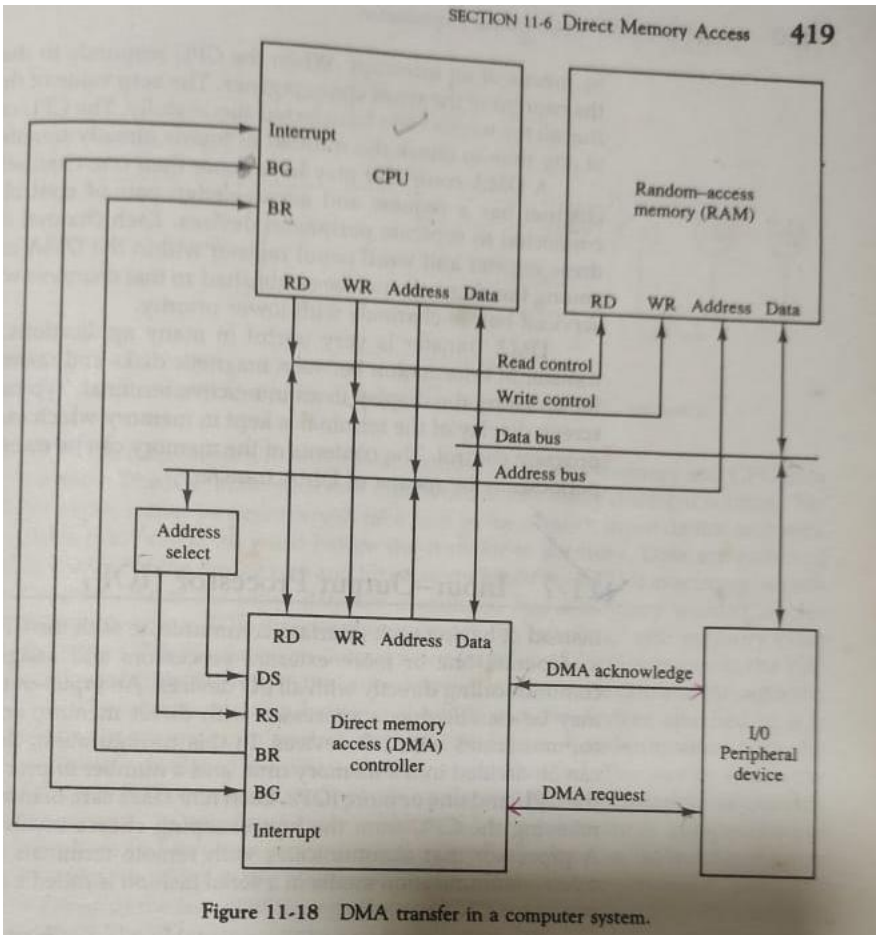


Figure 11-18 DMA transfer in a computer system.

(b)

I/O Mapped I/O	Memory Mapped I/O

I/O Mapped I/O	Memory Mapped I/O
I/O device is treated as an I/O device and hence given an I/O address.	I/O device is treated like a memory device and hence given a memory address.
I/O device has an 8 or 16 bit I/O address.	I/O device has a 20 bit Memory address.
Decoding is easier due to lesser address lines	Decoding is more complex due to more address lines
Decoding is cheaper	Decoding is more expensive
Works faster due to less delays	More gates add more delays hence slower
Allows max 2^16 = 65536 I/O devices	Allows many more I/O devices as I/O addresses are now 20 bits.
I/O devices can only be accessed by IN and OUT instructions.	I/O devices can now be accessed using any memory instruction.