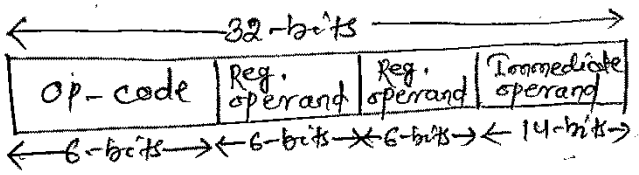
SPRINGER MID-SEMESTER EXAM-2017

SOLUTION SCHEME

1.(a)



1

op-code = 2^6 = 6-bits

Reg. operand = 2^6 = 6-bits

Immediate operand = 32 − (6+6+6) = 14-bits

Maximum value of the immediate operand = $2^{14}-1$

(b) To support LOAD-multiple and STORE-multiple. 1

(c) Difference between epc and pc 1

(d) R1 = 1 1 0 1 0 1 0 1 1

AshiftR #2, R1

After shift R1 = 1 1 1 1 0 1 0 1

To know the decimal value:

R1 = 1 1 1 1 0 1 0 1

1's complement = 0 0 0 0 1 0 1 0

+ 0 0 0 0 0 0 0 1

0 0 0 0 1 0 1 1

Ans = −11

(e)

	Instruction		Data Reference
	MOV	R1, (3000)	→ 1
LOOP:	MOV	R2, (R3)	→ 1
	ADD	R2, R1	→ 0
	MOV	(R3), R2	→ 1
	INC	R3	→ 0
	DEC	R1	→ 0
	BNZ	LOOP	→ 0
	HALT		→ 0

Loop will Rotate for 10 times.

Total = 1 + 10(1+1) = 21 | 1

2.

(a) Diagram | 1

working principle | 1

(b) $Z = (A - B + C) * (D / E * F) / G$

(i) One-address Instruction | 1

```
LOAD   A    // AC ← [A]
SUB    B    // AC ← [AC] − [B]
ADD    C    // AC ← [AC] + [C]
STORE  S    // S ← [AC]
LOAD   D    // AC ← [D]
DIV    E    // AC ← [AC] / [E]
MUL    F    // AC ← [AC] * [F]
MUL    S    // AC ← [AC] * [S]
DIV    G    // AC ← [AC] / [G]
STORE  Z    // Z ← [AC]
```

(ii) Zero - Address Instruction 1

```
PUSH  A
PUSH  B
SUB
PUSH  C
ADD
PUSH  D
PUSH  E
DIV
PUSH  F
MUL
MUL
PUSH  G
DIV
POP
```

(iii) RISC Instructions: 1

```
LOAD   A, R1
LOAD   B, R2
SUB    R1, R2, R1
LOAD   C, R3
ADD    R1, R3, R1
LOAD   D, R4
LOAD   E, R5
DIV    R4, R5, R4
LOAD   F, R6
MUL    R4, R6, R4
MUL    R1, R4, R1
LOAD   G, R7
DIV    R1, R7, R1
STORE  R1, Z
```

3. (a)
1. PCout, MARin, Read, select 4, ADD, Zin
2. Zout, PCin, Yin, WMFC
3. MDRout, IRin
4. Rlout, MARin, Read
5. Address_field_of_IRout, Yin, WMFC
6. MDRout, select Y, MUL, Zin
7. Zout, MDRin, Rlout, MARin, WRITE
8. WMFC, End

2.5

(b)
1. PCout, MARin, Read, select 4, ADD, Zin
2. Zout, PCin, Yin, WMFC
3. MDRout, IRin
4. Rlout, select 4, SUB, Zin
5. Zout, Rlin, MARin, Read
6. R2out, Yin, WMFC
7. MDRout, select Y, DIV, Zin
8. Zout, R2in, End.

2.5

4. (a) $S_5 = T_1 + T_3(I_2 + I_4)$ 1/2

$S_{10} = T_2(I_2 + I_3) + T_3 \cdot I_4 + T_4(I_1 + I_3) + T_5(I_2 + I_4)$ 1/2

Size of step decoder → 3x8 1/2

Size of Inst^n decoder → 2x2 1/2

(b) Diagram 1

working principle 1

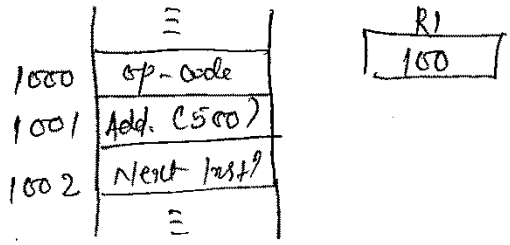
Advantage & Disadvantage 1

5. (a) XOR 1/2
Rotate 1/2
compare 1/2
shift 1/2

(b) 1. PCout, R=B, MARin, Read, IncPC 3
2. ~~MFC~~ WMFC
3. MDRoutB, R=B, IRin
4. R1outB, R=B, MARin, Read
5. R2outA, WMFC
6. MDRoutB, Select A, ADD, R2in, End.

6. (a) Diagram 1
Explanation 1

(b)



(i) EA = [R1] = 100 1
(ii) EA = 500 + 1002 = 1502 1
(iii) EA = 500 + 100 = 600 1

7. (a) (i) OK. ½

(ii) ERROR: Scalar factor can only be 1, 2, 4, or 8. ½

(iii) OK. ½

(iv) ERROR: ESP can't be used as index register. ½

(b) (i) Index with displacement mode 1

(ii) Base with index mode 1

(iii) Base with index and displacement mode. 1