AUTUMN END SEMESTER EXAMINATION-2018

3rd Semester B.Tech & B.Tech Dual Degree

DEC

EC2011 / EC_2011

[For 2018(L.E.) & 2017 Admitted Batches]

Time: 3 Hours | Full Marks: 50

Answer any SIX questions including question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. (a) The octal number $(651.124)_8 = (?)_{16}$. [1 × 10]

   (b) Write the complement of the expression A'B + CD'.

   (c) How can you convert the JK Flip-flop to a D Flip-flop?

   (d) Why a de-multiplexer (De-MUX) is called data selector?

   (e) Which counter have less propagation delay (synchronous/ asynchronous)? Explain why?

   (f) 7-bit ring counter's initial state is 0100010. After how many clock cycles will it return to the initial state?

   (g) The output frequency of a Mod-12 counter is 6kHz. Find the input frequency.

   (h) Detect and correct errors if any, in the even parity Hamming code words. 1110110

   (i) Compare the Moore and Mealy machines.

   (j) How many bits are required for a DAC, so that its full-scale output is 12.6 V and resolution 200 mV?

2. (a) i) Perform the BCD subtraction of 786 – 427, using the 10's complement method. [2+2]

ii) Convert $[10101101]_2$ to its Gray code and $[1010111]_G$ to its binary.

(b) Design a 4:2 priority encoder given the priority D_2>D1>D_3>D_0 where all D_i's are input to the encoder. [4]

3. (a) Simplify the following Boolean expression and implement the simplified expression with logic gates. [4]

$(A + B)(\overline{A}\overline{C} + C)(\overline{\overline{B} + AC})$

(b) Simplify the Boolean function using K-maps to obtain (i) minimal SOP and (ii) minimal POS expression and implement in AOI logic. [4]

$Y = \sum_m(0,2,3,6,7) + \sum_d(8,10,11,15)$

4. (a) Design a full-adder using NAND gates only. [4]

(b) Implement the following logic function using an 8×1 MUX. [4]

$F(A,B,C,D) = \sum_m(0,1,3,4,8,9,15)$

5. (a) Convert D Flip-flop to J-K Flip-flop and Vice-versa [4]

(b) Describe the working principle of bidirectional shift register with the help of logic diagram and mode control table. [4]

6. (a) Design an Asynchronous Mod-9 counter using J-K FFs. [4]

(b) A type-D counter that goes through states 0, 2, 4, 6, 0..... [4]

7. (a) Design a sequence detector that produces an output '1' whenever the non-overlapping sequence 1011 is detected using Mealy Model. [6]

(b) Draw the circuit diagram of two-input TTL NAND gate. [2]

8. Answer *any two* questions. [4×2]

(a) With the help of neat diagram, explain the working of the successive approximation type ADC.

(b) Design the synchronous BCD counter using J-K FFs.

(c) Explain the BCD-to-7 segment decoder.

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