KIIT UNIVERSITY, BHUBANESWAR
SPRING MID SEMESTER EXAMINATION-2015
DIGITAL ELECTRONIC CIRCUITS
[EC-2009]

Full Marks: 25 **Duration : 2Hrs**

Answer any FIVE questions including question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

(1) a) "Gray codes are cyclic but not sequential & self-complementing." Justify. [1x5]

b) Perform following arithmetic: (i) BCD subtraction (943 - 458),
(ii) (-21) - (-13) using 2's complement method.

c) Show that, $P\bar{Q} + PR + Q\bar{R} = P + Q\bar{R}$ where P, Q and R are Boolean variables.

d) Implement Half-Subtractor using **2:4 decoder** (having active HIGH output lines) and **one OR gate.**

e) Why the row and column numbers of the K- map are assigned in Gray code rather than binary numerical order, explain in brief.

(2) Obtain the minimized expression for the following 4-variable Boolean expression using K-map method and implement the minimized expression using **only NOR gates.** [5]
$F(W,X,Y,Z) = \sum m\,(0,2,5,10,11,15) + d(1,3,7)$

(3)a)i) What is the difference between 'Ripple carry adder' and 'Look-ahead carry adder' explain in brief. [2+2]

ii) 'A 4-bit adder circuit could be used to convert BCD codes to Excess-3 codes'. Justify this statement using proper circuit diagram in brief.

b) Implement XOR gate using minimum numbers of XNOR gates only. [1]

(4)a) What is Decoder? Draw the circuit diagram and truth table of 2-4 decoder having active-LOW output terminals. [2]

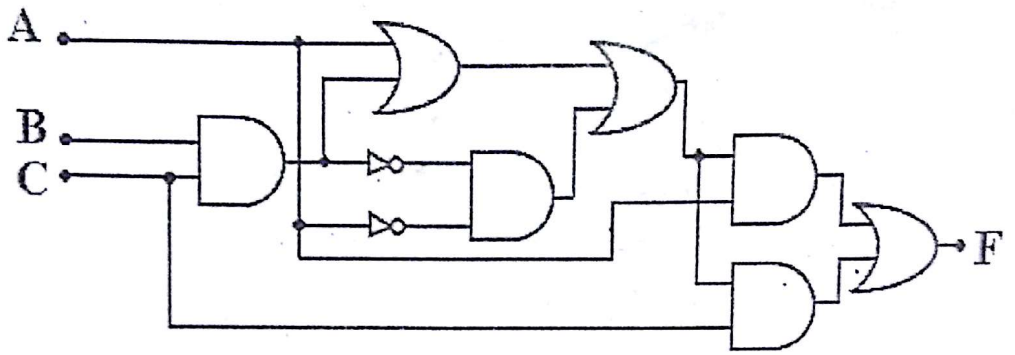
b) Implement the given function 'F' using a **3-8 decoder having active HIGH output terminals** and **NOR gates only.** [3]

$$F(P,Q,R) = PQ + QR + PR$$

(5) a) Design 4-bit combined adder/subtractor circuit using **Full adder modules & XNOR gates only** and explain the working in brief.

b) If the received 7-bit Hamming code is '1110100' then find the 4-bit data word.
[Assume (i) Even parity system, (ii) At most single bit error may take place]

(6) a) Simplify the given logic circuit and implement the simplified expression using **only NAND gates.**



b) Determine the **decimal value of the binary string** '101011' in [1]
(i) Sign-Magnitude form,
(ii) Sign-1's Complement form,
(iii) Sign-2's Complement form,
(iv) Unsigned binary number

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1303046
49
51
38

1303119
1303121
1303126
1303132
1303134
1303136
1303137
1303145
152
154

Solutions

Spring Mid Semester Examination-2015

Digital Electronic Circuit (EC-2009)

(1) a) Gray codes are

- Cyclic code (Unit distance code) because only one bit changes from one code to another consecutive code
- Not Sequential code because in any Gray code by adding '1' we don't get next consecutive code
- Not Self-complementing code because in Gray codes if any two Gray codes are 1's complement of each other then it is not necessary that their corresponding decimal values must be 9's complement of each other.

b) i) BCD subtraction (943 - 458)

1001	0100	0011
−0100	0101	1000
0100	1110	1011
	−0110	−0110
0100	1000	0101
4	8	5

(ii) (-21) - (-13) using 2's complement method

-21 in sign 2's complement : 101011

-13 in sign 2's complement : 110011

2's complement of '110011' : 001101

Now

(101011) + (001101) = 111000 = (-8) in 2's complement form

c) $P\bar{Q} + PR + Q\bar{R} = P + Q\bar{R}$

From L.H.S.

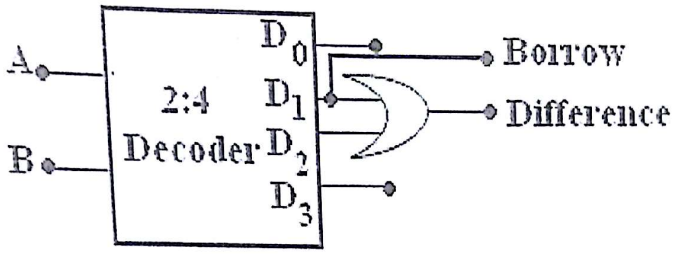
$P\bar{Q} + PR + Q\bar{R}$

$= P(\bar{Q} + R) + Q\bar{R}$

$= P(\overline{Q\bar{R}}) + Q\bar{R}$

$= P + Q\bar{R}$ = R.H.S.

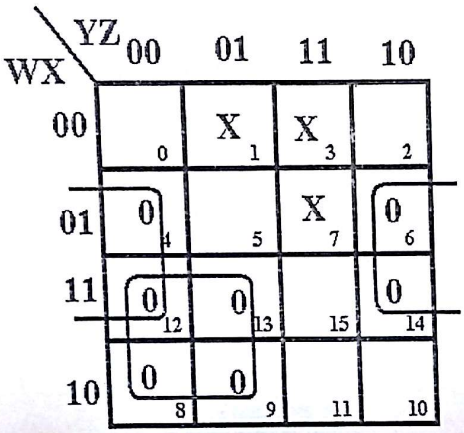
d) Half-Subtractor using **2:4 decoder** (having active HIGH output lines) and **one OR gate.**



e) In K-map Gray codes are used to maintain the **adjacency of cells**

- Gray codes are Cyclic code (Unit distance code) so only one bit changes from one code to another

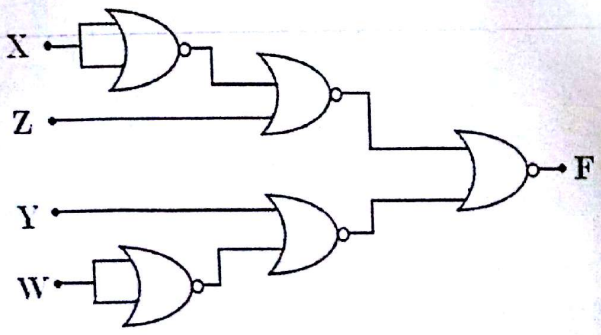
(2) $F(W,X,Y,Z) = \sum m\,(0,2,5,10,11,15) + d(1,3,7)$
$F(W,X,Y,Z) = \prod M(4, 6, 8, 9, 12, 13, 14)\,.\,d\,(1,3,7)$ [1]



[1.5]

Expression: $F\,(W, X, Y, Z) = (\overline{X}+Z).(\overline{W} + Y)$ [1]

Circuit Diagram: [1.5]



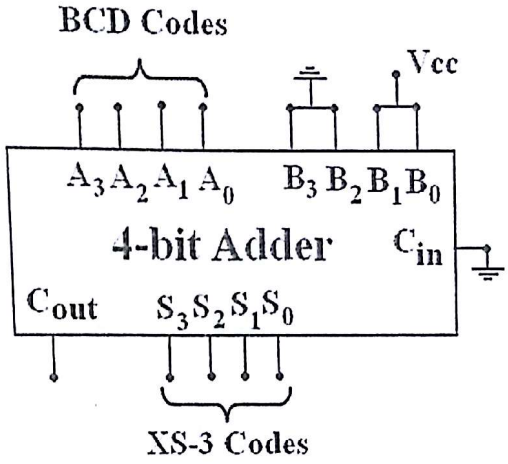
midterm . grouping 2.5.

(3) a) i) Difference between 'Ripple carry adder' and 'Look-ahead carry adder':

- Ripple carry adder is slow while Look- ahead carry adder is fast. [0.5]
- **For explanation** [1.5]

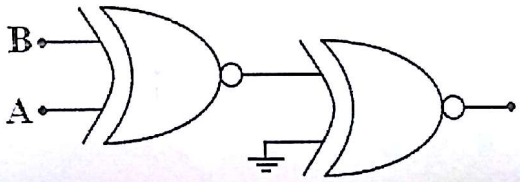
(3) a) ii) BCD codes to Excess-3 codes using 4-bit adder circuit:

- Excess-3 code = BCD code + 0011 [0.5]

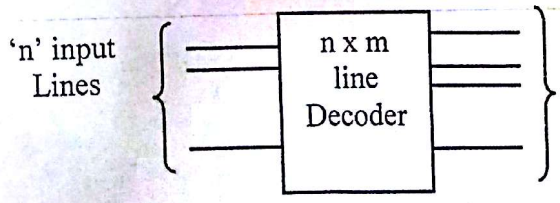


[1.5]

(3) b) XOR gate using minimum numbers of XNOR gates only [1]



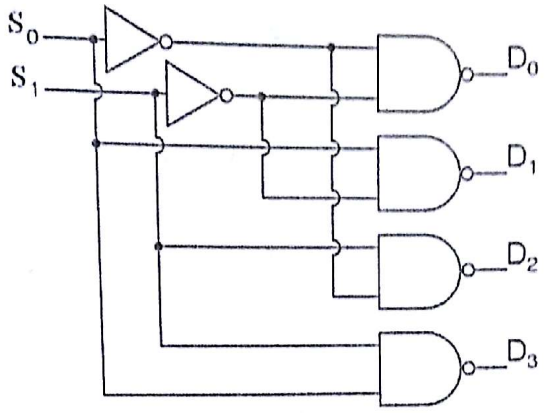
(4) a) A decoder is a logic circuit that converts an n-bit binary input code into 2^n output lines, such that each output line will be activated for only one of the possible combinations of inputs.



[0.5]

where $m = 2^n$

- **2-4 decoder having active-LOW output terminals** [1]



- **Truth table:** [0.5]

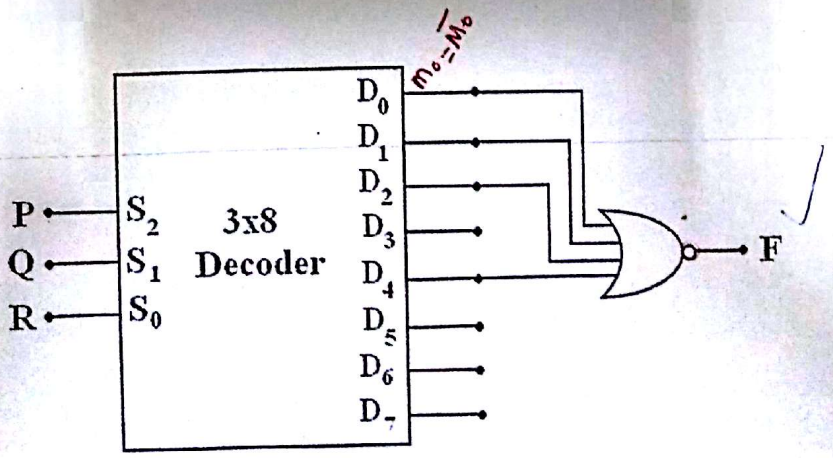
S_1	S_0	D_0	D_1	D_2	D_3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

(4) b) $F(P,Q,R) = PQ + QR + PR$

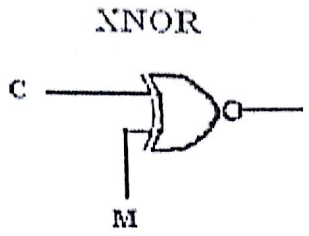
$= \sum m\,(3, 5, 6, 7)$ [1]

$= \Pi M\,(0, 1, 2, 4)$ ✓ [0.5]

- Implementation of function **'F'** using a **3 x 8 decoder having active HIGH output terminals** and **NOR gates only:** [1.5]

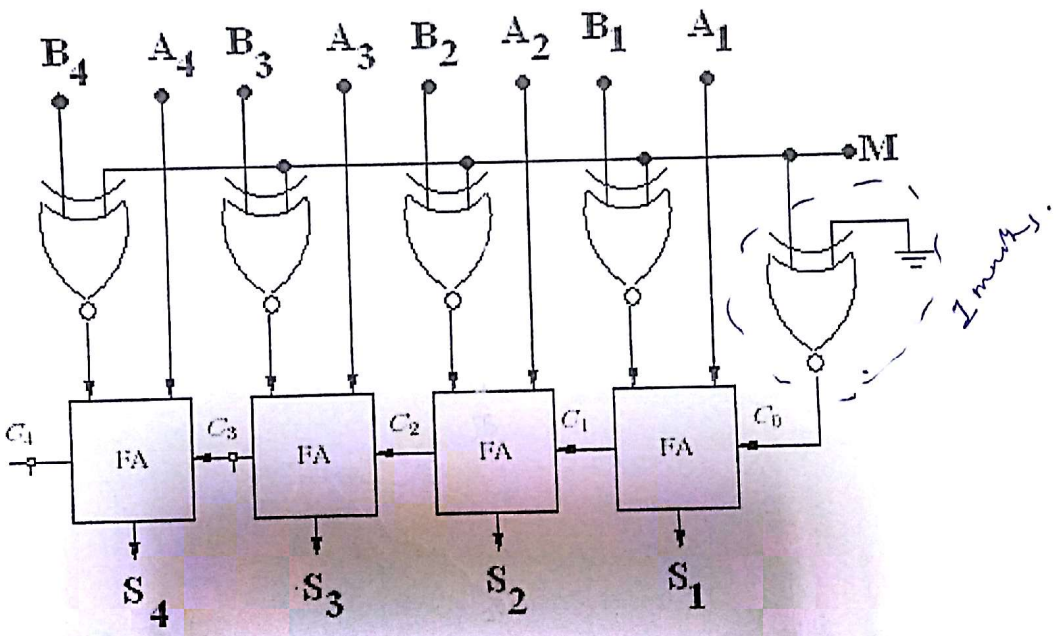


(5) a) **4-bit combined adder/subtractor circuit using full adders & XNOR gates:**



For M=0, Inverter
M=1, Buffer

[1]



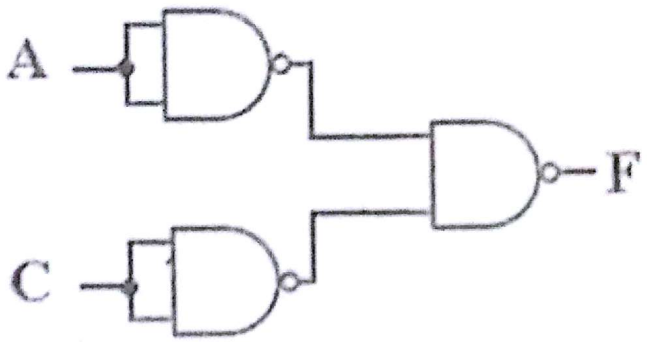
[1.5]

For M = 0 circuit performs **subtraction** (All XNOR gates are in INVERTER mode) [1.5]
M = 1 circuit performs **addition** (All XNOR gates are in BUFFER mode)

(5) b) Received 7-bit Hamming code :1110100
Location of error : 5th [0.5]
Hamming code after correction : 1110000 [0.25]
4-bit Data word : 1000 ~~[0.5]~~ [0.25]

(6) a) Simplified Boolean expression of the given circuit is $F = A + C$

Implementation of the simplified expression using only NAND gates



(6) b) Binary string '101011' in

(i) Sign-Magnitude form	=> - 11	[0.25]
(ii) Sign-1's Complement form	=> - 20	[0.25]
(iii) Sign-2's Complement form	=> -21	[0.25]
(iv) Unsigned binary number	=> 43	[0.25]