Invigilator's Signature and Date

Set-1

KIIT DEEMED TO BE UNIVERSITY

Spring End Semester Examination-2022

Roll No.	
Registration No.	
Name	
Date of Exam	

COMPUTER ORGANIZATION (CS 3042)

6th Semester B.Tech (Open Elective-I / Minor-I)

SECTION-A

(Answer All Questions)

Time: 30 Minutes **Full Marks = 2 × 7 = 14 Marks**

Question No	Question	Write the correct option here.
Q.No:1	Define Computer architecture and computer organization. **Answer:**	
Q.No:2	PC does the same function as MAR, and then justify your answer by keeping two registers instead of one. **Answer:**	

Q.No:3	What is the content of R_0 after executing the following instruction Rshift L #2, R_0 (Where R_0 is of 8 bit data and its content is 11111001.) **Answer:**	
Q.No:4	An instruction SUB 3000 a) Subtracts 3000 to the value in Accumulator and stores the result in the memory location 3030 b) Subtracts the value in memory location 3000 to the value in Accumulator and stores the result in Accumulator c) Subtracts 3000 to the value in Accumulator and stores the result in Accumulator d) None of the above	
Q.No:5	Hardwired control unit is relatively inflexible"-Justify the statement. **Answer:**	
Q.No:6	2K SRAM cells are there and if the memory is byte addressable than find the number of external connection. **Answer:**	
Q.No:7	Explain the meaning of Privileged Exception. **Answer:**	

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SECTION-B

(Answer Any Three Questions.)

Time: 1 Hour and 30 Minutes **Full Marks = 12 × 3 = 36 Marks**

Q.No:8 With a neat sketch explain about multiple bus CPU organization. write the control signals to execute following instruction using same organization (i) ADD R1,R2,(R3) (ii) SUB R1,R2,R3 [12]

Q.No:9 a. Define parallel processing and explain the flynn's classification of computer with suitable diagram. [6]

b. Consider a pipeline having 4 phases with duration 60, 50, 100 and 80 ns. Given latch delay is 10 ns. [6].

Calculate-

I. Pipeline cycle time
II. Non-pipeline execution time
III. Speed up ratio
IV. Pipeline time for 1000 tasks
V. Sequential time for 1000 tasks
VI. Throughput

Q.No:10 A. Discuss Memory Hierarchy and with a suitable diagram explain the working principle of SRAM chip. [6]

B. If a computer system uses 16 bit memory addresses. It has 2K-byte cache organized in a direct-mapped manner. With 64 bytes per cache block. Assume that the size of each memory word is 1 byte . [6]

I. Find the Size of tag, block and word.
II. If 4 way set associative is used then find the size of tag and set

Q.No:11 Explain Direct Memory Access method with its requirement and explain the daisy chain method for handling simultaneous interrupt request? [12]

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