DOE - 30/9/16.

Mid-Semester Examination
School of Computer Engineering
KIIT University, Bhubaneswar-24

Time: 2hrs ***Full Mark:25***

(Answer any five questions including question No.1 which is compulsory.
The figures in the margin indicate full marks.)
(Instruction format: Opcode src2, src1/dest)

1) Short Questions [1 × 5]

a) At the end of a memory read operation, the MDR is loaded with a binary combination, how that combination is interpreted as an instruction or an operand to an instruction?

b) The content of register R1 is 1011001100110011.Write the instruction for performing the following operations:

i. Clear the LSB of R1 to 0.
ii. Set the MSB of R1 to 1.

c) The content of register R1is 11010110. What will be the decimal value after execution of RotateL #2, R1. [Assume the number is represented in 2's complement format]

d) "Hardwired Control Unit is relatively inflexible"-Justify the statement.

e) A CPU has only three instructions I1, I2 and I3, which use the following signals in time steps T1-T5:

I1:	I2:	I3:
T1:A_{in},B_{out},Cin	T1:C_{in},B_{out},D_{in}	T1:D_{in},A_{out}
T2:PC_{out},B_{in}	T2:A_{out},B_{in}	T2:A_{in},B_{out}
T3:Z_{out},A_{in}	T3:Z_{out},A_{in}	T3:Z_{out},A_{in}
T4:B_{in},C_{out}	T4:B_{in},C_{out}	T4:D_{out},A_{in}
T5:End	T5:End	T5:End

Write the logic function for generating the signal A_{in}?

2) Write a program to evaluate the given arithmetic expression :- [5]

$Z = (R + P) * E + K * B - L / G - S$

i) Using a general register computer with two address and three address instructions.
ii) Using an accumulator type computer with one address instructions.
iii) Using a stack organized computer with zero-address operation instructions.
iv) Using RISC computer instruction format.

3) [2.5+2.5]

a) Explain the basic operational concept involved in the execution of an instruction with an example.

b) Give two examples from each of the following type of computer instructions, explaining their functions :-
[i] Data Transfer Operation [ii] Logical Shift Operation [iii] Program Control Operation.

4) [1+2+2]

a) How many times a subroutine should be called so that the stack becomes full, Assume that the stack address space ranges from 2000 to 1600 and each stack word consumes 4 bytes and machine is byte addressable.[Note: No parameter, return value, registers, local variables are stored in the stack due to subroutine call]

b) Match columns:

A	B
Indirect	Relocatable code
Index	Passing array as a parameter
Base Register	Array
Auto increment	while (*A++)

c) Write the sequence of control steps for the following instructions for single bus CPU organization
Add (R3), R1.

The processor is driven by a continuously running clock, such that each control step is 2 ns in duration. How long will the processor have to wait in step2 and 5, assuming that a memory read operation takes 16ns to complete? What percentage of time is the processor idle during execution of this instruction?

5) [2+3]

a) Explain the working principle of micro-programmed control unit design with neat diagram.

b) Given the following program fragment

Main Program	First Subroutine	Second Subroutine
2000 ADD R1, R2	3000 SUB1 MOV R1,R2	4000 SUB2 SUB R6, R1
2004 XOR R3, R4	3004 ADD R5, R1	4004 XOR R1, R5
2008 CALL SUB1	3008 CALL SUB2	4008 RETURN
2012 SUB R4, R5	3012 RETURN	

Initially the stack pointer SP contains 5000.
What are the content of PC, SP, and the top of the stack?

i) After the subroutine call instruction is executed in the main program?
ii) After the subroutine call instruction is executed in the subroutine SUB1?
iii) After the return from SUB2 subroutine?

6) [1+4]

a) An instruction is a 24 bit instruction. It is a byte addressable memory. The PC contains 300. Which one of the following is a legal PC value:

a. 400 (b) 500 (c) 600 (d) 700

b) Write the sequence of control steps for the following instructions for single bus CPU organization

I. I1: ADD 10(R3), R4
II. I2: Branch<0 L1
III. I3: MUL -(R5), R5
IV. Design the logic function for WMFC control signal with reference to the above instructions i.e. I1 to I3.