KIIT, Deemed to be University
School of Electronics Engineering
Digital System Design Laboratory [EC 29005]

EXPERIMENT - 3

Aim:

Design and Simulation of 3 line to 8 line active high decoder using Verilog HDL.

Realization of 3 variable Boolean function using active low decoder.

Component/Software Used:

Component/Software	Specification
ICs	7413,7408
Bread Board, Power supply, LEDs, Resistors,Switches, Connecting wires	As per requirement
Software(s) Used	Vivado 2016.1

Theory:

Decoder:

Decoder is a combinational circuit that has 'N' input lines and maximum of $(2)^N$ unique output lines. The name "Decoder" means to translate or decode coded information from one format into another, so a digital decoder transforms a set of digital input signals into an equivalent decimal code at its output. Active High Decoder - The output line that is active will be HIGH(1) and rest all the outputs will be LOW(0). Active Low Decoder - The output line that is active will be LOW(0) and rest all the outputs will be HIGH(1)

This 3-to-8 line binary decoder consists of an array of eight AND gates. The three(3) binary inputs labeled I_0 , I_1 and I_2 are decoded into one of 8 outputs, hence the description of 3 -to - 8 binary decoder. Each output represents one of the minterms of the 3 input variables, (each output is equals to a minterm).

The binary inputs I_0 , I_1 and I_2 determine which output line from D_0 to D_7 is "HIGH" at logic level "1" while the remaining outputs are held "LOW" at logic "0" so only one output can be active (HIGH) at any one time. Therefore, whichever output line is "HIGH" identifies the binary code present at the input, in other words it "de-codes" the binary input. Truth table of 3:8 active high Decoder is shown in Table 3.1 . In case of active low decoder output line from D_0 to D_7 is "LOW" while the remaining outputs are held "HIGH" so only one output can be active (LOW) at any one time as shown in Table 3.2.

Inputs			Outputs							
I_2	I_1	I_0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Table 3.1: Truth table of 3:8 active high Decoder

$$D_0(I_2, I_1, I_0) = m_0 = \overline{I_2}\,\overline{I_1}\,\overline{I_0}$$
$$D_1(I_2, I_1, I_0) = m_1 = \overline{I_2}\,\overline{I_1}\,I_0$$
$$D_2(I_2, I_1, I_0) = m_2 = \overline{I_2}\,I_1\,\overline{I_0}$$
$$D_3(I_2, I_1, I_0) = m_3 = \overline{I_2}\,I_1\,I_0$$
$$D_4(I_2, I_1, I_0) = m_4 = I_2\,\overline{I_1}\,\overline{I_0}$$
$$D_5(I_2, I_1, I_0) = m_5 = I_2\,\overline{I_1}\,I_0$$
$$D_6(I_2, I_1, I_0) = m_6 = I_2\,I_1\,\overline{I_0}$$
$$D_7(I_2, I_1, I_0) = m_7 = I_2\,I_1\,I_0$$

Boolean Expression of Outputs of 3:8 Decoder

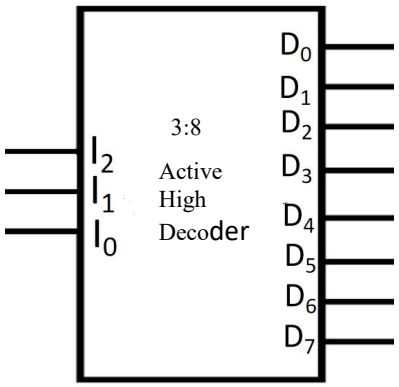

Figure 3.1: Block diagram of 3:8 Decoder

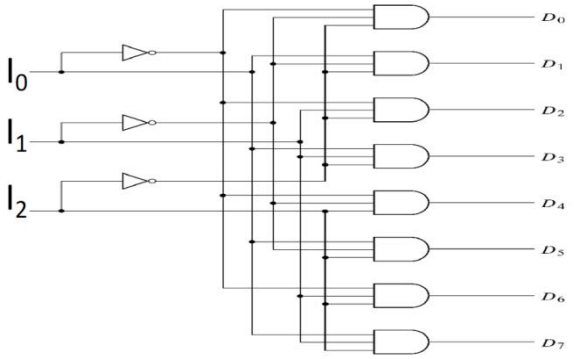

Figure 3.2: Logic diagram of 3:8 Decoder

Inputs			Outputs							
I_2	I_1	I_0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

Table 3.2: Truth table of 3:8 active low Decoder

$$D_0(I_2, I_1, I_0) = \overline{m_0} = \overline{\overline{I_2}\,\overline{I_1}\,\overline{I_0}}$$
$$D_1(I_2, I_1, I_0) = \overline{m_1} = \overline{\overline{I_2}\,\overline{I_1}\,I_0}$$
$$D_2(I_2, I_1, I_0) = \overline{m_2} = \overline{\overline{I_2}\,I_1\,\overline{I_0}}$$
$$D_3(I_2, I_1, I_0) = \overline{m_3} = \overline{\overline{I_2}\,I_1\,I_0}$$
$$D_4(I_2, I_1, I_0) = \overline{m_4} = \overline{I_2\,\overline{I_1}\,\overline{I_0}}$$
$$D_5(I_2, I_1, I_0) = \overline{m_5} = \overline{I_2\,\overline{I_1}\,I_0}$$
$$D_6(I_2, I_1, I_0) = \overline{m_6} = \overline{I_2\,I_1\,\overline{I_0}}$$
$$D_7(I_2, I_1, I_0) = \overline{m_7} = \overline{I_2\,I_1\,I_0}$$

Boolean Expression of Outputs of 3:8 active low Decoder

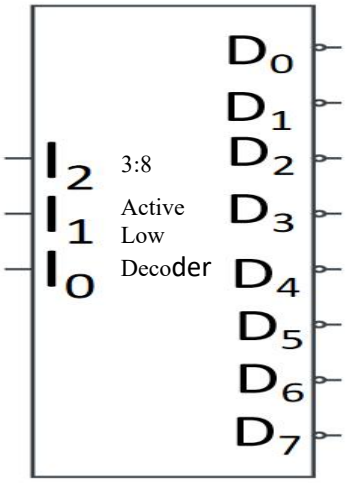

Figure 3.3: Block diagram of 3:8 Decoder

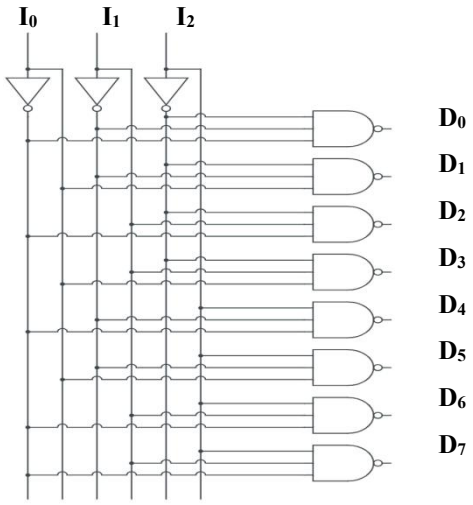

Figure 3.4: Logic diagram of 3:8 Decoder

The IC-74138 is 3:8 active low decoder its pin diagram is shown in Figure 3.5. The IC-74138 has 3 binary inputs A, B, and C which are equivalent to I_0 , I_1 and I_2 respectively. It has 8 outputs Y_0 to Y_7 those are equivalent to D_0 to D_7 respectively. If the device is enabled, these inputs determine which one of the eight normally HIGH outputs will go LOW. The IC has two active LOW and one active HIGH enables (G1, G2A and G2B) which will be helpful in cascading of decoders. The enable pins must be active for normal operation of decoder. The functioning of the IC74138 is illustrated in the Table 3.3, where "X" denotes the Don't care in the table.

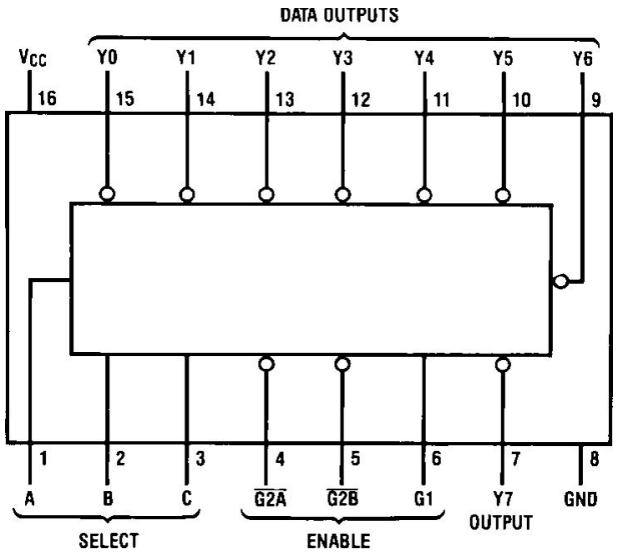

Figure 3.5: Pin diagram of IC 74138

Inputs						Outputs							
Enable Inputs			Select										
G2B	G2A	G1	C	B	A	0	1	2	3	4	5	6	7
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0
x	x	0	x	x	x	1	1	1	1	1	1	1	1
x	1	x	x	x	x	1	1	1	1	1	1	1	1
1	x	x	x	x	x	1	1	1	1	1	1	1	1

Table 3.3: Function table of IC 74138

Boolean function implementation:

Any Boolean function may be represented in sum-of-minterms or product-of-maxterms form, a hardware implementation of the function is provided by a decoder that creates the function's minterms and external gates that construct their logical sum.

The process for creating a Boolean function with a decoder and external gates requires that the Boolean function be defined as a sum-of-minterms or product-of-maxterms. Then, a decoder is chosen to create all the minterms or maxterms of the input variables. The inputs to each gate are chosen from the decoder outputs based on the list of minterms or maxterms for function. This approach is illustrated by implementing a Boolean function given below.

$$F(X,Y,Z) = \sum (0,3,5,6) = m_0 + m_3 + m_5 + m_6$$
$$= \prod (1,2,4,7) = \overline{m_1}\ \overline{m_2}\ \overline{m_4}\ \overline{m_7}$$

To implement the above Boolean function a 3:8 active low decoder is chosen and AND gated are required. The implementation of the Boolean function using the block diagram of the decoder IC 74138 is shown below in Figure 3.6

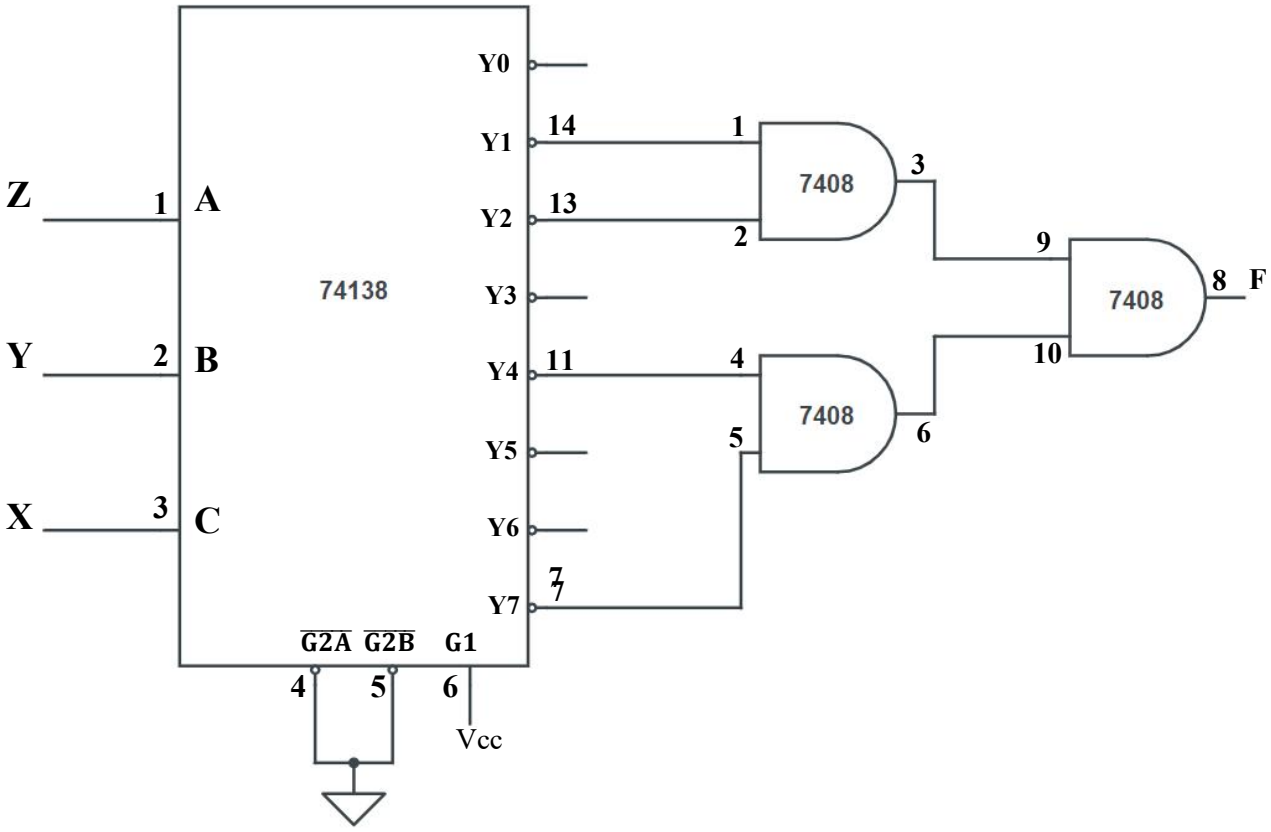

Figure 3.6: Block diagram of Boolean function using 3:8 Decoder

Procedure

For Software Simulation:

a) Create a module with required number of variables and mention it's input/output.
b) Write the description of given Boolean function using operators or by using the built in primitive gates.
c) Synthesize to create RTL Schematic.
d) Create another module referred as test bench to verify the functionality and to obtain the waveforms of input and output.
e) Follow the steps required to simulate the design and compare the obtained output with the corresponding truth table.
f) Take the screenshots of the RTL schematic and simulated waveforms.

Note: Students need to write the Verilog HDL code by their own for which they can refer Appendix - A if required.

For Hardware implementation:

a) Turn off the power of the Trainer Kit before constructing any circuit.
b) Connect **power supply (+ 5 V DC)** pin and **ground** pin to the respective pins of the trainer kit.
c) Place the ICs properly on the bread board in the Trainer Kit.
d) Connect VCC and GND pins of each chip to the power supply and ground bus strips on the bread board.
e) Connect the input and output pins of chips to the input switches and output LEDs respectively in the Trainer Kit.
f) Check the connections before you turn on the power.
g) Apply various combinations of inputs according to truth tables and observe outputs of LEDs.

Observation:

To be written by students

Design Problem:

Design and Simulation of 3bit binary to Gray code converter using decoder.

Solution:

Binary to Gray code converter is a logical circuit that is used to convert the binary code into its equivalent Gray code. By putting the MSB of 1 below the axis and the MSB of 1 above the axis and reflecting the (n-1) bit code about an axis after 2^{n-1} rows, we can obtain the n-bit gray code.

In Table 3.4 the truth table of 3-bit binary to Gray code converter is shown. The implementation of the Gray code converter using the block diagram of the decoder IC 74138 is shown below in Figure 3.7.

Inputs			Outputs		
B_2	B_1	B_0	G_2	G_1	G_0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

$$G_2(B_2, B_1, B_0) = \sum (4,5,6,7)$$

$$G_1(B_2, B_1, B_0) = \sum (2,3,4,5)$$

$$G_1(B_2, B_1, B_0) = \sum (1,2,5,6)$$

Table 3.4: Truth table of 3-bit binary to Gray code converter and its minterms

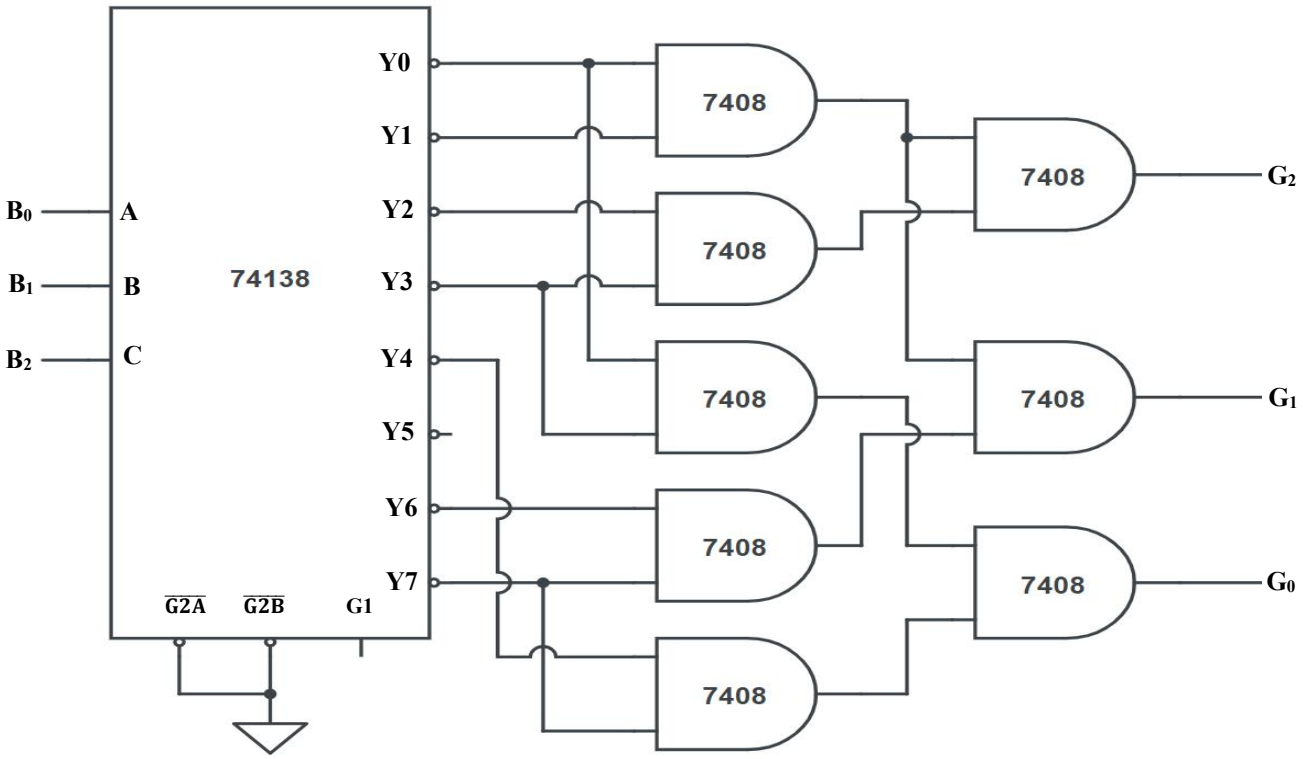

Figure 3.7: Block diagram of 3-bit binary to Gray code converter using decoder

Conclusion:

To be written by students.

Sample viva-voice questions

1. What is a decoder?
2. Differentiate between active low output and active high output.
3. Differentiate between decoder and de-multiplexer.
4. What is an encoder?
5. What is a priority encoder?
6. Give the applications of decoder.
7. Design Full Subtractor using decoder.
8. Which digital system translates coded characters into a more useful form?
9. Design Full adder using decoder.
10. Implement 3 to 8 line decoder using 2 to 4 line decoder.