6. (a) Explain the classification of data transfer techniques? Explain DMA transfer technique in brief. [4]

(b) A computer system consists of main memory and two level of cache memory whose specifications are given below :- [4]

CACHE-1→ Size of cache memory is 8192 bytes
Cache memory access time is 20 nanosecond.
Each block consists of 1 word.
Hit ratio is 95%.

CACHE-2→ Size of cache memory is 256 Kbytes.
Cache memory access time is 20 nanosecond.
Each block consists of 4 word.
Cache memory uses 4-way set-associative.

For the same system the given main memory access time is 100 nanosecond. Apply the above given set-associative cache memory mapping in order to calculate hit ratio for CACHE-2, if the average access time is 16 nanosecond.

SECTION-D

7. (a) An instruction is stored at location 100 with its address field at location 101. The address field has the value 250. A processor register R1 contains the value 50. Evaluate the effective address if the addressing mode of the instruction is given as bellow:- [4]

I. Direct
II. Immediate
III. Register indirect
IV. Index mode where R1 register

(b) $(-12)_{10} * (+11)_{10} = ?$ [4]

Design the booth multiplication process (Draw the flow chart) to find the product of the above given numbers.

8. (a) Design a larger memory structure of capacity 8M × 32 using 512K × 8 memory chips. [4]

(b) $(13)_{10} \div (4)_{10} = ?$ [4]

Evaluate the result using non-restoring division technique.

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21/06/2019

SUPPLEMENTARY EXAMINATION-2019

4th Semester B.Tech & B.Tech Dual Degree

COMPUTER ORGANIZATION AND ARCHITECTURE

CS-2006 / CS 2006

(For 2018(L.E) & 2017 Admitted Batches)

Time: 3 Hours Full Marks: 50

Answer any SIX questions.
Question paper consists of four sections-A, B, C, D.
Section A is compulsory.
Attempt minimum one question each from Sections B, C, D.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

(Instruction format: Opcode src1/dest, src2)

SECTION-A

1. Answer all the questions. [1 × 10]

(a) At the end of a memory read operation, the MDR is loaded with a binary combination, how that combination is interpreted as an instruction or an operand to an instruction?

(b) The access time of a cache memory and main memory is 10ns and 100ns respectively. What is the average access time of the given system if the hit ratio is about 80%?

(c) The content of a register R1 is 11111110. What will be the decimal value in R1 after the execution of the following instruction?

ASHL #2, R1

[Assume the numbers are represented in 2's complement format]

(d) Why RISC architecture leads better performance than CISC architecture?

(e) Write "COMPUTER" using Big Endean and Little Endean format considering word length as 32 bits.

(f) "Hardwired Control Unit is relatively inflexible"- Justify the statement.

(g) How cycle-stealing mode is different from burst mode data transfer in DMA.

(h) Explain with example (2 examples) from each of following categories of instruction type.
   i) Data Transfer instruction
   ii) Program Controller instruction

(i) A computer has 64 bit instruction and 15 bit address. If there are 256 three address instruction and 525 two address instruction, how many one address instructions are possible?

(j) How does the processor interacts with memory while executing an instruction or program? Explain with diagram.

SECTION-B

2. (a) Explain cache memory mapping function? Explain different classification of cache memory mapping function in brief using diagrams. [4]

A block-set-associative cache consists of a total of 128 blocks, divided into 8-block sets. The main memory contains 4096 blocks, each consisting of 16 words. Assuming a 32-bit byte-addressable address space, how many bits are there in each of the Tag, Set, and Word field?

(b) Explain IEEE 754 format for representing floating point numbers in single precision and double precision format. [4]

Represent the decimal number 85.45 using IEEE 754 single precision floating point format.
Differentiate between different special numbers like ZERO, INFINITY, DENORMAL NUMBER and Not a Number.

3. (a) Write the assembly language code segment to evaluate the following arithmetic expression: [4]

$$X = A * (B - C) + K / (B + L)$$

Use the following instruction format:-
   I. 2-Address instruction format.
   II. Stack-Organization instruction format.

(b) Define parallel processing. Discuss each of the Flynn's classification with necessary diagrams. [4]

SECTION-C

4. (a) Discuss the function of virtual memory. Identify the role of TLB in virtual memory operation (with diagram). [4]

(b) Explain the importance of interrupt vector in I/O Processing? Distinguish the function of daisy chain method in order to handle simultaneous interrupt request. [4]

5. (a) Explain single-bus organization inside the CPU with the help of a suitable diagram. [4]
Implement single-bus organization in order to generate required control signals for the following given instructions.
   I. MUL R3, 10(R2)
   II. ADD (R3)-, R6

(b) Consider the program fragment given bellow:- [4]

Main Program	First Subroutine		Second Subroutine	
112 SUB R2, R3	604 SUB1	MOV R6, R7	304 SUB2	ADD R3, R2
116 DIV R4, R1	608	SUB R3, R4	308	MUL R6, R8
120 CALL SUB1	612	CALL SUB2	312	ADD R7, R9
124 ADD R6, R1	616	RETURN	316	RETURN

Initially the stack pointer SP contains 100.
Apply the concept of subroutine call to find the content of PC, SP, and top of stack (TOS)?
   i) Before the subroutine call instruction is executed in the main program?
   ii) After the subroutine call instruction is executed in the main program?
   iii) After the subroutine call instruction is executed in the subroutine SUB1?
After the return from SUB2 subroutine?