Gene

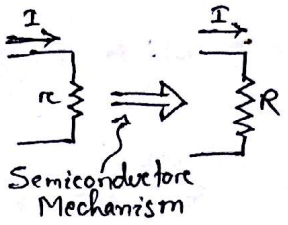
BJT

Bipolar = The charge carriers pass through two dissimilar semiconductor material, so called Bipolar.
IN NPN → from N to P & then from P to N
IN PNP → from P to N & then from N to P
If the charge carriers pass through in one semiconductor material, called as Unipolar, example FET.

Junction = When two dissimilar materials joined (metallugically) then a junction formed. Here two junctions are
- Emitter Base Junction (EBJ)
- Collector Base Junction (CBJ)

Transistor = Transfer Resistor —

Basic Principle is the current I from a low resistance area is transfered by a semiconductor mechanism to a high resistance area, gives rise to an amplification action.

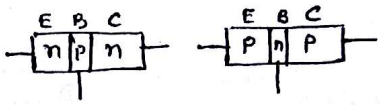


If R > rc
then IR > Irc

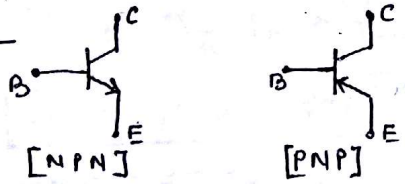
What is BJT ?

- It is semiconductor device
- It is a three terminal device
- Emitter – heivily doped.
  Base – Lightly doped.
  Collector – Moderately Doped.
- Operation –

EBJ	CBJ	
Forward Bias	Reverse Bias	→ Active
Reverse Bias	Forward Bias	→ Cutoff (off)
Forward Bias	Forward Bias	→ Saturation (on)

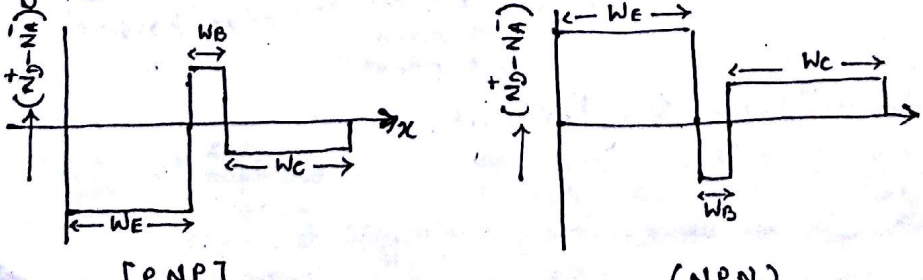


- It can be used as amplifier in Active operation and it is required to act as a switch then operated between cutoff & saturation.
- Symbol —

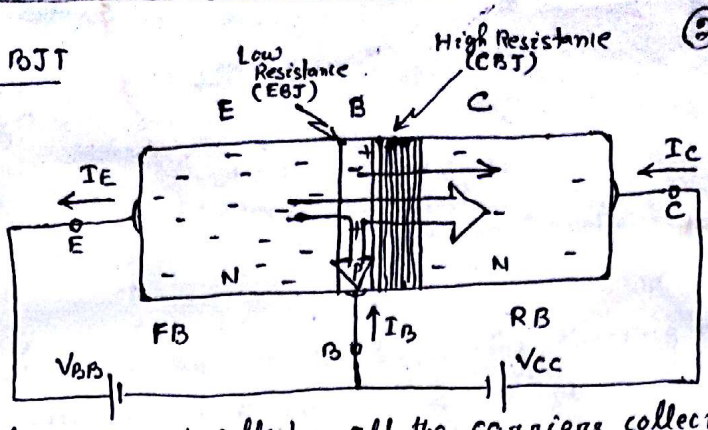


Arrow head shows the direction of current.

- Doping Profile —



General Active Operation of BJT



- E-B is forward Biased & C-B is Reversed Biased
- EBJ gives low resistance CBJ gives high resistance So current passes from low resistance → high.
- The majority carriers emitted from emitter & flow through base to collector. And at collector all the carriers collected.
- The minority carrier from base also passes to collector through CBJ.
- Very less no. of majority carrier of emitter passes through Base b/c it is very thin.
- All the current shown are in reverse direction of flow of majority carriers (electrons)

Current Analysis in BJT

Let N = No of majority carriers emitted from emitter. ⟹ constitute I_E

αN = " " " " passes to collector ⟹ αI_E

$(1-\alpha)N$ = " " " " " to Base ⟹ $(1-\alpha)I_E$

P = No of minority carries flow from Base to Collector ⟹ I_{CBO}.
due to Reverse Bias of CBJ.

So Current Relations are →

$$I_C = \alpha I_E + I_{CBO} \quad \text{——①}$$

$$I_B = (1-\alpha)I_E - I_{CBO} \quad \text{——②}$$

$$I_E = I_C + I_B \quad \text{——③}$$

where
I_C = Collector Current
I_B = Base Current
I_E = Emitter Current
I_{CBO} = Leakage Current due to minority carrier flow.

Derived Relation

We know $I_E = \alpha I_E + I_{CBO}$

$= \alpha(I_C + I_B) + I_{CBO}$

$\Rightarrow (1-\alpha) I_C = \alpha I_B + I_{CBO}$

$\Rightarrow I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$

$$\Rightarrow \boxed{I_C = \beta I_B + (1+\beta) I_{CBO}}$$

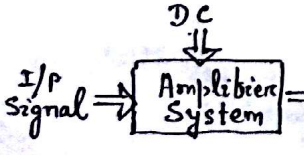
$$\Rightarrow \boxed{I_C = \beta I_B + I_{CEO}}$$

where $\beta = \frac{\alpha}{1-\alpha}$

& $(1+\beta) I_{CBO} = I_{CEO}$

Amplifier ?

classified as ⟸ Voltage Amp, Current Amp, Power Amp



Amplify means to increase the strength of a week signal.

Voltage, Current, Power

- Application of external DC voltage (having no information b/c f=0) is known as biasing. Due to the biasing the amplifier is prepared to amplify the i/p signal.
- If individual i/p signal is fed to Amplifier then actual replica can be produced at o/p.

Note

For Analysis & Design of Amplifier system

DC Response
- open ckt capacitors
- Remove AC inputs

AC Response
- short ckt capacitors
- Remove DC inputs
- known as Small Signal Analysis

Biasing ?

Application of external dc voltage to the device for forcing the device to operate at a fixed level of current & voltage.

For maintaining of fixed level of current and voltage in the device on the entire characteristic is known as operating point/ Bias point/ Quiescent point / Q-point / Inactive point / still point.

Need of Biasing

Generally the BJT is used for amplification purpose. So it is needed to force the device to operate to provide an actual replica of a max possible i/p signal.

- The Base-Emitter should be Forward Bias & Collector-Base should be Reverse Bas

  Means $V_{BE_Q} \geq V_{BE_T}$ where V_{BE_T} is Base Emitter Junction Voltage.

  & $V_{CE_Q} \geqslant V_{CE_{sat}}$

- To maintain the zero signal collector current (I_c) should be greater than equal to individual signal current (i_c)

  $I_c \geqslant i_c$

- Q-point should be choosen at the mid point of the load line for a given circuit for max possible i/p signal variation.

  Means $V_{CE_Q} = \frac{V_{CE_{max}}}{2}$ & $I_{C_Q} = \frac{I_{C_{max}}}{2}$

- Other conditions are to be maintain are

  $I_{CEO} \leqslant I_{C_Q} \leqslant I_{C_{sat}}$ or $I_{C_{max}}$

  $V_{CE_{sat}} \leqslant V_{CE_Q} \leqslant V_{CE_{max}}$

  $V_{CE_Q} I_{C_Q} \leqslant P_{C_{max}}$

  [where $P_{C_{max}}$ or P_D is the max collector dissipation level provided in the specification sheet]

Power Dissipation (Max)

Denoted by $P_{C_{max}}$ or P_D

Defined by $\boxed{P_{C_{max}} = V_{CE} I_C}$

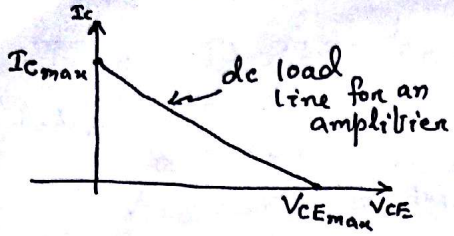
Note This max rating is decreased 5 mW for every 1° rise in temperature above 25°C.

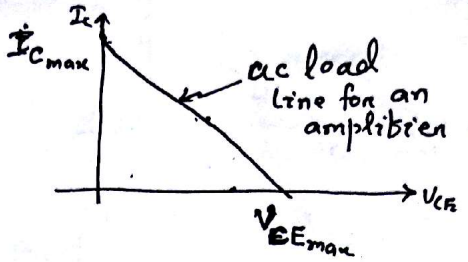
(Q) How to draw max rating curve in a characteristic curve if $P_{C_{max}}$ or P_D is specified for a BJT ? Explain pictorially.

Load Line

The line between max o/p voltage & max o/p current in the device output side used as amplifier.

The amplifier uses two voltages, one is constant dc bias voltage and other one is ac signal voltage. So two load lines can be defined for one amplifier ckt.





- Two load lines intersect at a point, that point is Q-pt.

- AC load line gives the idea of max change of o/p current & o/p voltage in the device due to application of ac signal.

DC Load line –

$$I_{emax} \text{ or } I_{csat} = \frac{\text{DC Voltages at o/p loop}}{\text{Resistance at o/p loop}} \quad \Big| \text{ short ckt the device}$$

$$V_{CEmax} = \text{DC Voltages at o/p loop} \quad \Big| \text{ open ckt the device}$$

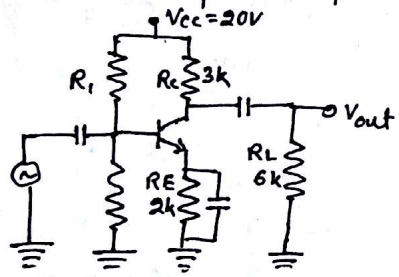
AC Load line –

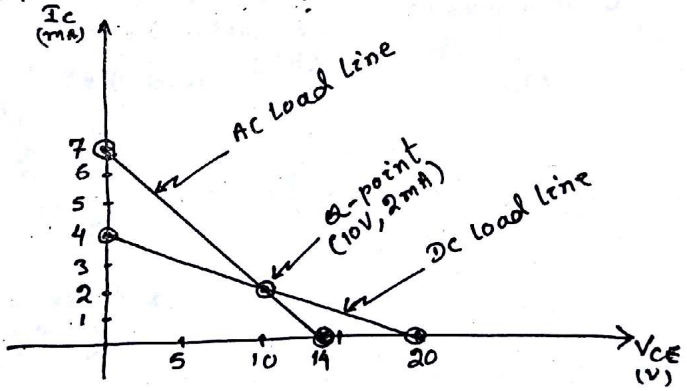
$$I_{csat} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$$

$$V_{cmax} = V_{CEQ} + I_{CQ} R_{ac}$$

where R_{ac} = Available load resistance at o/p side

Example Find & draw dc & ac load line of the CE ckt given & what is the max peak-to peak signal that can be obtained?





DC Load line

$$I_{csat} = \frac{V_{CC}}{R_C + R_E} = 4\,mA$$

$$V_{CEmax} = V_{CC} = 20V$$

Q-pt Calculated

$$(V_{CEQ}, I_{CQ}) = (10V, 2\,mA)$$

AC load line

$$R_{ac} = R_C \| R_L = 2k$$

$$\therefore I_{csat} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} = 7\,mA$$

$$V_{CEmax} = V_{CEQ} + I_{CQ} R_{ac} = 14V$$

For Max Peak

$I_{CQ} * R_{ac} = 4V$ = Max peak o/p signal

So Max Peak to Peak o/p signal

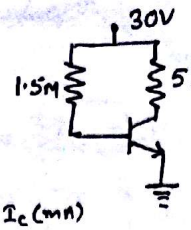
$= 2 \times 4V = 8V$.

Note If the voltage gain of the amplifier is 40 then the max i/p signal that should give an unclipped o/p signal is.

$$V_i = \frac{V_{out}}{A_V} = \frac{8V}{40} = 0.2V$$

So V_i should be peak to peak of 0.2V.

DC Load line for an Amplifier



Assume $\beta = 100$ & Ideal BJT means $V_{BE} = 0V$

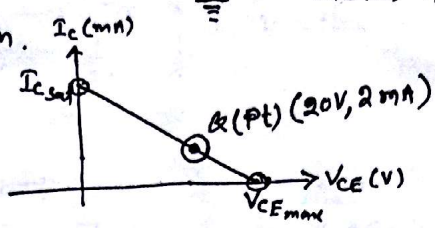
So $I_{Csat} = \frac{30V}{5k} = 6mA$

$V_{CEmax} = 30V$

Load eqn $I_C = -\frac{V_{CE}}{R_C} + \frac{V_{CC}}{R_C}$

Here $y = -mx + C$ straight line eqn.

having slope $m = -\frac{1}{R_C}$



calculated $I_{CQ} = 2mA$

$V_{CEQ} = 20V$ for the ckt.

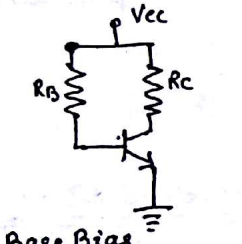
Defn of Q-Point / Bias Point / Operating Point.

It is the point on the dc load line, which represents the value of I_C & V_{CE} that exists in a BJT ckt (amplifier) when there is no i/p signal is applied.

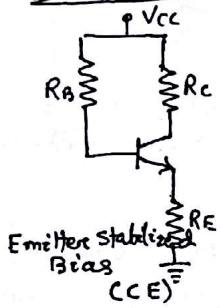
If there is a change in R_B & β occures the Q-pt shifted on the load line.

For best position of the Q-pt for max use of amplifier ckt is mid point of the load line.

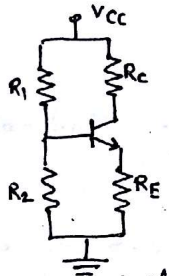
Different Bias Arrangement



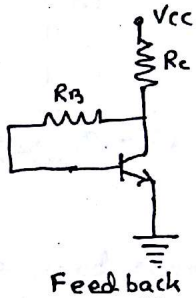
Base Bias or Fixed Bias (CE)



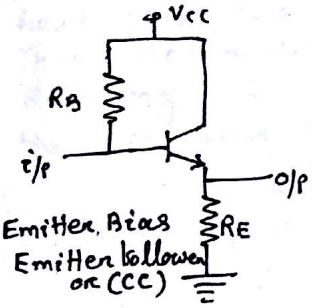
Emitter Stabilized Bias (CE)



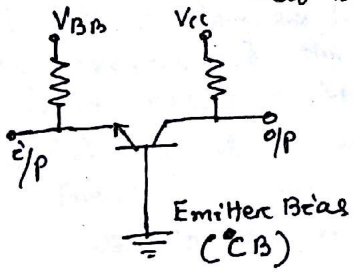
Voltage Divider Bias or Self Bias (CE)



Feedback Bias or Collector to Base Bias (CE)



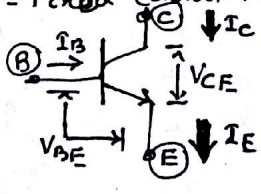
Emitter Bias Emitter Followed or (CC)



Emitter Bias (CB)

DC Analysis

- Learn how to draw dc load line for different ckt
- Learnn how to locate Q-pt.
- To find out I_{BQ} = Fixed Base Current, I_{CQ} = Fixed Collector Current.
  I_{EQ} = Fixed Emitter Current.



- To find out terminal voltages of the device.
  V_{CE} = Voltage betn Collector & Emitter
  V_{BE} = Voltage betn Base & Emitter
  V_{CB} = Voltage betn Collector & Base.
- To find out terminal voltages w.r.t. reference, or ground.
  V_B = ?
  V_C = ?
  V_E = ?