Ghanashyam Rout — (2)

KIIT UNIVERSITY, BHUBANESWAR

Re-Mid Semester Examination-Spring'2014

DIGITAL ELECTRONIC CIRCUITS

[EC-402]

Full Marks: 25 **Duration: 2Hrs**

Answer all five questions.

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

(1) a) For what minimum value of propagation delay in each flip-flop will a 10 bit ripple counter skip a count when it is clocked at 10 MHz? [1x5]

b) Differentiate synchronous and asynchronous input terminals of flip-flop, explain with the help of J-K FF.

c) What is *don't care term* and how can such term arise in practice?

d) Define (i)Self-complementing code,(ii)Sequential codes. Give examples of both.

e) Show that, $AB+\bar{A}C+BCDE = AB+\bar{A}C$

(2) a) Design a MOD-6 synchronous up-counter using JK-FFs. [2.5]

b) Using 2-4 decoders (having enable input) design 3-8 decoder with enable input so that the new 3-8 decoder can be used for further expansion. [2.5]

(3) a) Implement 4-bit odd parity generator using a multiplexer having three select lines. [2.5]

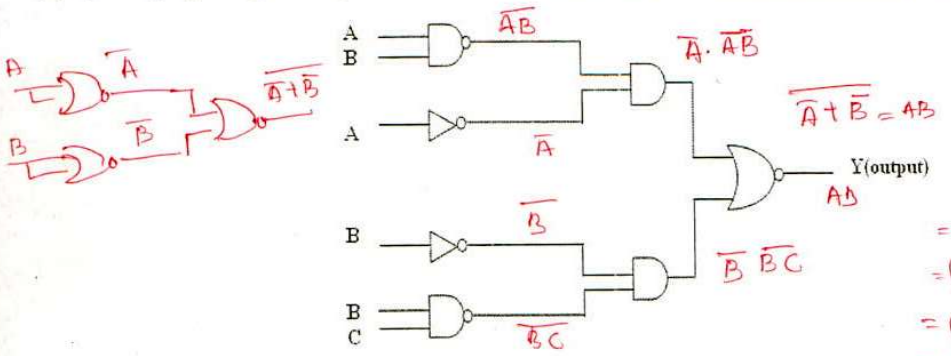
b) Design J-K Flip-Flop using **2:1 MUX** and a **T Flip-Flop.** [2.5]

(4) a) Obtain the minimized expression for the following 4-varible Boolean expression using K-map method and implement the minimized expression using NAND gates only. [2.5]

$F(P,Q,R,S) = \Pi M(0,1,4,10,11,14).d(2,7,8,13)$

b) Design a 4:2 priority encoder using given priority order **priority order : $D_2 > D_1 > D_3 > D_0$.** [2.5]
where D_3, D_2, D_1 and D_0 are input lines of encoder.

(5) a) Simplify the given logic circuit and implement the simplified circuit using only NOR gates. [2.5]



$\overline{\bar{A}\cdot\overline{AB} + \bar{B}\cdot\overline{BC}}$

$= \overline{\bar{A}\cdot\overline{AB}} \cdot \overline{\bar{B}\,\overline{BC}}$

$= (\bar{\bar{A}} + \overline{\overline{AB}})\,(\bar{\bar{B}} + \overline{\overline{BC}})$

$= (A + AB)(B + BC)$

$= A(1+B)\,B(1+C) = AB.$

b) Draw the circuit diagram of (i)MOD-6 Johnson counter (ii)MOD-4 Ring counter and compare N-bit Ring & Johnson counter from modulus and decoding circuit point of view. [2.5]

$\overline{\overline{AB}} = AB$

$\overline{A+B}$

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