8. (a) Design a Priority Encoder circuit having priority D2>D0>D3>D1; where D1,D2,D3,D4 are input to the encoder. [4]

(b) Compare with circuit diagram of 4-bit Ring & Johnson counter from modulus and decoding circuit point of view. [4]

*****

Pass word: 1OKM6

1 OKM 6

SPRING END SEMESTER EXAMINATION-2019

4th Semester B.Tech & B.Tech Dual Degree

DIGITAL ELECTRONICS

EC-2011

(For 2018(L.E) & 2017 Admitted Batches)

Time: 3 Hours Full Marks: 50

Answer any SIX questions.
Question paper consists of four sections-A, B, C, D.
Section A is compulsory.
Attempt minimum one question each from Sections B, C, D.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

SECTION-A

1. Answer the following questions. [1 × 10]

(a) "NAND gate follow commutative law but does not follow associative law"-Show how?

(b) Show that $\mathbf{AB + \bar{A}C = (A + C)\,(\bar{A} + B)}$ where A, B and C are Boolean variables.

(c) What is a priority encoder?

(d) Assume that a 4-bit Ripple counter is holding the count 0110. What will be the count after 31 clock pulses? $(0101)_2$

(e) Show how 1-bit Magnitude Comparator can be implemented in a decoder.

(f) Compare between Mealy and Moore State machines.

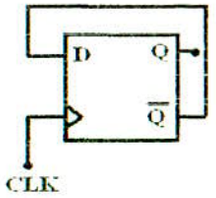
(g) Define Modulus of a Counter.

(h) Define the 'Resolution' of a digital to analog converter and calculate the resolution (in %) of a 10-bit digital to analog converter.

= 0.097

(i) Draw the logic diagram of CMOS Inverter.

(j) For the circuit given below find the frequency of output (Q) waveform if clock signal frequency is 10 MHz(Assume initially Q = 0).



SECTION-B

2. (a) With the help of a neat diagram, explain the working of a TTL NAND gate with Open-Collector Output and also mention the advantages of this configuration. [4]

   (b) What is Decoder? Explain it with a block diagram and Construct a 4:16 line decoder using 2-4 line decoder. [4]

3. (a) With the help of a neat diagram, explain the working of a 4-bit Successive Approximation type ADC with Analog input of 12.6 V. Find the digital output. What would be its conversion time if clock frequency is 1 MHz? If the analog input voltage is now increased to 14.8 V, what would be the new conversion time? Explain. [4]

   (b) Define the terms: [4]

   i) Threshold voltage ii) Fan-in iii) Fan-out iv) Noise Margin

SECTION-C

4. (a) Simplifythe following 4-variable Boolean expression using K-map method and implement the simplified expression using NOR gates only. [4]

   F(A,B,C,D) = ∑m (11,12,14) + ∑d (3,4,6)

   (b) Realize the logic function **F(P,Q,R,S) =P $\bar{Q}$ + R$\bar{S}$ + P$\bar{R}$** using 8:1 MUX.But8:1 MUX IC's are not available hence; use 4:1 MUX and 2:1 MUX to implement 8:1 MUX. [4]

5. (a) Construct a Synchronous counter that goes through states 0,2,3,5,6,7,0,2,3..... using S-R FFs.(Consider unused states as don't cares.) [4]

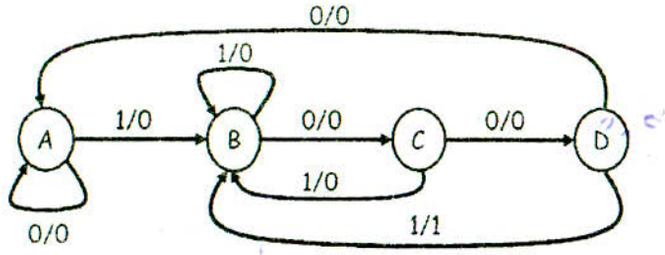
   (b) Construct a shift register using JK flip flop which will take 4 clock cycles for loading the data and 3 clock cycles for outputting it. Explain its operation briefly. [4]

6. (a) Analyse a BCD to Seven segment Display circuit with proper diagram. [4]

   (b) Construct a MOD-5 Asynchronous, Up counter using positive edge-triggered D Flip-Flops. [4]

SECTION-D

7. (a) Consider the following state diagram for a synchronous sequential circuit with one input **X** and one output **Z**. Analyse this state diagram and develop its circuit implementation using **JK flip-flop.** [4]



   (b) Design a combinational logic circuit that compares two 2 bit numbers, A and B, and determines their relative magnitudes. A>B, A<B, A=B. [4]

SPRING END SEM EXAMINATION-2019

DIGITAL ELECTRONICS (EC-2011) – SOLUTION & MARKING SCHEME

SECTION-A

Q.1

a) For AND function,
Commutative : $AB = BA$
Associative : $(AB)C = A(BC)$ [0.5]

For NAND function, $\overline{AB} = \overline{BA}$ → follow Commutative Law. [0.5]
But $(\overline{(AB)}.C) \neq (A(\overline{BC}))$ - does not follow Associative law.

b) L.H.S

$AB + \bar{A}C$

$= AB + \bar{A}C + BC$ [Apply Consensus Law] [0.5]

$= A\bar{A} + AB + \bar{A}C + BC$ [Since, $A\bar{A} = 0$]

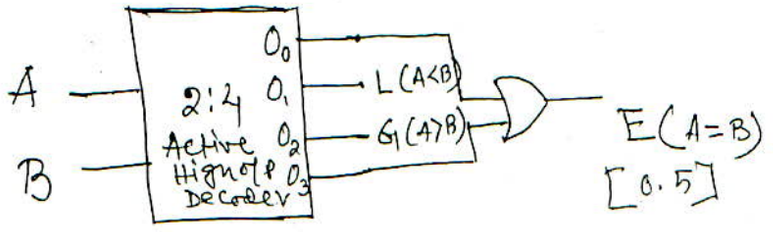
$= A(\bar{A} + B) + C(\bar{A} + B)$

$= (\bar{A} + B)(A + C)$. R.H.S. [0.5]

c) Priority encoder is an encoder that includes the priority function. The operation of the priority encoder is such that if two or more I/P's are HIGH at the same time, the I/P having the highest priority will take precedence. [1]

d). After 31 clock pulses count will be $(0101)_2$ [1]

e).



[0.5]

$L = \bar{A}B$

$G = A\bar{B}$ [0.5]

$E = A \odot B$

f). Mealy Model

i) It's o/p is a function of PS as well as Present i/p.

ii) I/p changes may affect the o/p of the ckt.

Moore Model [1]

i) It's o/p is a function of PS only.

ii) I/p changes do not affect the o/p.

g). The Modulus of a Counter is the total number of states it sequences through in each complete cycle. [0.5]

MOD Number $\leq 2^n$ [0.5]

Where, n = no. of FFs.

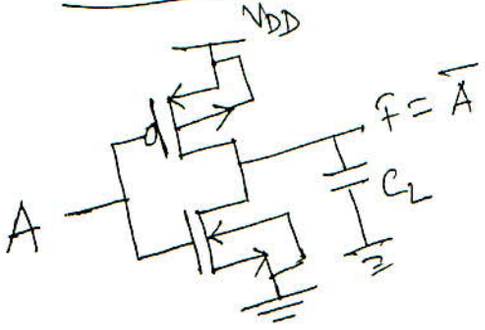
h). Resolution of DAC is defined as the smallest changes that can occur in the Analog o/p as a result of a change in the digital i/p. [0.5]

$$\% \text{ of Resolution} = \frac{1}{2^n - 1} \times 100$$

[here, $n = 10$]

$$= 0.097 \quad [0.5]$$

i) CMOS Inverter [1]



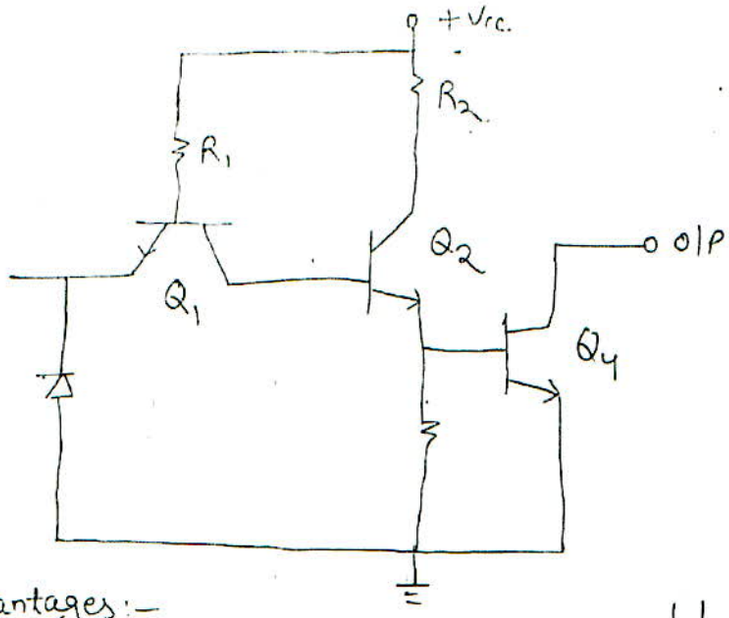
j). Q-output is a one-half the frequency of the clock input, it used as a divide-by-2 device. [0.5]

So, the o/p frequency will be $= \frac{10}{2}$

$= 5$ MHz [0.5]

Section-B

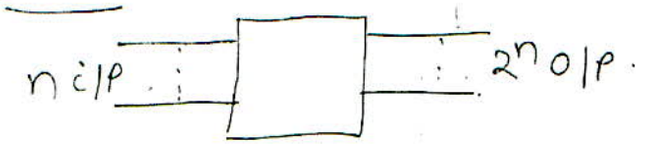
2(a) A TTL NAND Gate with open collector O/P :- L3



Advantages :- L1

Open collector may also be used to drive non gate loads such as LEDs, Small Solenoids etc as long as the load voltage and current is within the rating of open collector device.

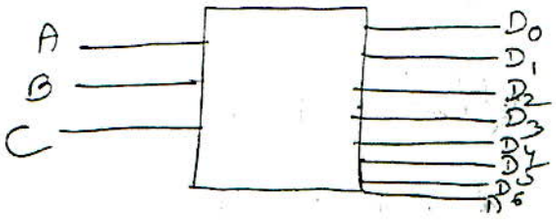
(b) Decoder :- L1 L5



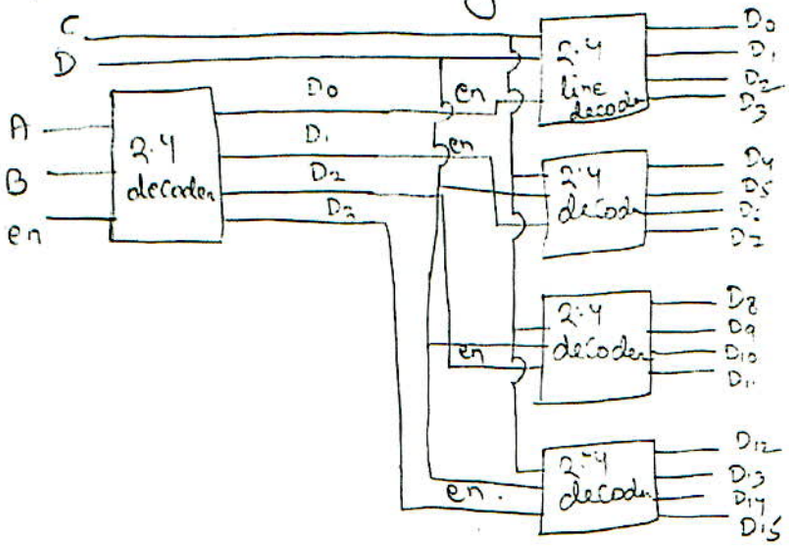
Decoders are used for Seven Segment display and memory address decoding.

Example :-

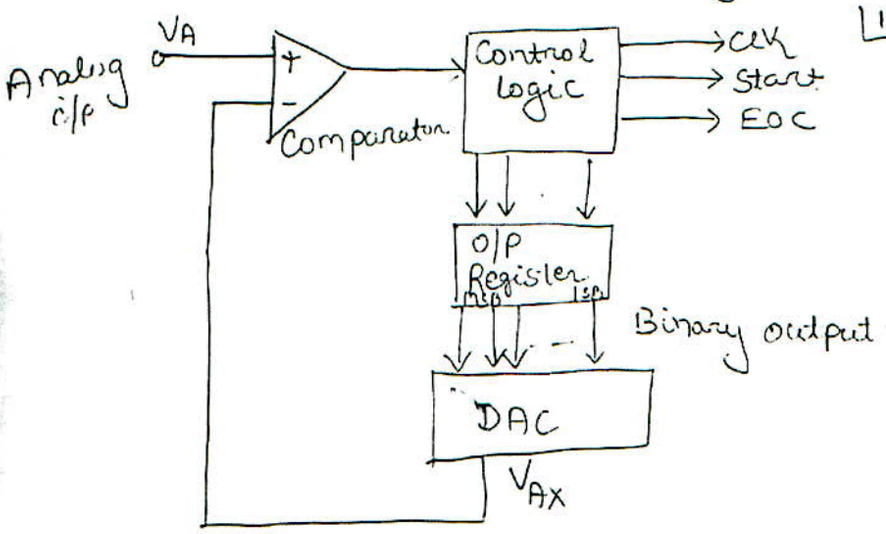
3 to 8 line decoder



4 to 16 line decoder using 2-4 line decoder :- 2.5



3(a) 4-bit Successive Approximation Type ADC



1

Explanation for 12.6V i/p 1

Conversion Time = 1

$(2^N - 1) \times 1$ clk cycle

$= 2^N \times 1\text{MS}$

$= 4 \times 1\text{MS} = 4\text{MS}$

Explanation for voltage 14.8 V o/p [1]

(b) Threshold voltage [1]

Fan-In [1]

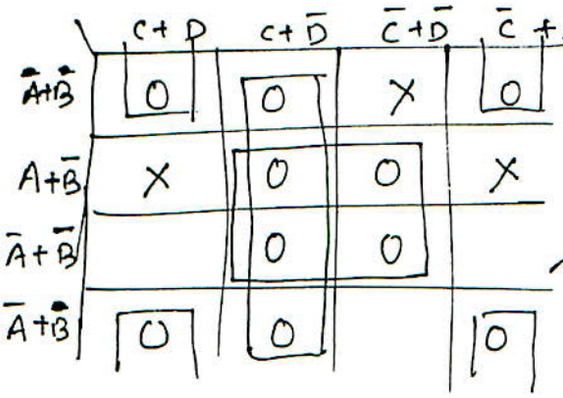
Fan-out [1]

Noise margin [1]

4 a:

$P(A,B,C,D) = \sum[m(11,12,14) + d(3,4,6)]$

$= \prod[M(0,1,2,5,7,8,9,10,13,15) \cdot d(3,4,6)]$

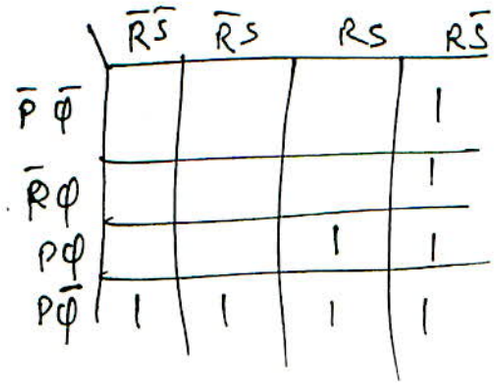


→ 3 quads [2]

$P = (B+D)(C+\bar{D})(\bar{B}+\bar{D})$

Diagram - [2]

b $F(P,Q,R,S) = P\bar{Q} + R\bar{S} + PR.$

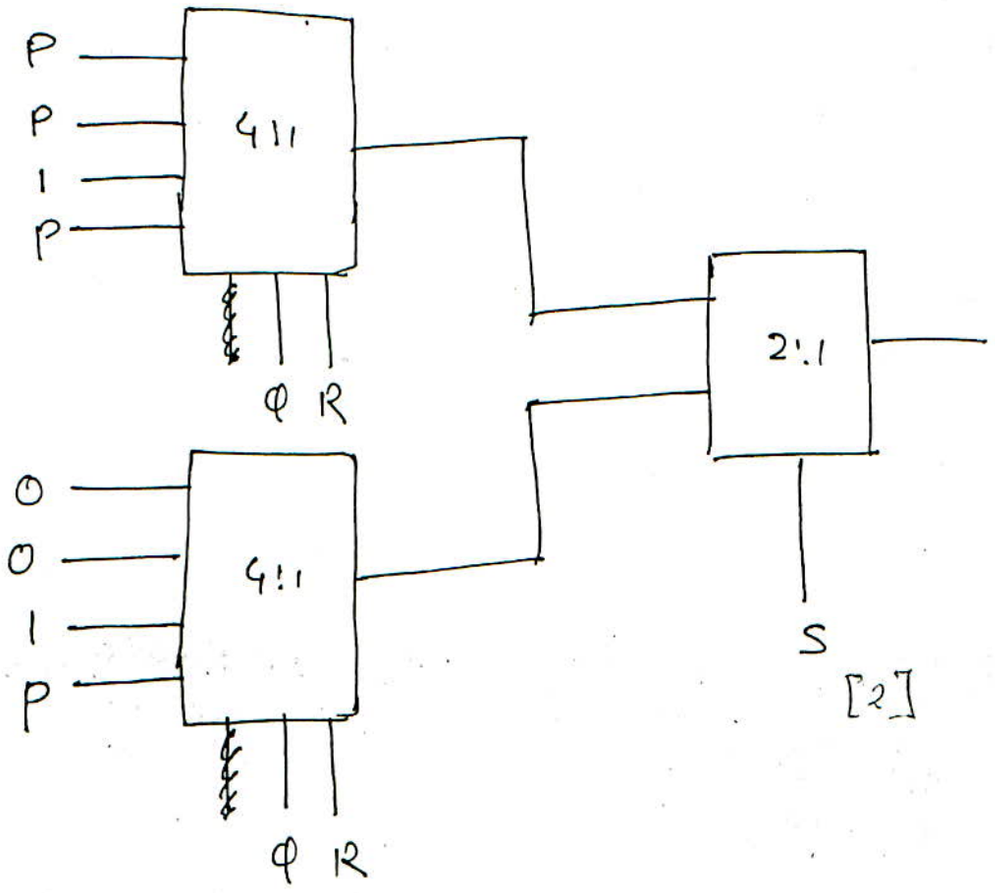


$\Rightarrow F(P,Q,R,S)$

$= \sum m(2,6,8,9,10,11,14,15)$

	$\bar{\varphi}R\bar{S}$	$\bar{\varphi}\bar{R}S$	$\bar{\varphi}RS$	$\bar{\varphi}RS$	$\varphi\bar{R}\bar{S}$	$\varphi\bar{R}S$	$\varphi R\bar{S}$	φRS
$\bar{P}$	0 0	0 1	1 2	0 3	0 4	0 5	1 6	0 7
P	1 8	1 9	1 10	1 11	0 12	0 13	1 14	1 15
$F = P$	P	1	P	0	0	1	P	

[2]



[2]

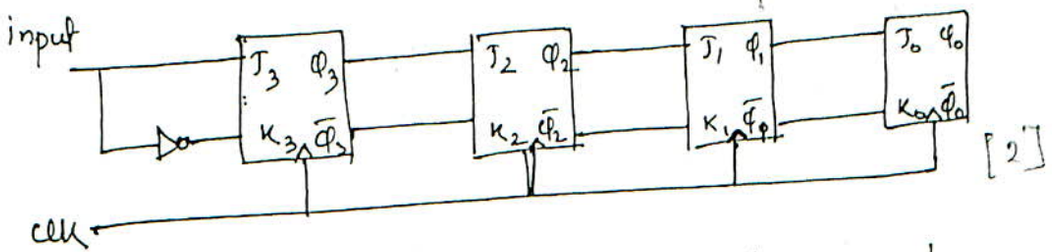
Note: If P, φ, R are kept as the select lines in the order, then the inputs from top to bottom will be $0, \bar{S}, 0, \bar{S}, 1, 1, 0, 1$ successively.

$S_2 = \bar{Q}_2 Q_0$ | $S_1 = \bar{Q}_1$ | $S_0 = Q_1 \bar{Q}_0$

$R_2 = Q_2 Q_1 Q_0$ | $R_1 = Q_1 Q_0$ | $R_0 = Q_2 Q_0$ [2]

Make the circuit diagram. – [1]

Qno 5 (b) 4bit SISO shift register using J-K FF.

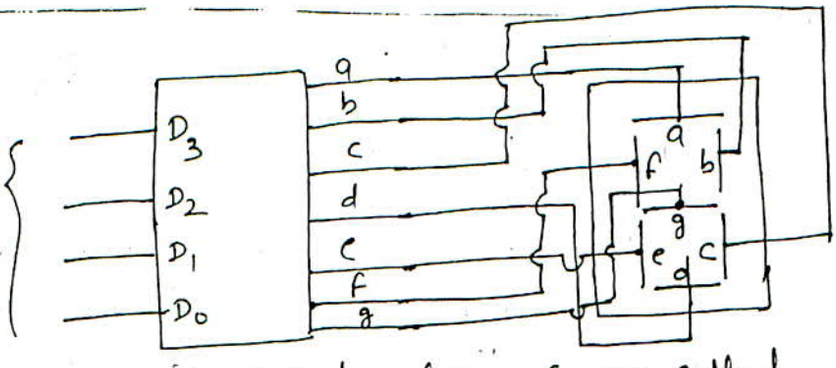


[2]

Timing Diagram (Change in state of FF's with each clock pulse)

Brief working – [2]

Qno 6 a.



$a = \Sigma m(0, 2, 3, 5, 6, 7, 8, 9) + d(10\text{-}15)$

$b = \Sigma m(0, 2, 3, 4, 7, 8, 9) + d(10\text{-}15)$ [2]

$c = \Sigma m(0, 1, 3, 4, 5, 6, 7, 8, 9) + d(10\text{-}15)$

$d = \Sigma m(0, 2, 3, 5, 6, 8, 9) + d(10\text{-}15)$

$e = \Sigma m(0, 2, 6, 8) + d(10\text{-}15)$

$f = \Sigma m(0, 4, 5, 6, 8, 9) + d(10\text{-}15)$

$g = \Sigma m(2, 3, 4, 5, 6, 8, 9) + d(10\text{-}15)$

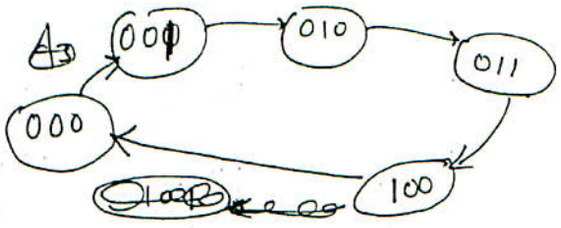
Analysis – [1]

Que 6 b Three steps:

(i) Make a basic MOD-8 using T FF (+ve edge)

(ii) " " " " " D FF

(iii) Using clr/Pre convert MOD 8 to MOD 5

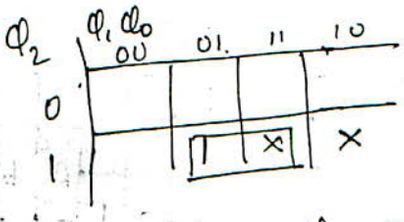


[1]

After 100, as soon as output goes to 101, it should be changed to 000.

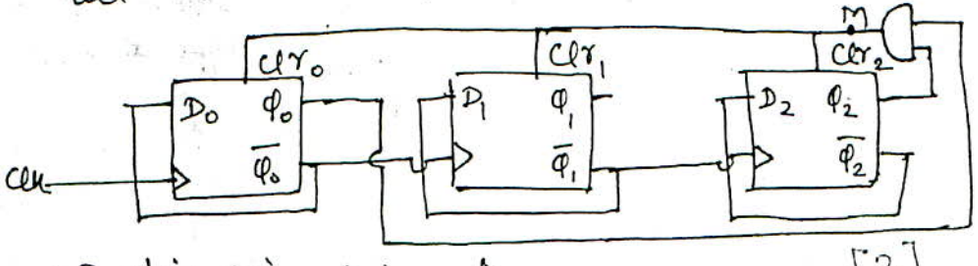
To remove ~~to~~ We can also use the states 110, 111 as don't cares.

M



$M = Q_2 Q_0$

M being the input which will control the clr inputs of all FF. When M = 1 all the ffs must be cleared.



Explain using timing diagram.

[3]

SECTION-D

7).

a).

State Table

PS	NS, o/p	
	x=0	x=1
A	A, 0	B, 0
B	C, 0	B, 0
C	D, 0	B, 0
D	A, 0	B, 1

[1]

State Assignment

$y_1 y_0$ ← state variables

A → 00
B → 01
C → 10
D → 11

Excitation Table [1]

PS	i/p	NS		I/P to FF		o/p
$y_1 y_0$	x	Y_1^+	Y_0^+	$J_1 K_1$	$J_0 K_0$	Z
0 0	0	0	0	0 X	0 X	0
0 0	1	0	1	0 X	1 X	0
0 1	0	1	0	1 X	X 1	0
0 1	1	1	1	0 X	X 0	0
1 0	0	1	0	X 0	1 X	0
1 0	1	1	1	X 1	1 X	0
1 1	0	0	0	X 1	X 1	0
1 1	1	0	1	X 1	X 0	1

From the excitation & o/p maps, the simplified expression for J_1, K_1, J_0, K_0 & Z are given by,

$J_1 = y_0 \bar{x}$; $J_0 = y_1 + x$; [1]

$K_1 = y_0 + x$; $K_0 = \bar{x}$; [1]

& $Z = y_1 y_0 x$

Logic Diagram (As per expression). [1]

b). Let two 2-bit numbers be $A = A_1 A_0$ & $B = B_1 B_0$.

The logic for 2-bit magnitude comparator.

(i) Logic Expression for (A > B).

$G(A>B) = A_1 \bar{B}_1 + (A_1 \odot B_1) \cdot (A_0 \bar{B}_0)$

(ii) Logic expression for A < B.

$L(A<B) = \bar{A}_1 \cdot B_1 + (A_1 \odot B_1) \cdot (\bar{A}_0 \cdot B_0)$

iii) Logic Expression for A = B

$E(A=B) = (A_1 \odot B_1) \cdot (A_0 \odot B_0)$. [2]

Logic Diagram As per Expression. [2]

8) a) $D_2 > D_0 > D_3 > D_1$

Truth Table

I/P's				O/P's		
D_0	D_1	D_2	D_3	A	B	V
0	0	0	0	X	X	0
1	X	0	X	0	0	1
0	1	0	0	0	1	1
X	X	1	X	1	0	1
0	X	0	1	1	1	1

[1.5]

$A = \sum m(1,2,3,5,6,7,10,11,14,15) + \sum d(0)$

$B = \sum m(1,4,5) + \sum d(0)$

Simplified expression for A, B & V are given by,

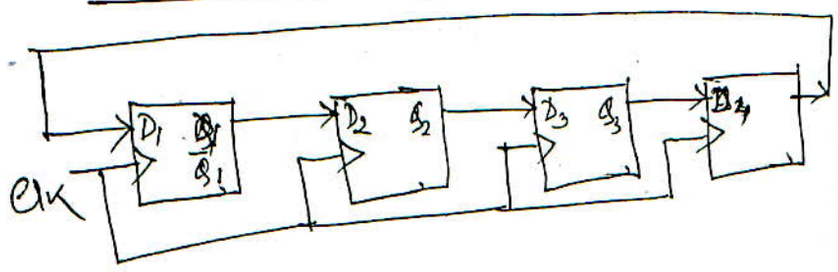
$A = D_2 + \overline{D_0}\,D_3$ [1.5]

$B = \overline{D_0} \cdot \overline{D_2}$

$V = D_0 + D_1 + D_2 + D_3$

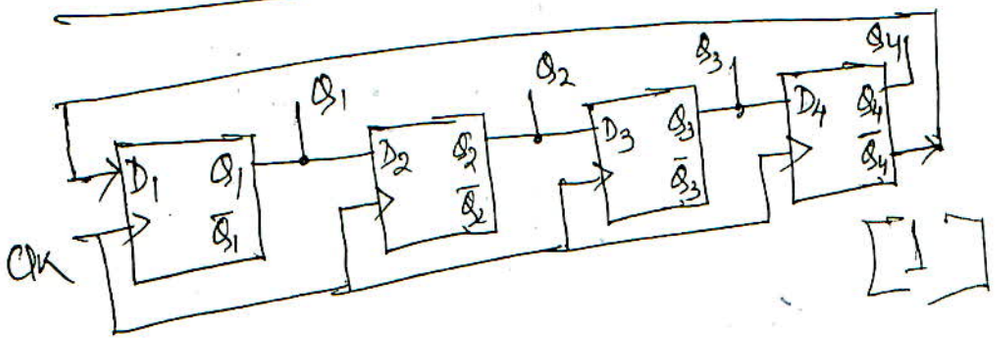
Logic Diagram as per expression. [1]

b). 4-bit Ring Counter



[1]

4-bit Johnson Counter.



[1]

Comparision: [2]