Mid-Semester Examination
School of Computer Engineering
KIIT University, Bhubaneswar-24

Time: 2hrs *Sub-COA* *B.Tech-6TH Sem.* *Full Marks: 25*

(Answer Question no-1 of Part-A and any three from Part-B)

PART-A [2X5=10]

1. a) Discuss different functional units of a digital computer system with its block diagram.
   b) A relative mode branch type instruction is stored in memory at an address 750. The branch is made to an address 500. What should be the value of the relative address field of the instruction?
   c) What is difference between write-through and write-back protocol?
   d) A computer has 58 instructions; each instruction requires at most 15 steps to complete its execution. What will be the specification of instruction and step counter decoder used in hardware control unit design?
   e) A processor is connected to 256GX32 memory module. What is the size of MAR and MDR registers?

PART-B [5X3=15]

2. [2.5×2]
   a) Explain Basic-Operational-Concepts of a computer system with the help of a block diagram.
   b) Write down the sequence of instructions for the execution of the following statement:
   X = (A-B)*(C+D) using,
   a. Zero addresses instructions b. One address instructions
   c. Two address instructions d. Three address instructions

3. [2.5×2]
   a) Discuss multi bus organization of a data path inside a processor with the help of a block diagram. Write down the control sequence of the instruction ADD (R_1), R_2, R_3 in three-bus organization, where (R_1), R_2 are used as source operand and R_3 is used as destination operand.
   b) An instruction is stored at location 500 with its address field at location 501. The address field contains the value 80. The contents of a processor register R_1 and an Index Register XR are 501 and 321 respectively. Determine the effective address and data operand (if any), if the addressing mode of the instruction is: (i) Direct (ii) Immediate (iii) Register indirect (iv) Relative (v) Index

4. [2.5×2]
   a) Outline the design principle of a hardwired control unit with necessary block diagram.
   b) Explain the operation of single-bus organized processor with necessary diagrams and its advantages and disadvantages over multi bus organized processor.

5. Write Short notes on **any two** of the following: [2.5×2]
   i. Memory Hierarchy and Locality-of-reference
   ii. Arithmetic, Logical and Shift Instructions
   iii. Microprogrammed control unit

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