

## KIIT UNIVERSITY, BHUBANESWAR SPRING MID SEMESTER EXAMINATION-2015

## DIGITAL ELECTRONIC CIRCUITS

[EC-2009]

Full Marks: 25 Duration : 2Hrs

Answer any FIVE questions including question No.1 which is compulsory.

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

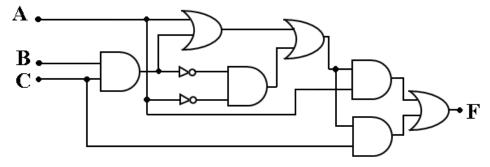
(1) a) "Gray codes are cyclic but not sequential & self-complementing." Justify. [1x5]**b)** Perform following arithmetic: (i) BCD subtraction (943 - 458), (ii) (-21) - (-13) using 2's complement method. Show that,  $P \bar{Q} + PR + Q \bar{R} = P + Q \bar{R}$  where P, Q and R are Boolean variables. Implement Half-Subtractor using 2:4 decoder (having active HIGH output lines) and one OR gate. Why the row and column numbers of the K- map are assigned in Gray code rather than e) binary numerical order, explain in brief. **(2)** Obtain the minimized expression for the following 4-variable Boolean expression using [5] K-map method and implement the minimized expression using **only NOR gates.**  $F(W,X,Y,Z) = \sum m (0,2,5,10,11,15) + d(1,3,7)$ (3)a)i) What is the difference between 'Ripple carry adder' and 'Look-ahead carry adder' explain [2+2]in brief. ii) 'A 4-bit adder circuit could be used to convert BCD codes to Excess-3 codes'. Justify this statement using proper circuit diagram in brief. Implement XOR gate using minimum numbers of XNOR gates only. [1] What is Decoder? Draw the circuit diagram and truth table of 2-4 decoder having active-(4)a[2] LOW output terminals. b) Implement the given function 'F' using a 3-8 decoder having active HIGH output [3]

F(P,Q,R) = PQ + QR + PR

terminals and NOR gates only.

- (5) a) Design 4-bit combined adder/subtractor circuit using <u>Full adder modules & XNOR</u> [4] gates only and explain the working in brief.
  - b) If the received 7-bit Hamming code is '1110100' then find the 4-bit data word.

    [Assume (i) Even parity system, (ii) At most single bit error may take place]
- (6) a) Simplify the given logic circuit and implement the simplified expression using <u>only</u> [4] <u>NAND gates.</u>



[1]

- b) Determine the decimal value of the binary string '101011' in
  - (i) Sign-Magnitude form,
  - (ii) Sign-1's Complement form,
  - (iii) Sign-2's Complement form,
  - (iv) Unsigned binary number

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