SUPPLEMENTARY EXAMINATION-2018

4th Semester B.Tech & B.Tech Dual Degree

DIGITAL ELECTRONICS

EC-2011

(For 2016 & 2015 Admitted Batches)

Time: 3 Hours | Full Marks: 60

Answer any SIX questions including question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

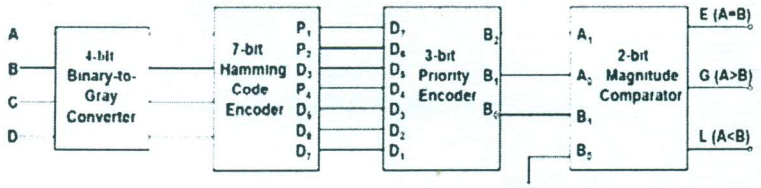
1. (a) Perform following arithmetic: (-30) + 14 using 2's complement method. [1 × 10]
   (b) How does XNOR gate can be used as a BUFFER?
   (c) Prove: $\bar{A} + AB = \bar{A} + B$.
   (d) Find the minterms and maxterms of F = $A + \bar{B}C$.
   (e) Design a half adder using NAND gates only.
   (f) Justify Gray code is reflective and cyclic.
   (g) Design AND gate using 2:4 decoder.
   (h) A 6-bit DAC has a step size of 50 mV. Determine the full-scale output voltage and the percentage resolution.
   (i) Define propagation delay and speed-power product.
   (j) Draw the excitation table of JK flip-flop.

2. (a) Obtain real minimal expression for the function F(A, B, C, D) = ∑m(2, 7, 8, 13) + ∑d(0, 5, 10, 15) using K map and implement the minimal expression using NAND gates only. [4]

(b) Design a 4-bit parallel adder/subtractor circuit using full adders and XNOR gates only and explain its operation in brief. [4]

(c) If $A = B \oplus C$ then find $B \oplus A$. [2]

3. (a) [4]



In the figure given above, ABCD = "1010" is a 4-bit Binary input data. Find all three outputs of the 2-bit magnitude comparator, assuming Odd parity system for Hamming Code Encoder and input line having highest decimal subscript is having the highest priority in the Priority Encoder.

(b) Implement the function $F(A, B, C) = B + \bar{A}C + A\bar{B}C$ using 3:8 active low decoder. [4]

(c) Design 1-bit magnitude comparatorusing 2:4 active high decoder and 2-input gates. [2]

4. (a) Design a 4:2 priority encoder having priority $D_1 > D_2 > D_0 > D_3$ where all D_i's are inputs to the priority encoder. [4]

(b) Implement the function $F(A,B,C,D)=AB + AD + B\bar{C}$ using 8 × 1 MUX. [4]

(c) Draw the block diagram of 4 × 1 MUX using 2 × 1 MUX only. [2]

5. (a) Design JK flip-flop using T flip-flop. [4]

(b) Design a synchronous counter that goes through states 0,1,4,5,7,0, 1, 4, …using JK flip-flops. [4]

(c) Design a 2-input CMOS NOR gate. [2]

6. (a) Explain Counter type analog to digital converter using neat circuit diagram and discuss the disadvantage of this converter. [4]

(b) Design a shift register using D flip-flop which will take 4 clock cycle for loading the data and next 3 clock cycles for outputting it and in total it takes 7 clock cycles. Explain its operation briefly. [4]

(c) Differentiate between Ring counter and Johnson Counter. [2]

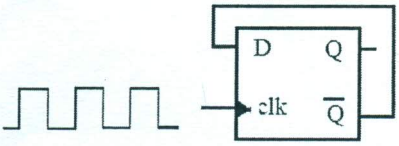
7. (a) With the help of a neat diagram explain the working of a two-input totem-pole TTL NANDgate and also mention advantages of this configuration. [4]

(b) Design a MOD-6 ripple counter using positive edge-triggered D flip-flops. [4]

(c) A 8×1 MUX has inputs A, B, and C connected to the selection lines S_2, S_1, S_0, respectively. The data inputs I_0 through I_7 are as follows: $I_1 = I_2 = I_7 = 0$; $I_3 = I_5 = 1$; $I_0 = I_4 = \overline{D}$; and $I_6 = D$. Determine the Boolean function implemented using the MUX. [2]

8. (a) Design a 2-input 2-output synchronous sequential circuit which produces an output (Z) = 1, when "1011" is detected using J-K flip-flop by Mealy Model designing. Assume Overlapping detection is used. [6]

(b) If the frequency of the clock signal is 50KHz as shown in the below figure then draw the output wave form and find the frequency of the of the output, Q. (Assume that initially D flip-flop is RESET) [4]



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