SPRING END SEMESTER EXAMINATION-2019

4th Semester B.Tech & B.Tech Dual Degree

COMPUTER ORGANIZATION AND ARCHITECTURE

CS 2006

(For 2018(L.E) & 2017 Admitted Batches)

Time: 3 Hours | Full Marks: 50

Answer any SIX questions.
Question paper consists of four sections-A, B, C, D.
Section A is compulsory.
Attempt minimum one question each from Sections B, C, D.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

SECTION-A

1. Answer the following questions. [1 × 10]

(a) Define Von-Neuman architecture. How is it different from Harvard architecture?

(b) Register R_1 and R_2 of a computer contains the decimal value 1200 and 1300. What are the effective address of memory operand in each of the following instruction? Assume second operand is the destination register.

i) LOAD 20 (R_2), R_1

ii) MOVE 300, R_5

iii) ADD (R_1), R_2

iv) MUL (R_1)+, R_5

(c) Compare and contrast between Static RAM cell and Dynamic RAM cell.

(d) Difference between memory mapped I/O and I/O mapped I/O.

(e) Specify the size of instruction decoder and step decoder size if the system supports 20 instruction and maximum 7 steps are required to complete the instruction.

(f) What is the hit ratio of a cache memory if cache memory access time is 30ns and main memory access time is 15ns and average access time is 42ns?

(g) In IA-32, which registers are used to fetch the instruction from memory as the PC does in other processor? Explain.

(h) What is the advantage of stack over link register in implementing subroutine calls?

(i) Assume you have 1 GB of RAM and 4KB of cache with block size of 64 bytes. What are the number of bits for tag, set, word field of 2-way set associative cache mapping respectively?

(j) How the problem associated with polling process is overcome by vectored interrupt technique?

SECTION-B

2. (a) Explain the following addressing mode with suitable example. [4]

i) Relative ii) Auto indexing

A computer has 45 bit instruction. It uses one register operand and one memory operand. There are 128 general purpose registers and 256M bytes of RAM. How many different operations the computer can perform? If there are 450 two address operations which uses both register and memory, then how many one address operations (which use only memory) are possible.[Assume, the system supports only direct addressing mode]

(b) Write the assembly language code segment to evaluate the following arithmetic expression: [4]

X = (A+B*C+D) / (E-F) using the following:

i) RISC instruction format

ii) Stack Organization

3. (a) Differentiate between RISC processor and CISC processor. [4]

(b) Write the IEEE 754 format for representing floating point numbers in single precision and double precision format. Represent the decimal number -20.25 using the IEEE 754 single precision floating point format. [4]

SECTION-C

4. (a) Explain multi-bus CPU organization with suitable diagram. Write control signal for the following instruction. Assume R2 is the destination register. [4]

ADD #50, R_1 , R_2

(b) Define parallel processing .Draw and analyze Flynn's classification of digital computer. [4]

5. (a) Using Booth's multiplication, multiply two numbers (-13) × (-10). Give the flow table of multiplication [4]

(b) Discuss virtual memory organization and explain how virtual address is translated into physical address with suitable diagram. [4]

6. (a) Design micro routine for single bus organization to execute the following instructions. Assume second operand is the destination register. [4]

ADD (R_1)+, R_2

(b) Explain the various data transfer techniques in I/O and briefly explain the working principle of DMA technique. [4]

SECTION-D

7. (a) Define the role of cache memory in memory organization. Why we use the mapping function? Specify the different mapping function name. [4]

A two-way set associative cache memory uses block of 4 words. The cache can have a total of 2048 words from main memory. The main memory size is 128K X 32.

i) Formulate main memory address partition

ii) What is the size of cache with tag bits?

(b) Divide 13 ÷ 4 using restoring and non-restoring technique. Give the flow table of both restoring and non-restoring division. [4]

8. (a) The memory access time is 1 nanosecond for a read operation with a hit in cache, 5 nanoseconds for a read operation with a miss in cache, 2 nanoseconds for a write operation with a hit in cache and 10 nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves 100 instruction fetch operations, 60 memory operand read operations and 40 memory operand write operations. The cache hit-ratio is 0.9. Find the average memory access time (in nanoseconds) in executing the sequence of instructions. [4]

(b) Design 2MX32 memory using 512KX8 memory chip. [4]

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