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AUTUMN END SEMESTER EXAMINATION-2016

3rd Semester B.Tech & B.Tech Dual Degree

DEC

EC-2011

(Regular-2015 Admitted Batch)

Time: 3 Hours **Full Marks: 60**

Answer any Six questions including question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. a) Show that **UV'+UW+VW'=U+VW'**, where U,V and W are Boolean variables. [1 × 10

   b) Perform following arithmetic
      (i) **BCD** addition(956+492)
      (ii) (-14)-(-4) using **2'complement** method

   c) Differentiate between **Decoder** and **Demultiplexer** with examples.

   d) Define **'Fan -In'** and **'Fan-Out'**.

   e) Find the minimum number of Flip-Flops required to design a counter that counts in prime number(2,3,5,...N,2) where **N<50**.

   f) Draw the circuit diagram of **CMOS NOR** gate.

   g) A **8-bit DAC** has a step size of 50mV.Determine full scale output voltage and percentage resolution.

   h) With the help of a **4:1 MUX**, implement a NOT gate.

   i) Draw a **D FF** using JK FF.

   j) Define 'positive logic system' and 'negative logic system'.

2. a) Obtain a minimized expression for the following Boolean Expression using K-map and implement the minimized expression using minimum number of **NAND** gate. [4

$$F(A,B,C,D)=\Sigma m(2,3,6,9,12).\Sigma d(5,8,15)$$

b) Design a **JK FF** using a D FF, a 2X1 MUX and a NOT gate. [4

c) State the difference between Mealy Model and Moore Model. [2

3. a) Design a 4:2 Priority Encoder such that the order of priority of the decimal inputs is given as $D_1>D_0>D_2>D_3$, where all Di's are inputs to the Priority Encoder. [4

b) Design a 4-bit **look-ahead carry adder** and explain how does the look-ahead carry adder speeds up the addition process. [4

c) '**XOR** and **XNOR** gates can be used as a buffer as well as an inverter'. Justify. [2

4. a) Design a synchronous sequential circuit using **Mealy Model** and **D FF** which produces an output an output Z = 1, when "**1001**" is detected. Assume Overlapping detection is used. [6

d) Draw and explain the operation of **Successive Approximation** type ADC. [4

5. a) Design a **Synchronous Counter** that goes through the states **0,1,4,5,7,0,1,...** using **D FF**. [4

b) Implement a **Full Subtractor** using a MUX having 2 select lines. [4

c) Convert (i) $(1A53)_{16}$ to decimal [2

(ii) $(734)_8$ to hexadecimal

6. a) Draw a logic diagram of a **4-bit PISO** Shift Register using **JK FF** and explain its operation. [4

b) Design a combinational circuit that converts **BCD to Excess-3** Code using minimum number of NAND gates. [4

c) Compare **N-bit Ring Counter, Johnson Counter and Ripple Counter** from modulous and decoding circuit point of view. [2

7. a) With the help of a neat diagram explain the working of **ECL OR/NOR** gate. [4

b) Design an Asynchronous **MOD-5** Up Counter using DFF only. [4

c) Differentiate between '**error detecting**' and '**error correcting**' codes. [2

8. a) Design a **2-bit Magnitude Comparator** using two 1-bit Magnitude Comparator and basic gates. [4

b) With the help of a neat diagram,explain the working of a **TTL NAND** gate with Totem Pole output and also mention the advantage of this configuration over open-collector output [4

c) Encode the 4- bit data **1000** into 7-bit Hamming Code [2

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