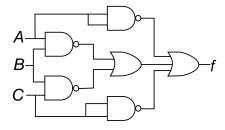
KIIT Deemed to be University AUTUMN MID-SEMESTER EXAMINATION –2018 DIGITAL ELECTRONICS (EC-2011), BRANCH: CSE, IT, CSSE, CSCE

Full Marks: 20 Duration: $1\frac{1}{2}$ hr

- Answer any FOUR questions including question No.1 which is compulsory.
- Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.
- 1. a) Perform following arithmetic: (i) **BCD Subtraction** (657-589) [1x5] (ii) (-14) (-6) using 2's complement method
 - b) What is a Carry Look Ahead Adder? What is its advantage over Ripple Carry adder?
 - c) Design a **XNOR** gate using *NAND logic*.
 - d) If we transmitted a 7-bit **even parity hamming code** through a noisy channel and at the receiver we obtained '1001001'. Decode the correct 4-bit data word.
 - e) Implement a 1 Bit Magnitude Comparator in a decoder circuit.
- 2. Obtain a minimized expression for the following Boolean function using **K-map** and [5] implement the minimized expression using 2-input **NAND gates** only.

$$F(A,B,C,D) = \sum_{i} m(1,5,6,12,13,14) + d(2,4)$$

- 3. a) Implement a **Full-Sub tractor** in an **Active Low Decoder** Circuit and using **2-input** gates [3] only.
 - b) **Simplify** and **minimize** the output(f) of the logic circuit given below: [2]



- 4. a) Design a combinational circuit with three inputs x, y, and z, and three outputs A, B, and [3] C. When the binary input is **0**, **1**, **2**, **or 3**, the binary output is **two greater** than the input. When the binary input is **4**, **5**, **6**, **or 7** the binary output is **three less** than the input.
 - b) "Minterms and Maxterms are **complement** of each other". Justify [2]
- 5. a) Design and explain a **4-bit Binary Adder-Subtractor** circuit using Full Adders and [3] **XNOR** gates only
 - b) Show: $AB + \overline{A}C + BCD = AB + \overline{A}C$ [2]