Multiplexer

Lecture by

Ganaraj P S

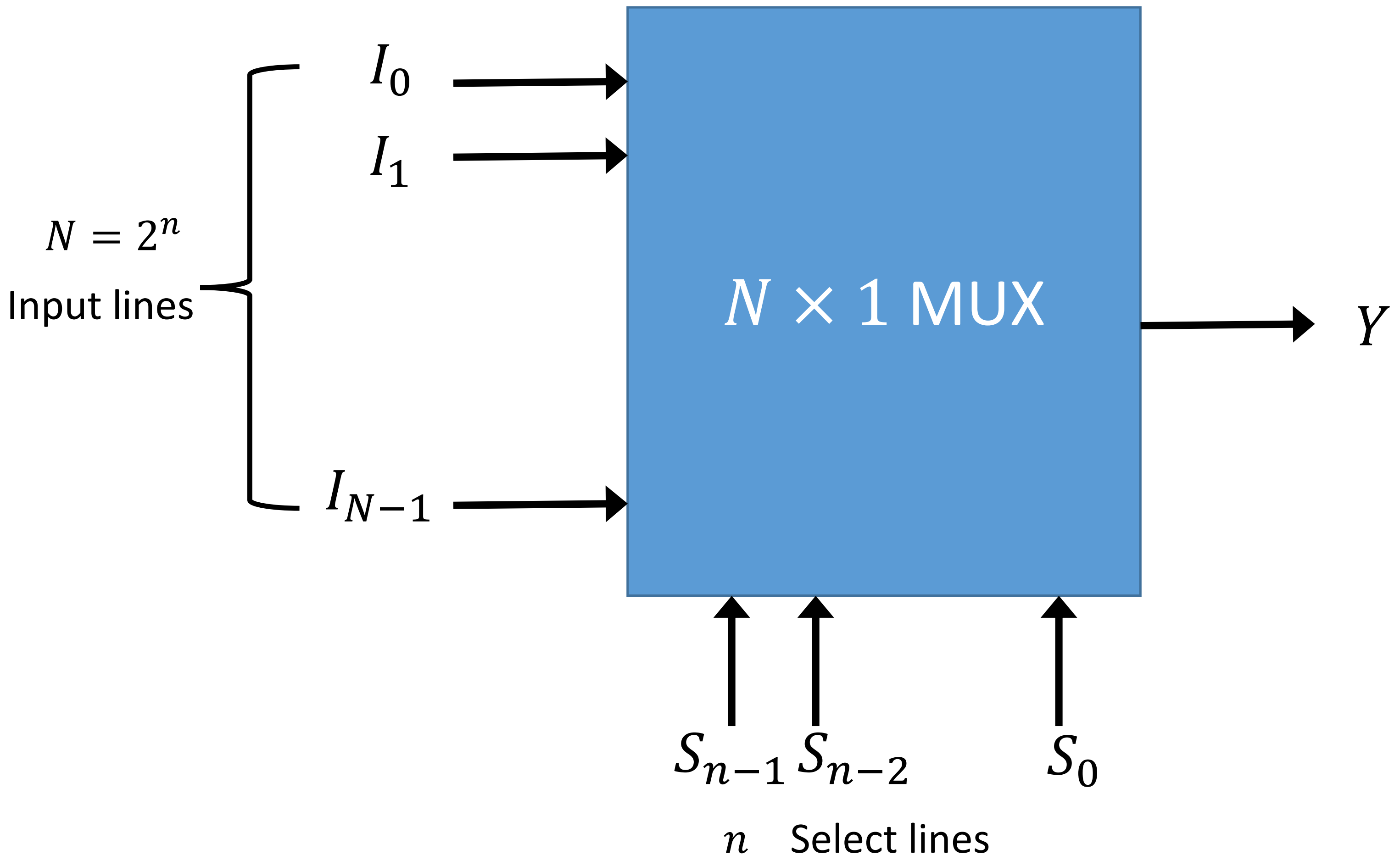
School of Electronics Engineering

Outline

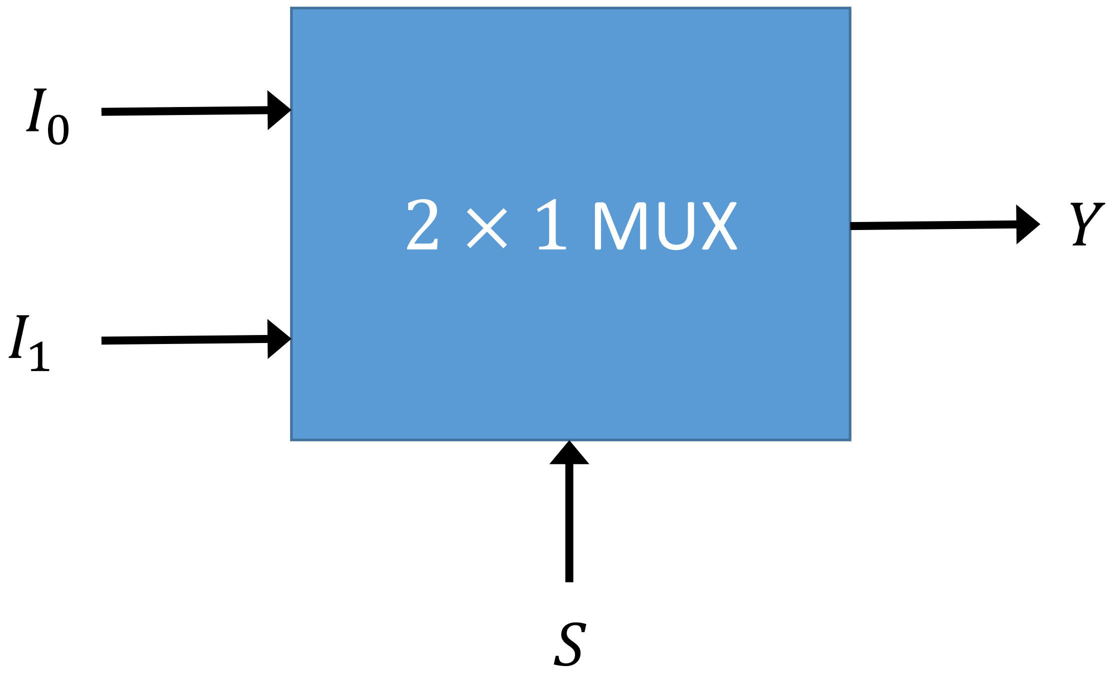
- 2×1 Multiplexer
- 4×1 Multiplexer
- 8×1 Multiplexer
- Higher-order Multiplexer design
- Boolean function realization using Multiplexers

What is a Multiplexer?

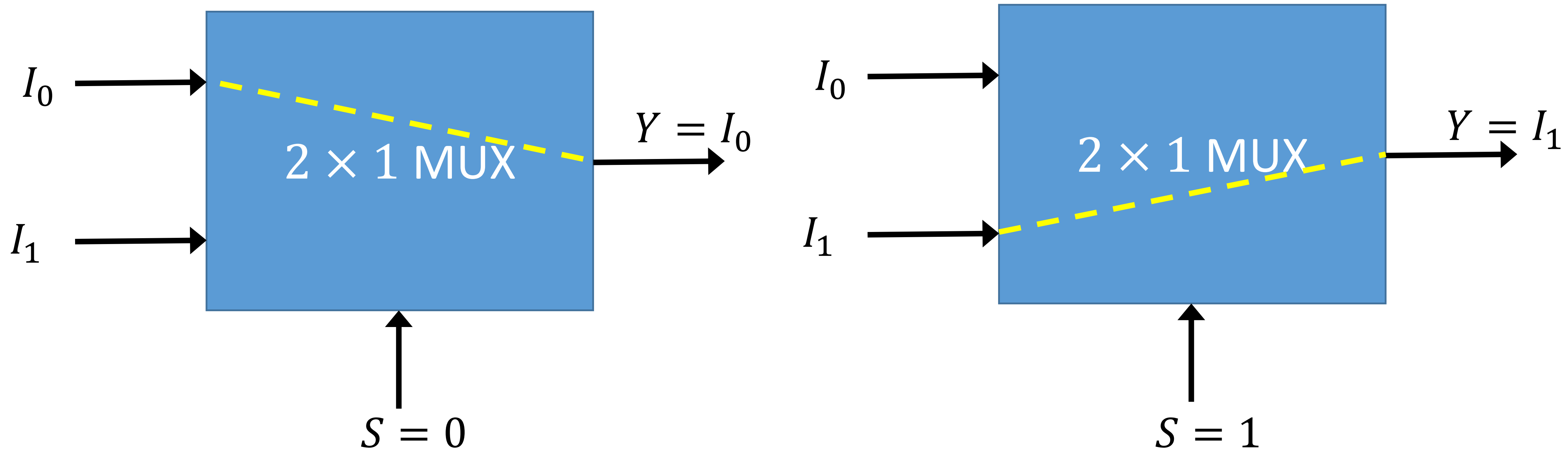
General diagram



2×1 MUX



Working of 2×1 MUX



Logic Circuit of 2×1 MUX

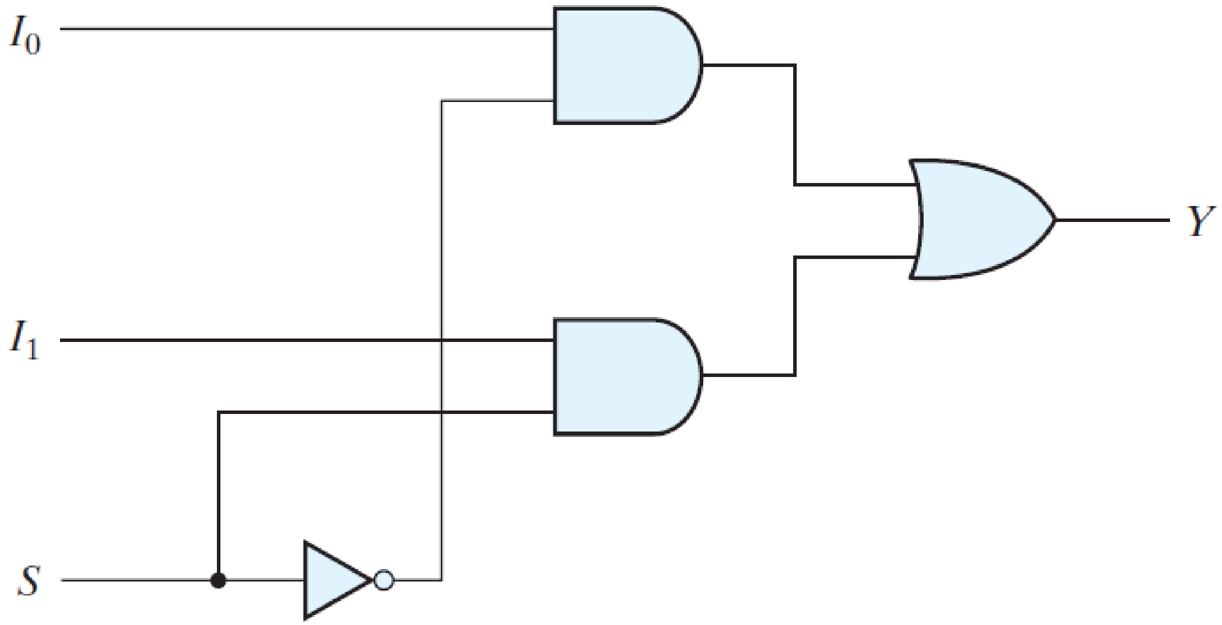
Truth table

Select line, S	Output, Y
0	I_0
1	I_1

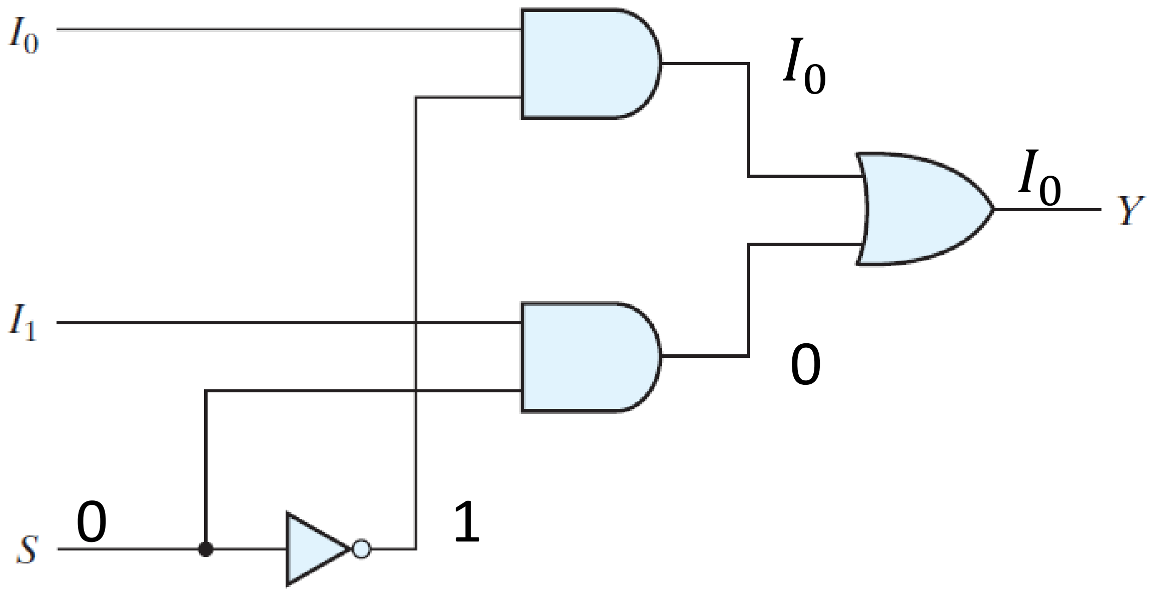
Logic expression

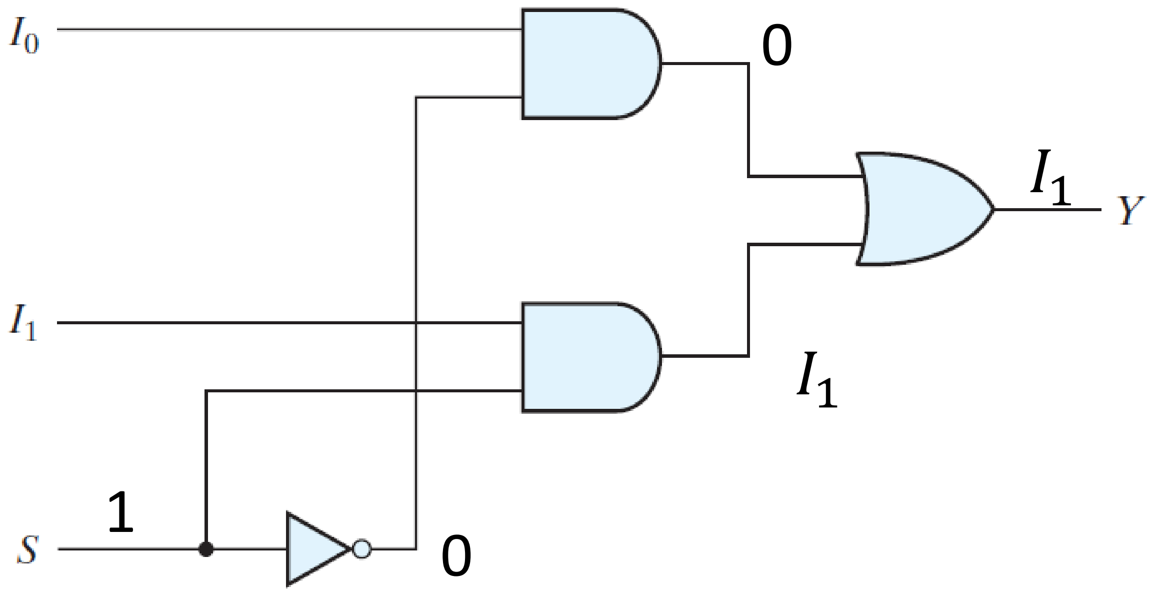
$$Y = I_0\bar{S} + I_1 S$$

Circuit based on AND-OR-Inverter logic



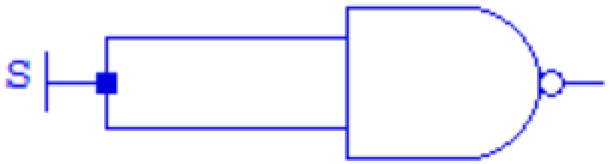
Analyzing Circuit Operation





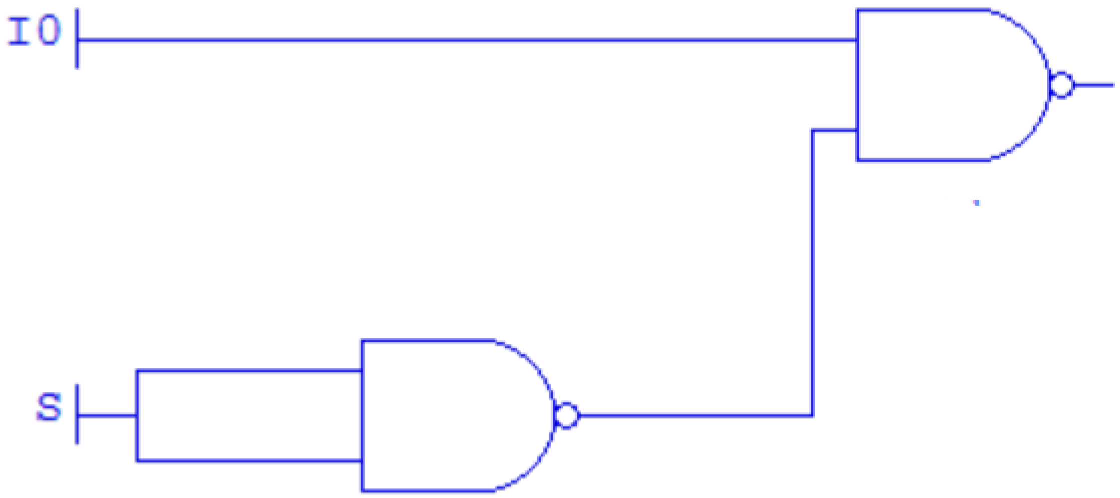
Logic Circuit of 2×1 MUX

- NAND based circuit
- $Y = I_0\bar{S} + I_1 S$
- $\bar{Y} = \overline{I_0\bar{S} + I_1 S}$
- $\bar{Y} = \overline{I_0\bar{S}}\ \overline{I_1 S}$
- $\bar{\bar{Y}} = Y = \overline{\overline{I_0\bar{S}}\ \overline{I_1 S}}$



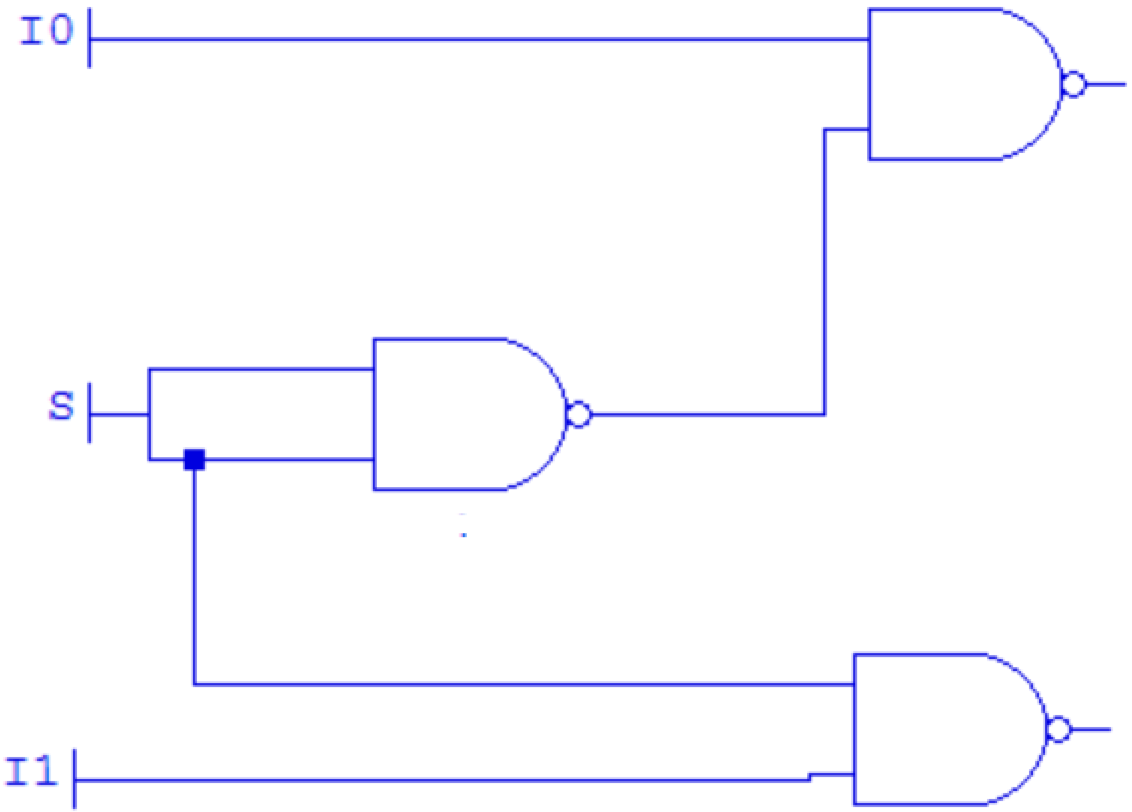
Logic Circuit of 2×1 MUX

- NAND based circuit
- $Y = I_0\bar{S} + I_1 S$
- $\bar{Y} = \overline{I_0\bar{S} + I_1 S}$
- $\bar{Y} = \overline{I_0\bar{S}}\ \overline{I_1 S}$
- $\bar{\bar{Y}} = Y = \overline{\overline{I_0\bar{S}}\ \overline{I_1 S}}$



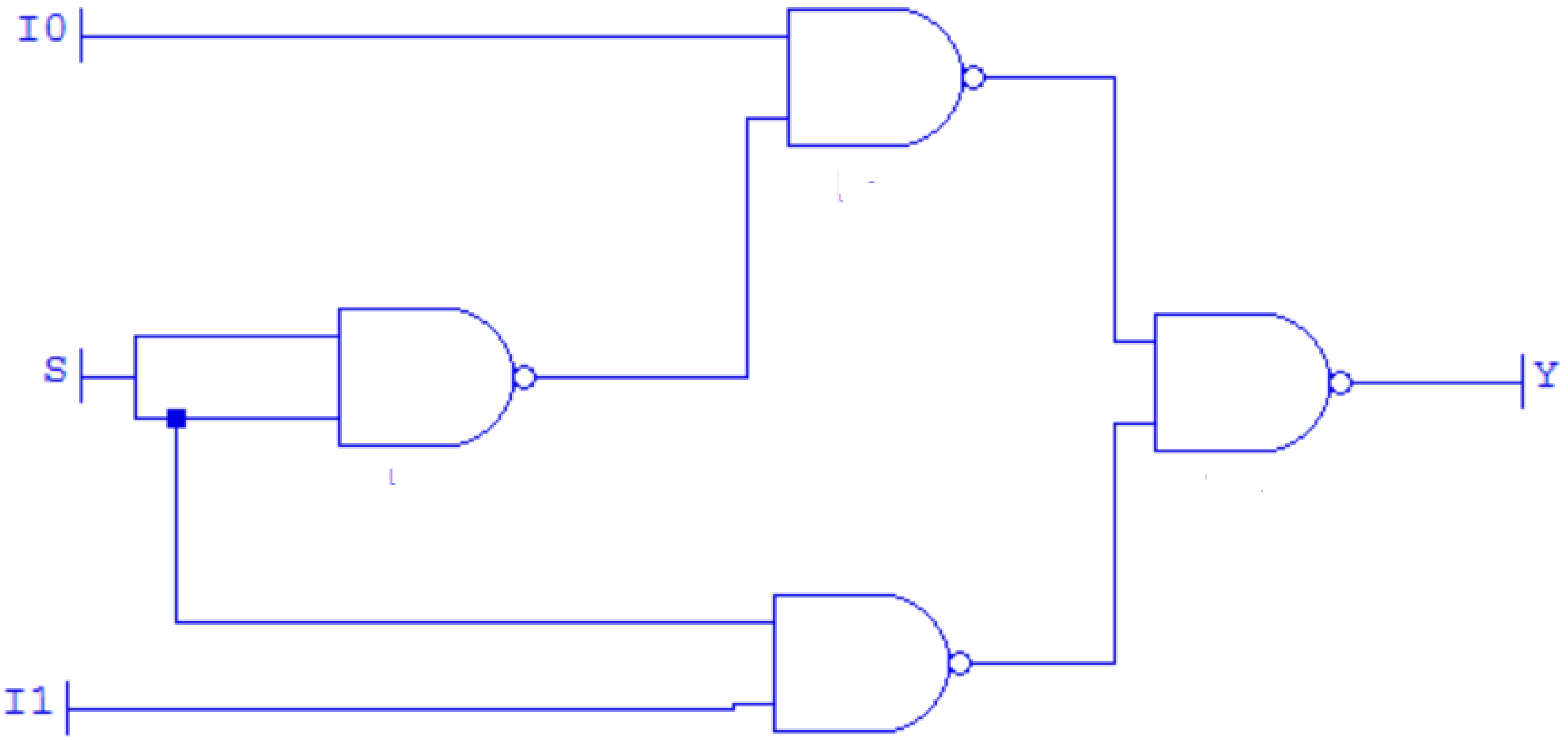
Logic Circuit of 2×1 MUX

- NAND based circuit
- $Y = I_0\bar{S} + I_1S$
- $\bar{Y} = \overline{I_0\bar{S} + I_1S}$
- $\bar{Y} = \overline{I_0\bar{S}}\ \overline{I_1S}$
- $\bar{\bar{Y}} = Y = \overline{\overline{I_0\bar{S}}\ \overline{I_1S}}$

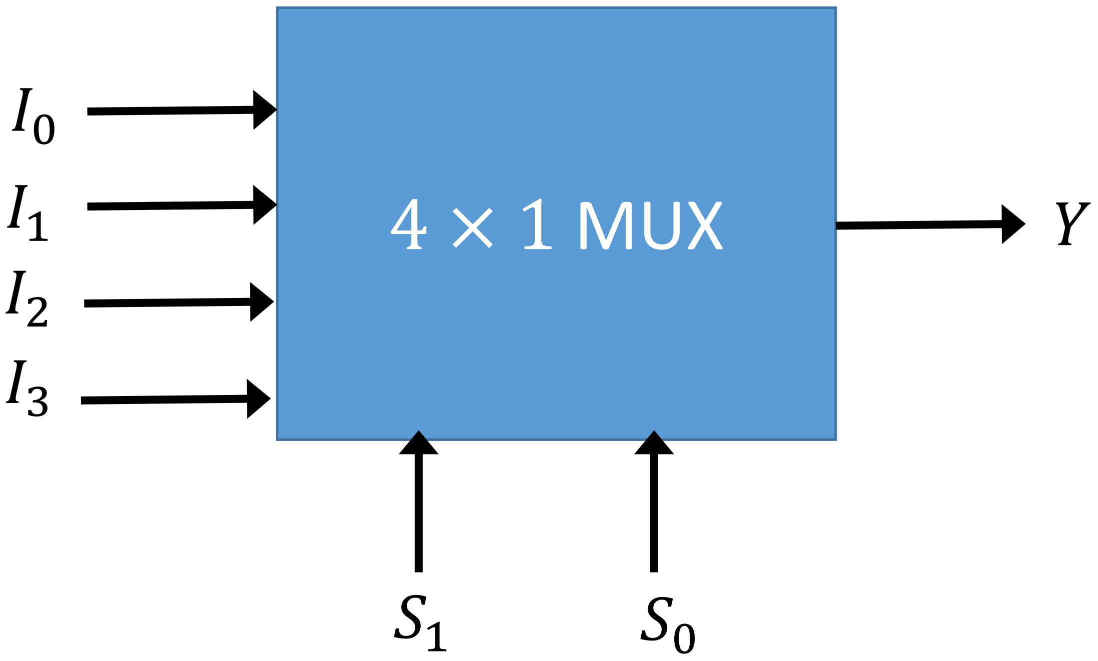


Logic Circuit of 2×1 MUX

- NAND based circuit
- $Y = I_0\bar{S} + I_1 S$
- $\bar{Y} = \overline{I_0\bar{S} + I_1 S}$
- $\bar{Y} = \overline{I_0\bar{S}}\ \overline{I_1 S}$
- $\bar{\bar{Y}} = Y = \overline{\overline{I_0\bar{S}}\ \overline{I_1 S}}$



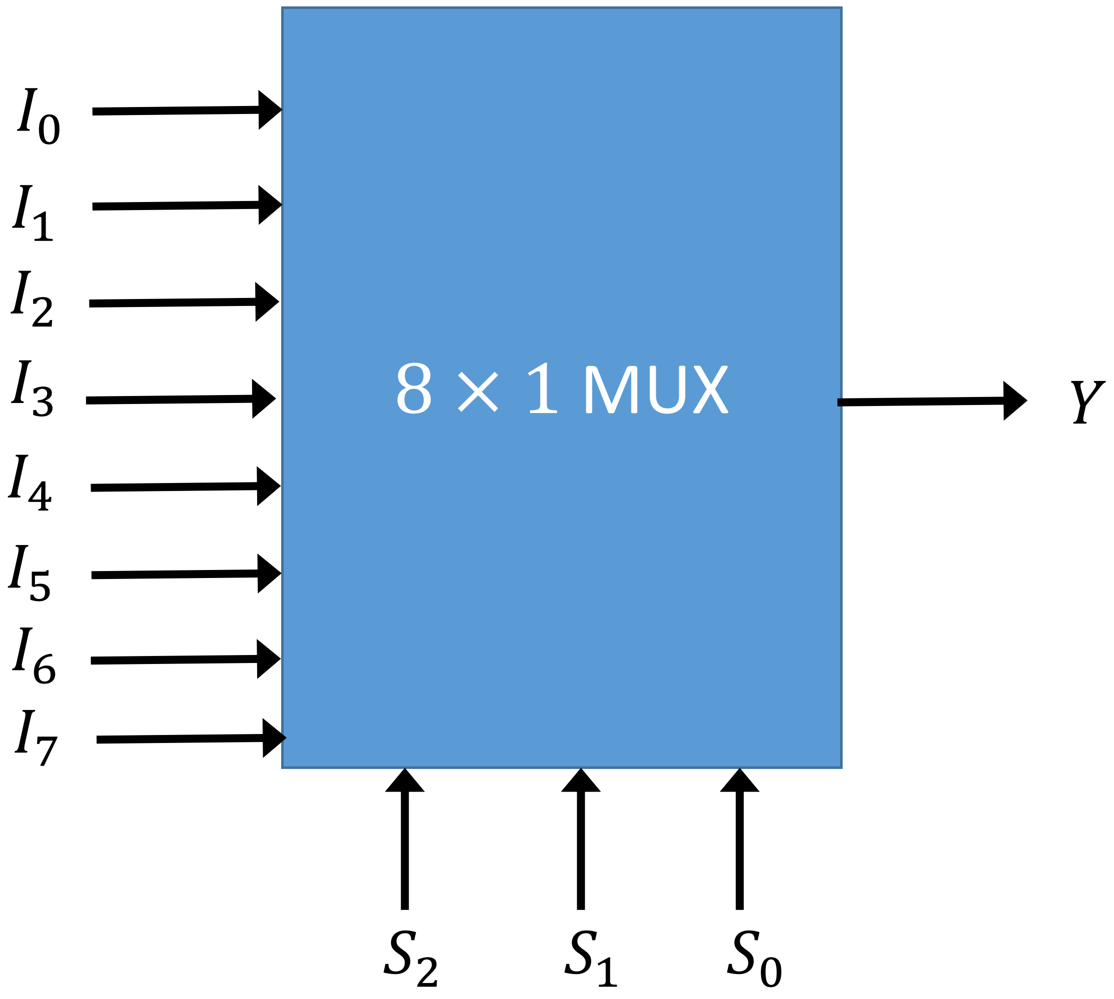
4×1 MUX



S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$Y = \overline{S_1}\,\overline{S_0}\,I_0 + \overline{S_1}S_0I_1 + S_1\,\overline{S_0}\,I_2 + S_1\,S_0I_3$$

8×1 MUX

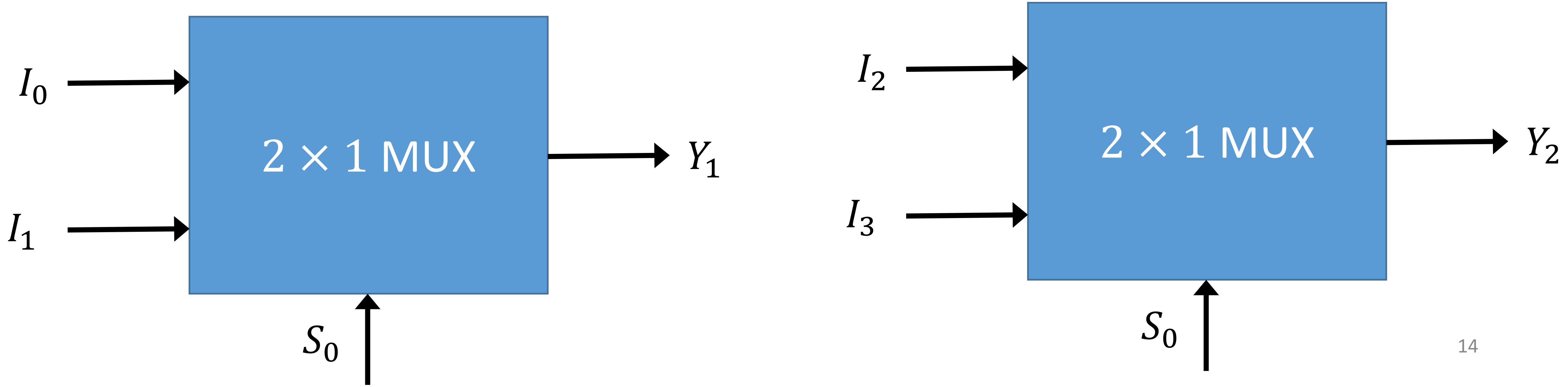


S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

4×1 MUX using 2×1 MUX

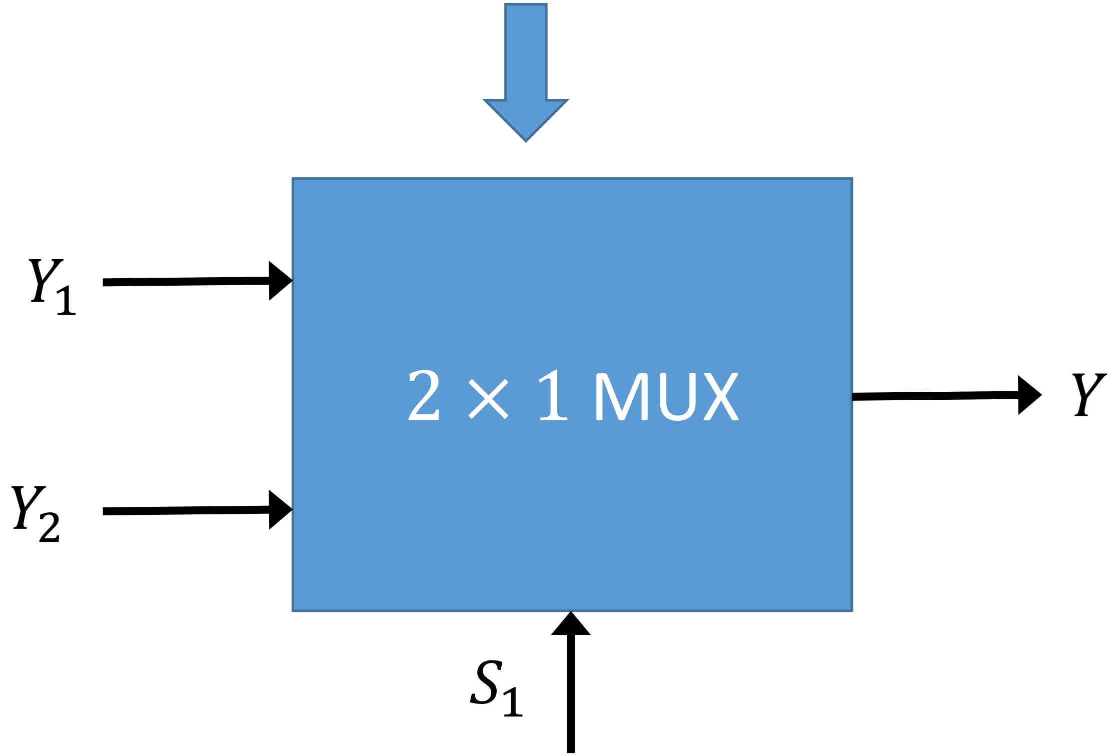
$$Y = \overline{S_1}\,\overline{S_0}\,I_0 + \overline{S_1}S_0 I_1 + S_1\,\overline{S_0}\,I_2 + S_1\,S_0 I_3$$

$$= \underbrace{(\overline{S_0}\,I_0 + S_0\,I_1)}_{Y_1}\overline{S_1} + \underbrace{(\overline{S_0}\,I_2 + S_0\,I_3)}_{Y_2}S_1 \quad = Y_1\overline{S_1} + Y_2 S_1$$

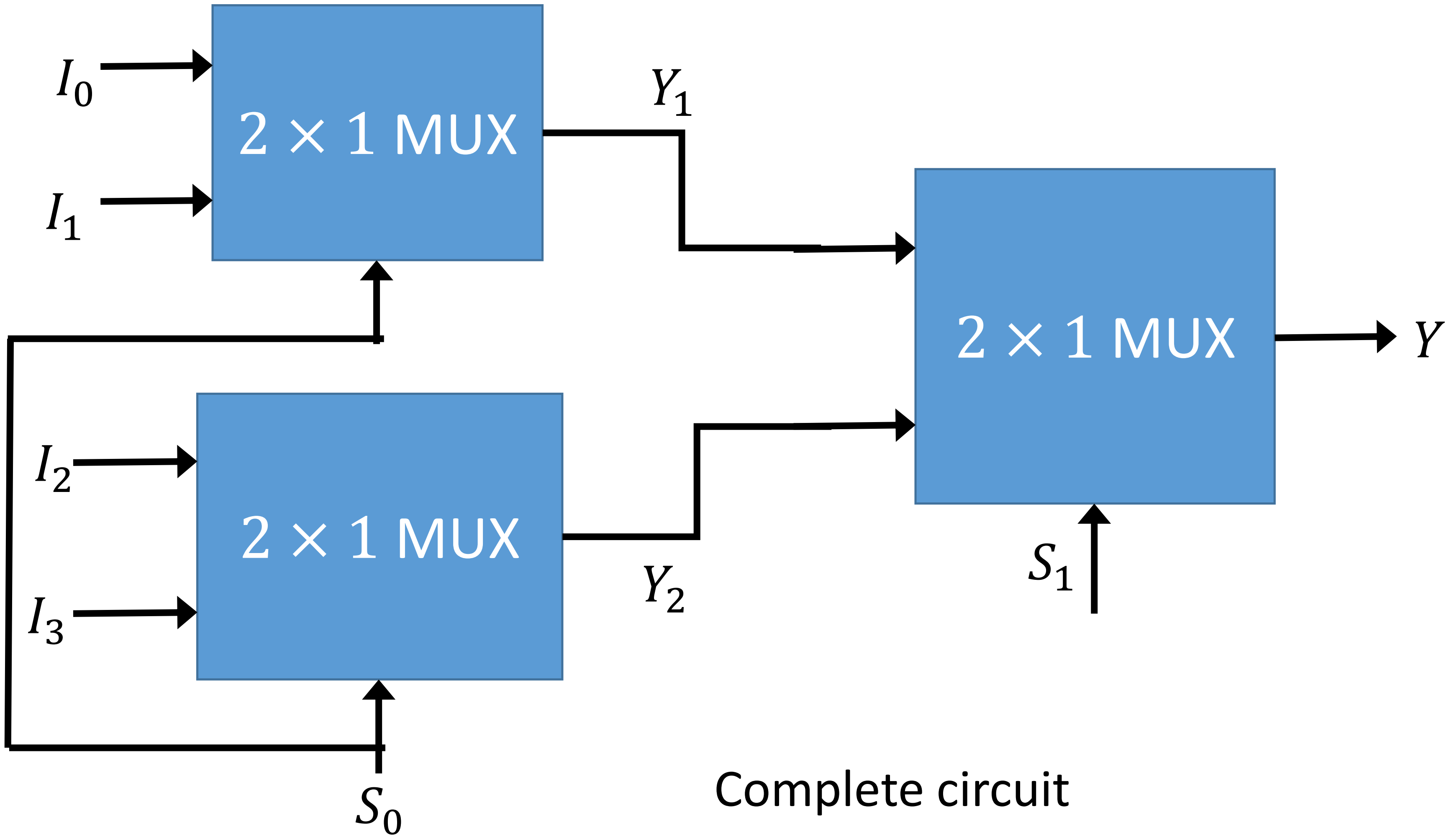


4×1 MUX using 2×1 MUX

$$Y = Y_1\overline{S_1} + Y_2S_1$$

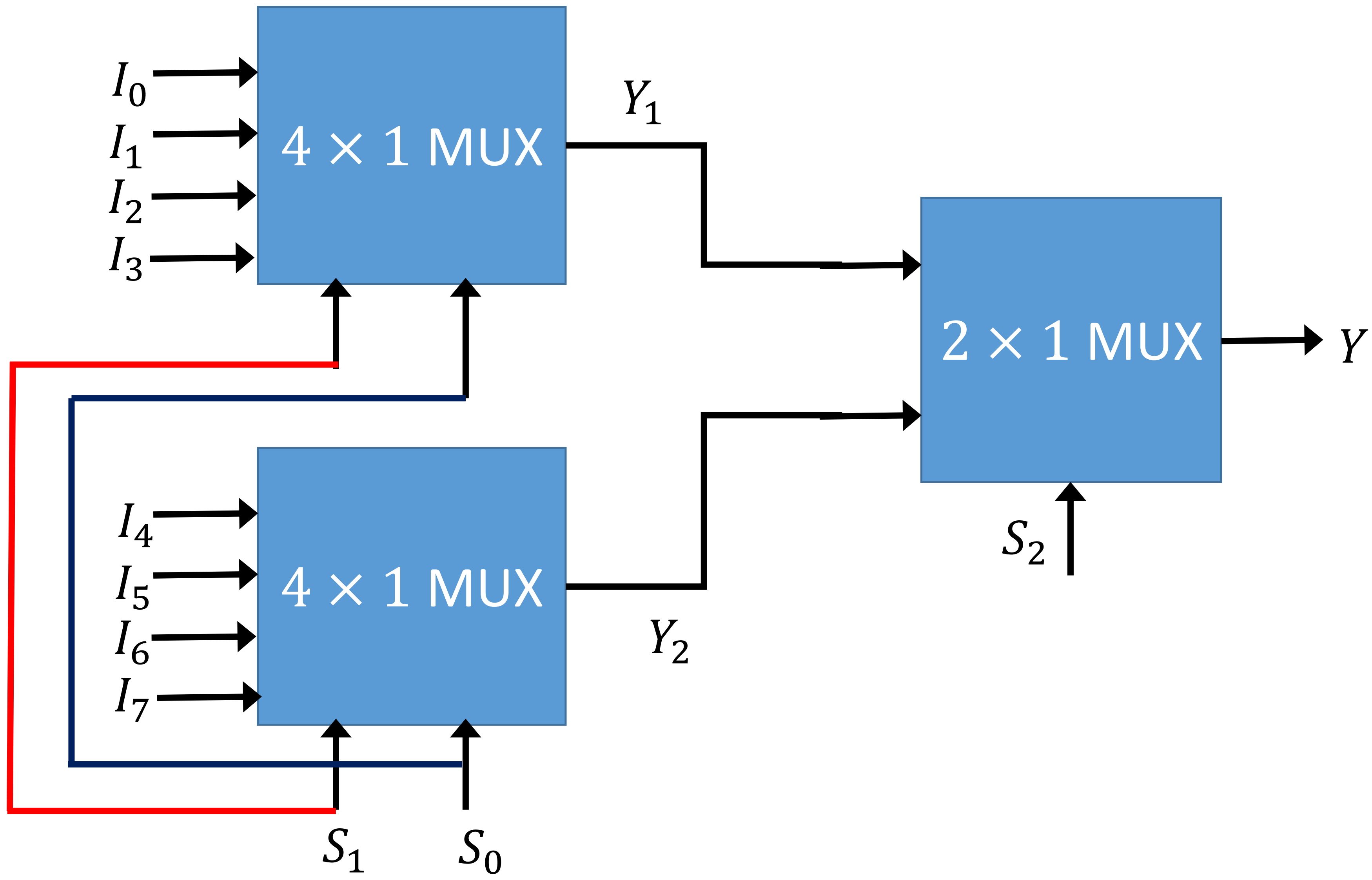


4×1 MUX using 2×1 MUX



Complete circuit

8×1 MUX using 4×1 and 2×1 MUX



Implementation of Boolean Functions Using MUX

Design Problem 1

- Implement the following function with a 4×1 MUX:

  $$F(a,b,c) = \sum m(1,3,5,6)$$

- Solution: Step 1- Construct a truth table

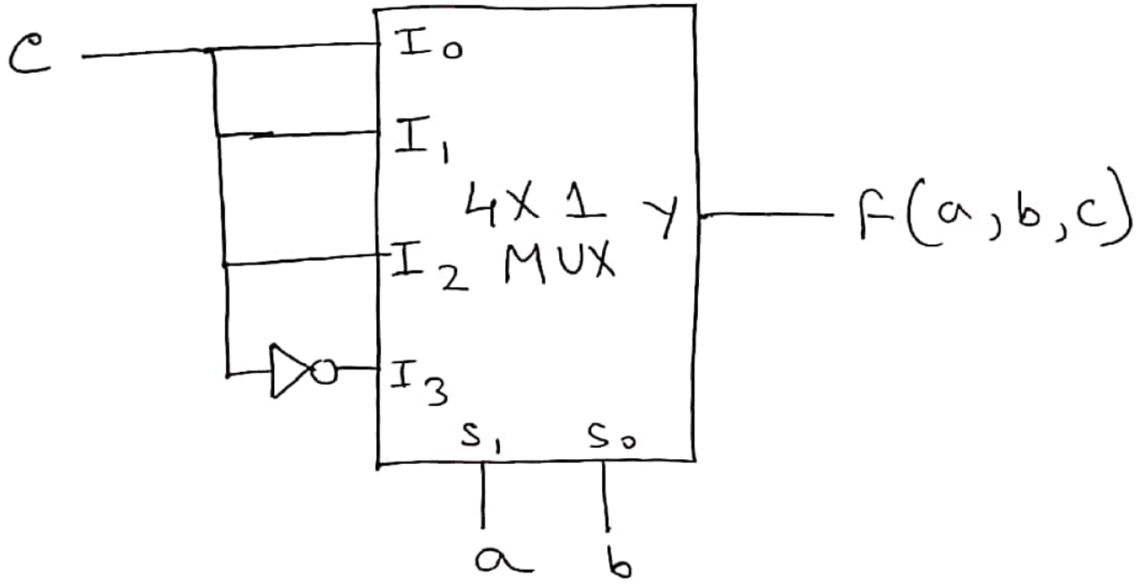
Inputs			Output	
a	b	c	$F(a,b,c)$	
0	0	0	0	$F = c$
0	0	1	1	
0	1	0	0	$F = c$
0	1	1	1	
1	0	0	0	$F = c$
1	0	1	1	
1	1	0	1	$F = \overline{c}$
1	1	1	0	

Design Problem 1

- Implement the following function with a 4×1 MUX:

$$F(a, b, c) = \sum m(1,3,5,6)$$

Inputs			Output	
a	b	c	$F(a,b,c)$	
0	0	0	0	$F = c$
0	0	1	1	
0	1	0	0	$F = c$
0	1	1	1	
1	0	0	0	$F = c$
1	0	1	1	
1	1	0	1	$F = \overline{c}$
1	1	1	0	



Design Problem 2

- Implement the function $F(a, b, c) = ab + \bar{b}\, c$ using a 4×1 MUX.
- Solution:
- Express in terms of minterms
- $F(a, b, c) = ab + \bar{b}\, c = 11\mathrm{X} + \mathrm{X}\,01 = 110 + 111 + 001 + 101$
- $F(a, b, c) = \sum m(1{,}5{,}6{,}7)$

Design Problem 2

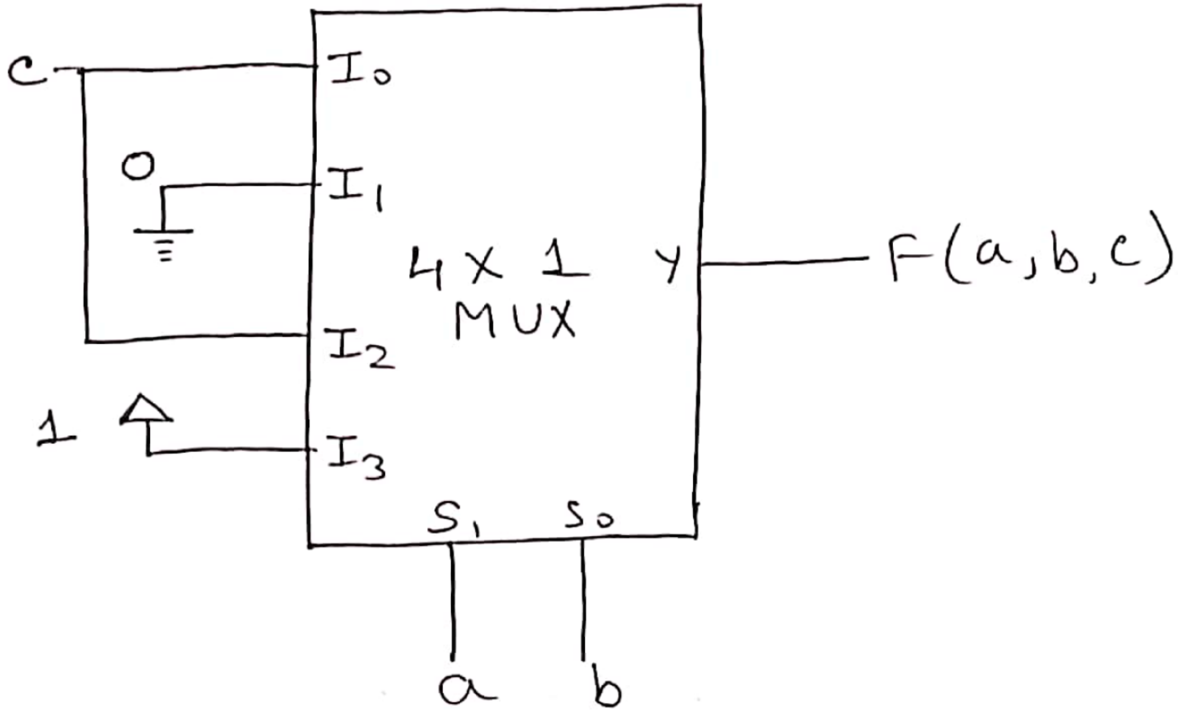
- Implement the function $F(a, b, c) = ab + \bar{b}\, c$ using a 4×1 MUX.
- Solution:
- $F(a, b, c) = \sum m(1,5,6,7)$

Inputs			Output	
a	b	c	F(a,b,c)	
0	0	0	0	F = c
0	0	1	1	
0	1	0	0	F = 0
0	1	1	0	
1	0	0	0	F = c
1	0	1	1	
1	1	0	1	F = 1
1	1	1	1	

Design Problem 2

- Implement the function $F(a, b, c) = ab + \bar{b}\,c$ using a 4×1 MUX.

Inputs			Output	
a	b	c	F(a,b,c)	
0	0	0	0	F = c
0	0	1	1	
0	1	0	0	F = 0
0	1	1	0	
1	0	0	0	F = c
1	0	1	1	
1	1	0	1	F = 1
1	1	1	1	

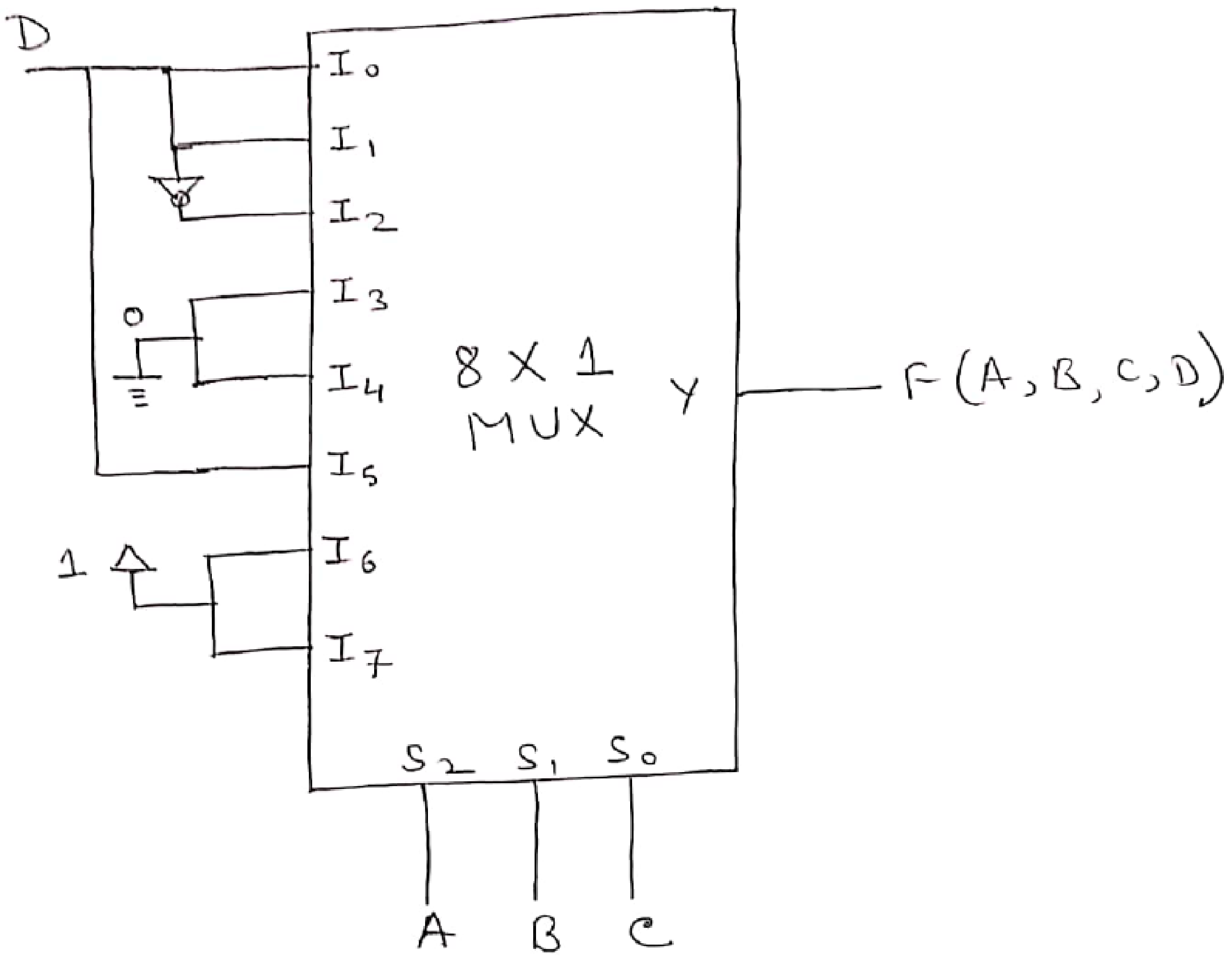


Design Problem 3

- Implement the following logic function using an 8×1 MUX:
  $F(A, B, C, D) = \prod M(0,2,5,6,7,8,9,10)$

Solution is shown in the next slide

Inputs				Output	
A	B	C	D	F(A, B, C, D)	
0	0	0	0	0	F = D
0	0	0	1	1	
0	0	1	0	0	F = D
0	0	1	1	1	
0	1	0	0	1	F = $\overline{D}$
0	1	0	1	0	
0	1	1	0	0	F = 0
0	1	1	1	0	
1	0	0	0	0	F = 0
1	0	0	1	0	
1	0	1	0	0	F = D
1	0	1	1	1	
1	1	0	0	1	F = 1
1	1	0	1	1	
1	1	1	0	1	F = 1
1	1	1	1	1	



END