8. (a) Design a Priority Encoder circuit having priority D2>D0>D3>D1; where D1,D2,D3,D4 are input to the encoder. [4]

(b) Compare with circuit diagram of 4-bit Ring & Johnson counter from modulus and decoding circuit point of view. [4]

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Pass word: 1OKM6

1 OK M 6

SPRING END SEMESTER EXAMINATION-2019

4th Semester B.Tech & B.Tech Dual Degree

DIGITAL ELECTRONICS

EC-2011

(For 2018(L.E) & 2017 Admitted Batches)

Time: 3 Hours Full Marks: 50

Answer any SIX questions.
Question paper consists of four sections-A, B, C, D.
Section A is compulsory.
Attempt minimum one question each from Sections B, C, D.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

SECTION-A

1. Answer the following questions. [1 × 10]

(a) "NAND gate follow commutative law but does not follow associative law"-Show how?

(b) Show that $\mathbf{AB + \bar{A}C = (A + C)\,(\bar{A} + B)}$ where A, B and C are Boolean variables.

(c) What is a priority encoder?

(d) Assume that a 4-bit Ripple counter is holding the count 0110. What will be the count after 31 clock pulses? $(0101)_2$

(e) Show how 1-bit Magnitude Comparator can be implemented in a decoder.

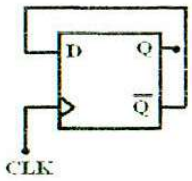
(f) Compare between Mealy and Moore State machines.

(g) Define Modulus of a Counter.

(h) Define the 'Resolution' of a digital to analog converter and calculate the resolution (in %) of a 10-bit digital to analog converter.

(i) Draw the logic diagram of CMOS Inverter.

(j) For the circuit given below find the frequency of output (Q) waveform if clock signal frequency is 10 MHz(Assume initially Q = 0).



SECTION-B

2. (a) With the help of a neat diagram, explain the working of a TTL NAND gate with Open-Collector Output and also mention the advantages of this configuration. [4]

   (b) What is Decoder? Explain it with a block diagram and Construct a 4:16 line decoder using 2-4 line decoder. [4]

3. (a) With the help of a neat diagram, explain the working of a 4-bit Successive Approximation type ADC with Analog input of 12.6 V. Find the digital output. What would be its conversion time if clock frequency is 1 MHz? If the analog input voltage is now increased to 14.8 V, what would be the new conversion time? Explain. [4]

   (b) Define the terms: [4]

   i) Threshold voltage ii) Fan-in iii) Fan-out iv) Noise Margin

SECTION-C

4. (a) Simplifythe following 4-variable Boolean expression using K-map method and implement the simplified expression using NOR gates only. [4]

   $F(A,B,C,D) = \sum m\,(11,12,14) + \sum d\,(3,4,6)$

   (b) Realize the logic function **$F(P,Q,R,S) = P\bar{Q} + R\bar{S} + P\bar{R}$** using 8:1 MUX.But8:1 MUX IC's are not available hence; use 4:1 MUX and 2:1 MUX to implement 8:1 MUX. [4]

5. (a) Construct a Synchronous counter that goes through states 0,2,3,5,6,7,0,2,3..... using S-R FFs.(Consider unused states as don't cares.) [4]

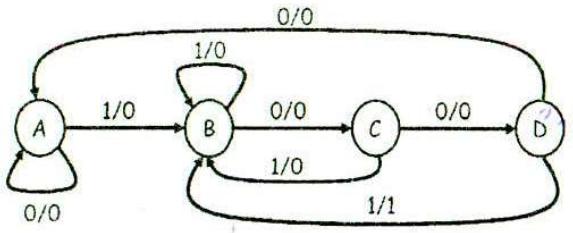
   (b) Construct a shift register using JK flip flop which will take 4 clock cycles for loading the data and 3 clock cycles for outputting it. Explain its operation briefly. [4]

6. (a) Analyse a BCD to Seven segment Display circuit with proper diagram. [4]

   (b) Construct a MOD-5 Asynchronous, Up counter using positive edge-triggered D Flip-Flops. [4]

SECTION-D

7. (a) Consider the following state diagram for a synchronous sequential circuit with one input **X** and one output **Z**. Analyse this state diagram and develop its circuit implementation using **JK flip-flop.** [4]



   (b) Design a combinational logic circuit that compares two 2 bit numbers, A and B, and determines their relative magnitudes. A>B, A<B, A=B. [4]