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2009 Adm. Batch Onwards
IV-B-Tech(Regular& Back)
DEC EC-402
[E&EE, E&TC, E&I, EE, IT, CSE]

FOURTH SEMESTER EXAMINATION-2012

DIGITAL ELECTRONICS CIRCUITS

EC-402

Full Marks: 60 **Time: 3 Hours**

Answer any six questions including question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and
All parts of a question should be answered at one place only.

Q1. a) What is *don't care term* and how can such term arise in practice? [1x10]
b) Differentiate synchronous and asynchronous input terminals of FFs, explain with the help of J-K FF.
c) 'XOR and XNOR gates can be used as a buffer as well as an inverter', Justify.
d) What is the difference between active LOW and active HIGH terminals?
e) Define (i)Self-complementing code,(ii)Sequential codes. Give examples of both.
f) Define Noise Margin and Fan-out?
g) Perform following arithmetic : (i) BCD addition (749+858),
(ii) **(-14) - (-6)** using 2's complement method.
h) Calculate the modulus of the counter which counts in **prime numbers** (2, 3, 5…N, 2, 3….) where N < 50.
i) What is the difference between SRAM and DRAM?
j) An 8-bit successive approximation type ADC has a resolution of 15mV.What will its digital output be for an analog input of 2.65V?

Q2. a) Design a synchronous sequential circuit which produces an output Z=1, whenever the following input sequence '10110' occurs. *(Assume overlapping is allowed and use Mealy Model)* [6]
b) Draw the logic diagram of a 4-bit Bi-directional shift register and explain in brief. [4]

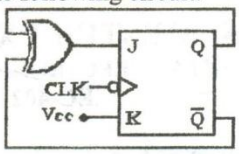
Q3. a) Design a synchronous counter that goes through states 0,2,3,5,6,7,0,2,3…… using J-K FFs. [4]
b) Using 2-4 decoders (having enable input) design **3-8 decoder with enable input** so that the new 3-8 decoder can be used for further expansion. [4]
c) Draw the circuit for 2-input NOR gate using CMOS logic. [2]

Q4. a) Implement 3-bit combined even and odd parity generator using a multiplexer having two select lines and XOR gate. *(Hint: Use XOR gate as a buffer and as an inverter)* [4]
b) With the help of a neat diagram explain the working of a two-input totem-pole TTL NAND gate and also mention some advantages of this configuration. [4]
c) What is the difference between PLA & PAL explain with suitable examples? [2]

Q5. a) With the help of a neat diagram explain the working of Counter type A/D converter circuit and also discuss the drawbacks of this converter in brief. [4]
b) Obtain the minimized expression for the following 4-varible Boolean expression using K-map method and implement the minimized expression using NAND gates only. [4]

$$F(P,Q,R,S) = \Pi M (0,1,4,7,10,11,13,14).d(2,7,8,13)$$

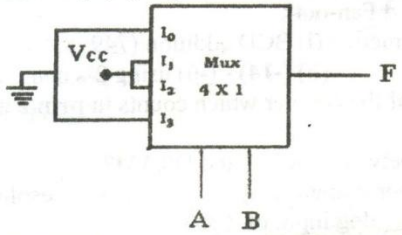
c) Find out the resulting output Q(t) of the FF for next 6 clock pulses assuming initial condition (Q=0 and $\bar{Q}$ =1) for the following circuit. [2]



Q6. a) Design a 4:2 priority encoder such that input having least decimal subscript should have highest priority (**Order of priority: D_0>D_1 >D_2>D_3,where all D_i's are inputs to the encoder**) [4]

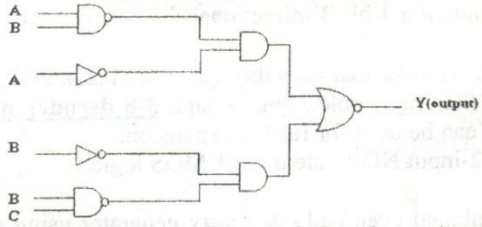
b) Encode 4-bit data word '1000' into a 7-bit even-parity Hamming code. If we transmitted a 7-bit even parity Hamming code through a noisy channel and at the receiver we obtained '1110110'.
Decode the correct 4-bit data word. (*Assume that at most a single bit error may occur in the code word during transmission)* [4]

c) Identify the Boolean function **F(A,B)** implemented with MUX, [2]



Q7. a) Draw the circuit diagram of (i)MOD-6 Johnson counter (ii)MOD-4 Ring counter and compare N-bit Ring & Johnson counter from modulus and decoding circuit point of view. [4]

b) Simplify the given logic circuit and implement the simplified circuit using only NOR gates. [4]



c) 'A decoder circuit having **enable input line** can be used as a demultiplexer circuit', Justify this statement with proper circuit diagram. [2]

Q8. a) What is the difference between Astable multivibrator and Monostable multivibrator? Design an Astable Multivibrator using 555 timer to generate a square wave of 2KHz frequency with 60% duty cycle. [4]

b) Design J-K Flip-Flop using **2:1 MUX** and a **T Flip-Flop.** [4]

c) A certain memory has a capacity of 16K x 32. [2]
(i) How many data I/P and O/P lines does it have?
(ii) How many address lines does it have?