Half Adder

```
module Half_Adder (C,S,A,B);
         input A,B;
         output C,S;
         assign S = A^B;
         assign C=A&B;
endmodule
                                              Half Subtractor
module Half_Subtractor (B,D,X,Y);
         input X,Y;
         output D,B;
         assign D = X^Y;
         assign B = (^X) & Y;
endmodule
                                                 Full Adder
module Full_Adder (Cout,S,A,B,Cin);
         input A,B,Cin;
         output Cout, S;
         assign S = (A^B)^Cin;
         assign Cout = (A&B) | ( (A^B) & Cin );
endmodule
                                              Full Subtractor
module Full_Subtractor (B,D,X,Y,Z);
         input X,Y,Z;
         output D,B;
         assign D = (X^Y)^Z;
         assign B = ((^{\sim}X)&Y) | (^{\sim}(X^{\wedge}Y) & Z);
endmodule
                                         3:8 Active High Decoder
module Decoder_3to8_H (D7,D6,D5,D4,D3,D2,D1,D0,I2,I1,I0);
         input I2,I1,I0;
         output D7,D6,D5,D4,D3,D2,D1,D0;
         assign D0 = (^{\sim}12)&(^{\sim}11)&(^{\sim}10);
         assign D1 = (\sim 12) \& (\sim 11) \& (10);
         assign D2 = (^{\sim}I2)&(I1)&(^{\sim}I0);
         assign D3 = (\sim 12) \& (11) \& (10);
         assign D4 = (12)&(^{11})&(^{10});
         assign D5 = (12)&(^{11})&(10);
         assign D6 = (12)&(11)&(\sim10);
         assign D7 = (12)&(11)&(10);
endmodule
```

3:8 Active Low Decoder

```
module Decoder_3to8_L (D8,D7,D6,D5,D4,D3,D2,D1,D0,I2,I1,I0); input I2,I1,I0; output D8,D7,D6,D5,D4,D3,D2,D1,D0; assign D0 = \sim ((\simI2)&(\simI1)&(\simI0)); assign D1 = \sim ((\simI2)&(\simI1)&(\simI0)); assign D2 = \sim ((\simI2)&(\simI1)&(\simI0)); assign D3 = \sim ((\simI2)&(\simI1)&(\simI0)); assign D4 = \sim ((\simI2)&(\simI1)&(\simI0)); assign D5 = \sim ((\simI2)&(\simI1)&(\simI0)); assign D6 = \sim ((\simI2)&(\simI1)&(\simI0)); assign D7 = \sim ((\simI2)&(\simI1)&(\simI0));
```

endmodule