KIIT UNIVERSITY, BHUBANESWAR
SPRING MID-SEMESTER EXAMINATION – 2019
DIGITAL ELECTRONICS (EC-2011)

Full Marks: 20 **Duration: 1hour 30 mins**

- ***Answer any FOUR questions including question No.1 which is compulsory.***
- ***The figures in the margin indicate full marks.***
- ***Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.***

1) A. The two numbers represented in signed 2's complement form are ***P=11101101*** & ***Q=11100110***. If Q is subtracted from P, then obtain the value in ***signed 2's compliment*** form. ***[1X5]***

B. Why the row and column values of the **K-Map** are ordered in **Gray code** rather than binary numerical order, explain in brief.

C. Simplify the Boolean expression **F= (A+B+C)(D+E)' + (A+B+C)(D+E).**

D. A seven bit Hamming code is received as **1110110**. What is the correct code?

E. Implement **XOR** gate using 2- input NAND gates only

2) Given **F(w,x,y,z)= ∑m (0,2,5,10,11,15)+ ∑d(1,3,7).** Obtain the minimum POS form of F(w,x,y,z) using K-maps and also implement the minimized expression using ***minimum numbers of NOR gates only.*** ***[5]***

3) A. Two Half Adder are connected in cascade as shown in figure below. Find the output expressions of S and C. ***[3]***

[2]

B. State and prove **Consensus Theorem.**

4) A. Draw and explain a combined **4-bit combined adder/subtractor** block using full adders and **XNOR** gates only. ***[3]***

B. What is the advantage of **Look-Ahead Carry Adder**? Write the expression of C_1, C_2, C_3, C_4 in terms of C_0 and with proper Pi and Gi ***[2]***

5) A. Design a **2-bit Priority Encoder** where the input priorities are defined as $\mathbf{D_2 > D_3 > D_0 > D_1}$; where all $\mathbf{D_i}$**'s** are inputs to the priority encoder.. ***[3]***

B. Perform **BCD Subtraction** : (858-749) ***[2]***

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