



KIIT Deemed to be University
Online End Semester Examination(Spring Semester-2021)

Subject Name & Code:

Applicable to Courses:

Full Marks=50

Time:2 Hours

SECTION-A(Answer All Questions. Each question carries 2 Marks)

Time:30 Minutes

(7×2=14 Marks)

<u>Question No</u>	<u>Question Type (MCQ/SAT)</u>	<u>Question</u>	<u>CO Mapping</u>	<u>Answer Key (For MCQ Questions only)</u>
<u>Q.No:1</u>	<u>MCQ</u>	Arrange the following Memory/Storage Device in increasing order of proximity to the CPU. a) Registers, Electronic disk, Main Memory(RAM), Cache. b) Registers, Cache, Electronic disk, Main Memory(RAM). c) Registers, Cache, Main Memory(RAM), Electronic disk. d) Cache, Registers Main Memory(RAM), Electronic disk.	CO1	(c)
	<u>MCQ</u>	Arrange the following Memory/Storage device in increasing order of speed of execution. a) Magnetic tapes,	CO1	(c)

		<p>Electronic disk, Optical disk, Magnetic disk.</p> <p>b) Magnetic tapes, Electronic disk, Magnetic disk Optical disk,</p> <p>c) Magnetic tapes, Optical disk, Magnetic disk, Electronic disk.</p> <p>d) Magnetic tapes, Optical disk, Electronic disk Magnetic disk.</p>		
	<u>MCQ</u>	<p>A memory storage which is both volatile and non-volatile.</p> <p>a) Electronic disk b) Optical disk c) RAM d) Cache</p>	CO1	a)
	<u>MCQ</u>	<p>Arrange the following Memory/Storage device in increasing order of cost.</p> <p>a) Magnetic tapes, Registers, Optical disk, Magnetic disk.</p> <p>b) Magnetic tapes, Optical disk, Magnetic disk, Registers.</p> <p>c) Magnetic tapes, Cache, Magnetic disk, Registers.</p> <p>d) Magnetic tapes, Cache, RAM, Registers.</p>	CO1	(b)
<u>Q.No:2</u>	<u>MCQ</u>	<p>Which of the following is a valid process state transitions?</p> <p>a) Ready – Ready b) Ready – Waiting c) Waiting – Ready d) Waiting – Running</p>	CO2	(c)
	<u>MCQ</u>	<p>Which of the following is an invalid process state transitions?</p> <p>a) Ready – New b) Ready – Waiting c) Waiting – Running</p>	CO2	(d)

		d) All of the above		
	<u>MCQ</u>	CPU scheduler involves the following queue a) Device queue b) Ready queue c) Both of above d) None of above	CO2	(b)
	<u>MCQ</u>	Mid-term scheduler involves the following transition a)Ready-Running b)Running-Waiting c)Both of above d)None of above	CO2	(b)
<u>Q.No:3</u>	<u>MCQ</u>	Which of the following transition relates to non-preemption a) Running-Ready b) Running-Waiting c)Ready-Running d) Waiting-Ready	CO2	(b)
		If the fork() is called 'n' times by the parent process, then the number of total processes generated are: a) 2n b) n^2 c) $n^2/2$ d) 2^n	CO2	(d)
		Which of the following scheduling algorithms may produce starvation: a)FCFS b)Priority c) Only a d) Both a and b	CO2	(d)
		Increasing time quantum in Round Robin (RR) scheduling implies: a)RR behaves like FCFS b)Higher average turn around time c)RR behaves like SJF pre-emptive d)Only b	CO2	(a)

		e)None of the above		
Q.No:4		<p>Given a Resource allocation graph (RAG) with multiple instance multiple resources, choose the correct statement:</p> <ul style="list-style-type: none"> a) A cycle in RAG guarantees deadlock. b) A cycle in RAG means no deadlock. c) A cycle in RAG may or may not guarantee deadlock. d) Absence of cycle may guarantee no deadlock. 	CO4	(c)
		<p>Given a Resource allocation graph (RAG) with single instance multiple resources, choose the correct statement:</p> <ul style="list-style-type: none"> a) A cycle in RAG guarantees deadlock. b) A cycle in RAG means no deadlock. c) A cycle in RAG may or may not guarantee deadlock. d) Absence of cycle may guarantee no deadlock. 	CO4	(a)
		<p>Given a Resource allocation graph (RAG) 'm' resource types and 'n' processes, choose the correct statement:</p> <ul style="list-style-type: none"> a) RAG algorithm is more efficient than Banker's algorithm by a factor of 'm'. b) RAG algorithm is more efficient than Banker's algorithm by a factor of '1/m' 	CO4	(a)

		<p>types.</p> <p>c) RAG algorithm is more efficient than Banker's algorithm by a factor of 'm/n^2'.</p> <p>d) RAG algorithm is more efficient than Banker's algorithm by a factor of 'n^2/m'.</p>		
		<p>Given a Wait for graph (WFG) 'm' resource types and 'n' processes, choose the correct statement:</p> <p>a) WFG algorithm is more efficient than Deadlock detection algorithm by a factor of '$1/m$'.</p> <p>b) WFG algorithm is more efficient than Deadlock detection algorithm by a factor of 'm'.</p> <p>c) WFG algorithm is more efficient than Deadlock detection algorithm by a factor of 'n^2/m'.</p> <p>d) WFG algorithm is more efficient than Deadlock detection algorithm by a factor of 'm/n^2'.</p>	CO4	(b)
Q.No:5		<p>Given two atomic operations on semaphore $p(), v()$ choose the correct option:</p> <p>a) $p(): s++; v(): s++$</p> <p>b) $p(): s--; v(): s++$</p> <p>c) $p(): s++; v(): s--$</p> <p>d) $p(): s--; v(): s--$</p>	CO3	(b)

		<p>The problem of busy waiting in semaphore is solved by following functions:</p> <ul style="list-style-type: none"> a) wait(); sleep() b) wait(); signal() c) block(); wakeup() d) block(); wait() 	CO3	(c)
		<p>Given that P and Q are two processes on semaphores S, Q such that: Wait(S) Wait(Q); Wait(Q) Wait(S);</p> <p>Choose the correct option:</p> <ul style="list-style-type: none"> a) The above sequence will lead to a deadlock. b) The above sequence may lead to a deadlock. c) No deadlock will happen. d) None of the above. 	CO3	(a)
		<p>A solution for priority inversion may be:</p> <ul style="list-style-type: none"> (a) Priority acquiring (b) Priority reduction (c) Both of the above (d) None of the above 	CO3	(d)
		<p>Let processes P and Q access a shared variable S with critical section. Pick the correct statement:</p> <ul style="list-style-type: none"> a) P, Q modify S simultaneously b) Q then P may modify S. c) P then Q may modify S d) Both (b) and (c) e) None of the above 	CO3	(d)
Q.No:6		Given a logical		

		<p>memory of size 16KB and page size of 4B. If the physical memory has a total of 8 bits, (assume byte addressable memory), choose the most appropriate option:</p> <ul style="list-style-type: none"> a) Data insufficient b) 64 frames, 256B RAM, 12 page table entries c) 64 frames, 256B RAM d) 64 frames, 256B RAM, 256 KB page table size e) Address mapping not possible 	CO5	(d)
		<p>Given a logical memory of size 16KB and page size of 4B. If the physical memory has a total of x bits, (assume byte addressable memory), choose the most appropriate option:</p> <ul style="list-style-type: none"> a) Data insufficient b) $2^{(x-2)}$ frames, 256B RAM, 12 page table entries c) $2^{(x-2)}$ frames, 2^x B RAM, 2^x KB page table size d) 64 frames, 2^x B RAM, 2^x KB page table size e) Address mapping not possible 	CO5	(c)
		<p>Given a logical memory of size x KB and page size of 4B. If the size of physical memory and that of page table is 256B (assume byte addressable memory),</p>	CO5	

		<p>choose the most appropriate option:</p> <p>a) No. Of pages is 4K</p> <p>b) Size of logical memory is 16KB</p> <p>c) Data insufficient</p> <p>d) Both (a), (b)</p>		(d)
		<p>Given that the total number of TLB accesses is 100 and the total number of page table accesses is 20. If the TLB access time is 20 ns, page table and RAM access time is 100 ns each then there is:</p> <p>a) 45% slowdown in memory-access time</p> <p>b) 40% slowdown in memory-access time</p> <p>c) 50% slowdown in memory-access time</p> <p>d) Data insufficient</p>	CO5	(b)
<u>Q.No:7</u>		<p>External fragmentation may be dealt with schemes:</p> <p>a) Only Compaction</p> <p>b) Paging</p> <p>c) Only Paging, Segmentation</p> <p>d) Compaction, paging, segmentation</p>	CO5	(d)
		<p>Perform FIFO with the following page sequence: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5 having a frame size of 4. The number of page faults:</p> <p>a)9</p> <p>b)10</p> <p>c)11</p> <p>d) None of the above</p>	CO5	(b)

		Perform FIFO with the following page sequence: 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 1, 2, 0, 1, 7, 0, 1 having a frame size of 3. The number of page faults: a)15 b)11 c)13 d)10	CO5	(a)
		Perform LRU with the following page sequence: 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 1, 2, 0, 1, 7, 0, 1 having a frame size of 3. The number of page faults: a)15 b)12 c)13 d)10	CO5	(b)

SECTION-B(Answer Any Three Questions. Each Question carries 12 Marks)

Time: 1 Hour and 30 Minutes

(3×12=36 Marks)

<u>Question No</u>	<u>Question</u>	<u>CO Mapping (Each question should be from the same CO(s))</u>
<u>Q. No:8</u>	a) Explain the difference between batch, multiprogramming, time-sharing and distributed operating system. [2]	CO2

b) Consider process arrival as given below where N = right most significant digit of your Roll No.(ex:- for Roll No. 180854, N=4):

Process	CPU Burst Time(ms)	Arrival Time	Priority	
A	4	0	2	
B	3	3	3	
C	6	N	6	
D	5	5	N	
E	1	15	4	

Calculate the following for *priority (non preemptive)* and *round robin* (time quantum = 2 ms) CPU scheduling algorithm: [10]

- Average waiting time
 - Turnaround time for each process
 - Order of completion
- (hints:-higher digits indicate higher priority)

a) What is the drawback of preemptive priority scheduling algorithm? Explain method to solve it.

[2]

b) Consider process arrival as given below where N = right most significant digit of your Roll No.(ex:- for Roll No. 180854, N=4):

Process	CPU Burst Time(ms)	Arrival Time	Priority	
A	4	0	2	
B	3	1	3	
C	6	3	6	
D	5	N	N	
E	1	4	4	

Calculate the following for *priority (non preemptive)* and *round robin* (time quantum = 2 ms) CPU scheduling algorithm: [10]

- Average waiting time
 - Turnaround time for each process
 - Order of completion
- (hints:-higher digits indicate higher priority)

	<p>A) A.Define and differentiate between preemptive & non-preemptive scheduling. [2]</p> <p>B) Consider process arrival as given below where N = right most significant digit of your Roll No.(ex:- for Roll No. 180854, N=4):</p> <table><tr><th>Process</th><th>CPU Burst Time(ms)</th><th>Arrival Time</th><th>Priority</th></tr><tr><td>A</td><td>4</td><td>0</td><td>2</td></tr><tr><td>B</td><td>3</td><td>3</td><td>3</td></tr><tr><td>C</td><td>6</td><td>4</td><td>1</td></tr><tr><td>D</td><td>5</td><td>6</td><td>N</td></tr><tr><td>E</td><td>1</td><td>N</td><td>4</td></tr></table> <p>Calculate the following for <i>priority (non preemptive)</i> and <i>round robin</i> (time quantum = 2 ms) CPU scheduling algorithm: [10]</p> <p>(a)Average waiting time (b)Turnaround time for each process (c)Order of completion (hints:-higher digits indicate higher priority)</p>	Process	CPU Burst Time(ms)	Arrival Time	Priority	A	4	0	2	B	3	3	3	C	6	4	1	D	5	6	N	E	1	N	4	
Process	CPU Burst Time(ms)	Arrival Time	Priority																							
A	4	0	2																							
B	3	3	3																							
C	6	4	1																							
D	5	6	N																							
E	1	N	4																							
Q. No :9	<p>(a)What is “starvation” of process and how to prevent it? What do you mean by cascading termination? (6+6) (b)Find the total head movement for FCFS scheduling with following disk queue requests on I/O blocks: 98, 183, 37, 122, 14, 124, 65, 67. Head starts at N (where N= your Roll No. MODULUS 100) .</p> <p>(a)In terms of the variable pid, differentiate between a child process and a parent process? Draw the Queuing diagram representation of process scheduling for all types of schedulers. (6+6)</p> <p>(b)Find the total head movement for SSTF scheduling with following disk queue requests on I/O blocks: 98, 183, 37, 122, 14, 124, 65, 67. Head starts at Head starts at N (where N= your Roll No. MODULUS 100) .</p> <p>(a) What are the criteria for a good CPU scheduling algorithm? State the differences between Multi level queue scheduling(MQS) and Multi level feed back queue scheduling(MFQS)? Which of MQS or MFQS can lead towards starvation of processes? (6+6) (b) Find the total head movement for SCAN and C-SCAN scheduling with following disk queue requests on I/O blocks: 0, 14, 37, 53, 65, 67, 98, 122, 124, 183. Head starts at N (where N= your Roll No. MODULUS 100) . Which algorithm is more</p>	CO2 & CO6																								

	preferable and why?													
Q. No :10	<p>Consider a paging memory management system, where each entry of the page table consists of frame address, valid bit(1 bit), present bit(1 bit), protection bit(2 bits), modified bit(1 bit). The virtual address is 18bits, page size is 512 bytes, and page table is exactly fit into one page. The program is allocated with 3 page frames. The program generates the following 16 page numbers (which are part of the virtual address produced by): 0, 17, 18, M, 20, 2, 20, M, 17, 32, 0, 2, 2*M, 0, 16, M (Note: The page numbers are in decimal and M=sum of digits of your Roll No. MODULUS 10). (6+6)</p> <p>I. Calculate the number of page faults generated for the above page request, assuming a Optimal page replacement algorithm. II. Find the maximum size pf the program for single level paging.</p> <p>Consider a paging memory management system, where each entry of the page table consists of frame address, valid bit(1 bit), present bit(1 bit), protection bit(3 bits), modified bit(1 bit). The virtual address is 18bits, page size is 512 bytes, and page table is exactly fit into one page. The program is allocated with 3 page frames. The program generates the following 16 page numbers (which are part of the virtual address produced by): 0, 17, 18, M+2, 20, 2, 20, M, 31, 32, 0, 18, N, 0, 17, M (Note: The page numbers are in decimal and M=sum of digits of your Roll No. MODULUS 10). (6+6)</p> <p>I. Calculate the number of page faults generated for the above page request, assuming a Optimal page replacement algorithm. II. Find the maximum size pf the program for single level paging.</p> <p>Consider a paging memory management system, where each entry of the page table consists of frame address, valid bit(1 bit), present bit(1 bit), protection bit(2 bits), modified bit(1 bit). The virtual address is 18bits, page size is 512 bytes, and page table is exactly fit into one page. The program is allocated with 3 page frames. The program generates the following 16 page numbers (which are part of the virtual address produced by): 0, 17, 18, M, 20, 2, 20, M+4, 17, 32, 0, 2, M+2, 0, 16, M (Note: The page numbers are in decimal and M=sum of digits of your Roll No. MODULUS 10). (6+6)</p> <p>I. Calculate the number of page faults generated for the above page request, assuming a Optimal page replacement algorithm. II. Find the maximum size pf the program for single level paging.</p>	CO6												
Q. No :11	<p>Find a safe sequence(if any) for the following resource allocation table using deadlock detection algorithm.</p> <table><tr><td>Process</td><td>Alloc</td><td>Req</td><td>Avail</td></tr><tr><td>P0</td><td>0 1 0</td><td>2 2 2</td><td>4 3 3</td></tr><tr><td>P1</td><td>1 1 1</td><td>1 2 2</td><td></td></tr></table>	Process	Alloc	Req	Avail	P0	0 1 0	2 2 2	4 3 3	P1	1 1 1	1 2 2		CO4
Process	Alloc	Req	Avail											
P0	0 1 0	2 2 2	4 3 3											
P1	1 1 1	1 2 2												

P2	1 0 1	3 2 2
P3	2 1 2	4 2 3
P4	0 0 0	3 2 3

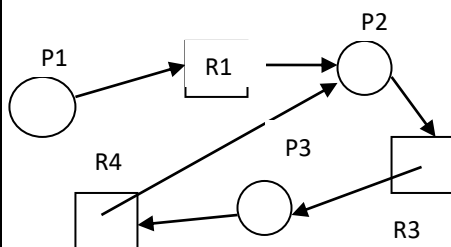
Does the system has deadlock, if so then which are the deadlocked processes? Also find any unsafe sequence and provide the value of 'Work' vector for it. (6+2+4)

Find a safe sequence(if any) for the following resource allocation table using Banker's algorithm.

<u>Process</u>	<u>Alloc</u>	<u>Max</u>	<u>Avail</u>
P0	0 1 0	2 2 2	4 3 3
P1	1 1 1	1 2 2	
P2	1 0 1	3 2 2	
P3	2 1 2	4 2 3	
P4	0 0 0	3 2 3	

Also find any unsafe sequence and provide the value of 'Work' vector for it. processes? (6+4+2)

Convert the following Resource Allocation Graph (RAG) to Wait for Graph (WFG)



Identify the cycle in the corresponding WFG. List the processes which are a part of deadlock.