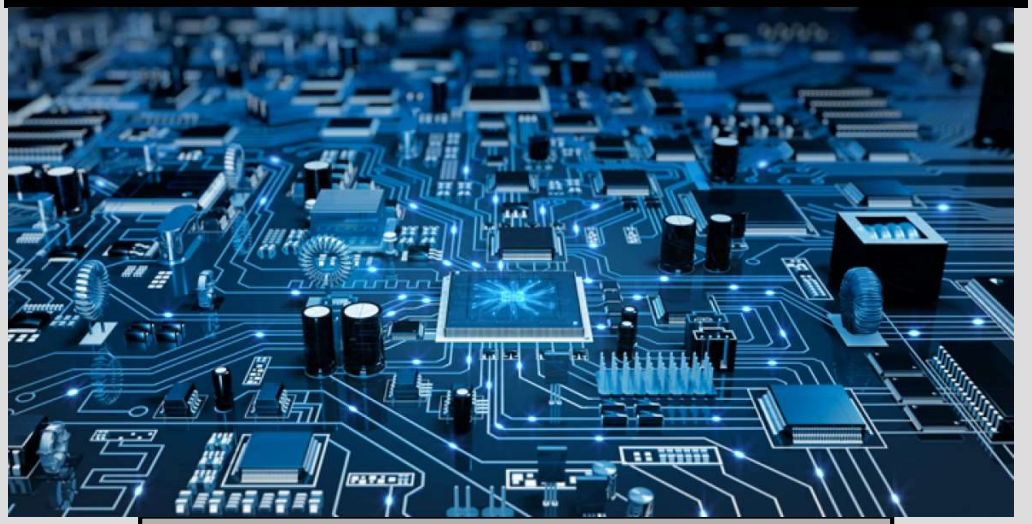
Digital System Design



Functions of Combinational Logic

In this chapter…

- **Objectives**
  - Adders
  - Comparators
  - Decoders
  - Encoders
  - Code converters
  - Multiplexers (data selectors)
  - De-multiplexers
  - Parity generators/checkers

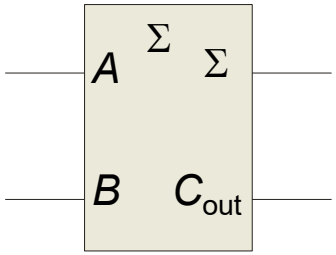
Half-Adder

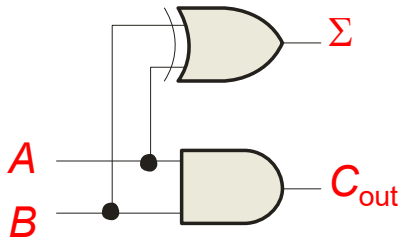
Basic rules of binary addition are performed by a **half adder**, which has two binary inputs (*A* and *B*) and two binary outputs (Carry out and Sum).

The inputs and outputs can be summarized on a truth table.

Inputs		Outputs	
A	*B*	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

The logic symbol and equivalent circuit are:



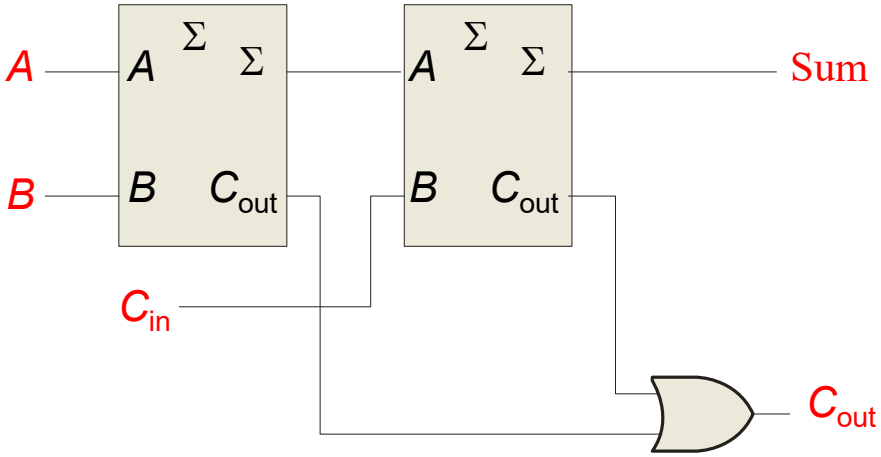


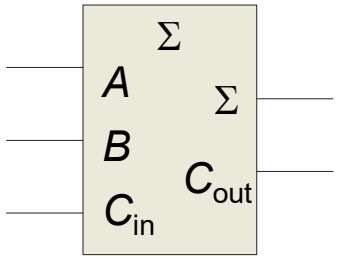
Full-Adder

By contrast, a **full adder** has three binary inputs (*A*, *B,* and Carry in) and two binary outputs (Carry out and Sum). The truth table summarizes the operation.

A full-adder can be constructed from two half adders as shown:

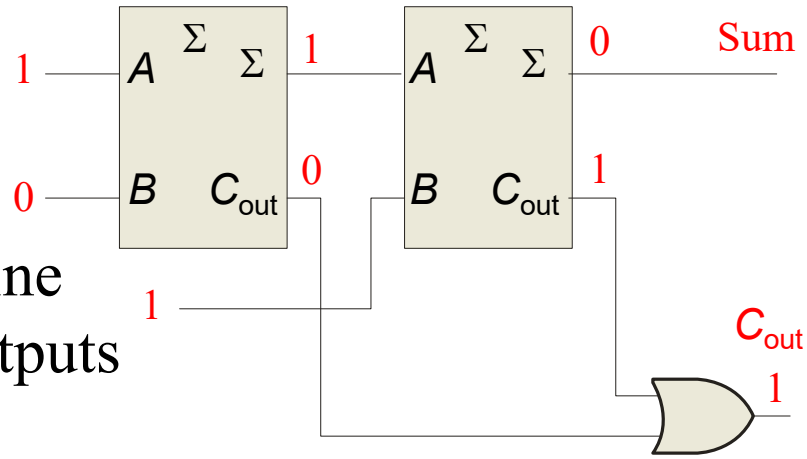
Inputs			Outputs	
A	*B*	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1





Symbol

Full-Adder



Example

For the given inputs, determine the intermediate and final outputs of the full adder.

Solution The first half-adder has inputs of 1 and 0; therefore the Sum =1 and the Carry out = 0.

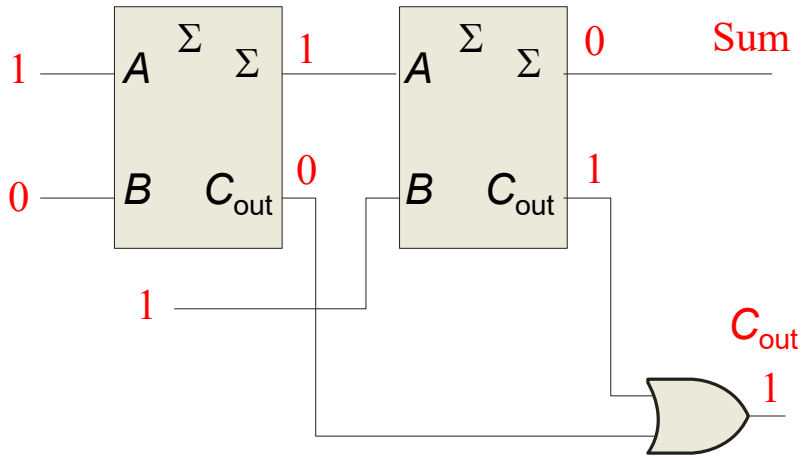
The second half-adder has inputs of 1 and 1; therefore the Sum = 0 and the Carry out = 1.

The OR gate has inputs of 1 and 0, therefore the final carry out = 1.

Full-Adder

Notice that the result from the previous example can be read directly on the truth table for a full adder.

Inputs			Outputs	
A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

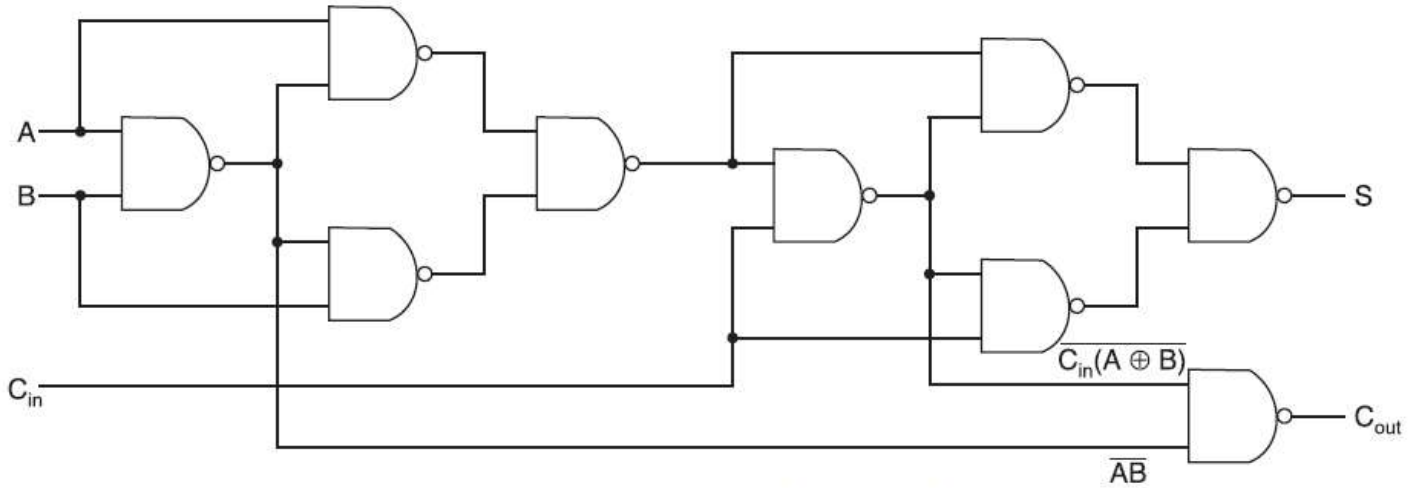


Full Adder using NAND gate

$$A \oplus B = \overline{\overline{A \cdot \overline{AB}} \cdot \overline{B \cdot \overline{AB}}}$$

$$S = A \oplus B \oplus C_{in} = \overline{\overline{(A \oplus B) \cdot \overline{(A \oplus B)C_{in}}} \cdot \overline{C_{in} \cdot \overline{(A \oplus B)C_{in}}}}$$

$$C_{out} = C_{in}(A \oplus B) + AB = \overline{\overline{C_{in}(A \oplus B)} \cdot \overline{AB}}$$



Logic diagram of a full-adder using only 2-input NAND gates.

Subtractor

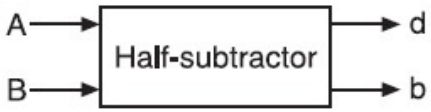
- The subtraction of two binary numbers may be accomplished by taking the complement of the subtrahend and adding it to the minuend.

Half Subtractor

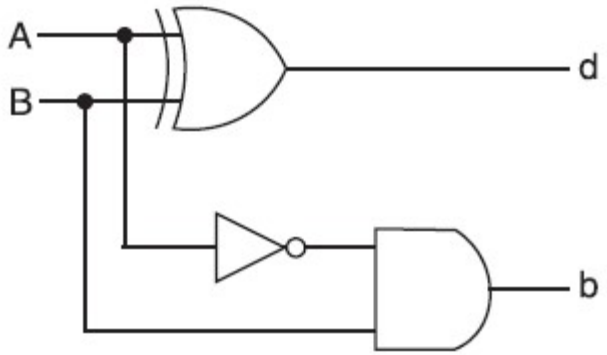
- A half-subtractor is a combinational circuit that subtracts one bit from the other and produces the difference.

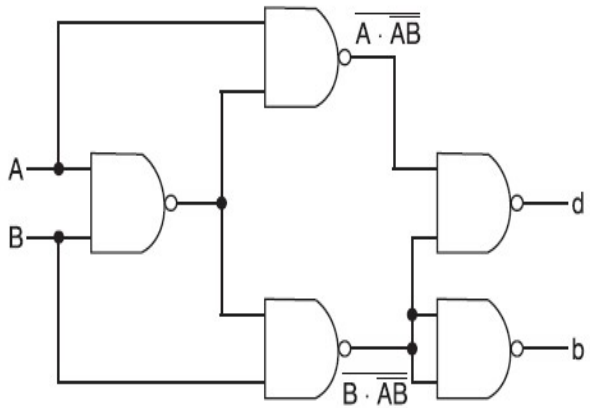
Inputs		Outputs	
A	B	d	b
0	0	0	0
1	0	1	0
1	1	0	0
0	1	1	1

(a) Truth table



(b) Block diagram



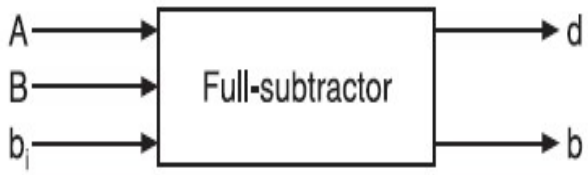


Full Subtractor

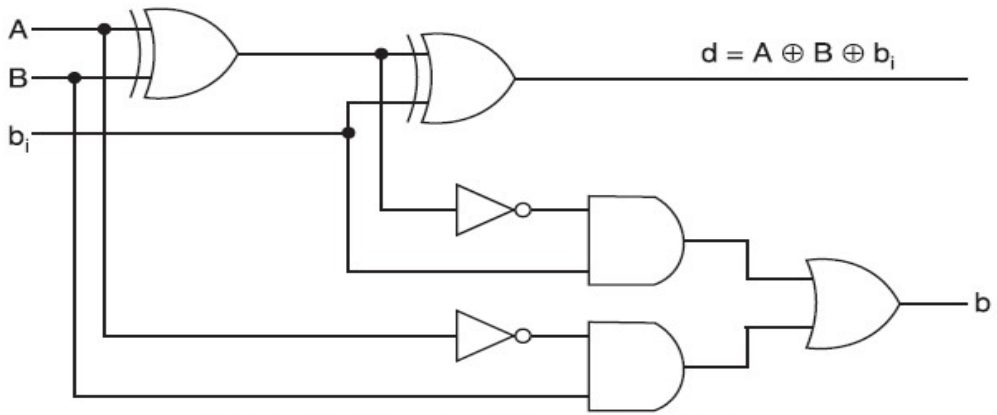
- It subtracts one bit (B) from another bit (A), when already there is a borrow bi from this column for the subtraction in the preceding column, and outputs the difference bit (d) and the borrow bit (b) required from the next column.
- The 1s and 0s for the output variables are determined from the subtraction of A – B – bi.

Inputs			Difference	Borrow
A	B	b_i	d	b
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

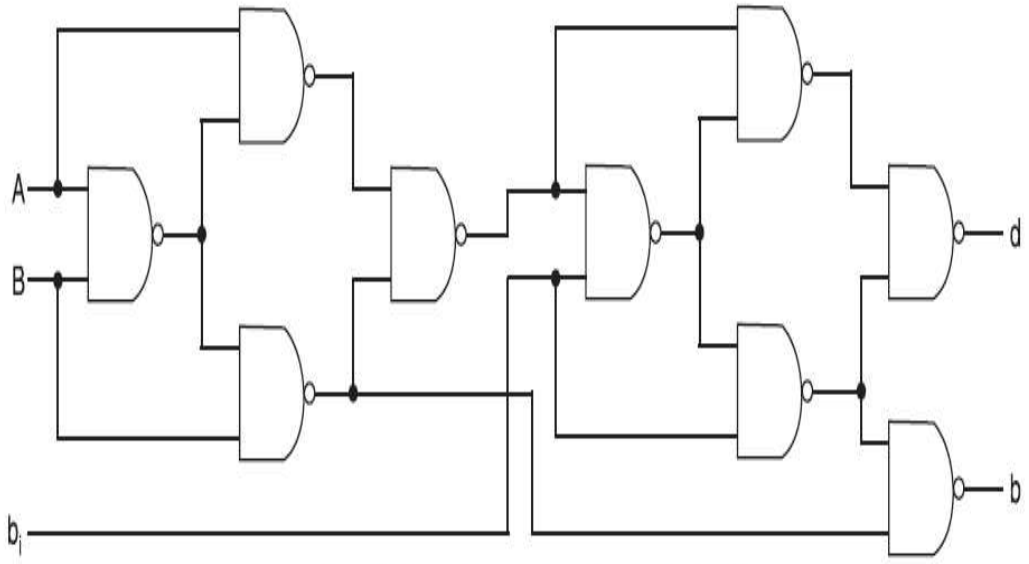
(a) Truth table



(b) Block diagram



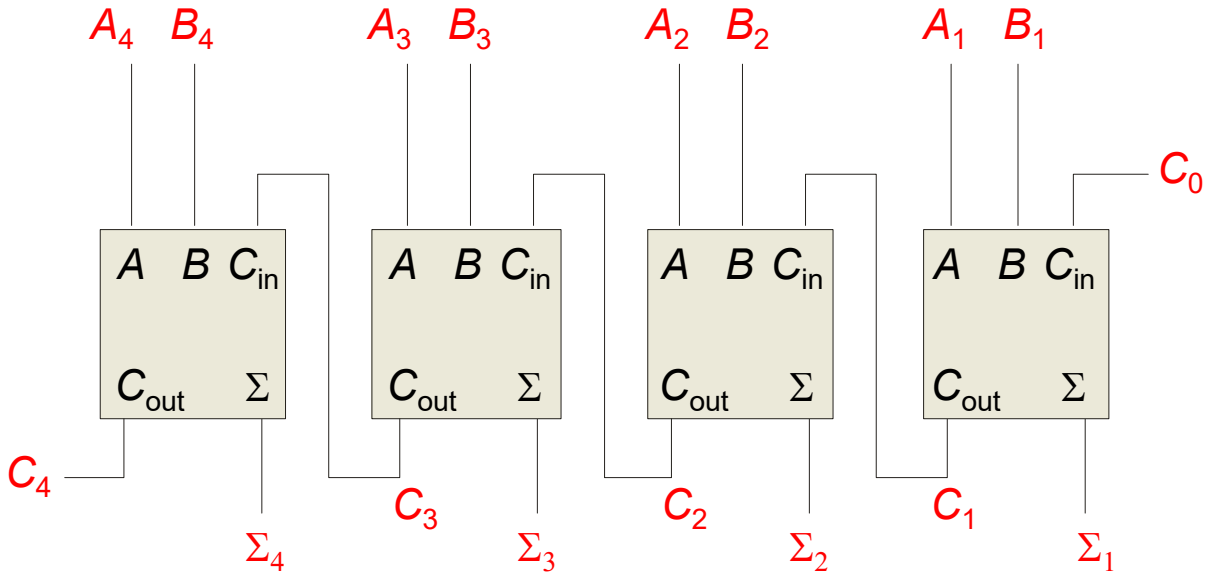
Logic diagram of a full-subtractor.



Logic diagram of a full-subtractor using only 2-input NAND gates.

Parallel Adders

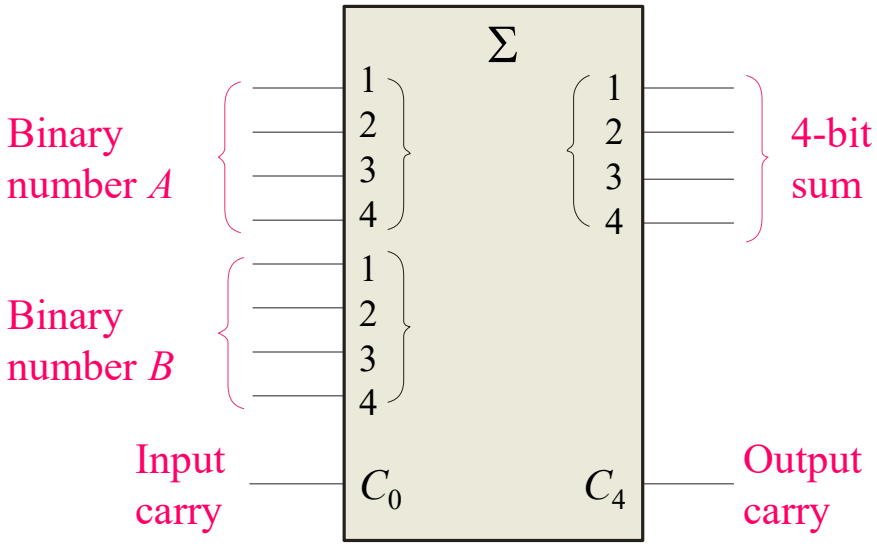
Full adders are combined into parallel adders that can add binary numbers with multiple bits. A 4-bit adder is shown.



The output carry (C_4) is not ready until it propagates through all of the full adders. This is called *ripple carry*, delaying the addition process.

Parallel Adders

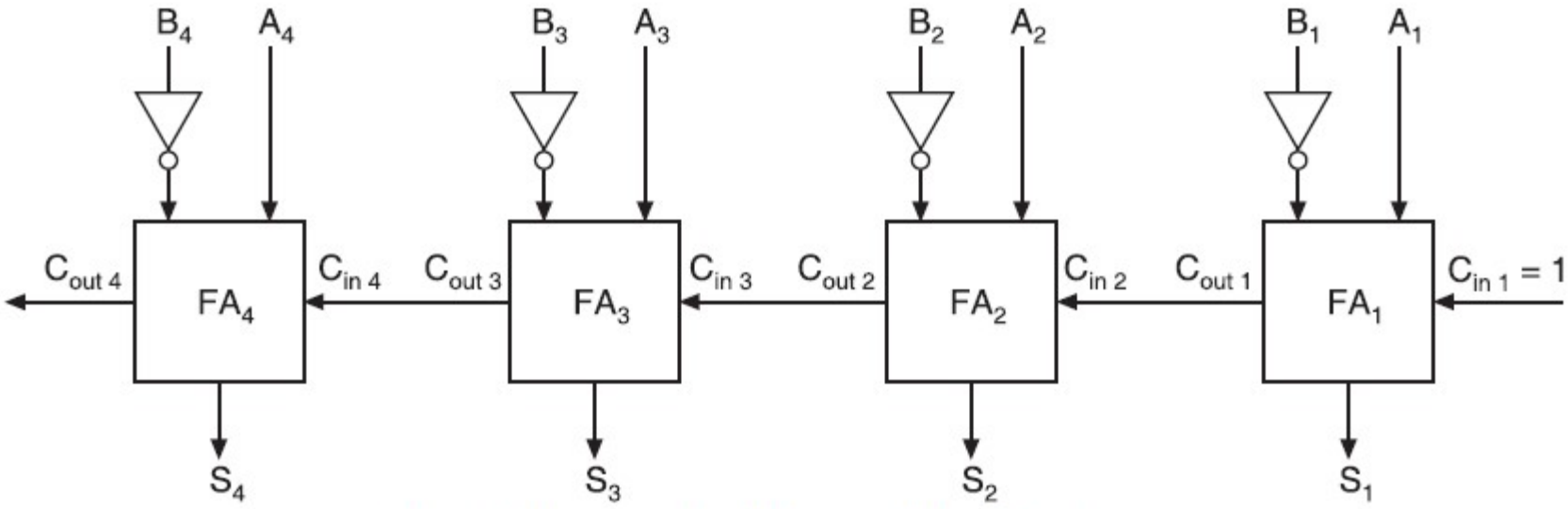
The logic symbol for a 4-bit parallel adder is shown. This 4-bit adder includes a carry in (labeled (C_0) and a Carry out (labeled C_4).



The 74LS283 is an example. It features *look-ahead carry*, which adds logic to minimize the output carry delay. For the 74LS283, the maximum delay to the output carry is 17 ns.

4-BIT PARALLEL SUBTRACTOR

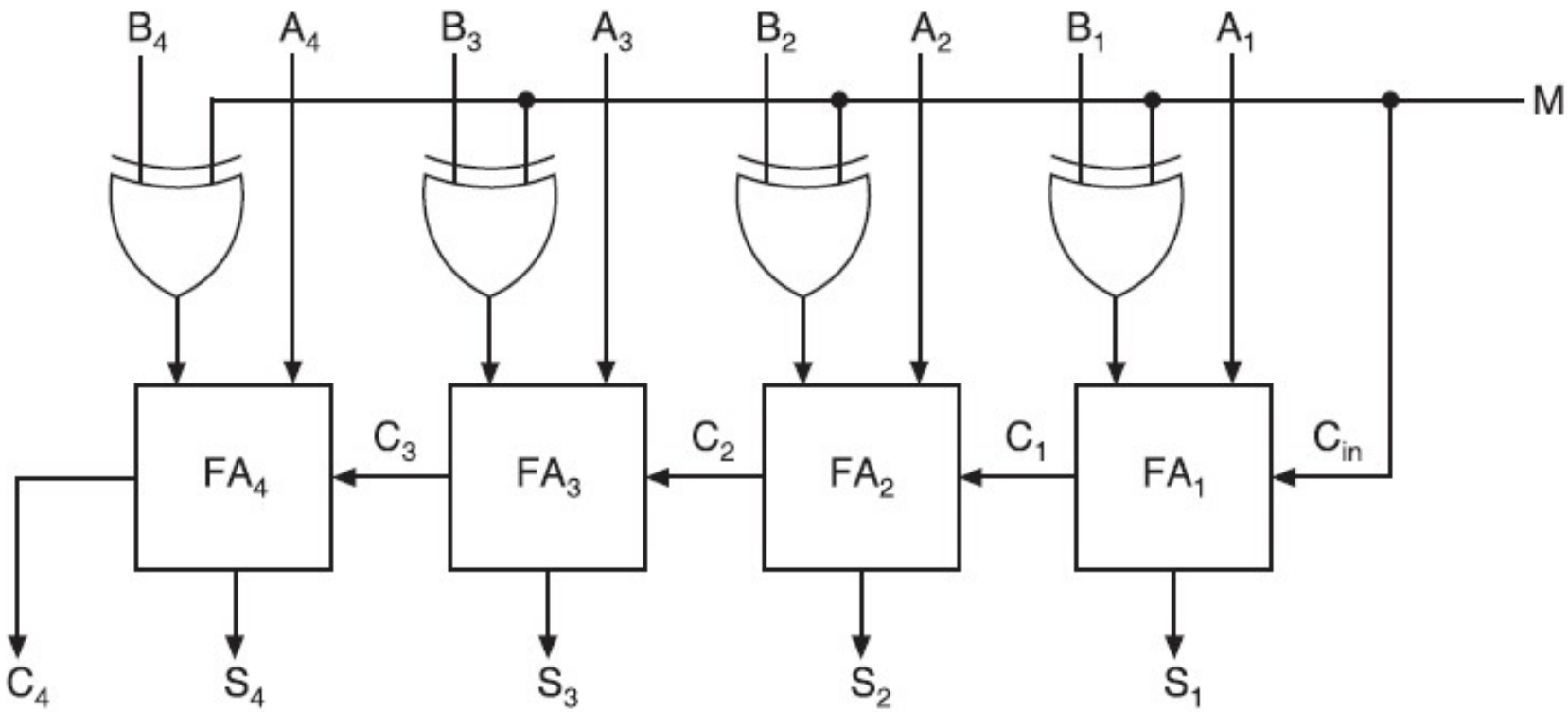
- The subtraction of binary numbers can be carried out most conveniently by means of complements.
- Remember that the subtraction A – B can be done by taking the 2's complement of B and adding it to A. The 2's complement can be obtained by taking the 1's complement and adding 1 to the least significant pair of bits.



Logic diagram of a 4-bit parallel subtractor.

BINARY ADDER-SUBTRACTOR

- Here the addition and subtraction operations are combined into one circuit with one common binary adder. This is done by including an X-OR gate with each full-adder.
- The mode input M controls the operation. When M = 0, the circuit is an adder, and when M = 1, the circuit becomes a subtractor.
- Each X-OR gate receives input M and one of the inputs of B. When M = 0, we have B ≈ 0 = B. The full-adder receives the value of B, the input carry is 0 and the circuit performs A + B. When M = 1, we have B ≈ 1 = B and C1 = 1.
- The B inputs are complemented and a 1 is added through the input carry. The circuit performs the operation A plus the 2's complement of B.



Logic diagram of a 4-bit binary adder-subtractor.

Code converters

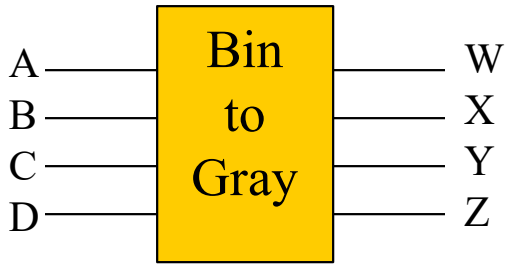
Coder converters are logic circuits that change one code to another.

Example

Design a logic circuit that converts 4-bit binary codes to gray codes

Solution

Step 1: determine the Truth Table of the logic circuit



	Binary	Gray		Binary	Gray
0	0000	0000	8	1000	1100
1	0001	0001	9	1001	1101
2	0010	0011	10	1010	1111
3	0011	0010	11	1011	1110
4	0100	0110	12	1100	1010
5	0101	0111	13	1101	1011
6	0110	0101	14	1110	1001
7	0111	0100	15	1111	1000

Example Solution

Design a logic circuit that converts 4-bit binary codes to gray codes

Step 1: determine the Truth Table of the logic circuit

Step 2: determine the minimum logic of each output with K-maps

	Binary (ABCD)	Gray (WXYZ)		Binary	Gray
0	0000	0000	8	1000	1100
1	0001	0001	9	1001	1101
2	0010	0011	10	1010	1111
3	0011	0010	11	1011	1110
4	0100	0110	12	1100	1010
5	0101	0111	13	1101	1011
6	0110	0101	14	1110	1001
7	0111	0100	15	1111	1000

$W = A$

CD \ AB	00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	0	0	1	1
10	0	0	1	1

$X = A \oplus B$

CD \ AB	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

$Y = B \oplus C$

CD \ AB	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	0	0	1
10	1	0	0	1

$Z = C \oplus D$

CD \ AB	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

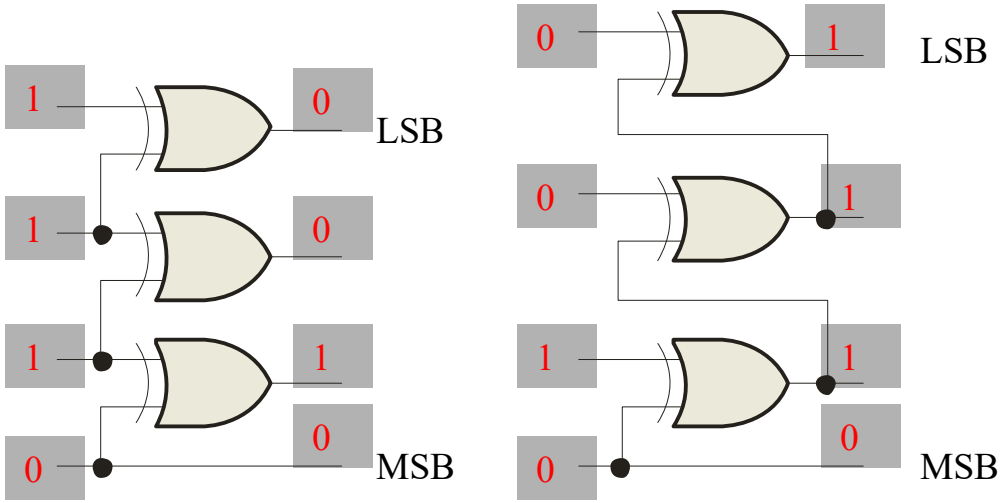
Code converters

The 4-bit binary-to-Gray converter and the Gray-to-binary converter.

Example

Show the conversion of binary 0111 to Gray and back.

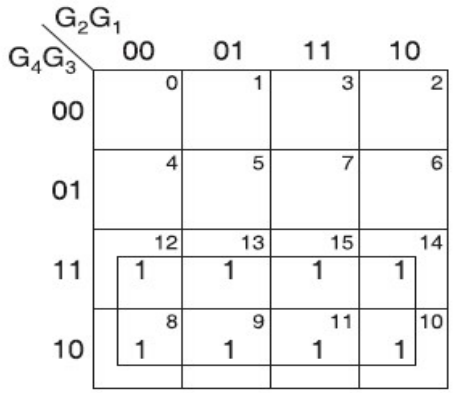
Solution



Design of a 4-bit Gray-to-Binary Code Converter

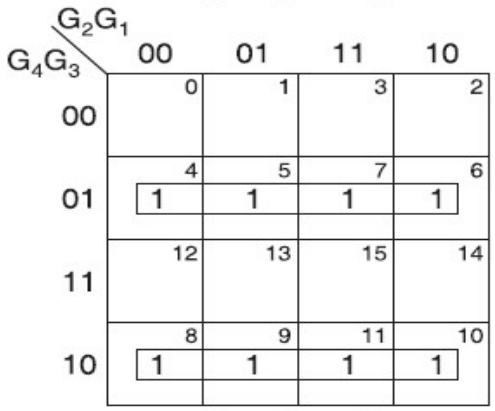
4-bit Gray				4-bit binary			
G_4	G_3	G_2	G_1	B_4	B_3	B_2	B_1
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

(a) Conversion table



$B_4 = G_4$

K-map for B_4



$B_3 = G_4 \oplus G_3$

K-map for B_3

$$B_4 = G_4$$

$$B_3 = \overline{G}_4 G_3 + G_4 \overline{G}_3 = G_4 \oplus G_3$$

$$B_2 = \overline{G}_4 G_3 \overline{G}_2 + \overline{G}_4 \overline{G}_3 G_2 + G_4 \overline{G}_3 \overline{G}_2 + G_4 G_3 G_2$$

$$= \overline{G}_4 (G_3 \oplus G_2) + G_4 (\overline{G_3 \oplus G_2}) = G_4 \oplus G_3 \oplus G_2 = B_3 \oplus G_2$$

$$B_1 = \overline{G}_4 \overline{G}_3 \overline{G}_2 G_1 + \overline{G}_4 \overline{G}_3 G_2 \overline{G}_1 + \overline{G}_4 G_3 G_2 G_1 + \overline{G}_4 G_3 \overline{G}_2 \overline{G}_1 + G_4 G_3 \overline{G}_2 G_1$$

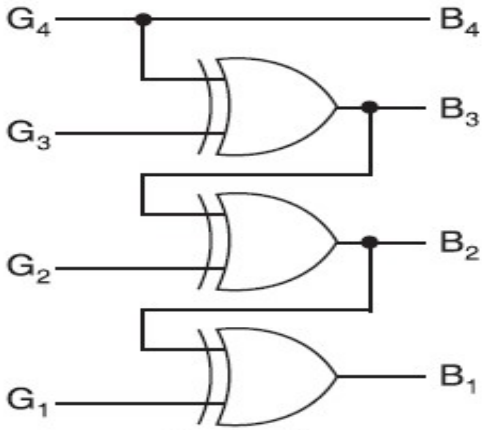
$$+ G_4 G_3 G_2 \overline{G}_1 + G_4 \overline{G}_3 G_2 G_1 + G_4 \overline{G}_3 \overline{G}_2 \overline{G}_1$$

$$= \overline{G}_4 \overline{G}_3 (G_2 \oplus G_1) + G_4 G_3 (G_2 \oplus G_1) + \overline{G}_4 G_3 (\overline{G_2 \oplus G_1}) + G_4 \overline{G}_3 (\overline{G_2 \oplus G_1})$$

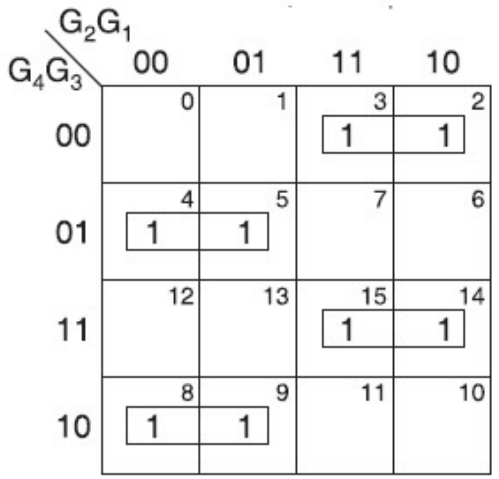
$$= (G_2 \oplus G_1)(\overline{G_4 \oplus G_3}) + (\overline{G_2 \oplus G_1})(G_4 \oplus G_3)$$

$$= G_4 \oplus G_3 \oplus G_2 \oplus G_1$$

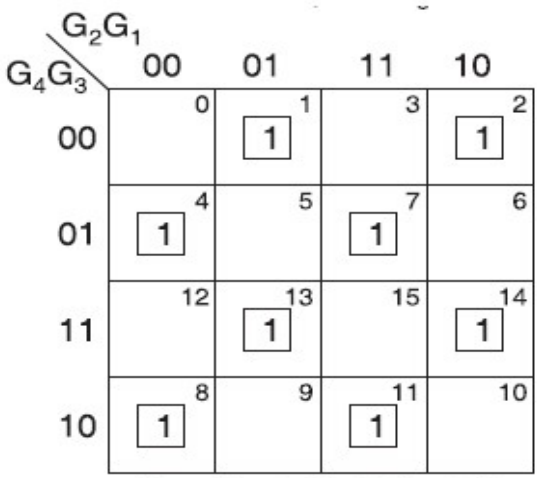
$$= B_2 \oplus G_1$$



Logic diagram



$B_2 = G_4 \oplus G_3 \oplus G_2$
K-map for B_2



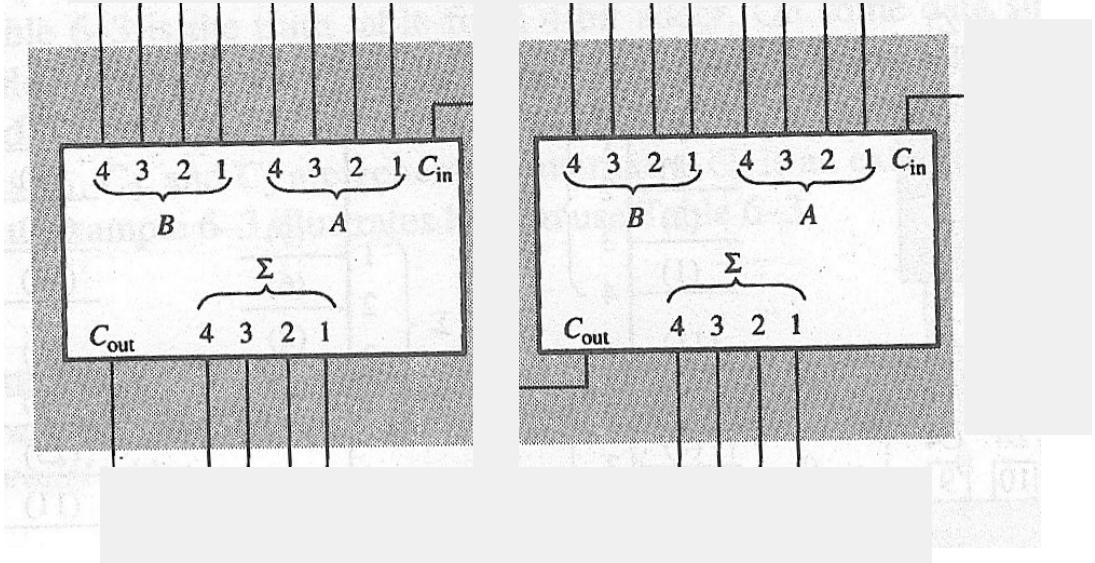
$B_1 = G_4 \oplus G_3 \oplus G_2 \oplus G_1$
K-map for B_1

Expanding Adders

Larger scale adders (adders with more inputs) may be implemented with multiple smaller scale adders

Example Solution

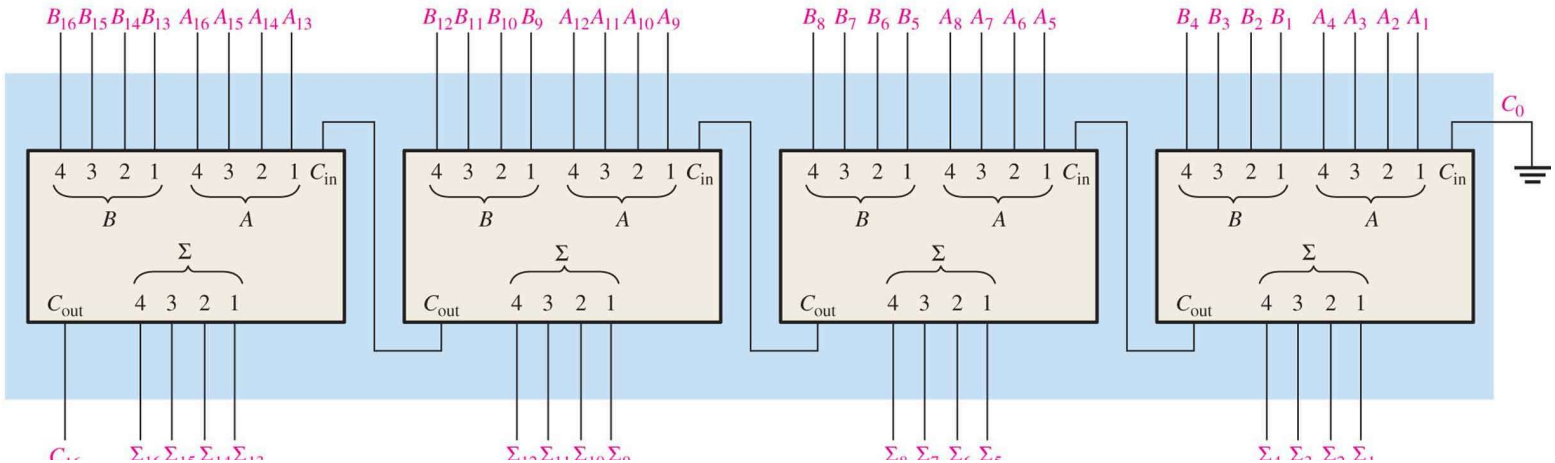
How could you realize a 8-bit adder with 4-bit adders?



Expanding Adders

Example Solution

How could you realize a 8-bit adder with 4-bit adders?



Comparators

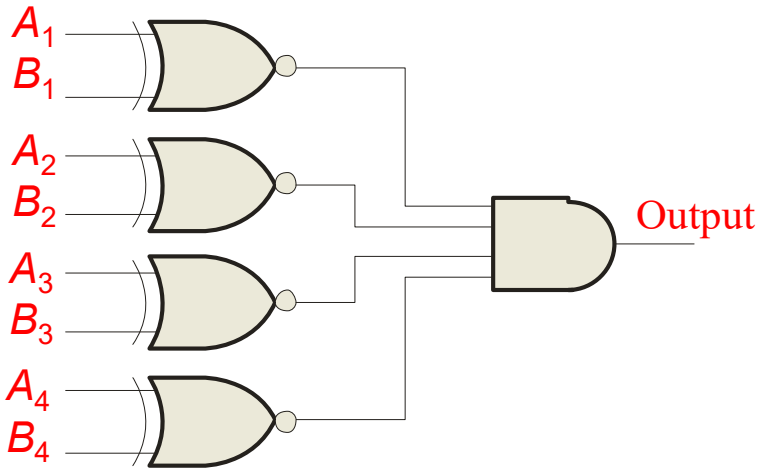
The function of a comparator is to compare the magnitudes of two binary numbers to determine the relationship between them. In the simplest form, a comparator can test for equality using XNOR gates.

Example

How could you test two 4-bit numbers for equality?

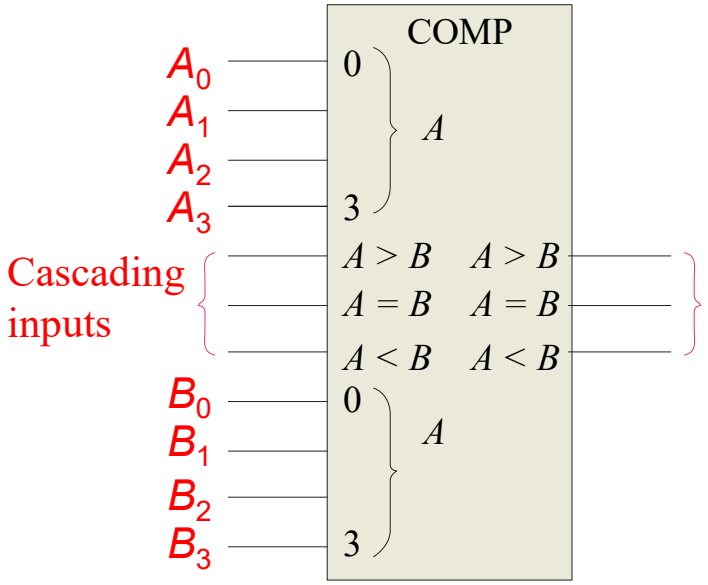
Solution

AND the outputs of four XNOR gates.



Comparators

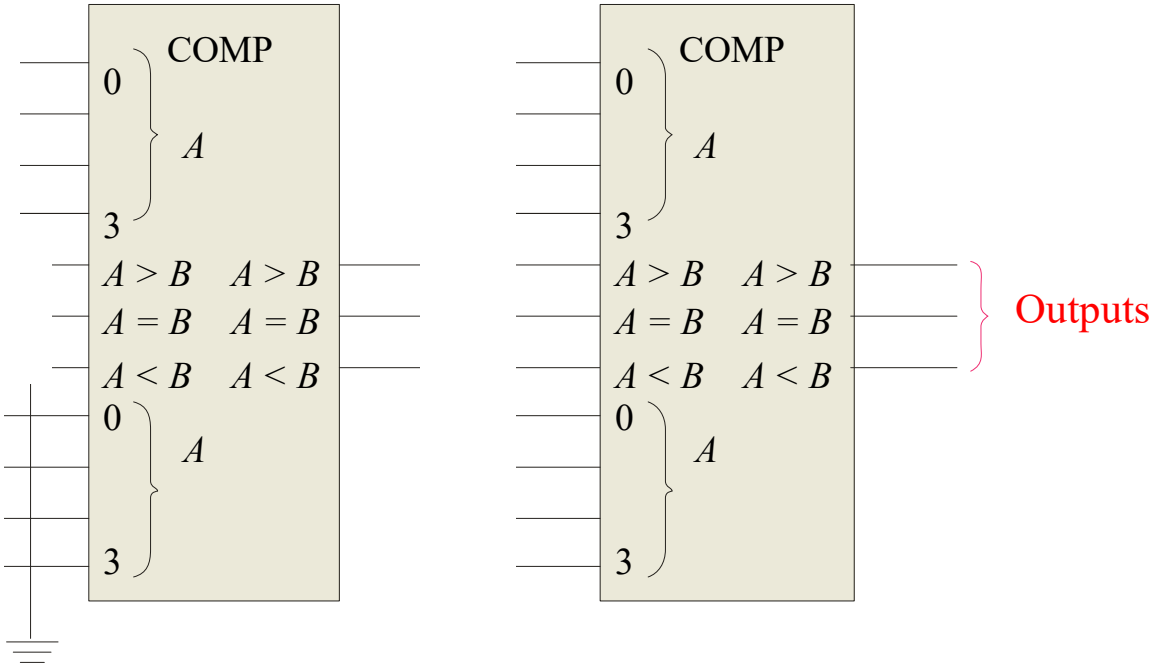
IC comparators provide outputs to indicate which of the numbers is larger or if they are equal. The bits are numbered starting at 0, rather than 1 as in the case of adders. Cascading inputs are provided to expand the comparator to larger numbers.



The IC shown is the 4-bit 74LS85.

Comparators

IC comparators can be expanded using the cascading inputs as shown. The lowest order comparator has a HIGH on the $A = B$ input.

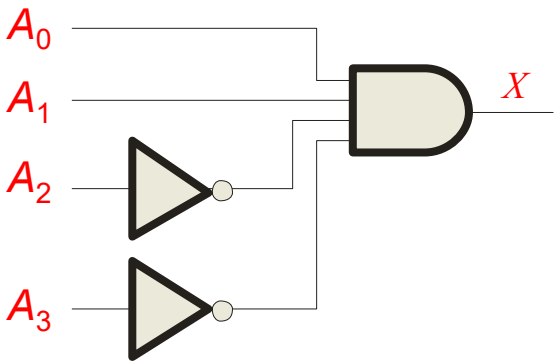


In this chapter…

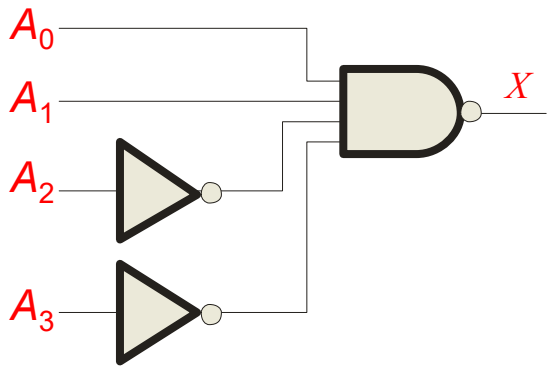
- **Objectives**
  - **Adders**
  - **Comparators**
  - Decoders
  - Encoders
  - Code converters
  - Multiplexers (data selectors)
  - De-multiplexers
  - Parity generators/checkers
- **Reading Assignment**
  - pp.285-332

Decoders

A **decoder** is a logic circuit that detects the presence of a specific input combination. Two simple decoders that detect the presence of the binary code 0011 are shown. The first has an active HIGH output; the second has an active LOW output.



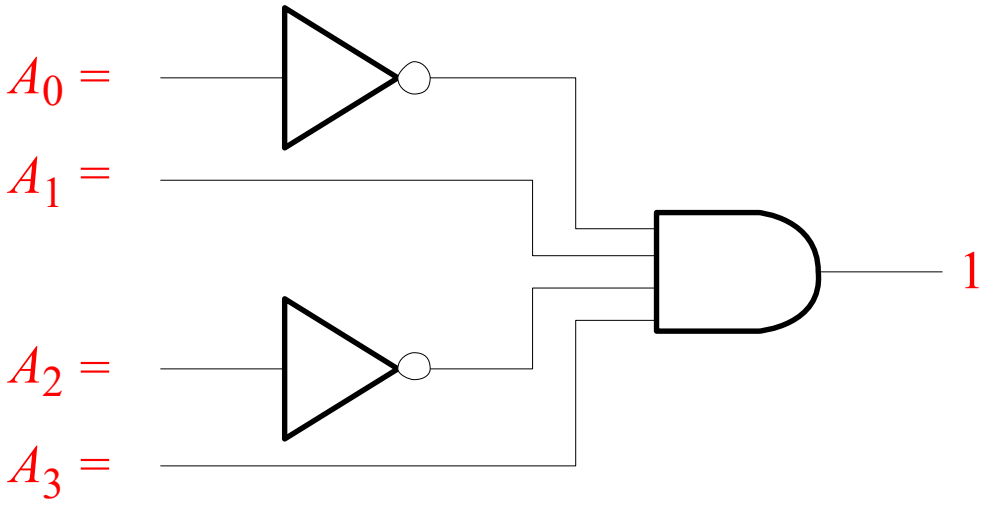
Active HIGH decoder for 0011



Active LOW decoder for 0011

Decoders

Question Assume the output of the decoder shown is a logic 1. What are the inputs to the decoder?

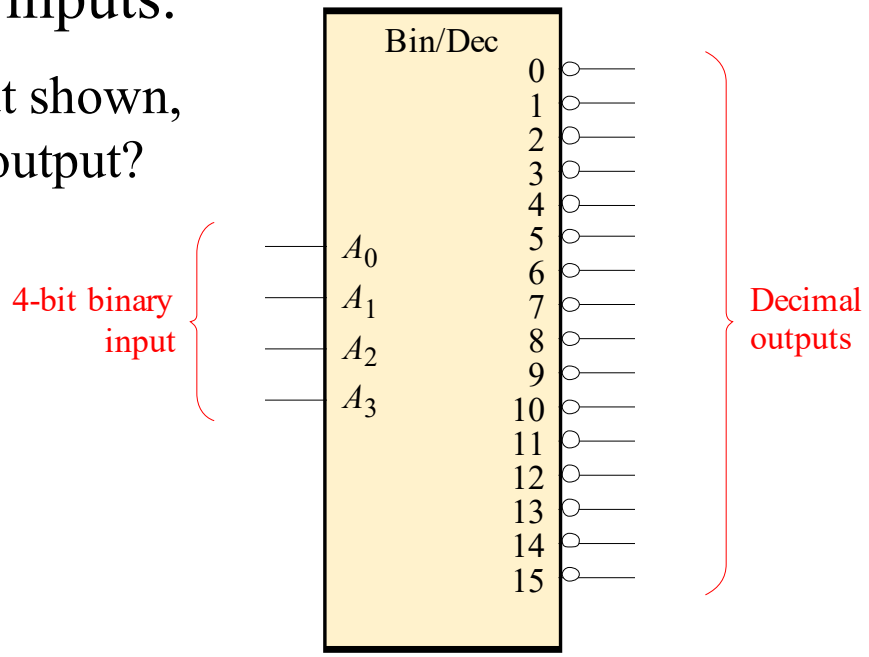


Decoders

IC decoders have multiple outputs to decode any combination of inputs. For example the binary-to-decimal decoder shown here has 16 outputs – one for each combination of binary inputs.

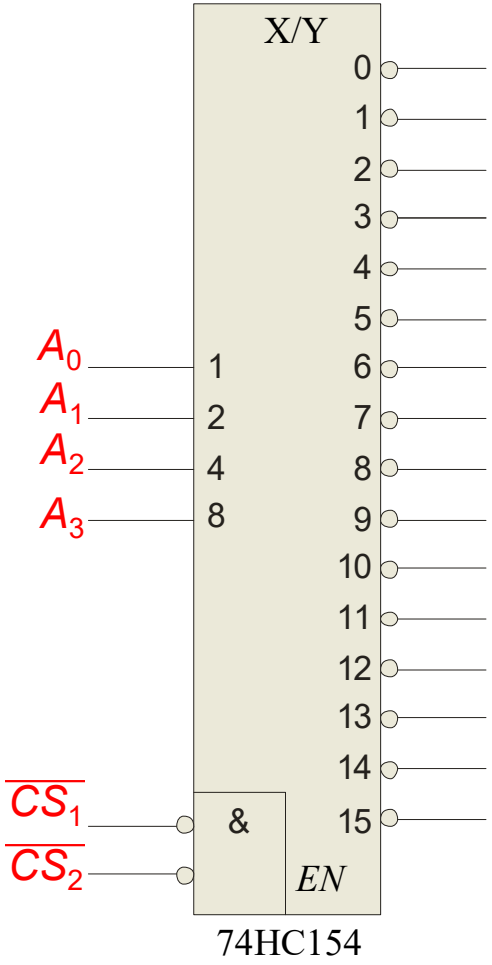
Question

For the input shown, what is the output?



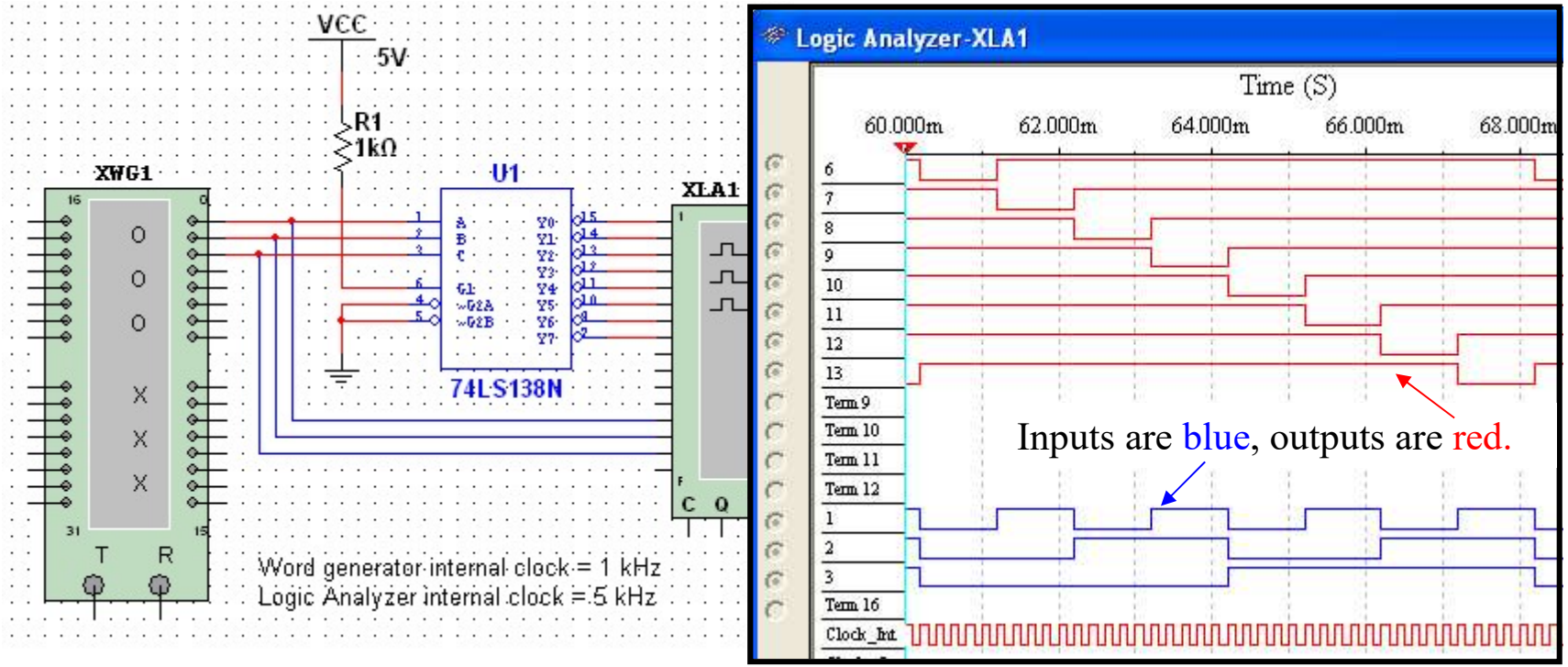
Decoders

A specific integrated circuit decoder is the 74HC154 (shown as a 4-to-16 decoder). It includes two active LOW chip select lines which must be at the active level to enable the outputs. These lines can be used to expand the decoder to larger inputs.



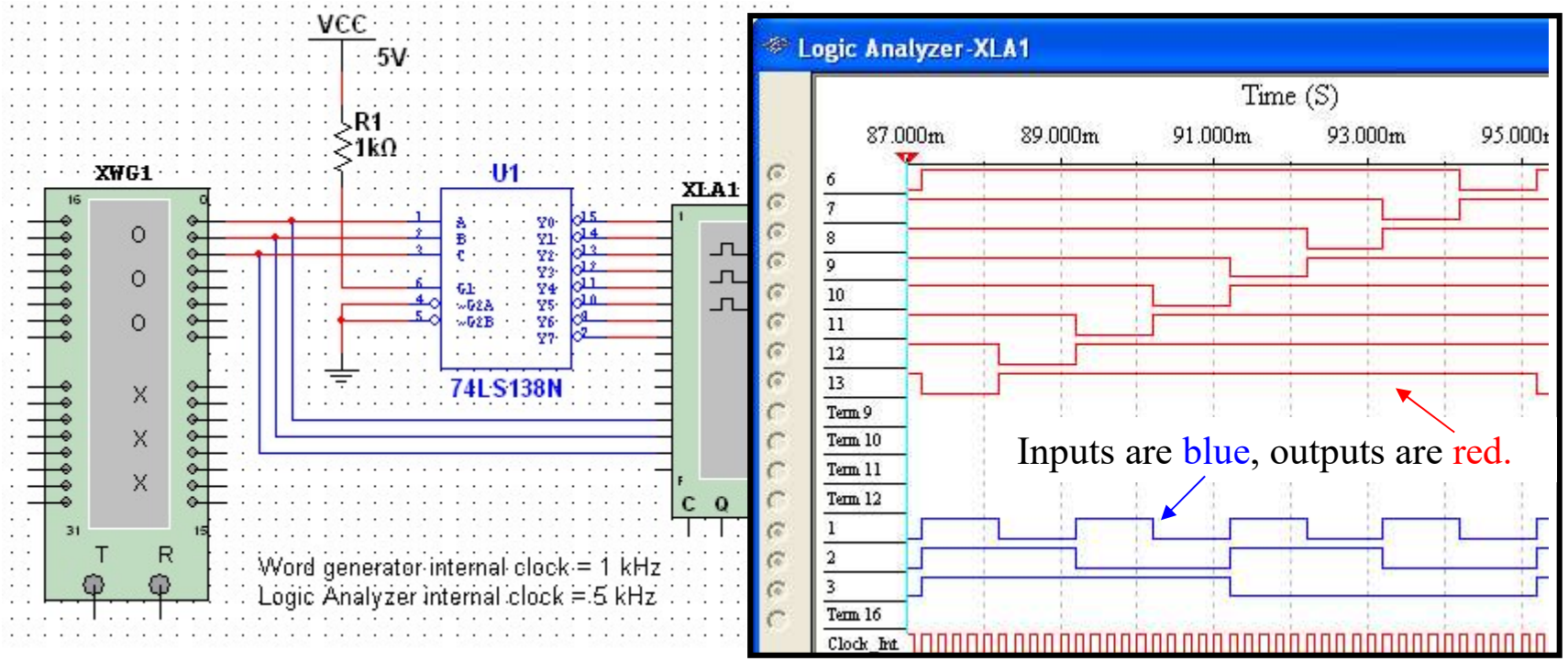
Decoders

The 74LS138 is a 3-to-8 decoder with three chip select inputs (two active LOW, one active HIGH). In this Multisim circuit, the word generator (XWG1) is set up as an up counter. The logic analyzer (XLA1) compares the input and outputs of the decoder.



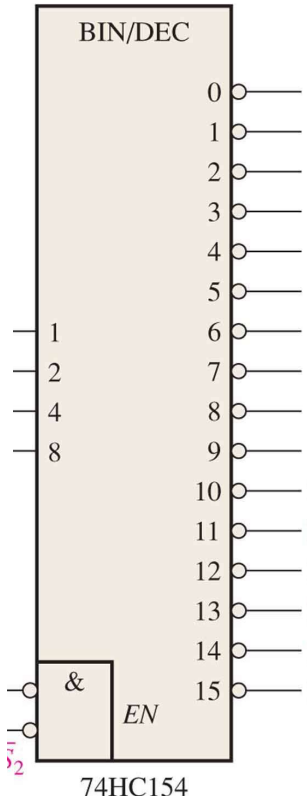
Decoders

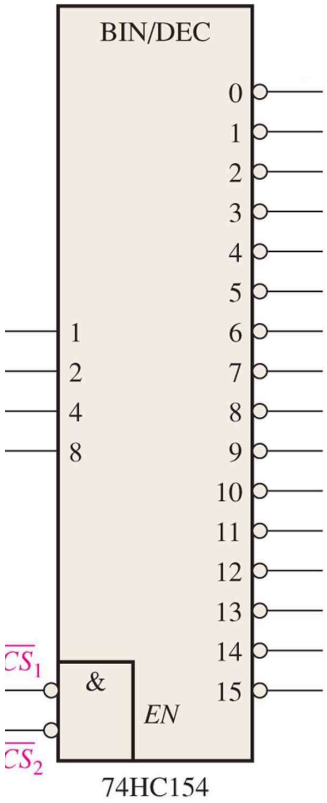
Question How will the waveforms change if the word generator is configured as a down counter instead of an up counter?



Expanding decoders

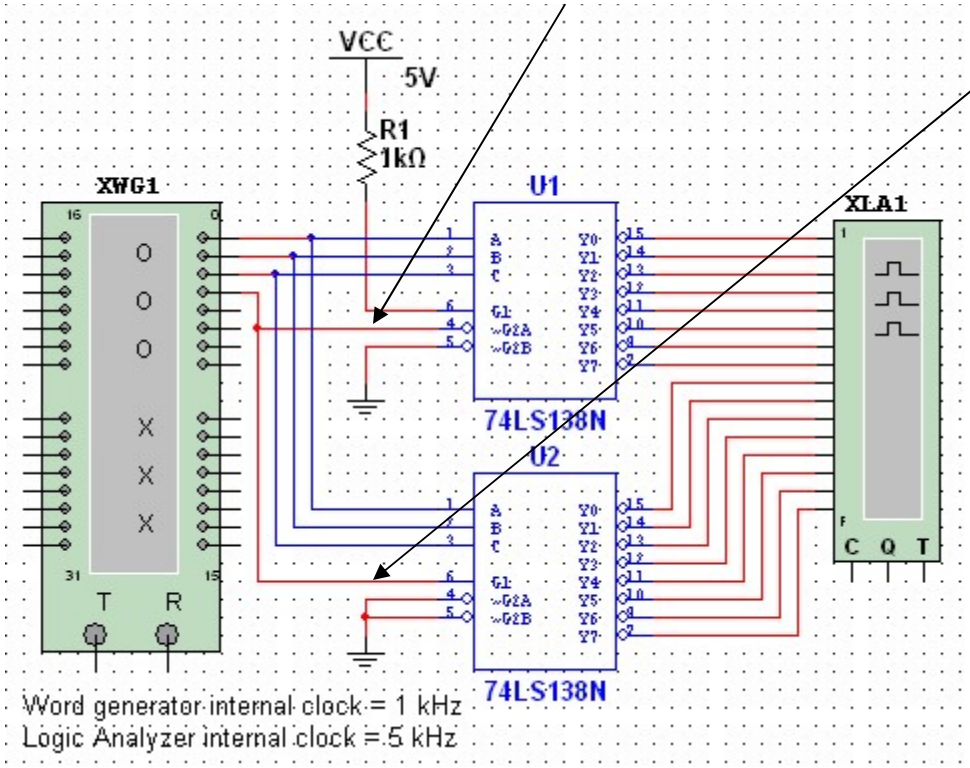
Decoders may be expanded with chip enable pins.





Decoders

The chip select inputs can be used to expand a decoder. In this circuit, two 74LS138s are configured as a 16 line decoder. Notice how the MSB is connected to one active LOW and one active HIGH chip select.



The next slide shows the logic analyzer output…

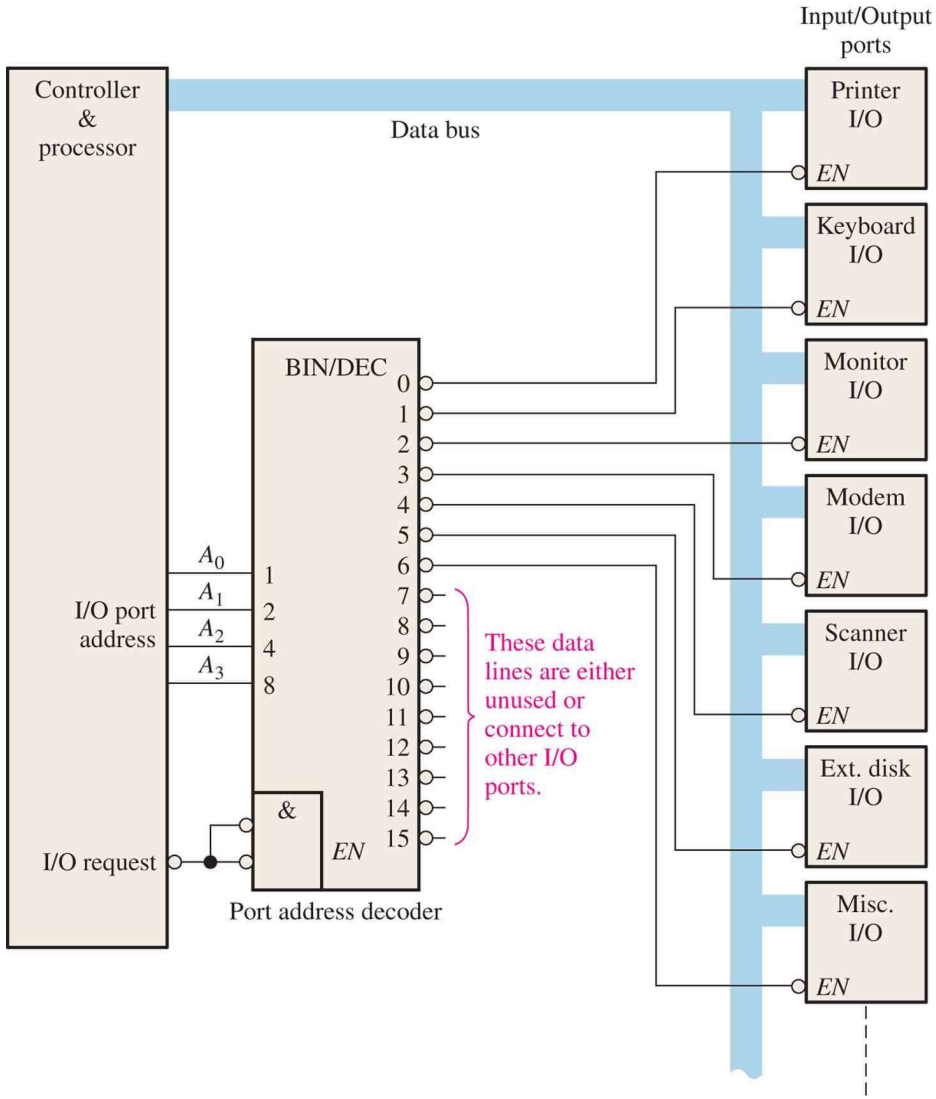
Decoders

Question

Is the word generator set as an up counter or a down counter? (The least significant decoder output at the top). It is an up counter.

Decoder Applications

Decoders can be used in computer systems for I/O addressing. In this example, the controller is able to control up to 16 I/O devices through 4 address lines.



Decoders and minterms

Each output of the decoder implement one minterm. And recall that all logic functions may be implemented with sum of minterms (std. SOP). So logic functions may be implemented with decoders by combining multiple outputs.

$\bar{A}_3\bar{A}_2\bar{A}_1\bar{A}_0$
$\bar{A}_3\bar{A}_2\bar{A}_1A_0$
$\bar{A}_3\bar{A}_2A_1\bar{A}_0$
$\bar{A}_3\bar{A}_2A_1A_0$
$\bar{A}_3A_2\bar{A}_1\bar{A}_0$
$\bar{A}_3A_2\bar{A}_1A_0$
$\bar{A}_3A_2A_1\bar{A}_0$
$\bar{A}_3A_2A_1A_0$
$A_3\bar{A}_2\bar{A}_1\bar{A}_0$
$A_3\bar{A}_2\bar{A}_1A_0$
$A_3\bar{A}_2A_1\bar{A}_0$
$A_3\bar{A}_2A_1A_0$
$A_3A_2\bar{A}_1\bar{A}_0$
$A_3A_2\bar{A}_1A_0$
$A_3A_2A_1\bar{A}_0$
$A_3A_2A_1A_0$

Decoders and minterms

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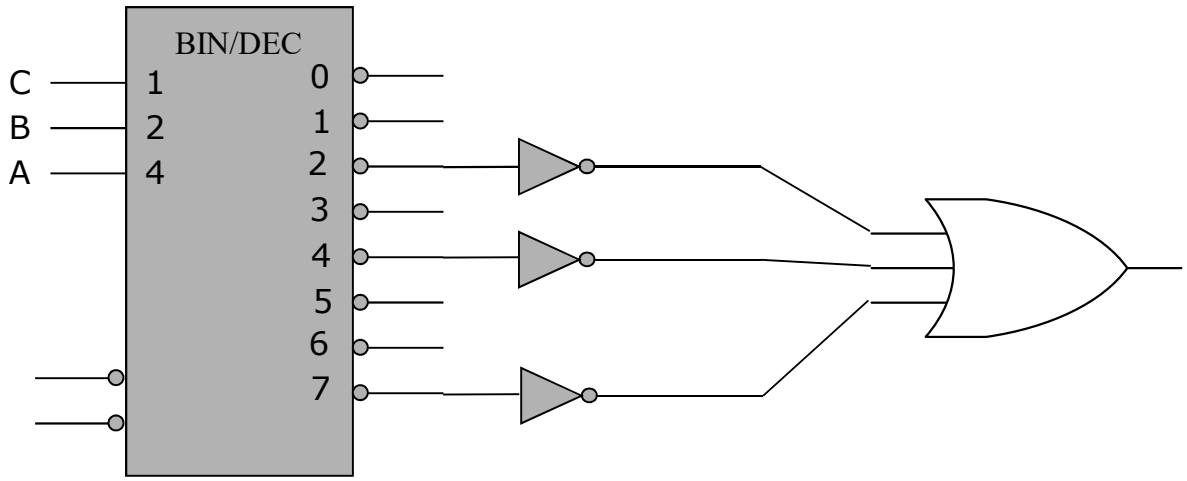
Example **Implement the logic function with a decoder:**
F=A'BC'+AB'C'+ABC

Solution



Decoders and minterms

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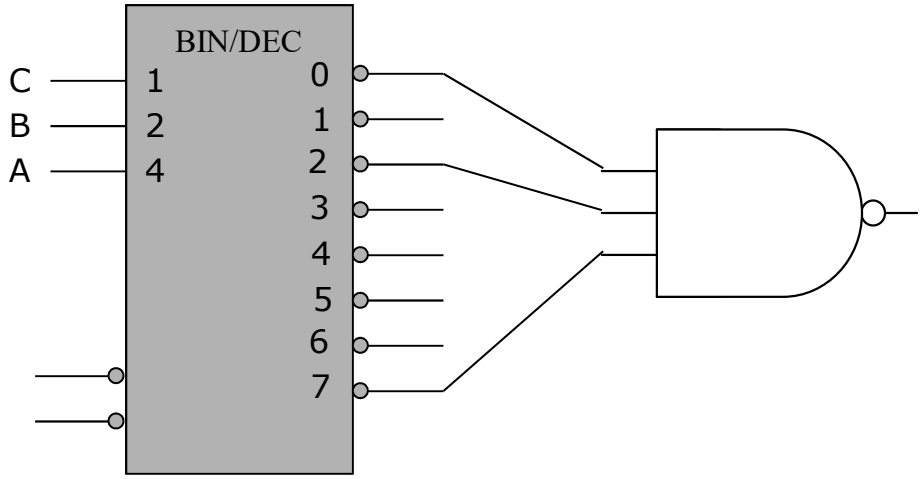
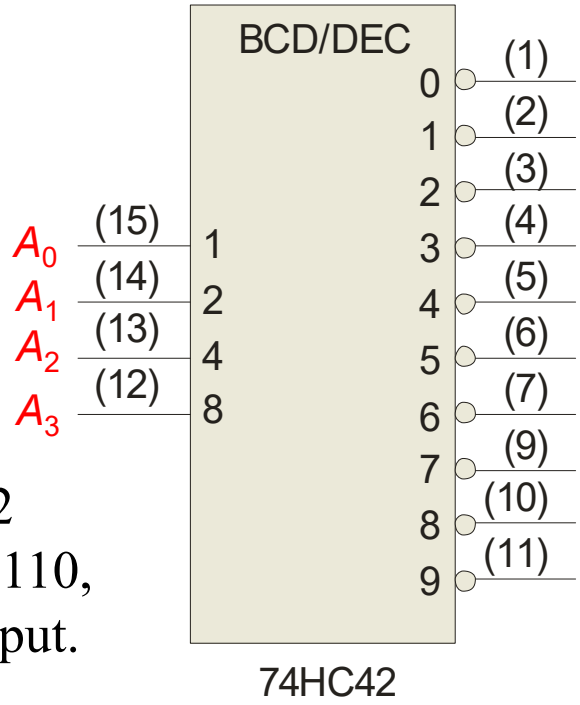


Decoders

BCD-to-decimal decoders accept a binary coded decimal input and activate one of ten possible decimal digit indications.



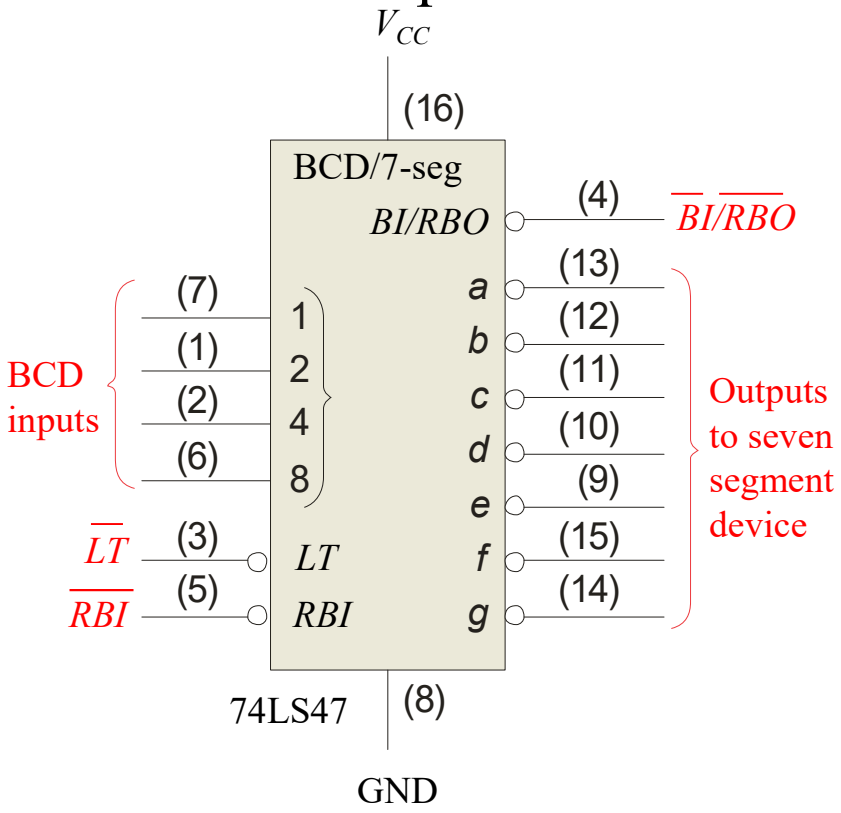
Example Assume the inputs to the 74HC42 decoder are the sequence 0101, 0110, 0011, and 0010. Describe the output.

Solution All lines are HIGH except for one active output, which is LOW. The active outputs are 5, 6, 3, and 2 in that order.

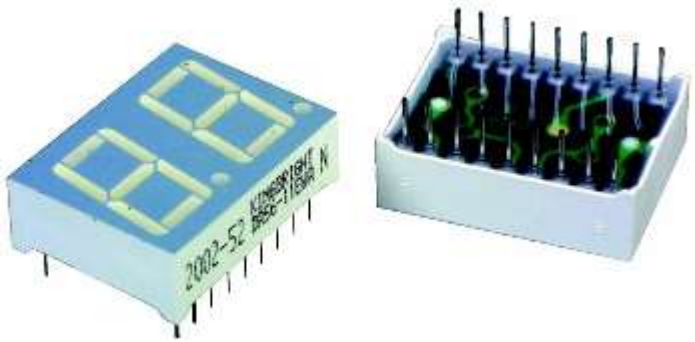
BCD-to-seven segment display Decoder/Driver

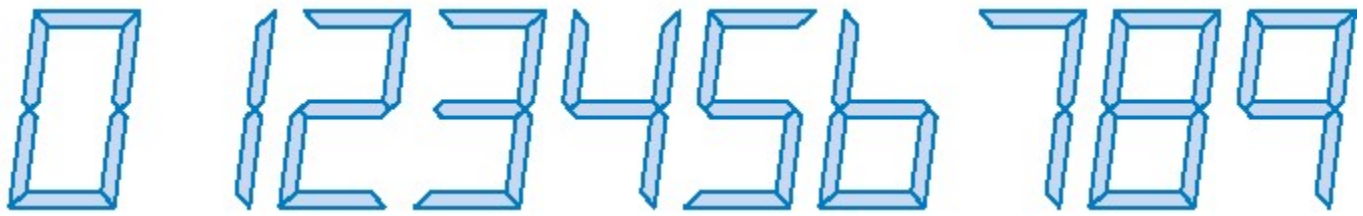
Another useful decoder is the 74LS47. This is a BCD-to-seven segment display with active LOW outputs.

The *a*-*g* outputs are designed for much higher current than most devices (hence the word driver in the name).

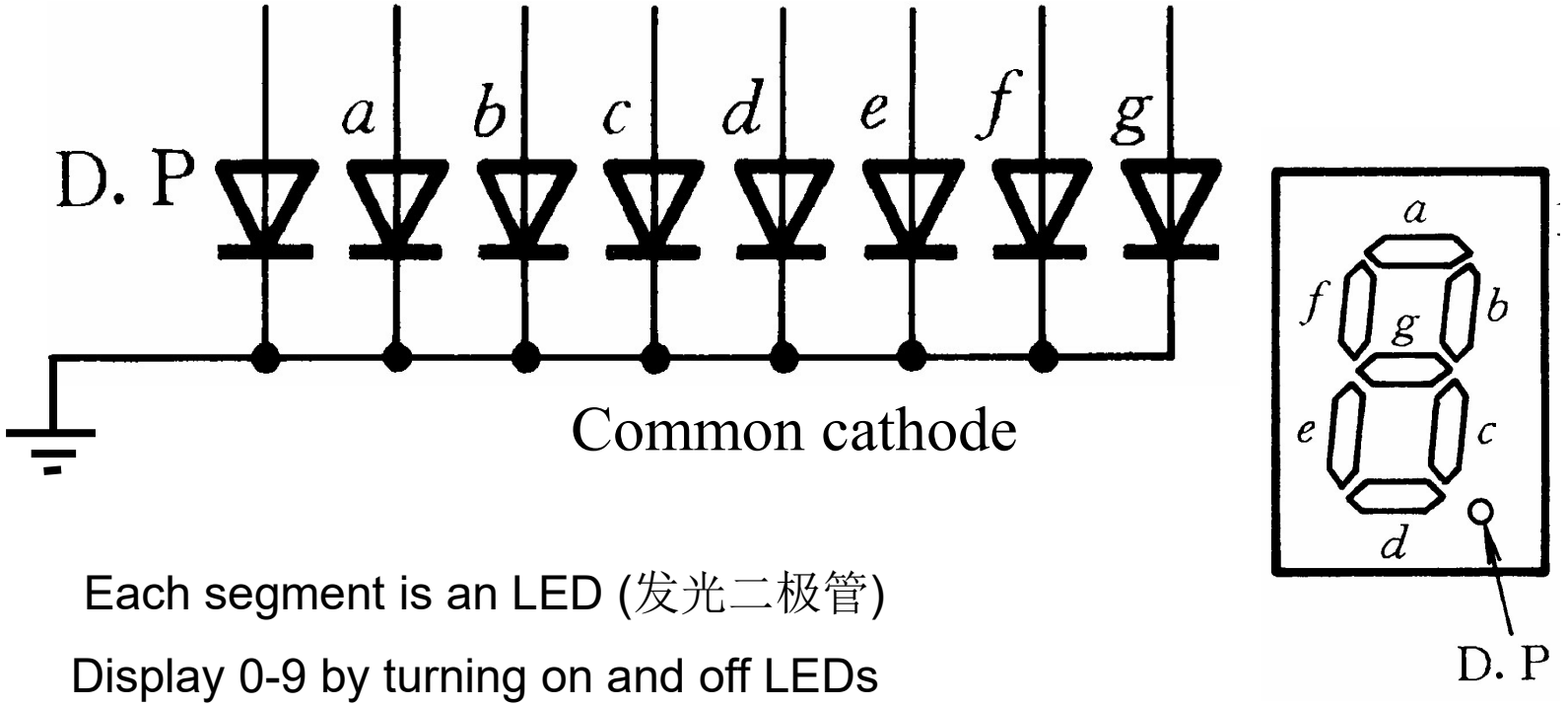


Seven segment display





Seven segment display



Each segment is an LED (发光二极管)

Display 0-9 by turning on and off LEDs

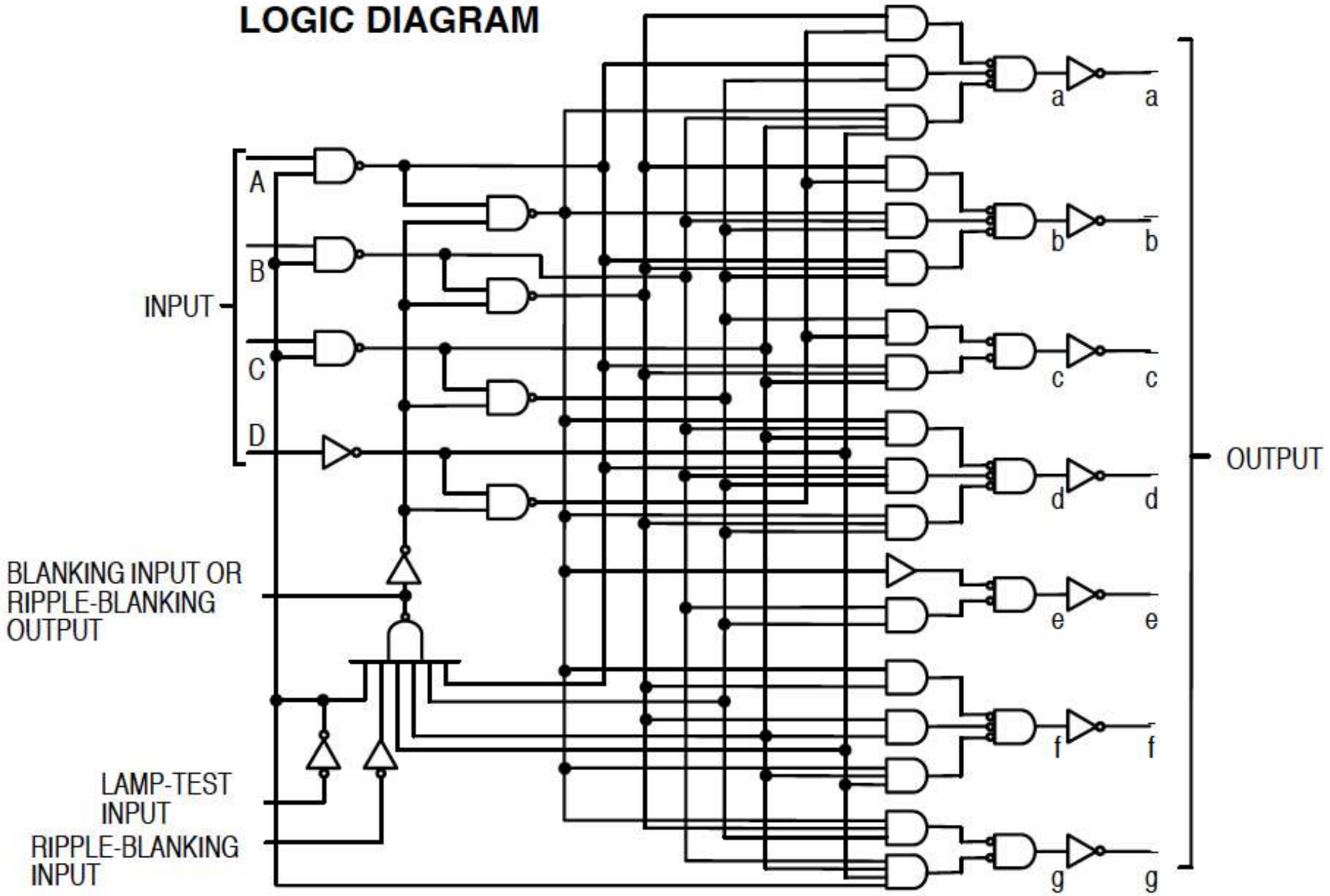
D.P: Decimal Point

BCD-to-seven segment display Decoder/Driver

- **$\overline{\text{LT}}$(Lamp Test)**
  - Active low input
  - In test mode when $\overline{\text{LT}}$ is low, LED are lit
  - Normal working mode when $\overline{\text{LT}}$ is 1
- **$\overline{\text{RBI}}$(Ripple blanking input)**
  - Active low input. 0 is suppressed when active.
- **$\overline{\text{BI}}$/$\overline{\text{RBO}}$(Blanking input/ripple blanking output)**
  - Active low input/output
  - Wired-and internally

SN54/74LS47

LOGIC DIAGRAM

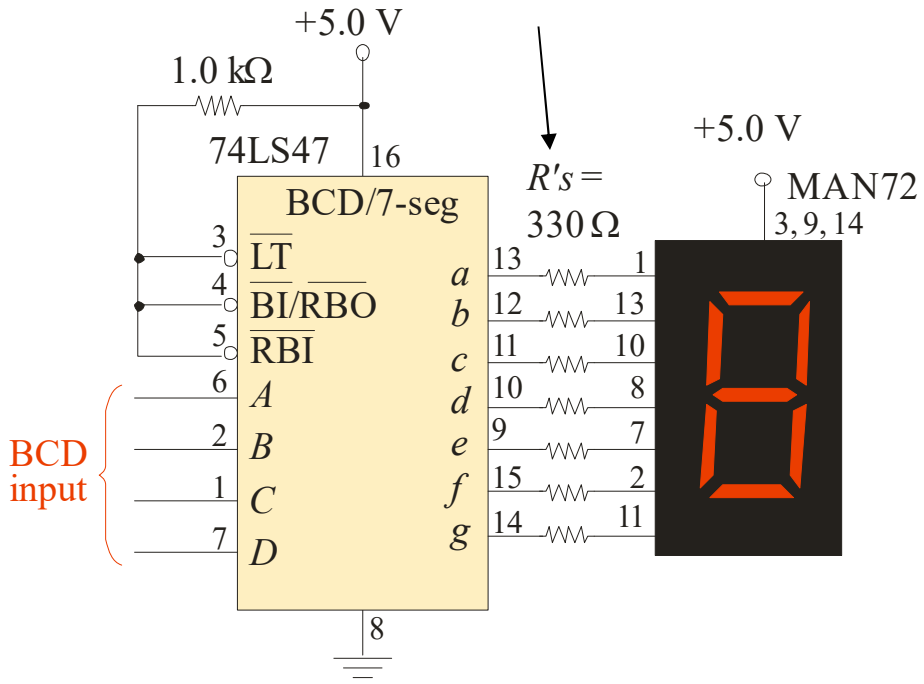


Truth Table SN54/74LS47

Decimal or Function	Inputs							Outputs							Note
	$\overline{LT}$	$\overline{RBI}$	A3	A2	A1	A0	$\overline{BI/RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	(Note 2)
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	(Note 2)
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(Note 3)
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(Note 4)
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(Note 5)

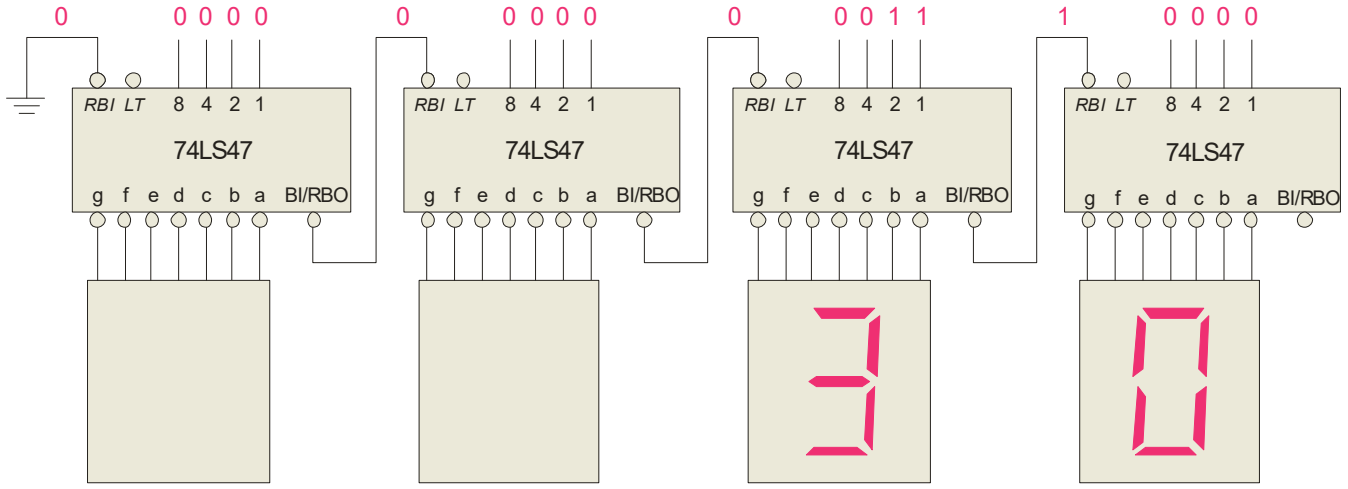
BCD Decoder/Driver

Here the 7447A is an connected to an LED seven segment display. Notice the current limiting resistors, required to prevent overdriving the LED display.



BCD Decoder/Driver

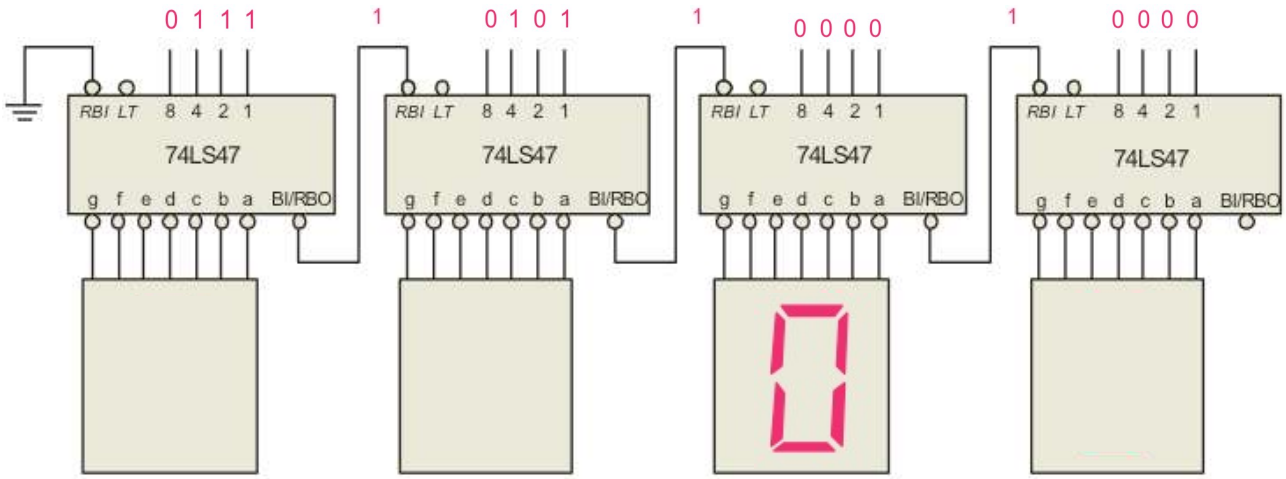
The 74LS47 features leading zero suppression, which blanks unnecessary leading zeros but keeps significant zeros as illustrated here. The $\overline{BI}/\overline{RBO}$ output is connected to the $\overline{RBI}$ input of the next decoder.



Depending on the display type, current limiting resistors may be required.

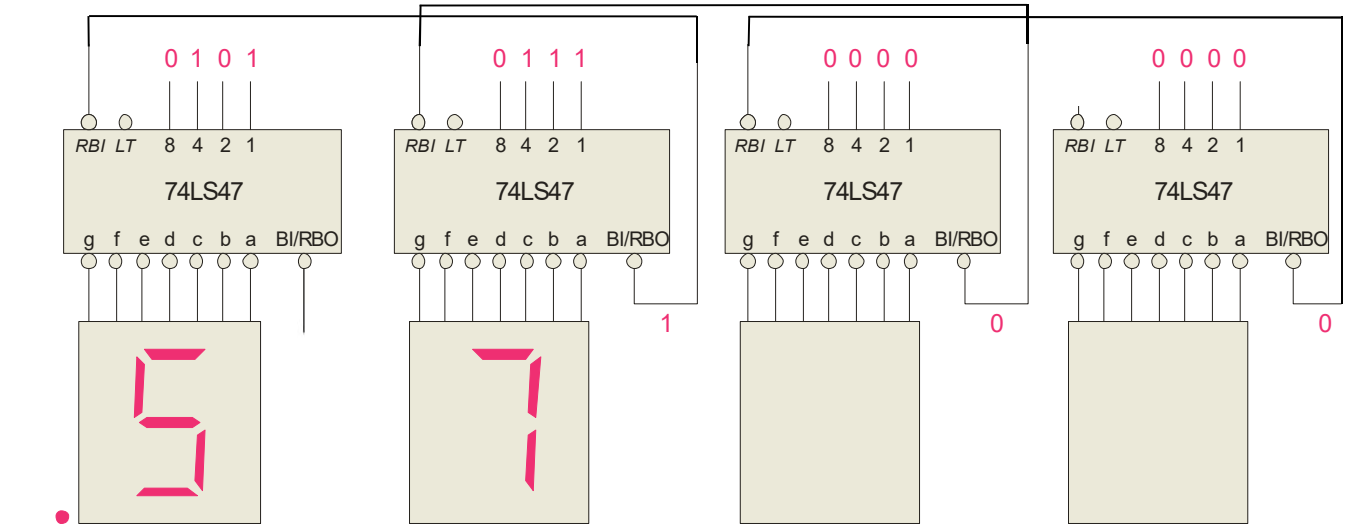
BCD Decoder/Driver

Question Determine the output on each display.



BCD Decoder/Driver

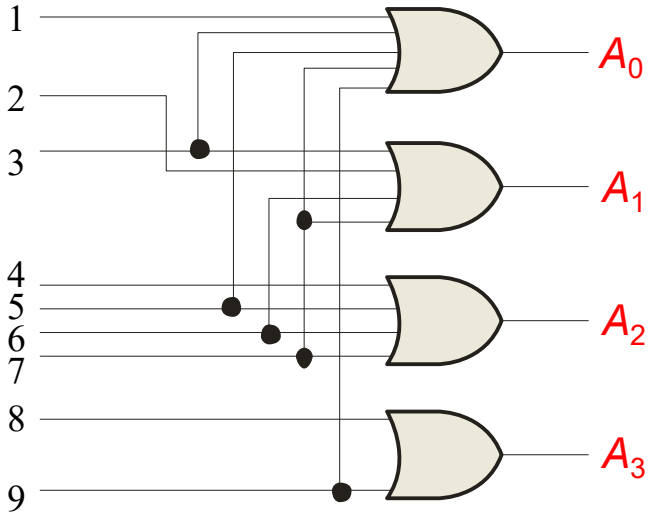
Trailing zero suppression blanks unnecessary trailing zeros to the right of the decimal point as illustrated here. The $\overline{RBI}$ input is connected to the $\overline{BI/RBO}$ output of the following decoder.



Encoders

An **encoder** accepts an active logic level on one of its inputs and converts it to a coded output, such as BCD or binary.

The decimal to BCD is an encoder with an input for each of the ten decimal digits and four outputs that represent the BCD code for the active digit. The basic logic diagram is shown. There is no zero input because the outputs are all LOW when the input is zero.



Encoders

An **encoder** accepts an active logic level on one of its inputs and converts it to a coded output, such as BCD or binary. A 8-line-to-3-line encoder has the following Truth Table.

	I0	I1	I2	I3	I4	I5	I6	I7	Y0	Y1	Y2
0	1	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	1	0	0
2	0	0	1	0	0	0	0	0	0	1	0
3	0	0	0	1	0	0	0	0	1	1	0
4	0	0	0	0	1	0	0	0	0	0	1
5	0	0	0	0	0	1	0	0	1	0	1
6	0	0	0	0	0	0	1	0	0	1	1
7	0	0	0	0	0	0	0	1	1	1	1

Question

How is the output related to the inputs?

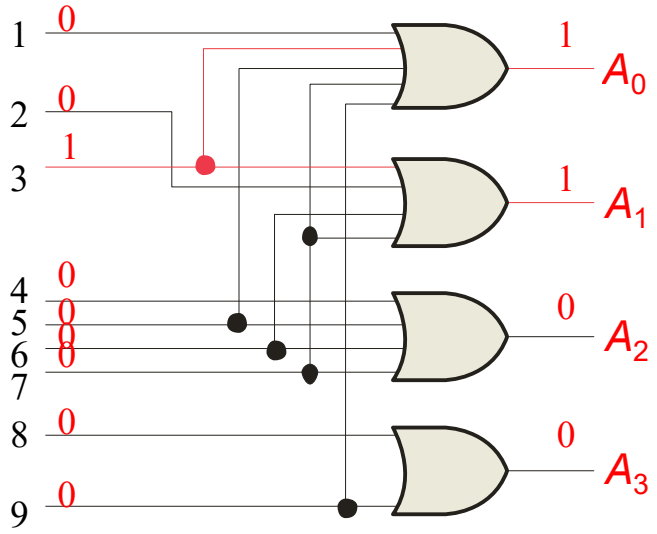
Encoders

Example

Show how the decimal-to-BCD encoder converts the decimal number 3 into a BCD 0011.

Solution

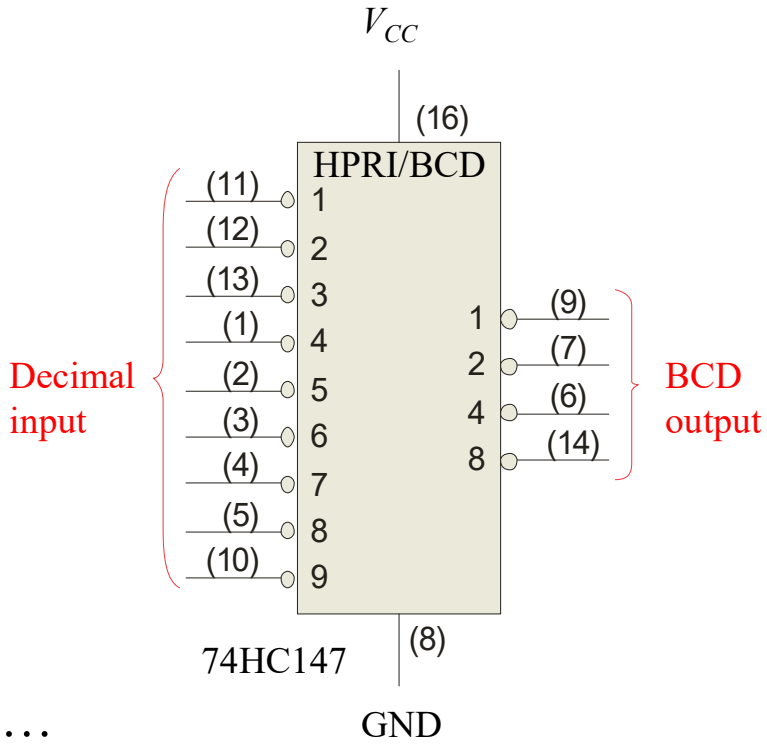
The top two OR gates have ones as indicated with the red lines. Thus the output is 0111.



Encoders

The 74HC147 is an example of an IC encoder. It is has ten active-LOW inputs and converts the active input to an active-LOW BCD output.

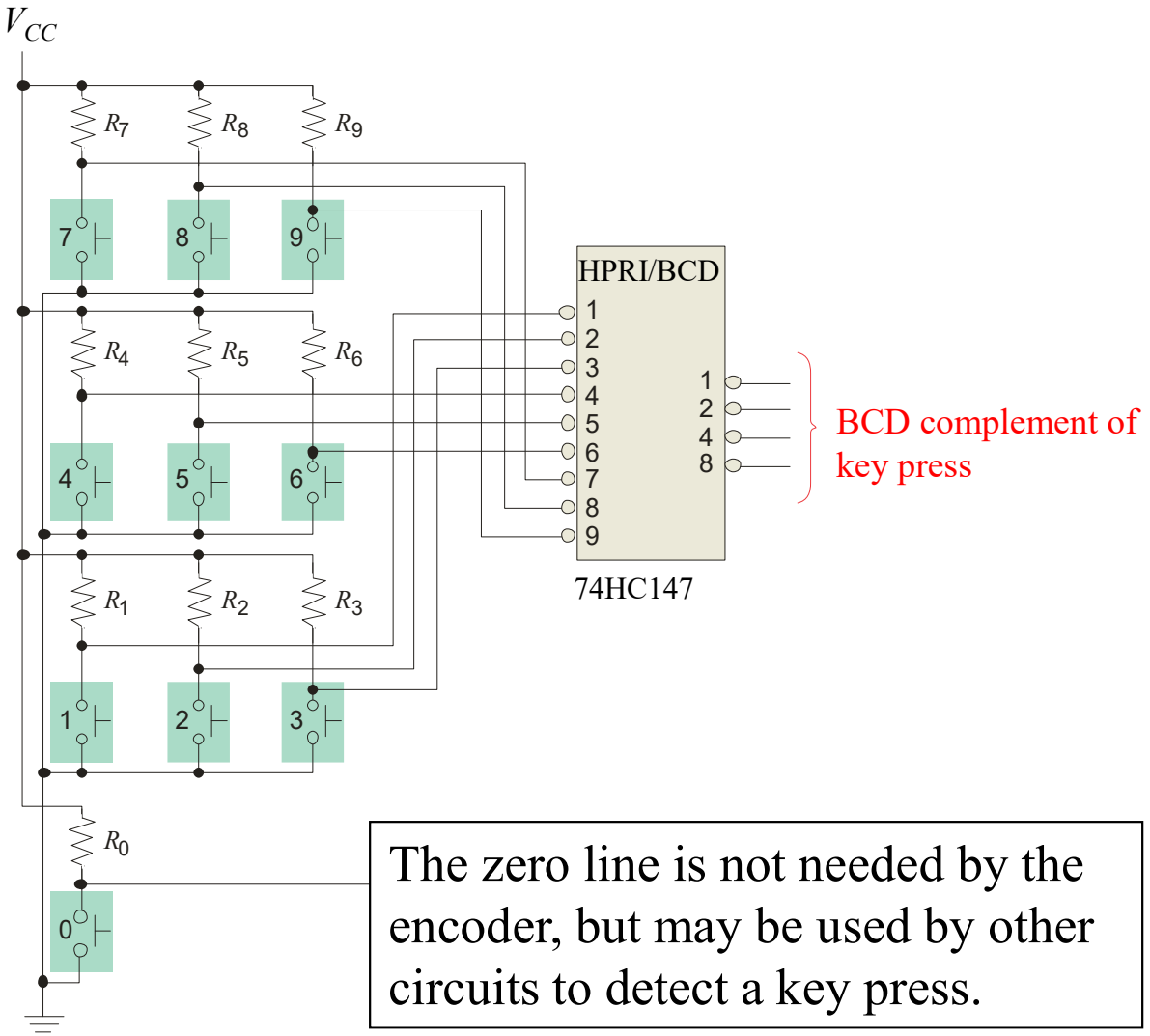
This device offers additional flexibility in that it is a **priority encoder**. This means that if more than one input is active, the one with the highest order decimal digit will be active.



The next slide shows an application …

Encoders

Keyboard encoder



The zero line is not needed by the encoder, but may be used by other circuits to detect a key press.

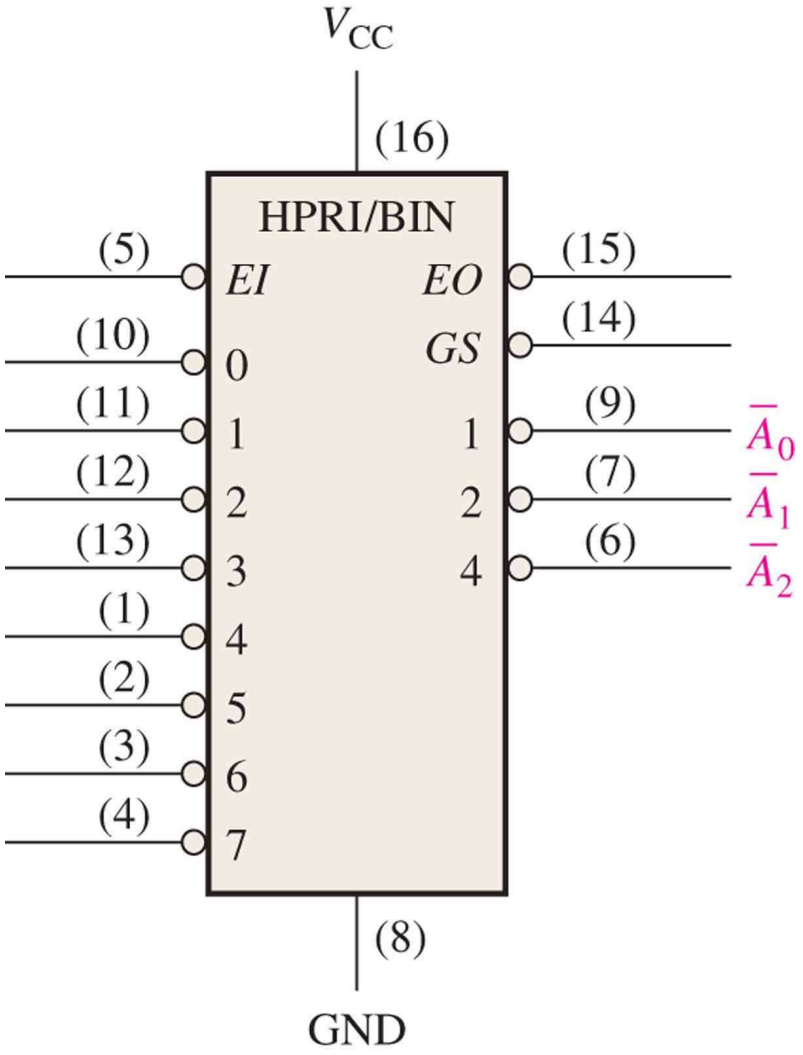
Encoders

74LS148
8-line-to-3-line encoder

$\overline{EI}$: Enable input

$\overline{EO}$: Empty output

$\overline{GS}$: Group Selection



Truth Table of 74LS148 - 8-line-to-3-line encoder

Inputs									Outputs				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	×	×	×	×	×	×	×	×	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	×	×	×	×	×	×	×	L	L	L	L	L	H
L	×	×	×	×	×	×	L	H	L	L	H	L	H
L	×	×	×	×	×	L	H	H	L	H	L	L	H
L	×	×	×	×	L	H	H	H	L	H	H	L	H
L	×	×	×	L	H	H	H	H	H	L	L	L	H
L	×	×	L	H	H	H	H	H	H	L	H	L	H
L	×	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H; high level, L; low level, X; irrelevant

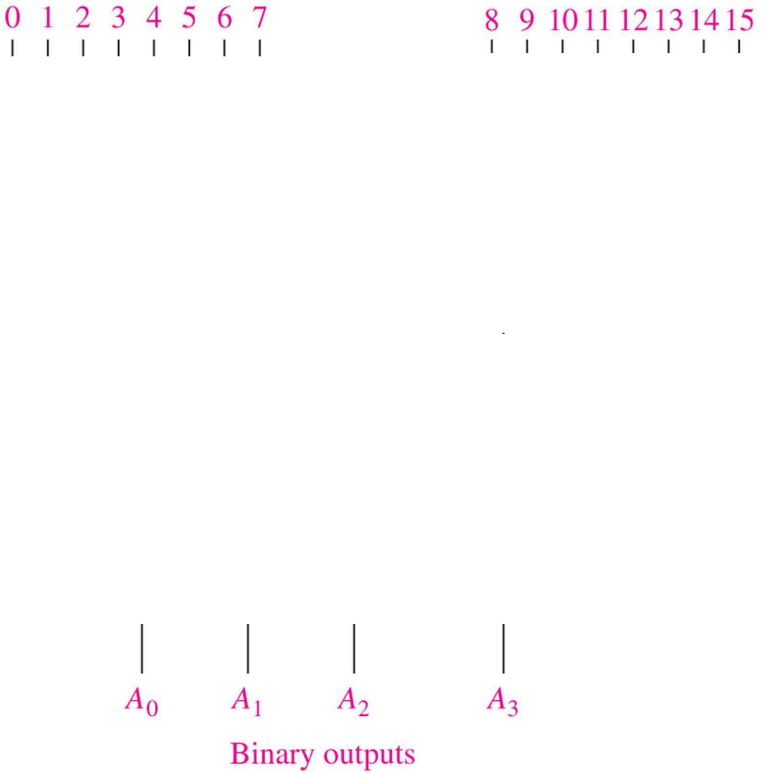
$\overline{EI}$: Enable input $\overline{EO}$: Empty output $\overline{GS}$: Group Selection

or, Got Something

Encoders Expansions

Question

How to implement a 16-to-4 encoder with two 8-to-3 encoders?



Encoders Expansions

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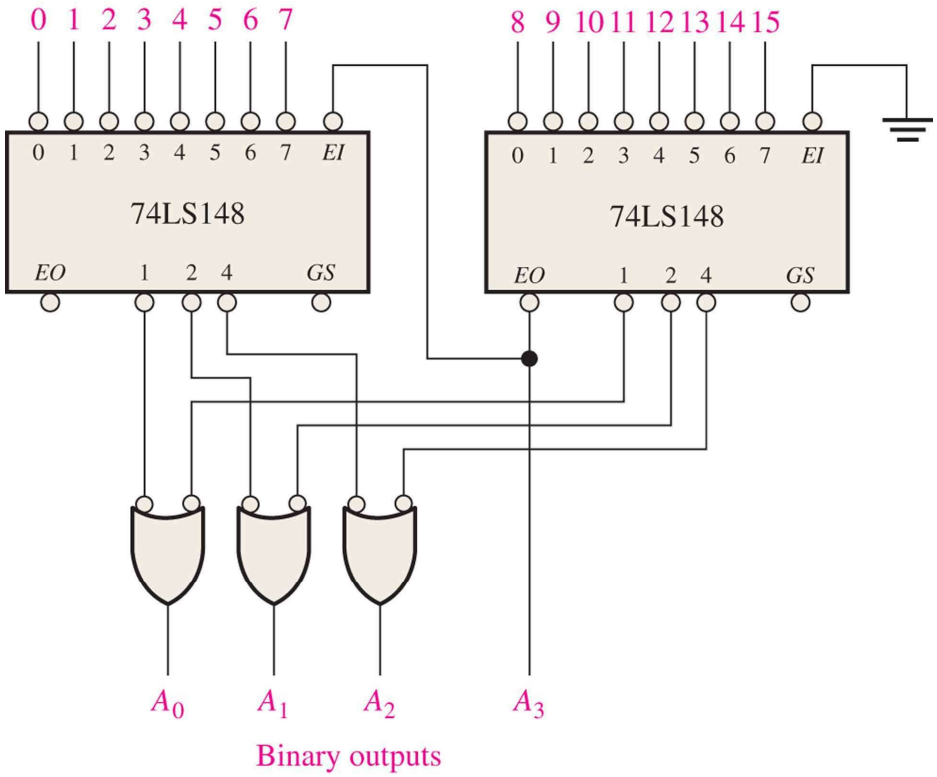
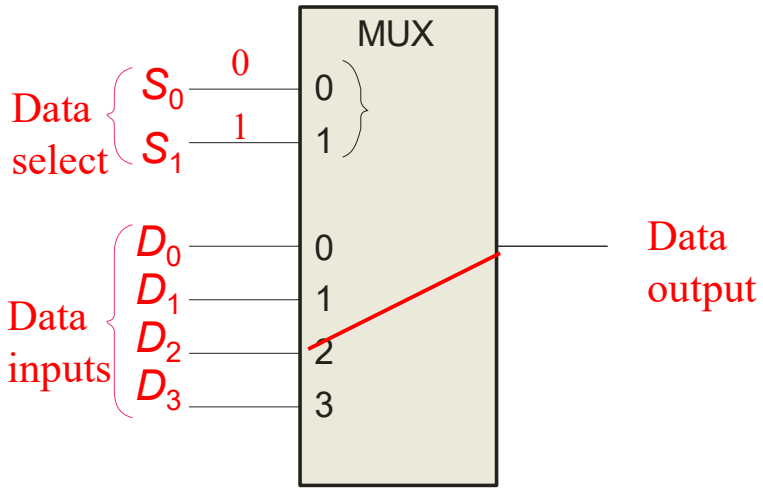
How to implement a 16-to-4 encoder with two 8-to-3 encoders?



Multiplexers

A multiplexer (MUX) selects one data line from two or more input lines and routes data from the selected line to the output. The particular data line that is selected is determined by the select inputs.

Two select lines are shown here to choose any of the four data inputs.



Question

Which data line is selected if $S_1S_0 = 10$? D_2

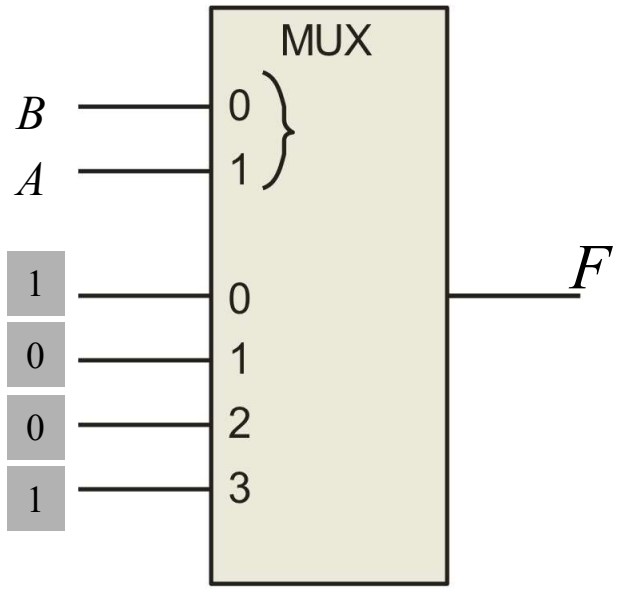
Multiplexers

A multiplexer (MUX) of N data selection inputs may be used to implement any logic function with up to N variables.

Example Implement $F=A'B'+AB$ with a 1-in-4 MUX

Solution

Connect the data inputs of the MUX to the corresponding logic value of the logic function.

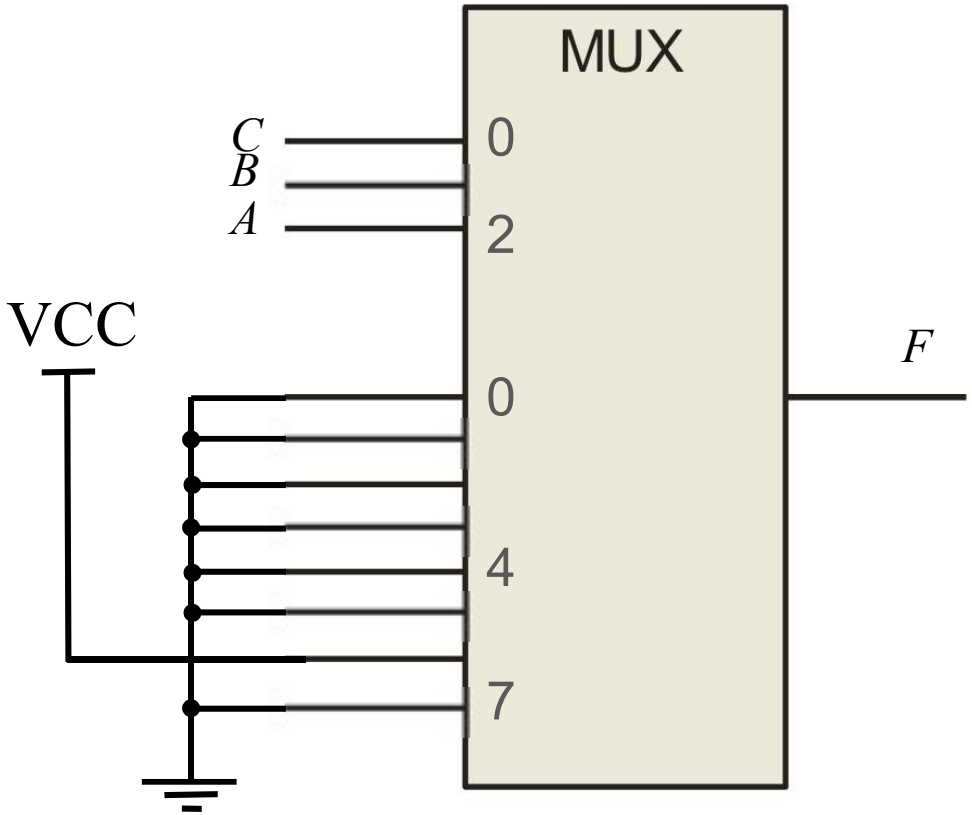


Multiplexers

Example

Implement $F=ABC'$ with a 1-in-8 MUX

Solution



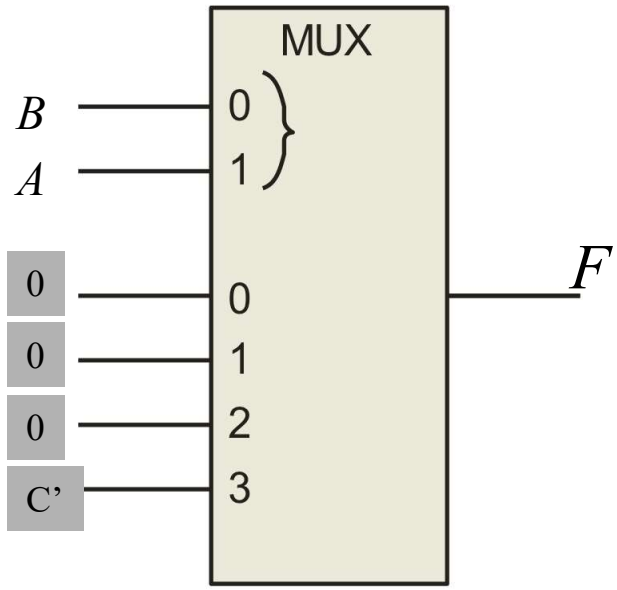
Multiplexers

A multiplexer (MUX) of N data selection inputs may also be used to implement any logic function with N+1 variables.

Example Implement $F=ABC'$ with a 1-in-4 MUX

Solution

Connect the data inputs of the MUX to the corresponding logic value of the logic function.



Multiplexers

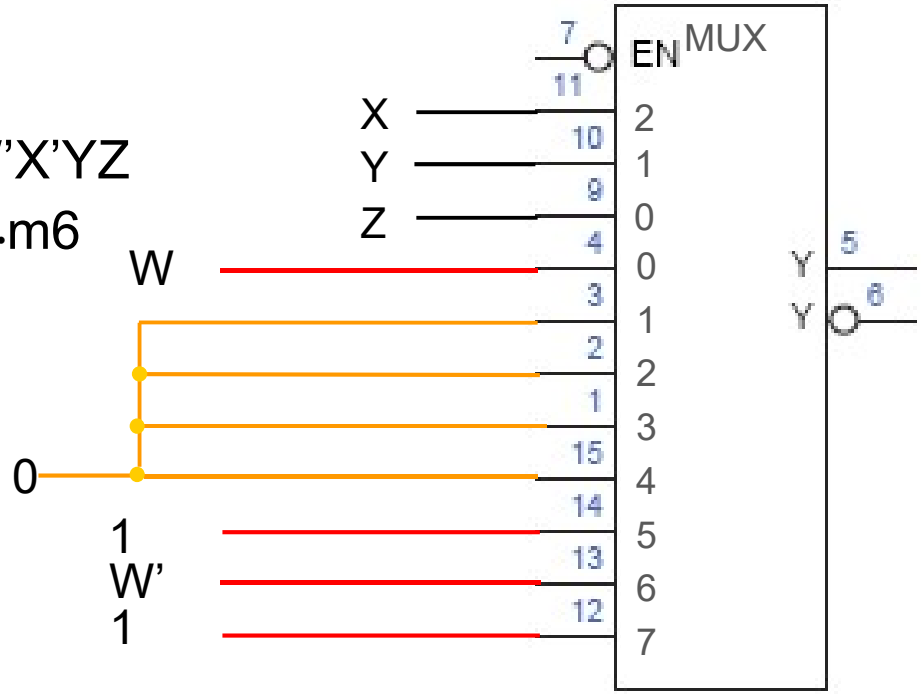
Example Implement F=WX'Y'Z'+XZ+W'X'YZ with a 1-in-8 MUX

Solution

Y=WX'Y'Z'+XZ+W'X'YZ

=WX'Y'Z'+XYZ+XY'Z+W'X'YZ

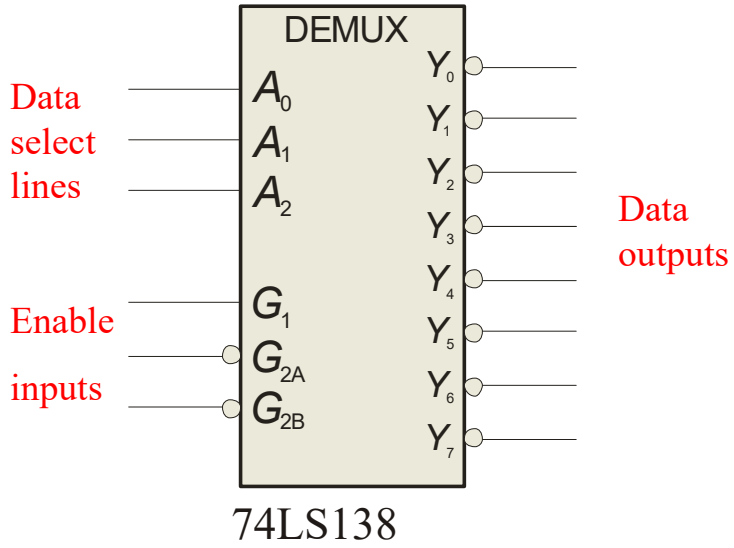
=W.m0+1.m7+1.m5+ W' .m6



Demultiplexers

A demultiplexer (DEMUX) performs the opposite function from a MUX. It switches data from one input line to two or more data lines depending on the select inputs.

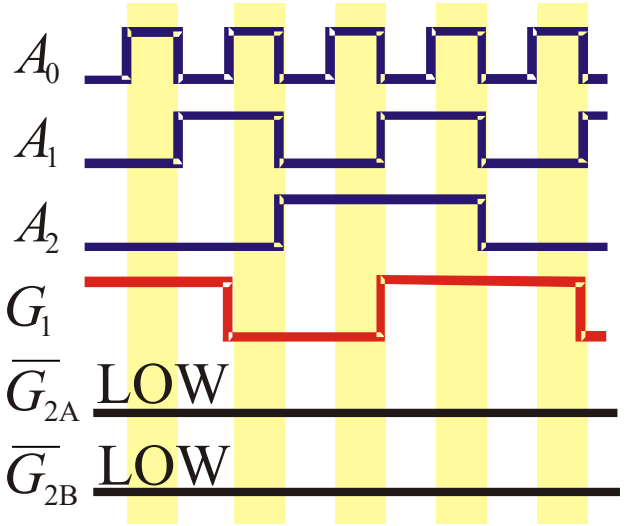
The 74LS138 was introduced previously as a decoder but can also serve as a DEMUX. When connected as a DEMUX, data is applied to one of the enable inputs, and routed to the selected output line depending on the select variables. Note that the outputs are active-LOW as illustrated in the following example…



Demultiplexers

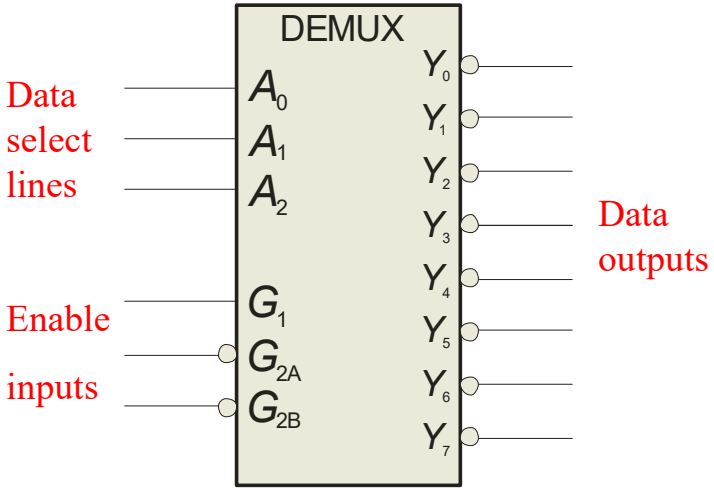
Example

Determine the outputs, given the inputs shown.



Solution

The output logic is opposite to the input because of the active-LOW convention. (Red shows the selected line).



Y_0

Y_1

Y_2

Y_3

Y_4

Y_5

Y_6

Y_7

Parity Generators/Checkers

Parity is an error detection method that uses an extra bit appended to a group of bits to force them to be either odd or even. In even parity, the total number of ones is even; in odd parity the total number of ones is odd.

Example The ASCII letter S is 1010011. Show the parity bit for the letter S with odd and even parity.

Solution

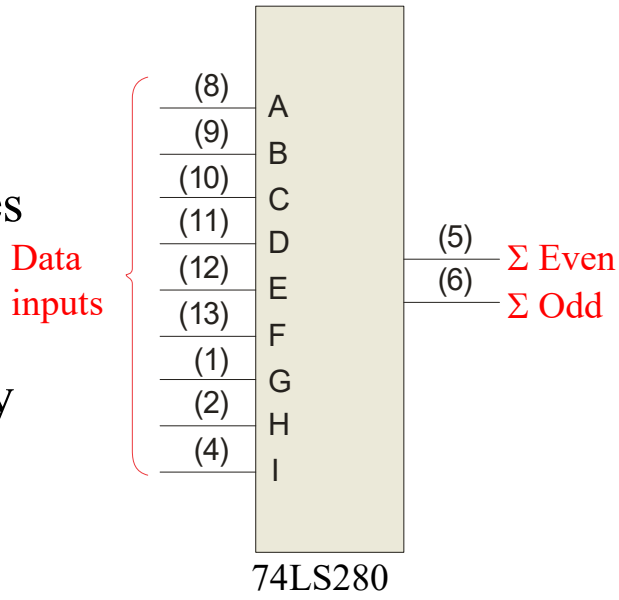
S with odd parity = 11010011

S with even parity = 01010011

Parity Generators/Checkers

The 74LS280 can be used to generate a parity bit or to check an incoming data stream for even or odd parity.

Checker: The 74LS280 can test codes with up to 9 bits. The even output will normally be HIGH if the data lines have even parity; otherwise it will be LOW. Likewise, the odd output will normally be HIGH if the data lines have odd parity; otherwise it will be LOW.



Generator: To generate <u>even</u> parity, the parity bit is taken from the <u>odd</u> parity output. To generate <u>odd</u> parity, the output is taken from the <u>even</u> parity output.

Selected Key Terms

Full-adder	A digital circuit that adds two bits and an input carry bit to produce a sum and an output carry.
Cascading	Connecting two or more similar devices in a manner that expands the capability of one device.
Ripple carry	A method of binary addition in which the output carry from each adder becomes the input carry of the next higher order adder.
Look-ahead carry	A method of binary addition whereby carries from the preceding adder stages are anticipated, thus eliminating carry propagation delays.

Selected Key Terms

Decoder	A digital circuit that converts coded information into a familiar or noncoded form.
Encoder	A digital circuit that converts information into a coded form.
Priority encoder	An encoder in which only the highest value input digit is encoded and any other active input is ignored.
Multiplexer (MUX)	A circuit that switches digital data from several input lines onto a single output line in a specified time sequence.
Demultiplexer (DEMUX)	A circuit that switches digital data from one input line onto a several output lines in a specified time sequence.

Quiz

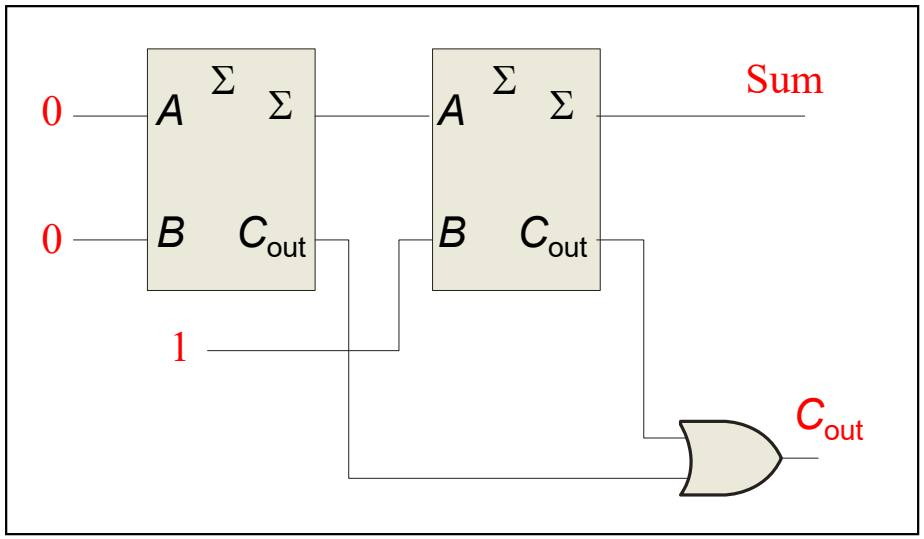
1. For the full-adder shown, assume the input bits are as shown with $A = 0$, $B = 0$, $C_{in} = 1$. The Sum and C_{out} will be

a. Sum = 0 $C_{out} = 0$

b. Sum = 0 $C_{out} = 1$

c. Sum = 1 $C_{out} = 0$

d. Sum = 1 $C_{out} = 1$



Quiz

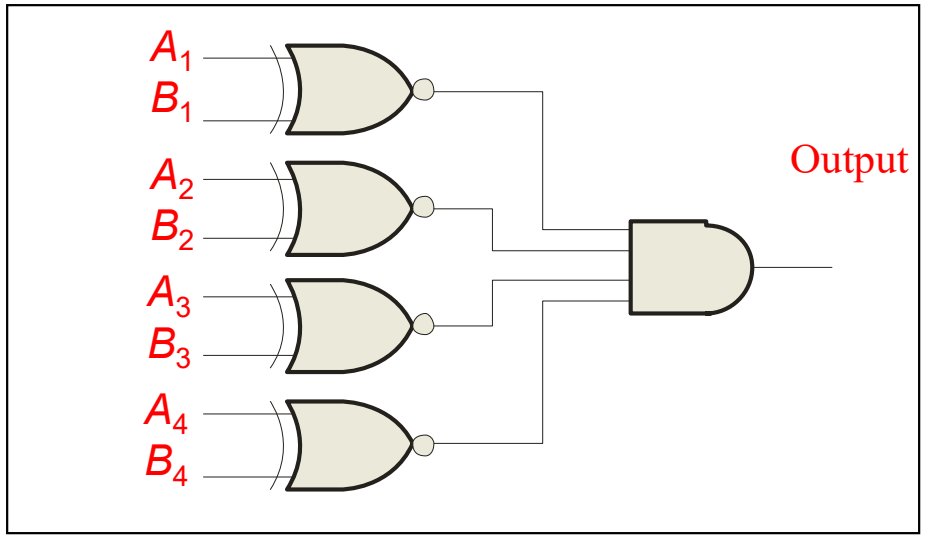
2. The output will be LOW if

a. $A < B$

b. $A > B$

c. both a and b are correct

d. $A = B$



Quiz

3. If you expand two 4-bit comparators to accept two 8-bit numbers, the output of the least significant comparator is

a. equal to the final output

b. connected to the cascading inputs of the most significant comparator

c. connected to the output of the most significant comparator

d. not used

Quiz

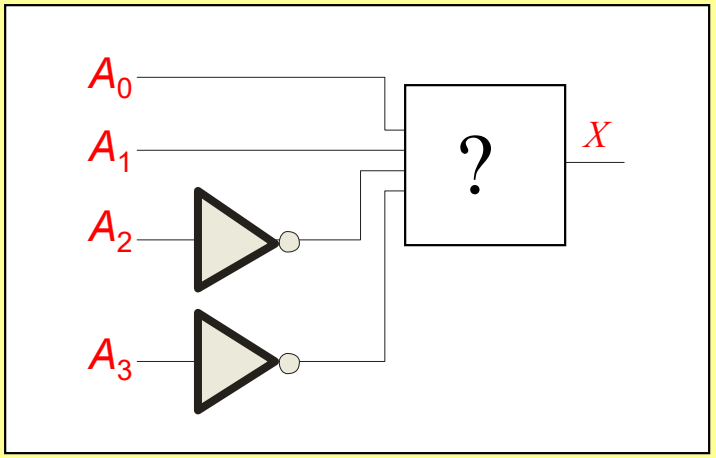
4. Assume you want to decode the binary number 0011 with an active-LOW decoder. The missing gate should be

a. an AND gate

b. an OR gate

c. a NAND gate

d. a NOR gate



Quiz

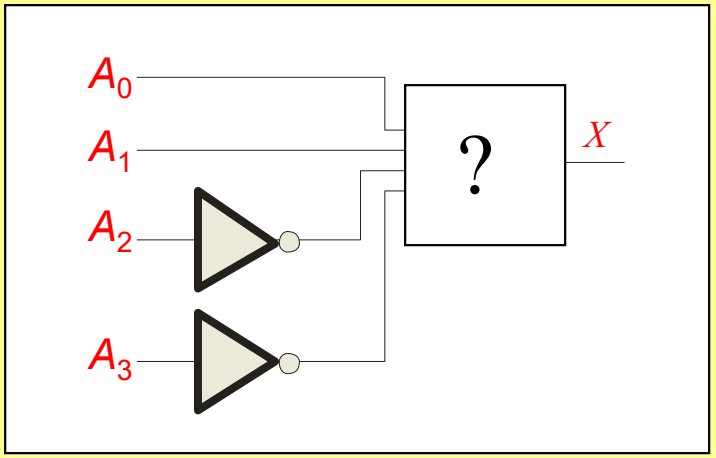
5. Assume you want to decode the binary number 0011 with an active-HIGH decoder. The missing gate should be

a. an AND gate

b. an OR gate

c. a NAND gate

d. a NOR gate



Quiz

6. The 74138 is a 3-to-8 decoder. Together, two of these ICs can be used to form one 4-to-16 decoder. To do this, connect

a. one decoder to the LSBs of the input; the other decoder to the MSBs of the input

b. all chip select lines to ground

c. all chip select lines to their active levels

d. one chip select line on each decoder to the input MSB

Quiz

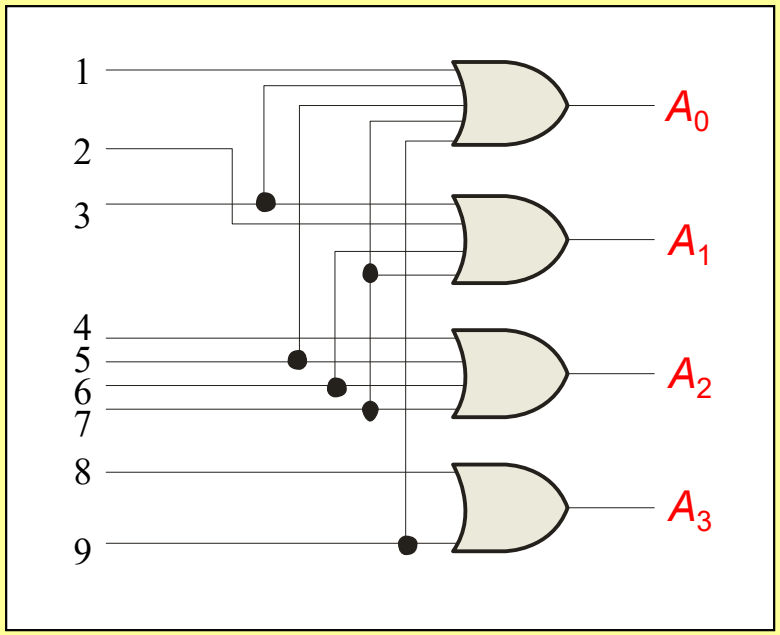
7. The decimal-to-binary encoder shown does not have a zero input. This is because

a. when zero is the input, all lines should be LOW

b. zero is not important

c. zero will produce illegal logic levels

d. another encoder is used for zero



Quiz

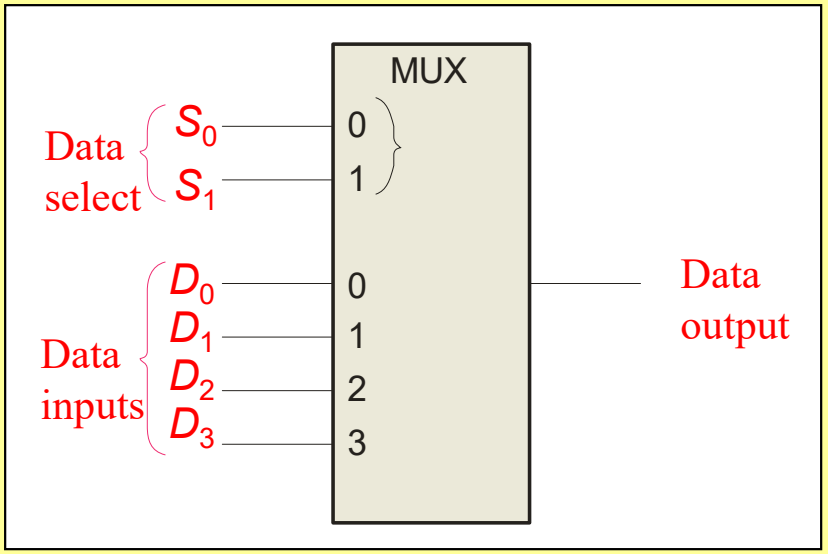
8. If the data select lines of the MUX are $S_1S_0 = 11$, the output will be

a. LOW

b. HIGH

c. equal to D_0

d. equal to D_3



Quiz

9. The 74138 decoder can also be used as

   a. an encoder

   b. a DEMUX

   c. a MUX

   d. none of the above

Quiz

10. The 74LS280 can generate even or odd parity. It can also be used as

a. an adder

b. a parity tester

c. a MUX

d. an encoder

Quiz

Answers:

1. c	6. d
2. c	7. a
3. b	8. d
4. c	9. b
5. a	10. b