AUTUMN MID-SEMESTER EXAMINATION-2022-23

School of Electronics Engineering

Kalinga Institute of Industrial Technology

Deemed to be University

3rd Semester

Subject: Digital Electronics (EC 2011) (Regular)

Time: 1.5 hours Full Marks: 20

The figures in the right-hand side indicate full marks.

All parts of a question should be answered at one place only.

Question No	Section-A	Question	CO Mapping	Marks
Q1.				[1x5]
a	SAT	Perform binary subtraction using 2's complement method: -14-(-6)	CO1	
b		Show that: PQ'+PR+QR'=P+QR'; where P, Q, and R are Boolean variable.	CO1	
c		Design Half-subtractor using 2-input NAND gates only.	CO2	
d		Design full-adder using two half-adders.	CO2	
e		Perform BCD operation : (i) 858-749 (ii) 00011001 + 00010100	CO1	
	Section-B			
Q2.	Reduce the expression f(A,B,C,D)=∑(1,5,6,12,13,14)+d(2,4) using K-Map, and implement the real minimal expression using NAND gate only.		CO1	[5]
	Or			
	Reduce the expression f(W,X,Y,Z)=∑(0,1,2,9,11,15)+d(8,10,14) using K-Map, and implement the real minimal expression using NOR gate only.		CO1	
Q3	Design a combinational circuit with 3 inputs X, Y, & Z and 3 outputs A, B, & C. When the binary inputs are corresponding to decimal equivalent of 0, 1, 2 or 3, then the binary outputs are 2 greater than the input, and when the binary inputs are corresponding to decimal equivalent of 4, 5, 6 or 7, then the binary outputs are 2 less than the input.		CO2	[5]
	Or			
	Design a combinational circuit using only 2-input XOR and OR gates which takes 4-bit binary data as input (A3A2A1A0) and generates the output data (B3B2B1B0) which is the 2's complement of the input.		CO2	
Q.4	Draw and explain a combined 4-bit Adder/Subtractor block using full adders and X-NOR gates only.		CO2	[5]
	Or			
	What is the difference between "Ripple carry adder" and "Look-ahead carry adder"? Explain with the help of circuit diagram .		CO2	