SPRING END SEMESTER EXAMINATION-2023

6th Semester B.Tech (Open Elective-I/Minor-I)

COMPUTER ORGANIZATION

CS 3042

(For 2021 (L.E), 2020 & Previous Admitted Batches)

Time: 3 Hours Full Marks: 50

Answer any SIX questions.
Question paper consists of four SECTIONS i.e. A, B, C and D.
Section A is compulsory.
Attempt minimum one question each from Sections B, C, D.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

SECTION-A

1. Answer the following questions. [1 × 10]

(a) What is Von Neumann architecture? How is it different from Harvard Architecture?

(b) A processor is connected to a 4G×32 bits memory module. A program is kept in 256th address of the memory and the length of each instruction is of 32 bits. Then find out the size of MAR, MDR, IR and PC.

(c) How many memory references are required for the execution of the following code, where LOCX LOCY denote memory locations? The rightmost operand is used as destination.

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MOV (LOCX), R1
ADD R1, (LOCY)
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(d) A computer has 58 instructions; each instruction requires at most 15 steps to complete its execution. What will be the specification of instruction decoder and step counter decoder used in hardware control unit design?

(e) Differentiate between Memory mapped I/O and I/O Mapped I/O.

(f) Explain differentiate types of locality of references.

(g) Differentiate between write through and write back cache.

(h) A computer has 64-bit instructions and 12 bit addresses. If there are 352 three address instructions, and 2256 no of two-address instructions then how many one-address instructions can be formulated?

(i) Represent 9.25 in IEEE single precision format.

(j) Write down merit and demerit of hardwired control unit.

SECTION-B

2. (a) A 20GHz processor executes a program having 200 instructions. The clock cycles required for executing different types of instructions is given below. Find out the time required by the processor to execute the program. [4]

Instruction type	**%age occurrence**	**Clock cycles**
ALU instructions	55%	1.0
Load-stores	40%	2.0
Jumps	5%	3.0

(b) Draw and explain the 3-bus CPU organization. Write the sequence of control signals to execute the following instruction using the same organization. [4]

ADD (R5),R1,R2

3. (a) What is virtual memory? How the virtual address is translated into physical address? Explain with suitable example. [4]

(b) Multiply 12 × -3 using Booth's algorithm. [4]

SECTION-C

4. (a) Design a 2M x 32 memory chip using 512k x 8 memory chips. [4]

   (b) What is DMA? Discuss DMA controller with neat diagram. [4]

5. (a) A block-set associative cache memory consists of 128 blocks divided into four block per set. The main memory consists of 16,384 blocks and each block contains 256 eight-bit words. [4]

      1. How many bits are required for addressing the main memory?
      2. How many bits are needed to represent the TAG, SET and WORD fields?

   (b) Explain the working principle of micro-programmed control unit with suitable diagram. [4]

6. (a) Design the internal organization of an 8M×8 bits RAM memory chip. Find out the total number of external pins required. [4]

   (b) Divide 8/3 using restoring division. [4]

SECTION-D

7. (a) What is static RAM? Explain cell organization with neat diagram. [4]

   (b) The instruction set of a processor consists of two instructions of 32bits each i.e; ADD R1, R2, (R3) and JUMP 3000. The processor has single bus CPU organization and hardwired control unit. Find out the logic expression and diagram for Z_{in} and End control signals. [4]

8. (a) Write the machine level instructions to compute the following expression using 3 and 0 address instruction format. [4]

$$X=(A-B+C\ (D*E-F))\ /\ (G+H*K)$$

(b) A cache consists of 128 blocks of 16 words each. Main memory is addressable by a 16-bit address. Main memory has 64k words. Obtain Tag bits in all 3 types of mapping techniques. [4]

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