

Instruction Set



An extensive set of instructions are provided to carry out various computational tasks.

According to the operation carried out by the computer, the instructions are classified into 3 categories.

1. Data Transfer Instruction

2. Data Manipulation

(a) Arithmetic Instruction

(b) Logical Instruction

(c) Shift Instruction

3. Program control Instruction.

Data Transfer Instructions: When data is moved from the source to the destination, source copy remains intact.

Name Mnemonics

Load LD

Store ST

Move MOV

Exchange XCH

Input IN

Output OUT

Push PUSH

Pop POP

DE \leftarrow HL (S05C, S05B)

IN: This instruction is used to take input from input device. (S05, S05)

IN # Portno, reg.

IN # 08H, R1

This instruction takes an input into processor register R1, from the device whose identification no is 08H. H indicates hexadecimal no.

OUT : This instruction is used to send offset from the processor register to an output device.

OUT reg, # Portno

OUT R1, # 09H

This instruction sends an offset from processor register R1, to an output device whose identification no is 09H.

Data Manipulation Instructions

Arithmetic

Name Mnemonics

Increment INC

Decrement DEC

Add ADD

Subtract SUB

Multiply MUL

Divide DIV

Add with carry ADC

Subtract with borrow SUBB

Logical & Bit Manipulation Instructions

Name . Mnemonics

1. AND

It is used to reset some specific bit position in a register keeping all other bits intact (unchanged)

Ex - AND #FF7H, R1

2. OR

It is used to set some specific bit position in a register, keeping all other bits intact (unchanged)

Example : OR #04, R1

3. XOR

(Exclusive OR)

It is used to clear the contents of a register

XOR R1, R1

4. Set Carry — SET C

It is used to set the Carry Flag

$CF \leftarrow 1$

5. Clear Carry — CLRC

It is used to Reset the carry flag

$CF \leftarrow 0$

6. Complement carry

It is used to complement the carry flag.

$CF \leftarrow \overline{CF}$

COMC

7. Enable Intercept

EI

It is used to set the Interrupt Flag.

$IF = 1$, interrupt activated.

$IF = 0$, interrupt deactivated.

INTR is an Intercept request signal to the processor.

When $IF = 1$, then only processor recognizes an intercept request and responds to it, else ignores the request coming on line INTR.

(Explain INTR, PIN and ISR)

8. DI → Disable Intercept

It is used to reset the intercept flag.

$IF \leftarrow 0$

When $IF = 0$, then the processor ignores the Interrupt request. DI instruction is used to mask (disable) the INTR signal.

9. Clear

CLR

10. complement

COM

Shift Instructions

• Shift n Rotate Instructions:

Name Mnemonic

Logical shift right SHR

Logical shift Left

SHL

Arithmetic

SHRA

shift right

Arithmetic shift Left

SHLA

Left

Rotate right

ROR

Rotate Left

ROL

Rotate Right

through carry

RORC

Rotate Left

through carry

ROLC

• SHL : Logical left shift for
signed numbers.

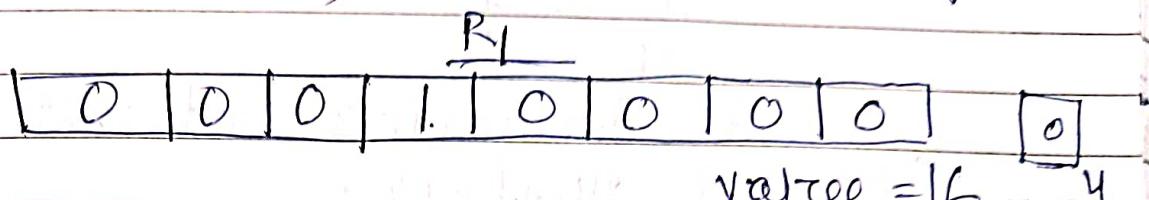
Provide a mean for shifting
block of bits within a register
or memory.



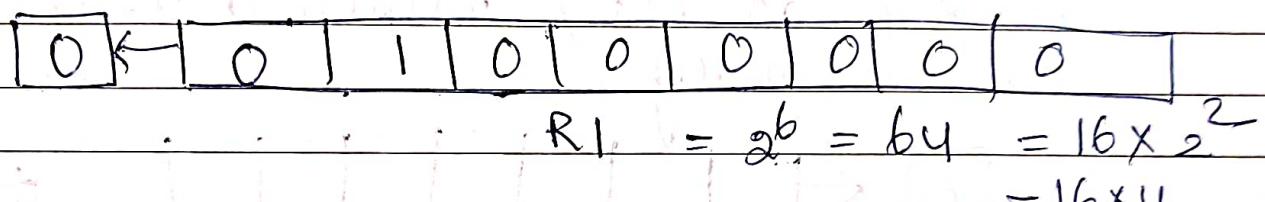
The contents of the operand are
shifted left by the number of

bits specified in the source operand of the instruction. The vacated bits are filled with zeros. The shifted bits are passed through the C flag, and then dropped. Left shifting an operand is equivalent to multiplying the operand by $2^{(\text{bit position shifted})}$.

a

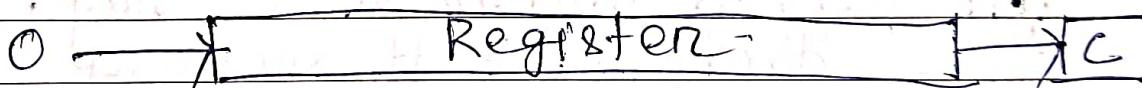


SHL #2, R1



- SHR : Logical right shift for unsigned numbers.

Provide a means for shifting blocks of bytes within a register or memory.



The contents of the operand are shifted right by the number of bits specified in the source operand of the instruction.

The vacated bits are filled with zeros.

The shifted bits are passed through the C flag, and then dropped.

Right shifting an operand is equivalent to dividing the operand by $2^{(\text{bit position shifted})}$.

$$R_1 = 16$$

R₁ | 0 | 0 | 0 | 1 | . | 0 | 0 | 0 | 0

SHR #2, R₁

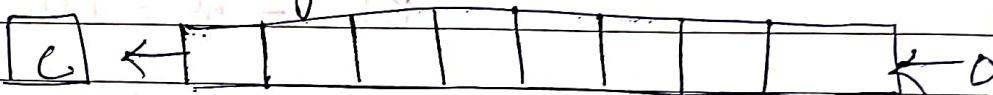
R₁ | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0

now R₁ = 4

$$\frac{16}{4} = 4$$

• SHLA: Arithmetic Left shift for signed numbers.

Provide a means for shifting block of bits within a register or memory.



The contents of the operand are shifted left by the number of bits specified in the source operand of the instruction. The vacated bits are filled with zeros. The shifted bits are passed through the C flag, and then dropped. Left shifting on Operand is equivalent to multiplying the Operand by $2^{(\text{bit positions shifted})}$.

R₁ | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0

SHLA #2, R₁

| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | R₁

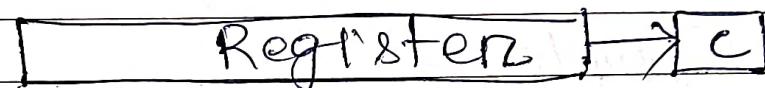
SHLA affect the overflow flag

The overflow flag will be 1, if the sign changes after the shift operation else will be zero.

Arithmetic Right Shift operation.

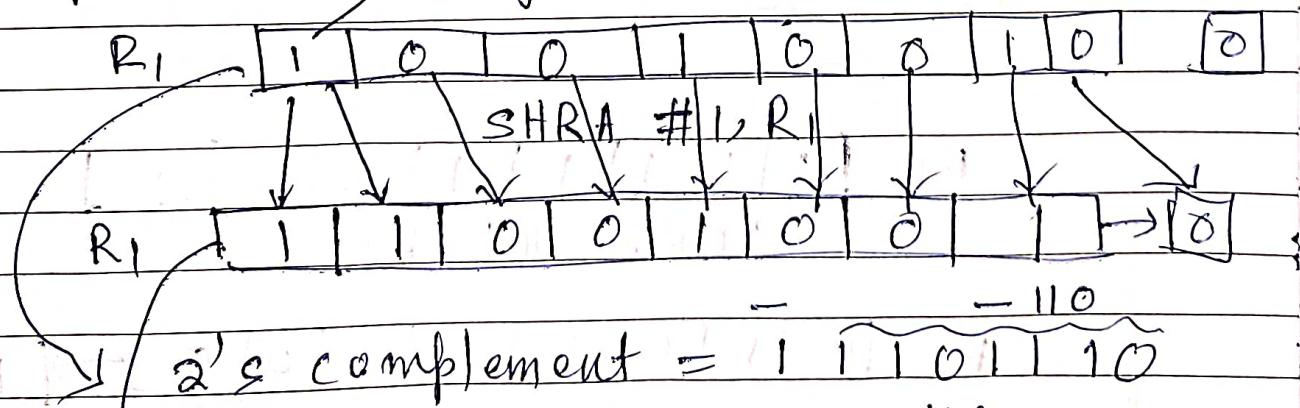
SHRA: Arithmetic right shift for signed numbers.

Provide a means for shifting a block of bits within a register or memory.



The contents of the operand are shifted right by the number of bits specified in the source operand of the instruction. The vacated bits are filled by the previous sign bit. The shifted bits are passed through the C-flag and then dropped.

Right shifting an operand is equivalent to dividing the operand by $2^{\text{bit position shifted}}$.



$$2\text{'s complement} = \overbrace{1110110}^{= -110}$$

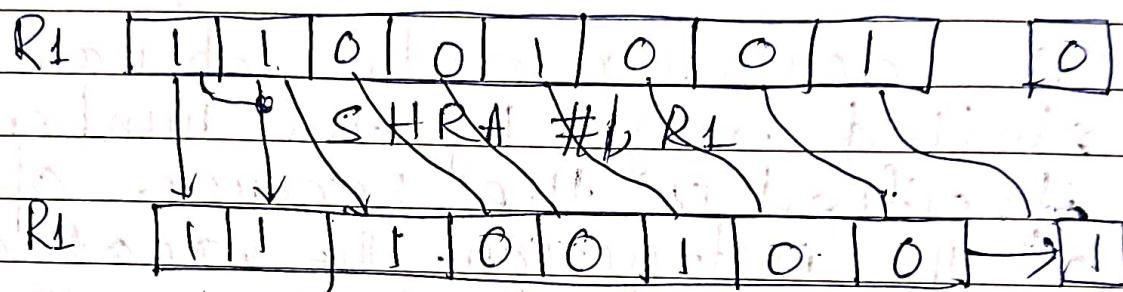
$$2\text{'s complement} = \overbrace{1011011}^{= -55}$$

$-110 \rightarrow -55$
~~-55~~ $\xrightarrow{2^1} -55$
 $1 \rightarrow$ 1 bit position shifted.

Numerically

Arithmetic Right shift instruction

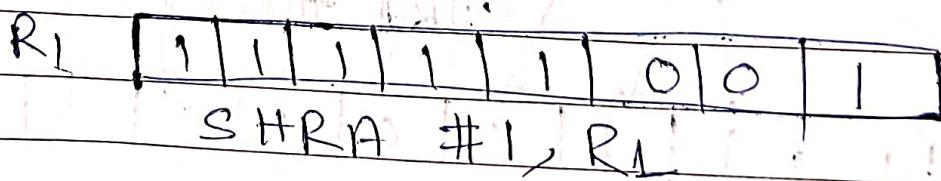
Example - 1



Here, R1 containing -55 before the shift operation, and after the SHRA, it contains -28 .

$$-55 \xrightarrow{2^1} = -27.5 = -28$$

Example - 2



Here R1 containing -7 before the shift operation, and after the

SHRA, it containing -4

$$\frac{-7}{2^1} = -3.5 \therefore -4$$

Example-3.

Before execution . . .

R1	0	0	0	0	1	1	1	1	0
SHRA #1, R1									

After

R1	0	0	0	0	0	1	1	1	1
----	---	---	---	---	---	---	---	---	---

Here, R1 contains +15 before the shift operation, and after the SHRA, it containing $+7 \cdot 5 = 7$.

$$\frac{15}{2} = 7.5 = 7$$

Example-4

The content of Registers R1 is 11010101. What will be the decimal value after execution of AshiftR #2, R1. [Assume the number is represented in 2's complement format]

Ans

R1	1	1	0	1	0	1	0	0
----	---	---	---	---	---	---	---	---

R1	1	1	1	0	1	0	1	0
----	---	---	---	---	---	---	---	---

R1	1	1	1	1	0	1	0	1	0
----	---	---	---	---	---	---	---	---	---

Hence, R₁ containing -43 before the shift operation, and after the ASHTR 2 times it contains -11.

$$\frac{-43}{2^2} = -(10 \cdot 7) = -11$$

Example-5

The content of Registers R₁ is 10001010. What will be the decimal value in R₁ after the execution of ASHR #1, R₁.

(Assume the numbers are written in 8's complement form)

Ans

R₁ | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0

ASHR #1, R₁

| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | → | 0

Hence R₁ containing -118 before the shift operation, and after the ASHTR 1 time it contains

$$\frac{-118}{2^1} = -59$$

Example-6

Execute the following instruction where R₀ is the 8 bit and its content is 11001011

- (i) ASHTR #1, R₀

$R_0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0$

A shift R #1, R₀

$R_0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | \rightarrow 1$

Here, R₀ contains -53 before the shift operation, and after the A shift R 1 time, it contains

$$\frac{-53}{2^1} = -26.5 = -27$$

Numerical 5

The content of register R₁ is 1011001100110011. Write the instructions for performing the following operations.

- (i) Clear the LSB of R₁ to 0.
- (ii) Set the MSB of R₁ to 1.

Note : LSB = Least significant byte.

MSB = Most significant byte.

Ans (i) AND #FF00H, R₁

(ii) OR #FF00H, R₁

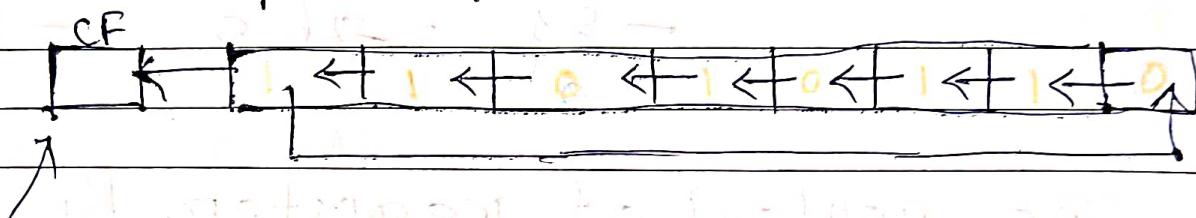
Rotate Instructions.



Rotate Left Instruction

(Rotatel) ROL

The bits of the destination are rotated left. The number of bits rotated is determined by the source operand. The bits rotated out of the most significant bit of the operand go to both the carry bit and the least significant bit of the operand.



Qs. The content of registers R1 is 11010110. What will be the decimal value after execution of Rotatel #2, R1. [Assume the number is represented in 2's complement format]

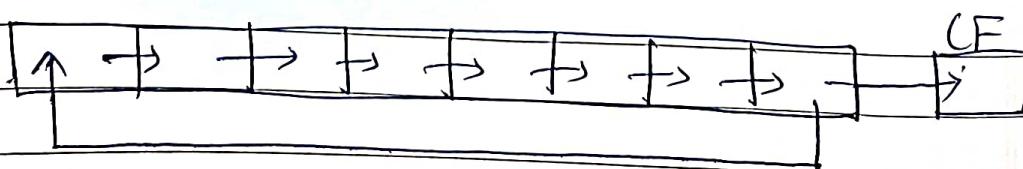
Ans- So after the Rotatel #2, R1, the content of R1 will become,

$$R1 = 10101101 \text{ (After the 1st rotation)}$$

$$R1 = 01011011 \text{ (After the 2nd rotation)}$$

Hence, MSB is 0. Hence R1 left is +ve so the $[R1]$ in decimal = $(01011011)_2 = 91$

Rotate Right Instruction (Rotater)

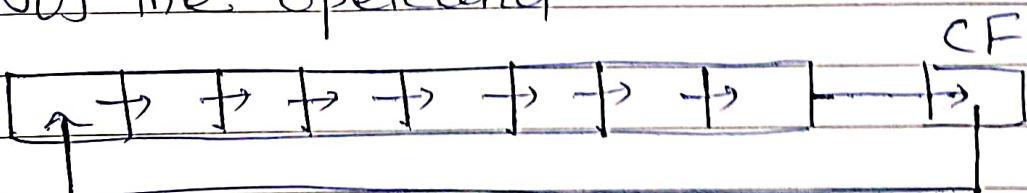


The bits of the destination are rotated right. The number of bits rotated is determined by the source operand. The bits rotated out of the least significant bit of the operand go to both carry bit and the most significant bit of the operand.

Rotate

~~Rotate Right through carry~~
Instruction (ROT4TERC) RORC

The bits of the destination are rotated right. The number of bits rotated is determined by the source operand. The bits rotated out of the least significant bit of the operand go to the carry bit and the previous carry bit goes to the most significant bit of the operand.



Rotate Left through Carry Instruction (ROTATELC) ROLC

The bits of the destination are rotated left. The number of bits rotated is determined by the source operand. The bits rotated out of the most significant bit of the operand go to both the carry bit and the previous carry bit. goes to the least significant bit of the operand.

