

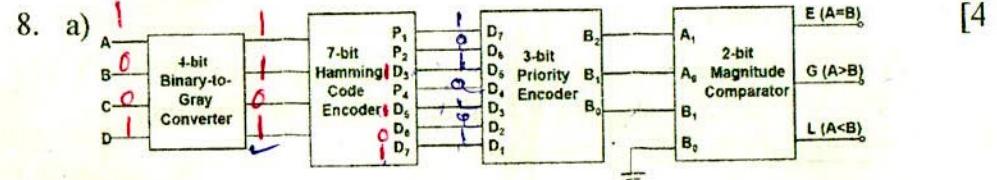
b) With the help of a neat diagram, explain the working of a 4-bit Successive Approximation type ADC with Analog input of 12.6V. Find the digital output. What would be its conversion time if clock frequency is 1 MHz? If the analog input voltage is now increased to 14.8 V, what would be the new conversion time? Explain.

c) A certain memory has a capacity of 64K x 16. [2]

(i) How many data input and data output lines does it have?

(ii) How many address lines does it have?

P 0001.

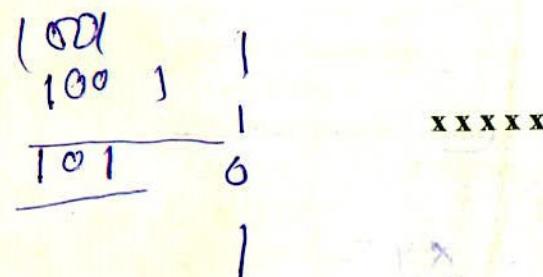


In the figure given above, ABCD=1001 is a 4-bit Binary input data. Find all three outputs of the 2-bit magnitude comparator, assuming Odd parity system for Hamming Code Encoder and input line having highest decimal subscript is having the highest priority in the Priority Encoder.

b) Implement the following logic function using an 8:1 MUX. [4]

$$F(A, B, C, D) = A\bar{B} + C\bar{D} + A\bar{C}$$

c) Compare N-bit Ring counter, Johnson counter & Ripple counter from modulus and decoding circuit point of view. [2]



SPRING END SEMESTER EXAMINATION-2013

4th Semester B.Tech / B.Tech Dual (M.Tech/MBA)

DIGITAL ELECTRONIC CIRCUITS EC-402

[Regular-2011 Admitted Batch & Back]

Full Marks: 60

Time: 3 Hours

Answer any SIX questions including Question No.1 which is compulsory.

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

1. (a) "Excess-3 codes are non-weighted, sequential & self-complementing." Justify. [1 x 10]

(000101111000.
1001)2

(b) Perform the BCD subtraction (476.7 - 297.8).

(c) With the help of a 4:1 MUX, implement a NOT gate.

$$Y = D_0 = 1, Y = D_1 = 0$$

(d) Show that $AB + \bar{A}C = (A+C)(\bar{A}+B)$ where A, B and C are Boolean variables. $AB + \bar{A}C$

(e) In a T Flip-Flop, the output is initially in SET state. If the input clock frequency is 6.25 MHz, find the frequency of the output waveform when (i) T = 0, (ii) T = 1. 3.125 MHz

(f) Assume that a 4-bit Ripple counter is holding the count 0110. What will be the count after 31 clock pulses? $9,1,1,15,1,5 = 31$

(g) Determine the decimal value of the signed binary number '101010' in (i) Sign-Magnitude form (ii) 1's Complement form and (iii) 2's Complement form.

- 22

(1)

(2)

- (h) Arrange the following logic families in increasing order of Propagation Delay and Power Dissipation per gate: - TTL, CMOS, ECL. $ECL < TTL < CMOS, CMOS < TTL < ECL$

- (i) How many OR gates are there in a 32×8 ROM and how many inputs does each OR gate of a 32×8 ROM have? $OR = 08, 8 \times P = 32$
- (j) The logic levels used in a 4-bit R-2R ladder DAC are: $1 \equiv 5\text{ V}$ and $0 \equiv 0\text{ V}$. Find the output voltage for digital input of 1011.

$$3.4375\text{V}$$

2. a) Design a J-K Flip-Flop using a D Flip-Flop, a 2:1 MUX and a NOT gate. $D = J\bar{Q}_n + K\bar{Q}_n$ [4]

- b) Obtain the minimized expression for the following 4-variable Boolean expression using K-map method and implement the minimized expression using NOR gates only.

$$F(A,B,C,D) = \sum m(11,12,14) + \sum d(3,4,6)$$

- c) Differentiate between PAL & PROM. $(B+D)(\bar{B}+\bar{D})(B+C)$ [2]

3. a) Design a 3-bit Even Parity Generator circuit using a Decoder with Active-Low outputs. $P = \sum m(1, 2, 4, 7)$ [4]

- b) Draw the logic diagram of a 4-bit P-I-S-O Shift Register using J-K Flip-Flops and explain its operation. [4]

- c) Explain 'High-state Fan-out' and 'High-state Noise Margin' of a logic gate. [2]

4. a) Design a synchronous sequential circuit which produces an output $Z = 1$, whenever the following input sequence '11010' occurs. (Assume overlapping is allowed and use Mealy Model) [6]

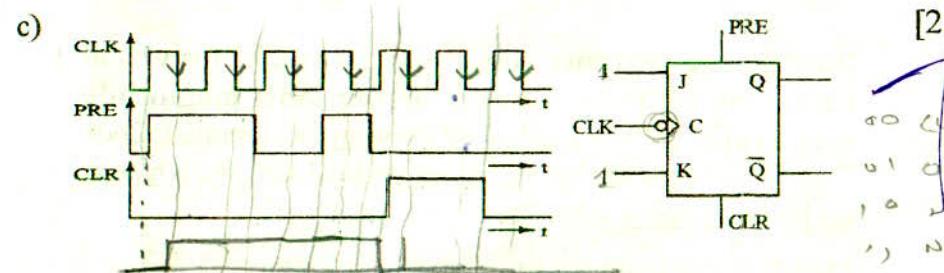
- b) With the help of a neat diagram, explain the working of a TTL NAND gate with Open-Collector output and also mention the disadvantages of this configuration. [4]

(2)

5. a) Design an Asynchronous Mod-5 Up-counter using D Flip-Flops. [4]
- b) Design a 4:2 Priority Encoder such that the order of priority of the decimal inputs is given as $D_2 > D_0 > D_1 > D_3$, where all D_i 's are inputs to the priority encoder. [4]
- c) Draw the circuit diagram of a 2-input CMOS NAND gate. [2]

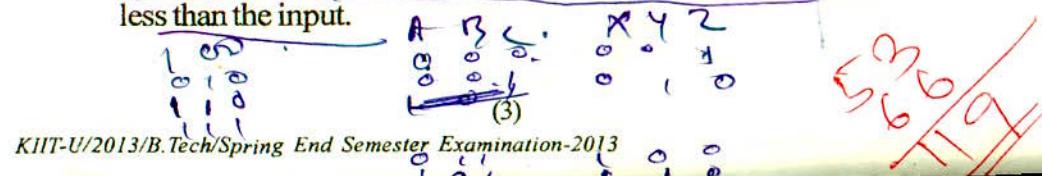
6. a) 'In Astable multivibrator, external trigger input is not required'. Justify. Design an Astable Multivibrator using 555 Timer IC to generate a square wave of 2 KHz frequency with 50% duty cycle. Given, $R_A = 3\text{ K}\Omega$. [4]

- b) Design a Synchronous counter that goes through states 0, 5, 3, 2, 6, 0, 5, 3... using S-R Flip-Flops. The counter should count only in 3-bit Gray codes. [4]



Sketch the Q waveform for the Flip-Flop shown in the above figure. Assume that $Q = 0$ initially and the Flip-Flop has *Active-High Asynchronous inputs*.

7. a) Design a Combinational circuit using 2-input basic gates only which has three inputs A, B & C and three outputs X, Y & Z. When the decimal equivalent of the binary input is 0, 1, 5 or 3, the decimal equivalent of the binary output is one greater than the input and when decimal equivalent of the binary input is 4, 2, 6 or 7, the decimal equivalent of the binary output is one less than the input. [4]



10/5/13

DEC (EC-402) SOLUTIONS2018
Solution

(a) Excess-3 codes are non-weighted because [1] ①
 in these codes, each digit position is not assigned any weight i.e. fixed value.

These codes are sequential because each succeeding code word is one binary number greater than its preceding code word.

These codes are self-complementing because the excess-3 code of the 9's complement of a no. N i.e. of $9-N$ can be obtained from the excess-3 code of N by interchanging all the 0's and 1's.

(b)

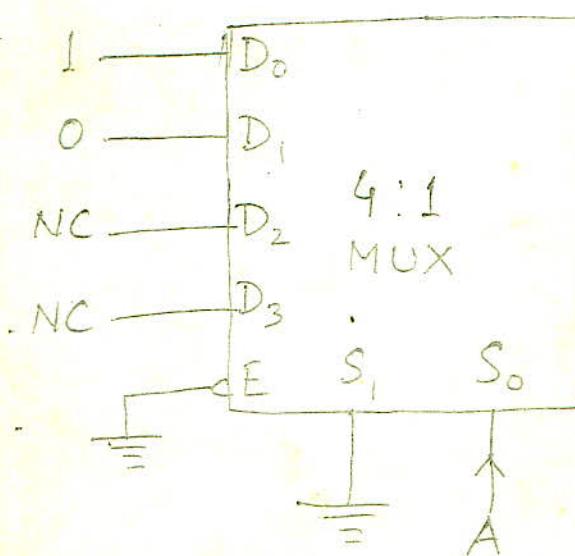
$$\begin{array}{r} \text{BCD code of } 476.7 \Rightarrow 0100 \ 0111 \ 0110 \cdot 0111 \\ \text{BCD code of } 297.8 \Rightarrow \underline{0010 \ 1001 \ 0111 \cdot 1000} \\ \hline 0001 \ 1101 \ 1110 \cdot 1111 \end{array}$$

(Apply BCD correction)

$$\begin{array}{r} \text{BCD code of } 178.9 \Rightarrow \underline{0001 \ 0111 \ 1000 \cdot 1001} \\ \hline 0110 \ 0110 \cdot 0110 \end{array}$$

$$\text{Ans} = (0001 \ 0111 \ 1000 \cdot 1001)_2$$

(c)



$$Y = \bar{A}$$

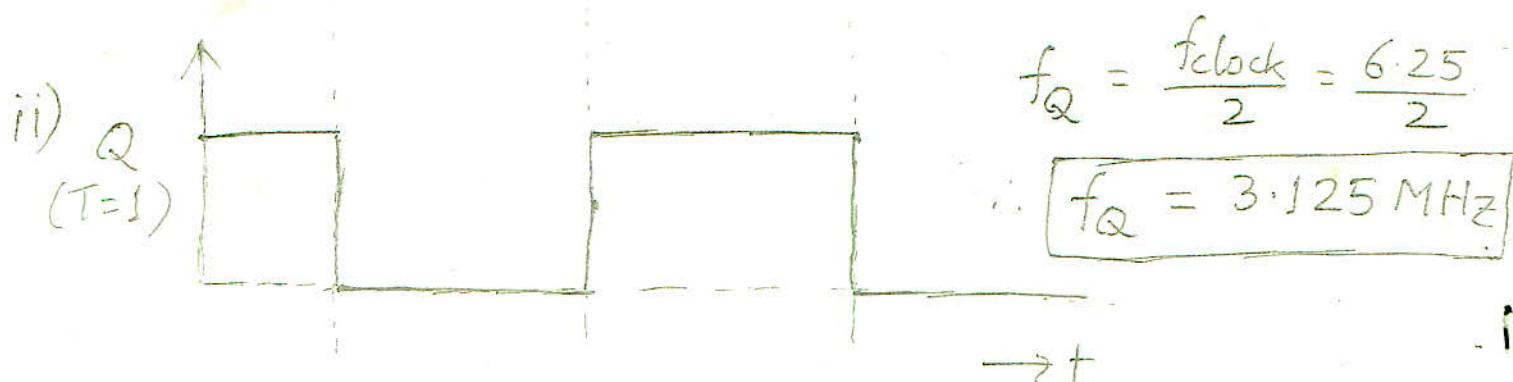
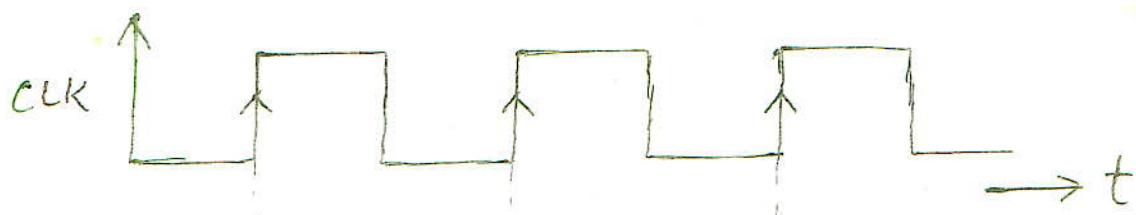
$$\begin{array}{ll} S_1 & S_0 = A \quad \text{Function} \\ \hline 0 & 0 \quad Y = D_0 = 1 \\ 0 & 1 \quad Y = D_1 = 0 \end{array} \quad \left. \begin{array}{l} Y = \bar{A} \\ (100) \end{array} \right\}$$

NC → No Connection

$$\begin{aligned}
 (d) \text{ R.H.S.} &= (A+C)(\bar{A}+B) \quad \textcircled{2} \\
 &= A\bar{A} + C\bar{A} + AB + CB \\
 &= 0 + \bar{A}C + AB + BC \cdot 1 \quad (\because A\bar{A} = 0) \\
 &= \bar{A}C + AB + BC(A+\bar{A}) \quad (\because A+\bar{A} = 1) \\
 &= AB + ABC + \bar{A}C + \bar{A}BC \\
 &= AB(1+C) + \bar{A}C(1+B) \\
 &= AB + \bar{A}C \quad (\because 1+C = 1, 1+B = 1) \\
 &= \text{L.H.S.}
 \end{aligned}$$

(e) In a T FF, $T=0 \Rightarrow Q_{n+1} = Q_n$ (NC) [1]
 $T=1 \Rightarrow Q_{n+1} = \bar{Q}_n$ (Toggle)

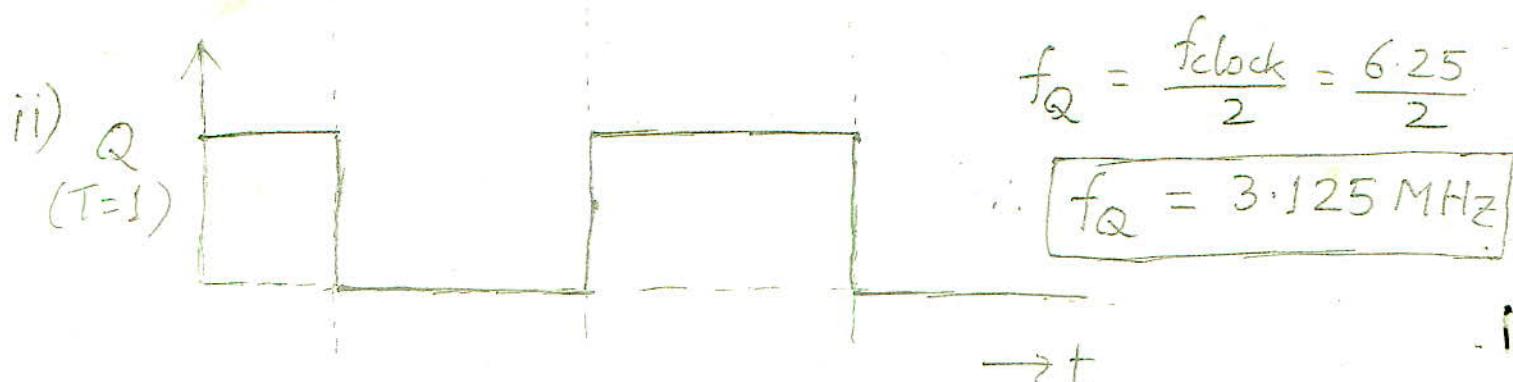
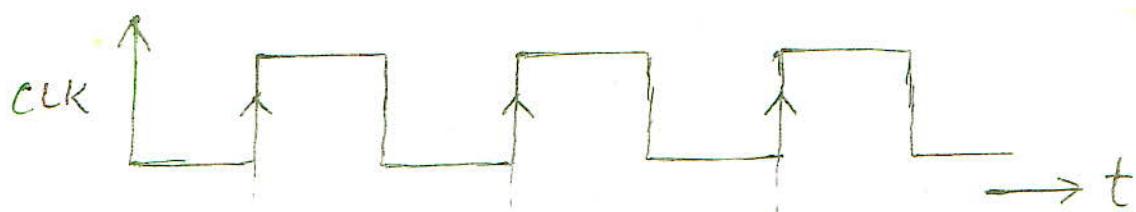
Given, $f_{\text{clock}} = 6.25 \text{ MHz}$



$$\begin{aligned}
 (d) \text{ R.H.S.} &= (A+C)(\bar{A}+B) \quad \textcircled{2} \\
 &= A\bar{A} + C\bar{A} + AB + CB \\
 &= 0 + \bar{A}C + AB + BC \cdot 1 \quad (\because A\bar{A} = 0) \\
 &= \bar{A}C + AB + BC(A+\bar{A}) \quad (\because A+\bar{A} = 1) \\
 &= AB + ABC + \bar{A}C + \bar{A}BC \\
 &= AB(1+C) + \bar{A}C(1+B) \\
 &= AB + \bar{A}C \quad (\because 1+C = 1, 1+B = 1) \\
 &= \text{L.H.S.}
 \end{aligned}$$

(e) In a T FF, $T=0 \Rightarrow Q_{n+1} = Q_n$ (NC) [1]
 $T=1 \Rightarrow Q_{n+1} = \bar{Q}_n$ (Toggle)

Given, $f_{\text{clock}} = 6.25 \text{ MHz}$



(f) A 4-bit Ripple Counter can count from 0000 [3] to 1111. [3]

| <u>Count sequence</u> | <u>No. of clock pulses</u> |
|-----------------------|----------------------------|
| 0110 to 1111 | 9 |
| 1111 to 0000 | 1 |
| 0000 to 1111 | 15 |
| 1111 to 0000 | 1 |
| 0000 to 0101 | 5 |
| | 31 |

$$\text{Count after 31 clock pulses} = (0101)_2 = (5)_{10}$$

(g) Given, Signed binary no. = 101010

| <u>Form</u> | <u>Decimal value</u> |
|---------------------|----------------------|
| i) Sign-Magnitude | -10 |
| ii) 1's complement | -21 |
| iii) 2's complement | -22 |

(h) Propagation Delay \Rightarrow ECL < TTL < CMOS

Power Dissipation per gate \Rightarrow CMOS < TTL < ECL

(i) For a 32×8 ROM,

No. of OR gates = 8

No. of inputs of each OR gate = 32

(j) Analog o/p voltage for digital i/p of 1000 = $E/2$

$$0010 = E_8$$

$$0001 = E/16$$

$$\therefore I = 5V, \therefore E = 5V$$

(4)

(4)

Analog o/p voltage for digital i/p of 1011

= Analog o/p voltage due to (1000) + (0010)

+ (0001) [By principle of superposition]

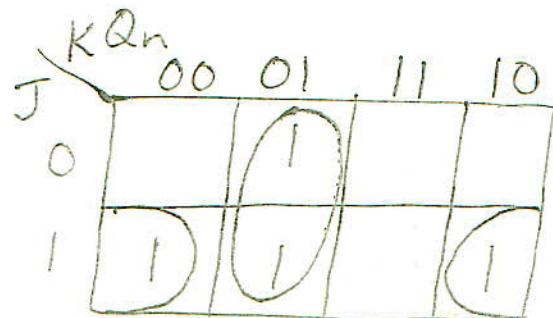
$$= \frac{E}{2} + \frac{E}{8} + \frac{E}{16}$$

$$= \frac{11}{16} E = \frac{11}{16} \times 5V = 3.4375V \text{ (Ans)}$$

2. a) FF conversion table [1]

| Ext. i/p's | | PS | | NS | FF i/p | |
|------------|---|----|---|-------|-----------|---|
| | | J | K | Q_n | Q_{n+1} | D |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 |

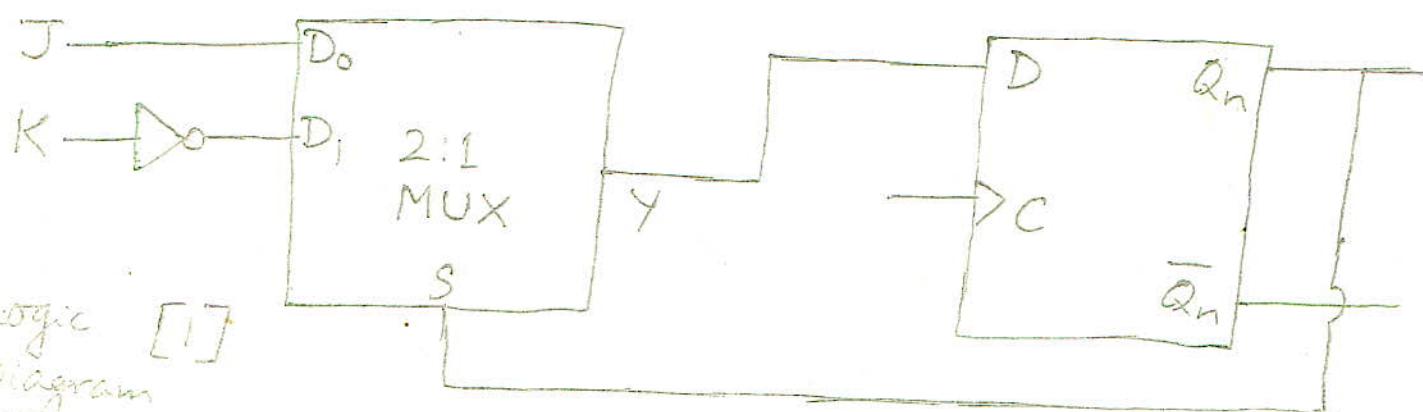
$$D = \sum m(1, 4, 5, 6)$$



K-Map [1]

From K-Map,

$$D = J\bar{Q}_n + \bar{K}Q_n \quad [1]$$



Logic Diagram [1]

5)

5)

5

b) $F(A, B, C, D) = \sum m(11, 12, 14) + \sum d(3, 4, 6)$

 $= \overline{M}(0, 1, 2, 5, 7, 8, 9, 10, 13, 15).$
 $\overline{\text{M}}(3, 4, 6) \quad [1/2]$

(b)

| | | CD | 00 | 01 | 11 | 10 |
|--|--|----|----|----|----|----|
| | | AB | 00 | 0 | X | 0 |
| | | 01 | X | 0 | 0 | X |
| | | 11 | | 0 | 0 | |
| | | 10 | 0 | 0 | | 0 |

 $F(A, B, C, D)$

$\Rightarrow = (B+D)(\bar{B}+\bar{D})(B+C)$

[1]

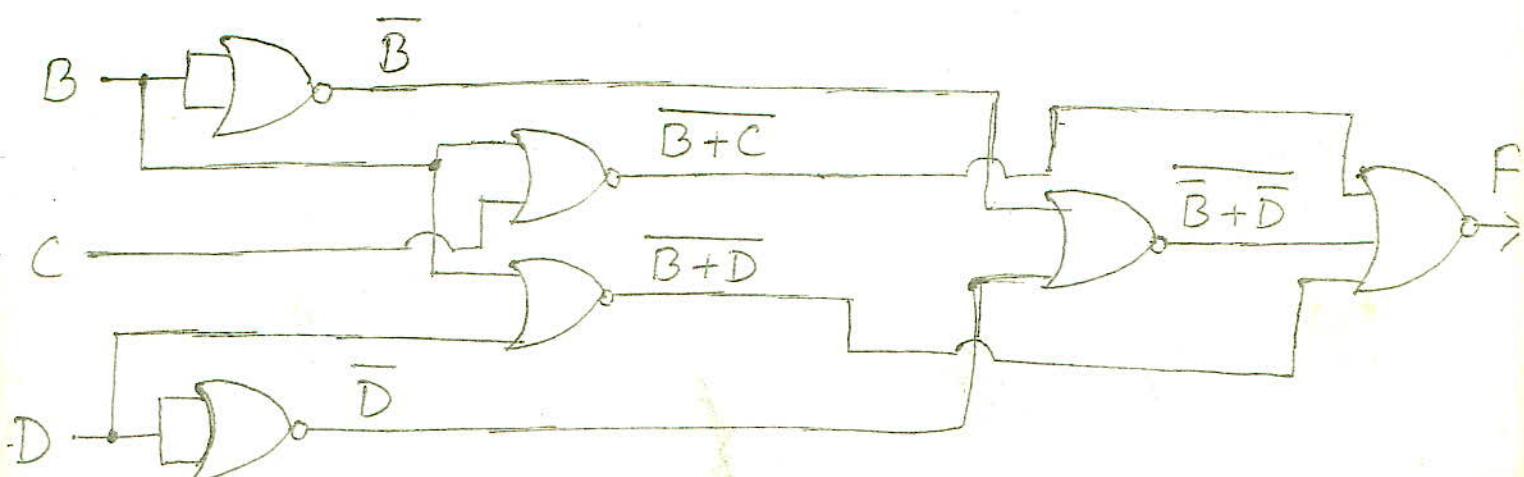
K-Map [1]

$F(A, B, C, D) = \overline{(B+C)(B+D)(\bar{B}+\bar{D})}$

$= \overline{B+C} + \overline{B+D} + \overline{\bar{B}+\bar{D}}$

$\therefore F(A, B, C, D) = \overline{\overline{F(A, B, C, D)}}$

$= \overline{\overline{B+C} + \overline{B+D} + \overline{\bar{B}+\bar{D}}} \quad [1/2]$

Logic Diagram using only NOR gates [1]

(6) [2]

c) PAL

1. OR array is fixed and AND array is programmable.
2. AND array can be programmed to get desired minterms.
3. Any Boolean function in SOP form can be implemented using PAL.
4. Cheaper and simpler.

PROM

1. AND array is fixed and OR array is programmable.
2. All minterms are decoded.
3. Only Boolean functions in Standard SOP form can be implemented using PROM.
4. Cheaper and simple to use.

3. a) TT for 3-bit Even parity generator circuit [1]

| 3-bit data | | | Parity bit generated ↑ P |
|------------|---|---|--------------------------------|
| A | B | C | |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

$P = 1$ when the no.
of 1's in A, B, C
is odd.

$$P = f(A, B, C)$$

$$P = \sum m(1, 2, 4, 7) \quad [1]$$

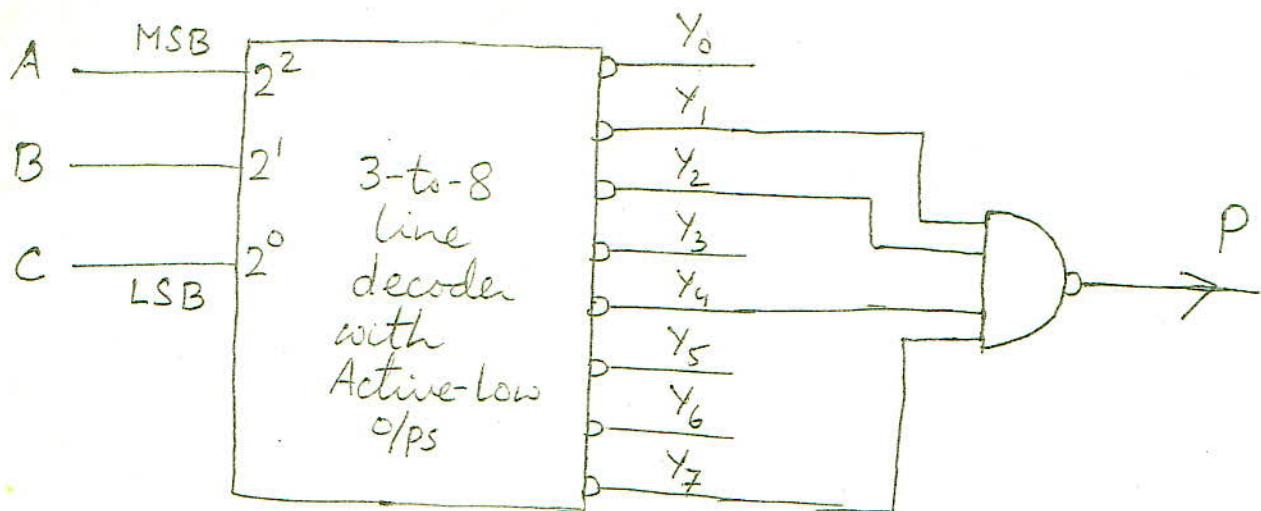
The logical function 'P' is to be implemented using a 3-to-8 line decoder with Active-Low of

(6)

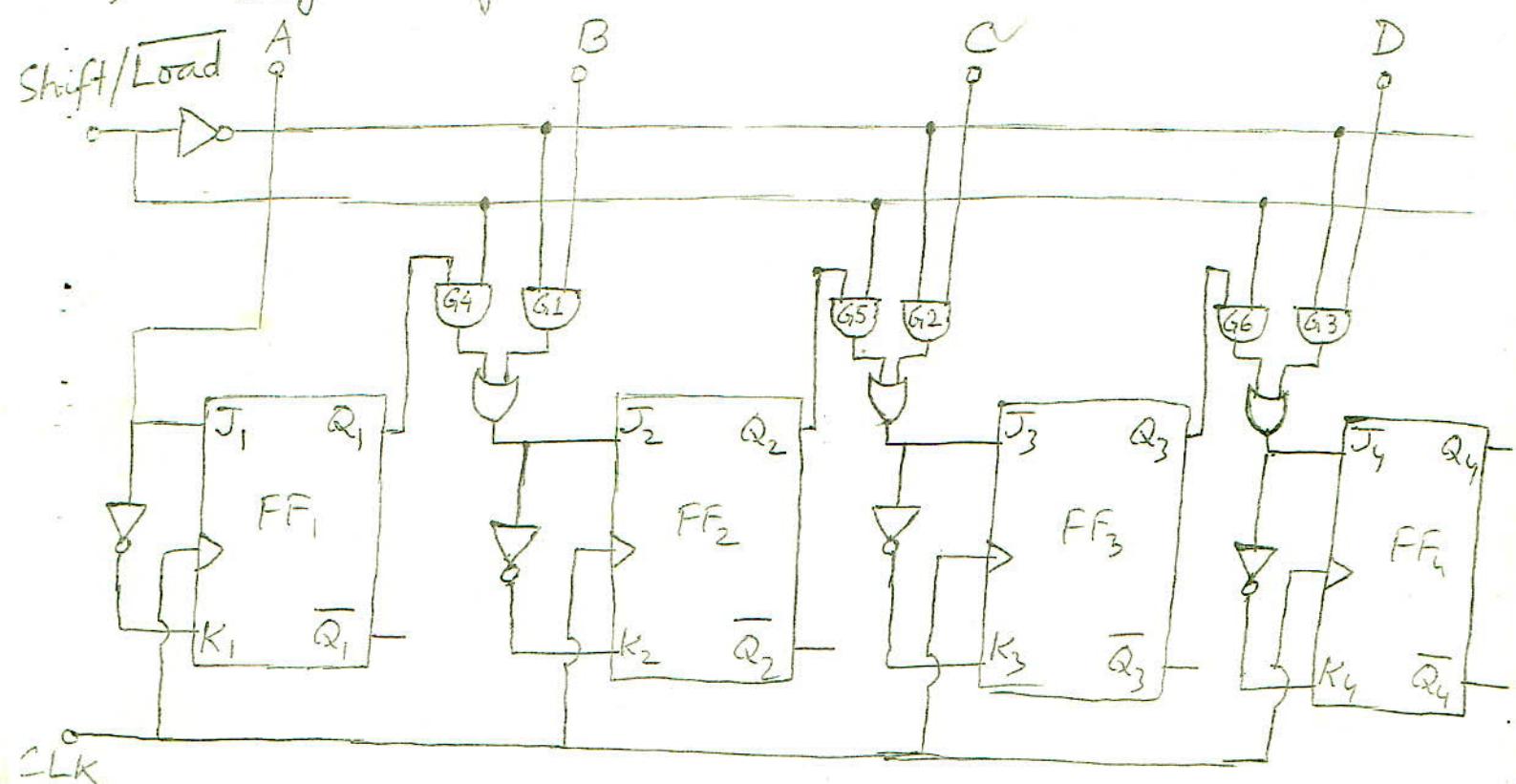
⑦

Logic Diagram [2]

⑦



b) Logic Diagram [2½]



A B C D \rightarrow 4-bit Parallel i/p data

Operation of 4-bit P-I-S-O Shift Register [1½]

- 1) The data bits are entered simultaneously into their respective stages on parallel lines, but the data bits are transferred out of the register serially i.e. on a bit-by-bit basis.
- 2) The signal Shift/Load allows the 4-bit data to be entered in parallel form into the register and the data to be shifted out serially from terminal Q_4 .

- 3) The OR gate allows either the normal shifting operation or the parallel data entry, depending on which AND gates are enabled by the level on the Shift/Load input.
- 4) $\text{Shift}/\overline{\text{Load}} = 0 \Rightarrow$ Gates G₄, G₅, G₆ disabled
 Gates G₁, G₂, G₃ enabled
 allowing the parallel data i/p to appear at the J, K i/p's of the respective FFs.
- 5) $\text{Shift}/\overline{\text{Load}} = 1 \Rightarrow$ Gates G₁, G₂, G₃ disabled
 Gates G₄, G₅, G₆ enabled allowing the data bits to shift-right from one stage to the next.

6) Truth Table for ABCD = 1101

| Clk | Shift/Load | A | B | C | D | J₁, K₁ | J₂, K₂ | J₃, K₃ | J₄, K₄ | Q₁, Q₂, Q₃, Q₄ |
|----------------|-----------------------|--------------|--------------|--------------|--------------|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 0 0 0 |
| 1 | 1 | 0 | x | x | 0 | 1 | 1 | 0 | 1 | 1 1 0 |
| 2 | 1 | 0 | x | x | 0 | 1 | 0 | 1 | 0 | 0 1 1 0 ^{CLSE} |
| 3 | 1 | 0 | x | x | 0 | 1 | 0 | 1 | 1 | 0 0 1 1 ^{1st} |
| 4 | 1 | 0 | x | x | 0 | 1 | 0 | 1 | 0 | 0 0 1 1 ^{2nd} |
| | | | | | | | | | | ^{3rd} |
| | | | | | | | | | | ^{4th} |

4 clock pulses are required for 4-bit P-I-S-O Shift-right operation. [%]
 (MSB)

(9) Fan-out of the gate when its o/p is at logic 1

$$Q. \text{ High state fan-out} = \frac{I_{OH}(\text{max})}{I_{IH}}, \quad (9) \quad [1]$$

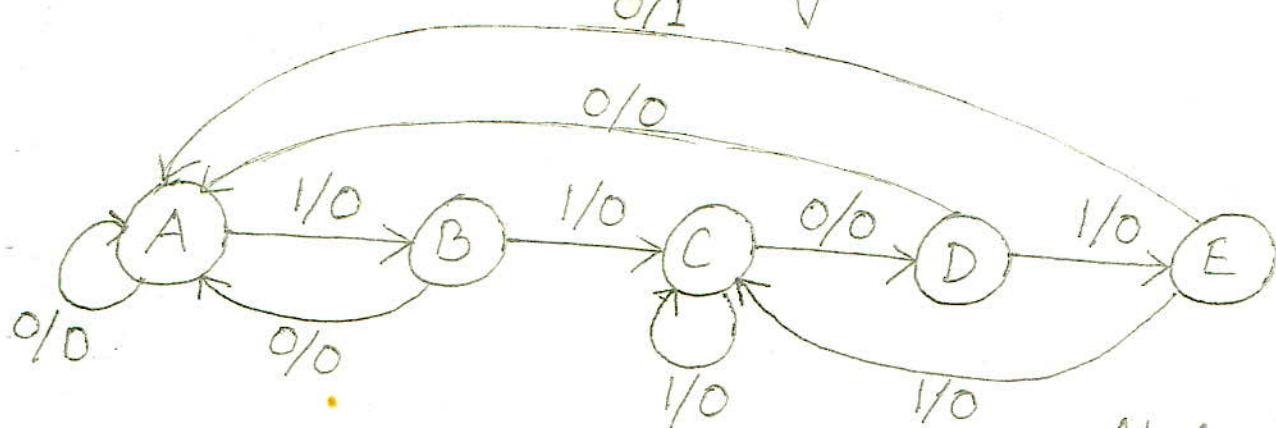
where $I_{OH}(\text{max})$ is the maximum current that the driver gate can source when it is in a 1 state and I_{IH} is the current drawn by each driven gate from the driver gate. [1]

High state noise margin (NM_H) = $V_{OH}(\text{min}) - V_{IH}(\text{min})$
 where $V_{OH}(\text{min})$ is the minimum voltage level required at the o/p of a gate for that o/p to be treated as logic 1 and $V_{IH}(\text{min})$ is the minimum voltage level required at the i/p of a gate for that i/p to be treated as a logic 1.
 NM_H is the difference between the lowest possible HIGH o/p and the minimum i/p voltage required for a HIGH.

4) a) For the input sequence '11010', overlapping is not possible.

For i/p sequence 11010 (5-bit), 5 states are required.
 Let the states be A, B, C, D, E.

'A' is the initial/startng state



State Diagram [1½]

(Mealy, Non-overlapping)

At A → 0

B → 1

C → 11

D → 110

E → 1101

(10)

(10)

State Assignment \Rightarrow $A = 000$ $C = 010$ $E = 100$
 (arbitrary) $B = 001$ $D = 011$

There are 5 states, so 3 state variables are reqd.
 3 state variables can have a max. of 8 states.
 So, states (000, 001, 010, 011, 100) are utilized
 and states (101, 110, 111) are invalid. [1/2]

State Table [1/2]

| PS | NS, Z | |
|----|-------|-------|
| | $x=0$ | $x=1$ |
| A | A, 0 | B, 0 |
| B | A, 0 | C, 0 |
| C | D, 0 | C, 0 |
| D | A, 0 | E, 0 |
| E | A, 1 | C, 0 |

Transition and Output Table [1/2]

| PS $y_1 y_2 y_3$ | NS ($y_1 y_2 y_3$) | | Output (Z) | |
|---------------------|----------------------|-------|------------|-------|
| | $x=0$ | $x=1$ | $x=0$ | $x=1$ |
| A $\rightarrow 000$ | 000 | 001 | 0 | 0 |
| B $\rightarrow 001$ | 000 | 010 | 0 | 0 |
| C $\rightarrow 010$ | 011 | 010 | 0 | 0 |
| D $\rightarrow 011$ | 000 | 100 | 0 | 0 |
| E $\rightarrow 100$ | 000 | 010 | 1 | 0 |
| 101 | XXX | XXX | X | X |
| 110 | XXX | XXX | X | X |
| 111 | XXX | XXX | X | X |

} Don't care for invalid states

| y_1, y_2 | y_3 | 00 | 01 | 11 | 10 |
|------------|-------|----|----|----|----|
| 00 | 0 | 1 | | | |
| 01 | 1 | 0 | | | |
| 11 | X | X | X | X | |
| 10 | | X | X | | |

$$D_3 = y_2 \bar{y}_3 \bar{x} + \bar{y}_1 \bar{y}_2 \bar{y}_3 x$$

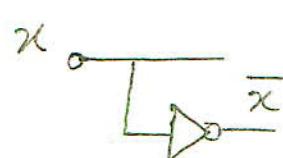
| y_1, y_2 | y_3 | 00 | 01 | 11 | 10 |
|------------|-------|----|----|----|----|
| 00 | 0 | | | | |
| 01 | 1 | | | | |
| 11 | X | X | X | X | |
| 10 | 1 | | X | X | X |

$$Z = y_1 \bar{x}$$

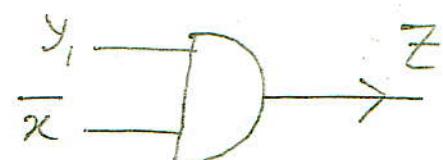
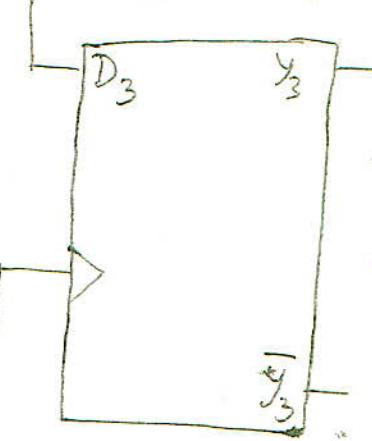
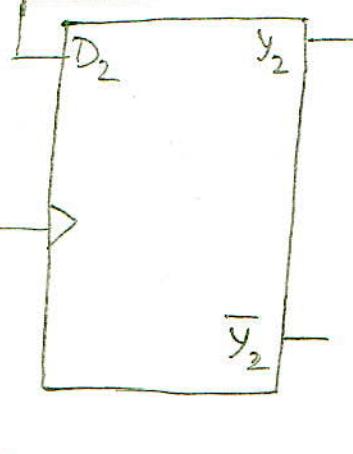
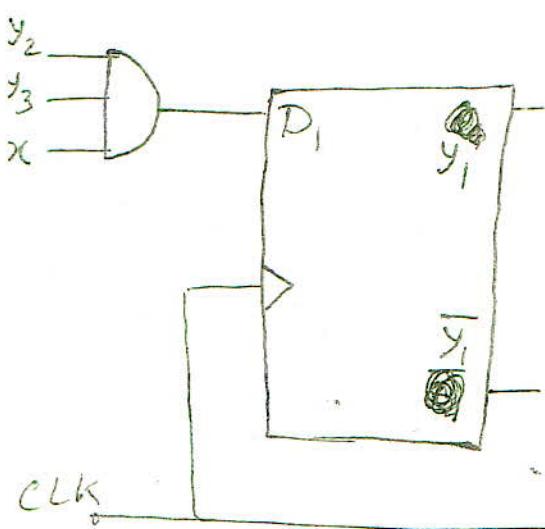
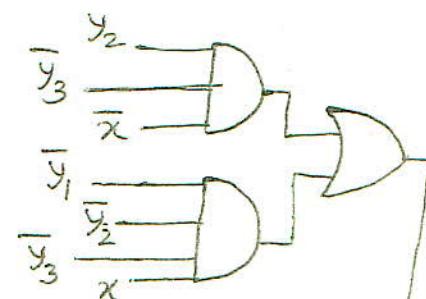
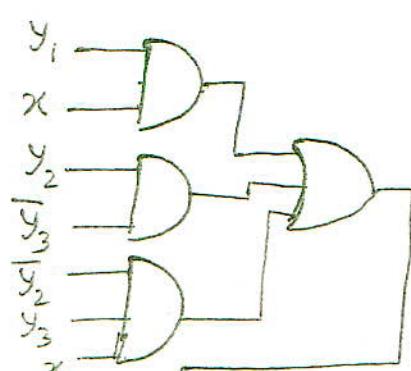
(12)

[1/2]

Q

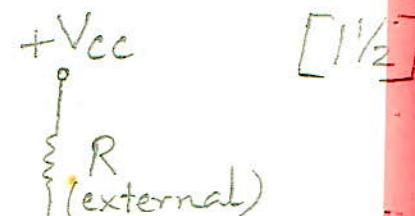
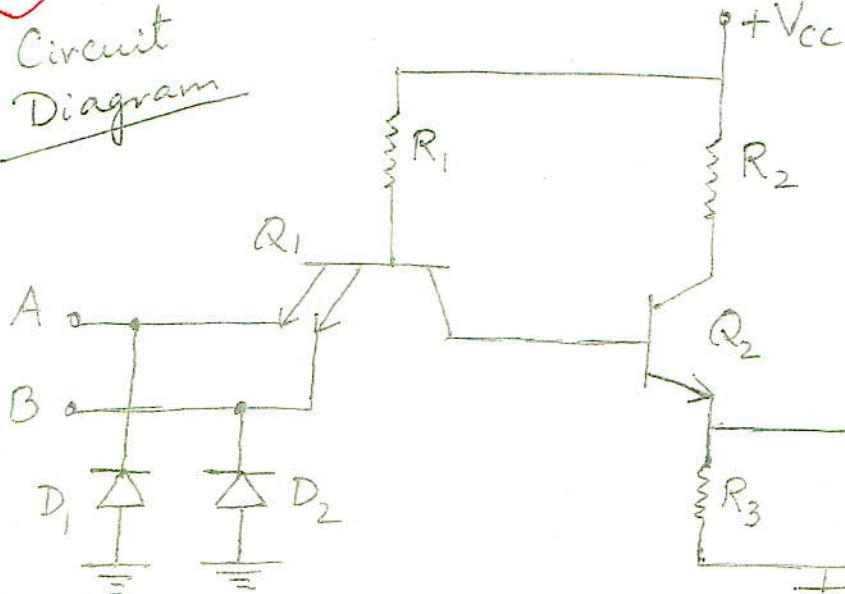


[1]



b) Open-Collector TTL 2-input NAND gate with ext. resistor

Circuit
Diagram



[1/2]

(13)

(13)

(13)

Working [1½]

- 1) D_1 and D_2 are input clamping diodes, which protect Q_1 from being damaged by the negative spikes of voltages at the inputs. When negative spikes appear at the input terminals, the diodes conduct and bypass the spikes to ground.
- 2) In the open-collector TTL, the output is at the collector of Q_3 with nothing connected to it, therefore the name "open collector".
- 3) In order to get the proper HIGH and LOW logic levels out of the circuit, an external pull-up resistor R is connected to V_{cc} from the collector of Q_3 . Since the o/p is pulled to logic HIGH level through a resistor, it is called the passive pull-up.
- 4) For TTL logic, $0 - 0.8V \equiv \text{Logic 0}$, $2 - 5V \equiv \text{Logic 1}$.
- 5)

| A | B | Q_1 | Q_2 | Q_3 | O/p ($\overline{A \cdot B}$) | |
|----|----|-------|-------|-------|--------------------------------|---|
| OV | OV | ON | | | OFF | |
| OV | 5V | OFF | | | OFF | $V_{cc} = +5V \equiv 1$ |
| 5V | OV | OFF | | | ON | $V_{ce3}(\text{sat}) \approx 0.2V \equiv 0$ |
| 5V | 5V | ON | | | ON | |

Disadvantages [1]

- 1) Larger propagation delay due to large RQ_{load} value
- 2) Greater power dissipation as compared to TTL Totem pole output.

- a) A Mod-5 Up-counter has 5 stable states 000, 001, 010, 011 and 100. Invalid states are 101, 110 and 111.

$$\text{Count}_{\max} \leq 2^n - 1$$

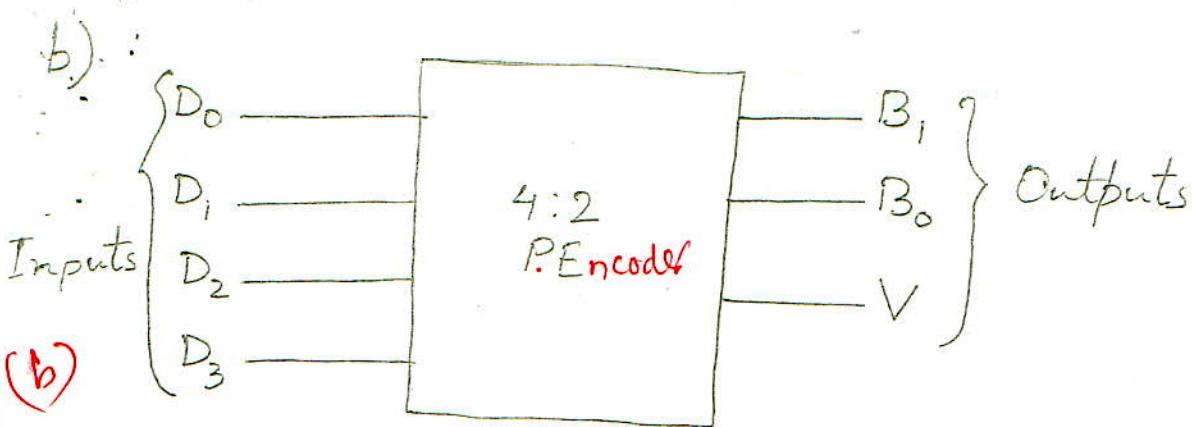
$$\Rightarrow 4 \leq 2^n - 1 \Rightarrow 5 \leq 2^n$$

$$n_{\min} = 3 \text{ FFs}$$

[1½]

(15)

(15)



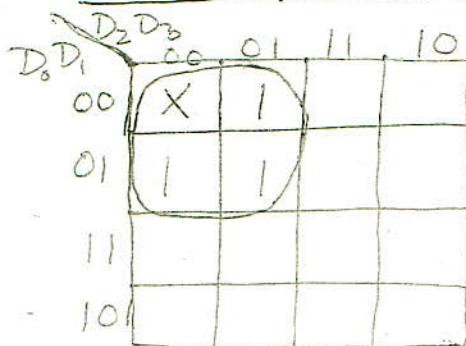
'V' is a valid bit indicator that is set to 1 when one or more input(s) are equal to 1.

$D_2 \quad D_0 \quad D_1 \quad D_3$ \rightarrow Priority decreases

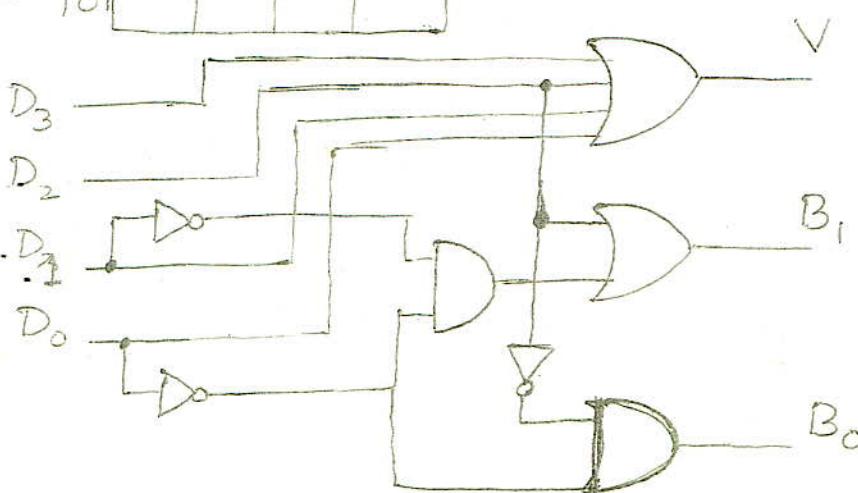
TT [1½]

| D_0 | D_1 | D_2 | D_3 | B_1 | B_0 | V |
|-------|-------|-------|-------|-------|-------|---|
| 0 | 0 | 0 | 0 | X | X | 0 |
| 1 | X | 0 | X | 0 | 0 | 1 |
| 0 | 1 | 0 | X | 0 | 1 | 1 |
| X | X | 1 | X | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 |

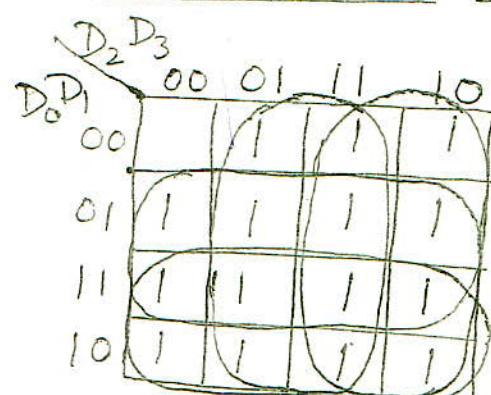
K-map for B_0 [½]



$$B_0 = \overline{D}_2 \overline{D}_0$$

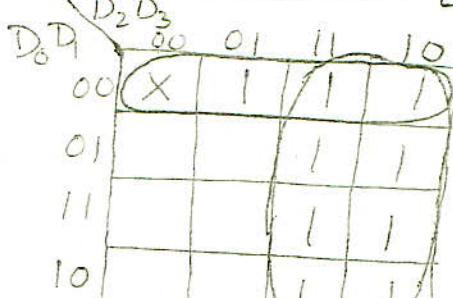


K-map for V [½]



$$V = D_3 + D_2 + D_1 + D_0$$

K-map for B_1 [½]



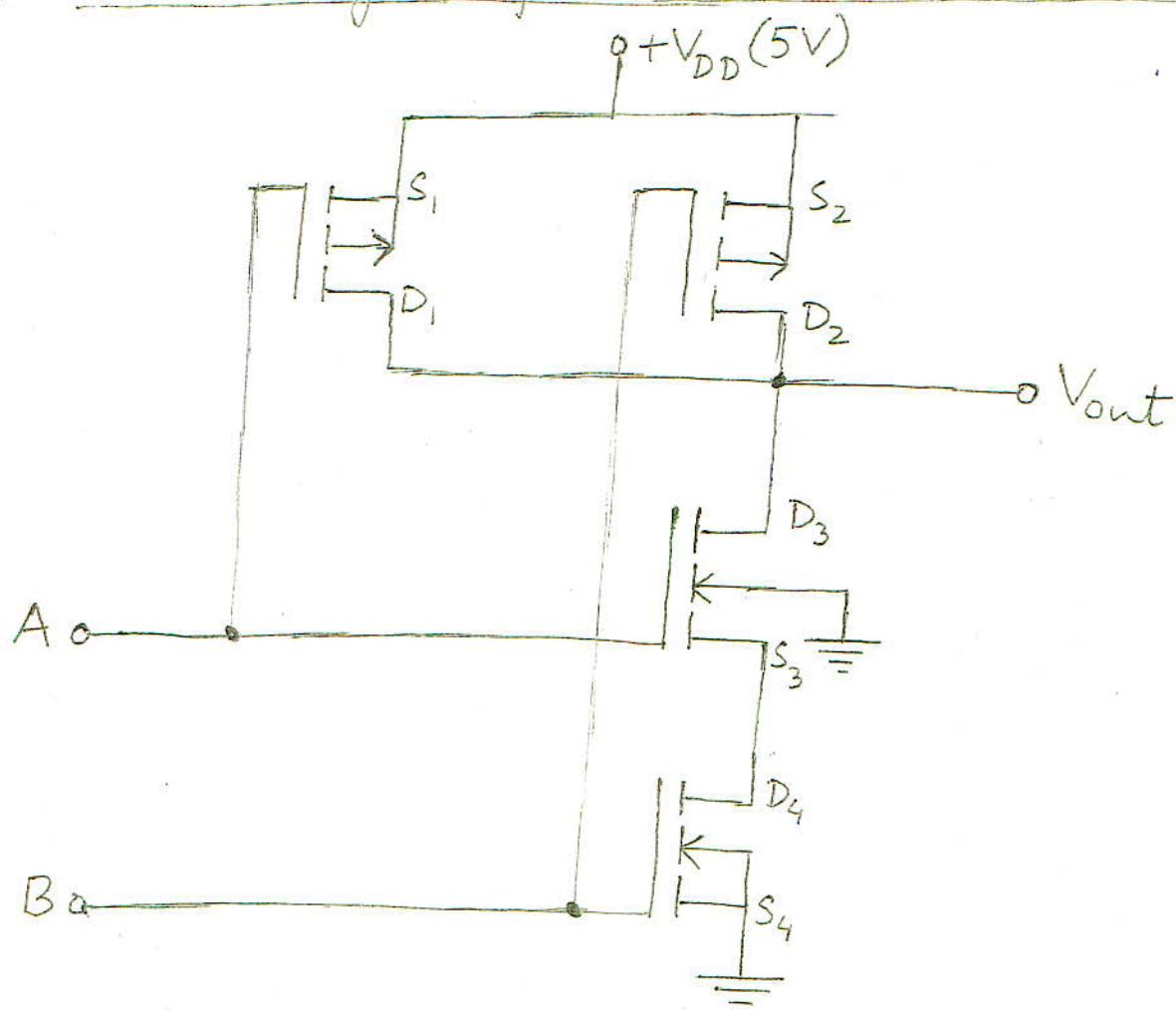
$$B_1 = D_2 + \overline{D}_1 \overline{D}_0$$

← Logic Diagram [1]

(16)

(16)

c) Circuit diagram of a 2-input CMOS NAND gate [2]



6. a) ① An astable multivibrator has two states and both of them are quasi-stable.
 ② The moment it is connected to the supply, it keeps on switching back and forth (oscillating) between its quasi-stable states, without requiring any trigger input.
 ③ Hence it is also called a free running multivibrator.

[1]

Design [2]

$$\left. \begin{array}{l} t_1 = 0.693 R_B C \\ t_2 = 0.693 R_A C \end{array} \right\} \begin{array}{l} t_1 \rightarrow \text{Discharging time constant} \\ t_2 \rightarrow \text{Charging time constant} \end{array}$$

For 50% duty cycle, $t_1 = t_2$ i.e. $R_A = R_B = 3K\Omega$

$$f = 2 \text{ KHz} \Rightarrow T = \frac{1}{2 \times 1000} = 0.5 \text{ ms}$$

$$\therefore t_1 = t_2 = \frac{T}{2} = 0.25 \text{ ms}$$

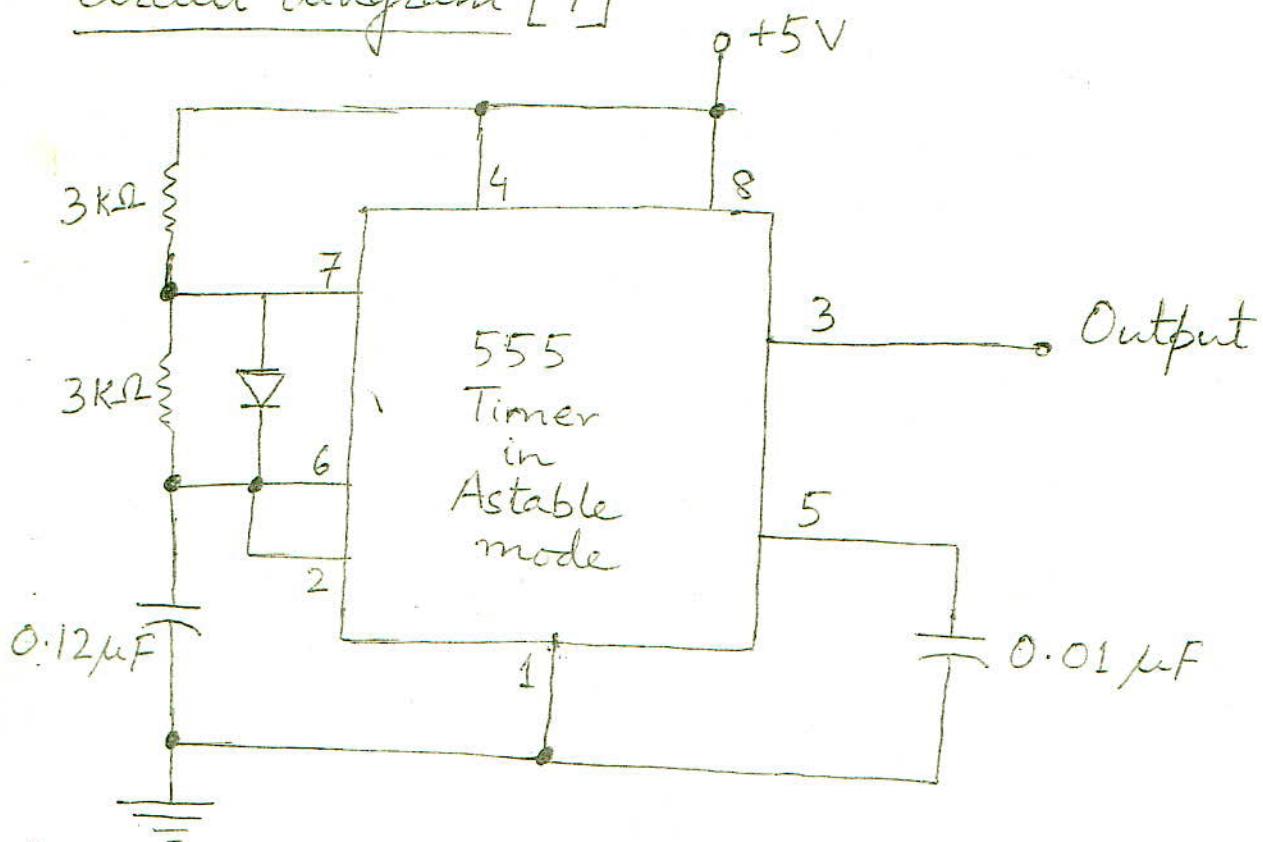
(17)

17

11

$$C = \frac{t_1}{0.693 \times R_B} = \frac{0.25 \times 10^{-3}}{0.693 \times 3 \times 10^3} = 0.12 \mu F$$

Circuit diagram [1]



b) Gray code counting sequence $\rightarrow 000, 111, 010, 011, 101$

Invalid states $\rightarrow 001, 110, 100$ (Don't care excitation)

Excitation Table [1½] $6 \leq 2^n - 1 \Rightarrow [n_{\min} = 3 \text{ FFs}]$

| PS | NS | Required excitations | | | |
|---------------|---------------|----------------------|-----------|-----------|--|
| $Q_3 Q_2 Q_1$ | $Q_3 Q_2 Q_1$ | $S_3 R_3$ | $S_2 R_2$ | $S_1 R_1$ | |
| 0 0 0 | 1 1 1 | 1 0 | 1 0 | 1 0 | |
| 1 1 1 | 0 1 0 | 0 1 | x 0 | 0 1 | |
| 0 1 0 | 0 1 1 | 0 x | x 0 | 1 0 | |
| 0 1 1 | 1 0 1 | 1 0 | 0 1 | x 0 | |
| 1 0 1 | 0 0 0 | 0 1 | 0 x | 0 1 | |

$$S_3 = \sum m(0, 3) + \sum d(1, 4, 6); R_3 = \sum m(5, 7) + \sum d(1, 2, 4, 6)$$

$$S_2 = \sum m(0) + \sum d(1, 2, 4, 6, 7); R_2 = \sum m(3) + \sum d(1, 4, 5, 6)$$

$$S_1 = \sum m(0, 2) + \sum d(1, 3, 4, 6); R_1 = \sum m(5, 7) + \sum d(1, 4, 6)$$

| | $Q_2 Q_1$ | 00 | 01 | 11 | 10 |
|-------|-----------|----|-----|----|----|
| Q_3 | 0 | 1 | (X) | 1 | |
| | 1 | X | | | X |

$$S_3 = \overline{Q}_3 (\overline{Q}_2 + Q_1)$$

| | $Q_2 Q_1$ | 00 | 01 | 11 | 10 |
|-------|-----------|-----|----|----|----|
| Q_3 | 0 | | X | | X |
| | 1 | (X) | 1 | 1 | X |

$$R_3 = Q_3$$

19

[1/2]

| | $Q_2 Q_1$ | 00 | 01 | 11 | 10 |
|-------|-----------|-----|----|----|-----|
| Q_3 | 0 | 1 | X | | (X) |
| | 1 | (X) | | X | (X) |

$$S_2 = \overline{Q}_1$$

| | $Q_2 Q_1$ | 00 | 01 | 11 | 10 |
|-------|-----------|----|-----|----|----|
| Q_3 | 0 | | (X) | 1 | |
| | 1 | X | X | | X |

$$R_2 = \overline{Q}_3 Q_1$$

[1/2]

| | $Q_2 Q_1$ | 00 | 01 | 11 | 10 |
|-------|-----------|-----|----|----|-----|
| Q_3 | 0 | 1 | X | X | (1) |
| | 1 | (X) | | | X |

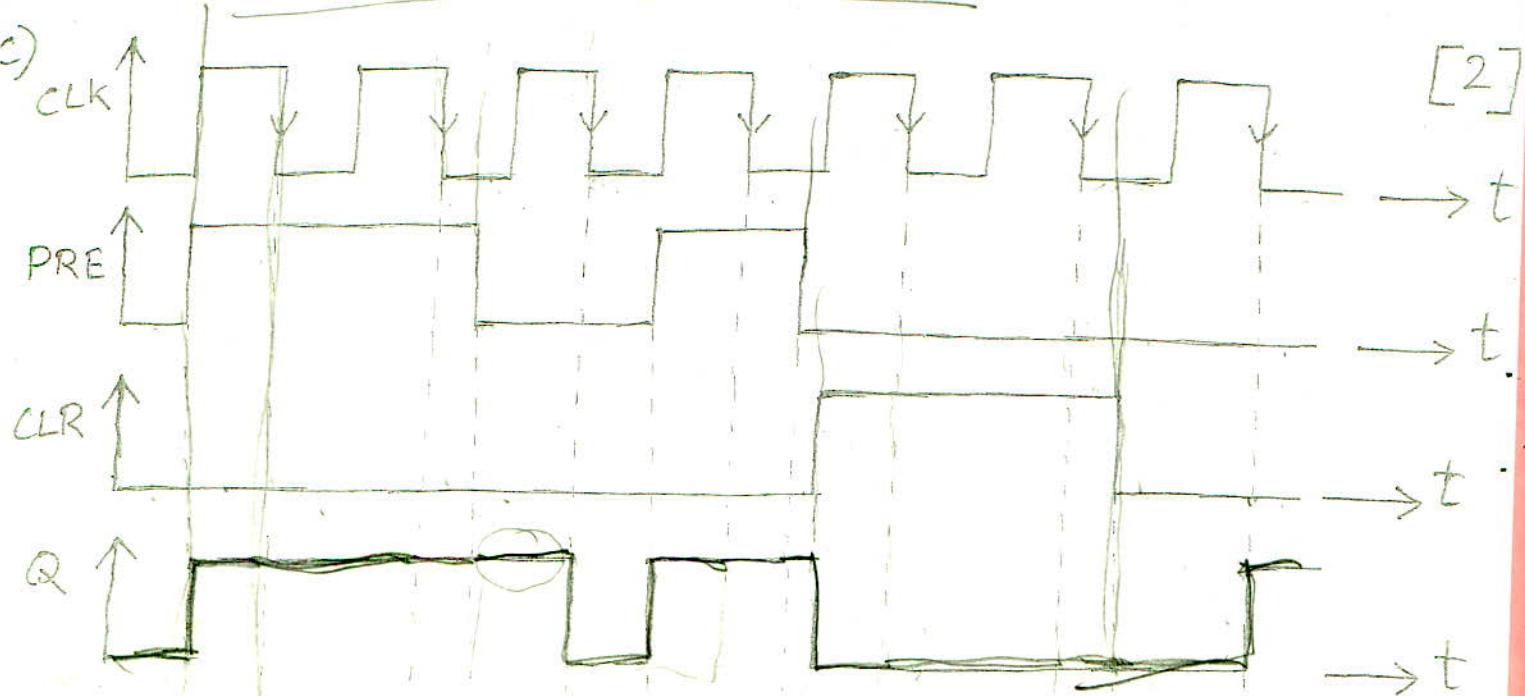
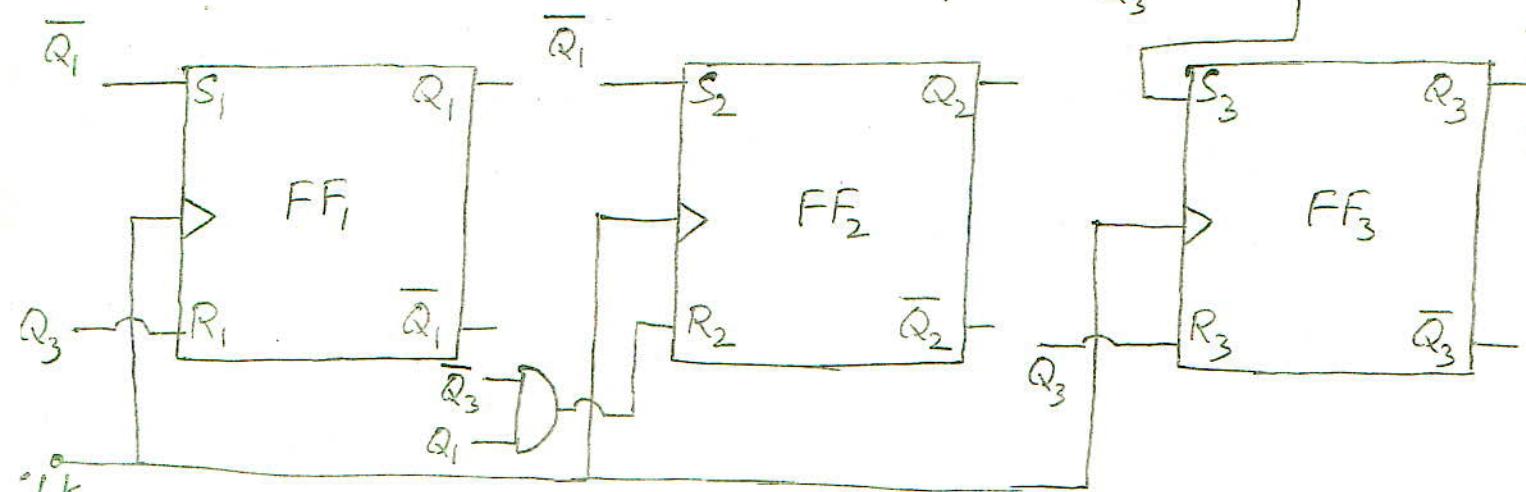
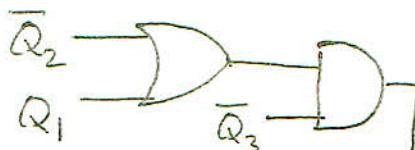
$$S_1 = \overline{Q}_1$$

| | $Q_2 Q_1$ | 00 | 01 | 11 | 10 |
|-------|-----------|-----|----|----|----|
| Q_3 | 0 | | X | | |
| | 1 | (X) | 1 | 1 | X |

$$R_1 = Q_3$$

[1/2]

Logic Diagram [1]



7. a) TT [1½]

| Dec. | A | B | C | X | Y | Z |
|------|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 2 | 0 | 1 | 0 | 0 | 0 | 1 |
| 3 | 0 | 1 | 1 | 1 | 0 | 0 |
| 4 | 1 | 0 | 0 | 0 | 1 | 1 |
| 5 | 1 | 0 | 1 | 1 | 1 | 0 |
| 6 | 1 | 1 | 0 | 1 | 0 | 1 |
| 7 | 1 | 1 | 1 | 1 | 1 | 0 |

| | | | |
|---|---|---|---|
| 0 | 1 | 3 | 5 |
| 6 | 7 | | |

(19)

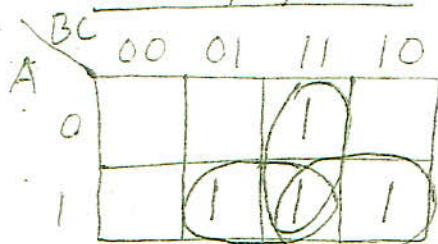
From the TT,

$$X = \sum m(3, 5, 6, 7)$$

$$Y = \sum m(1, 4, 5, 7)$$

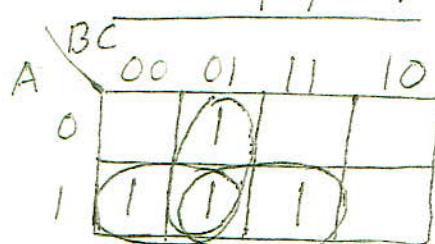
$$Z = \sum m(0, 2, 4, 6)$$

K-map for X [1½]



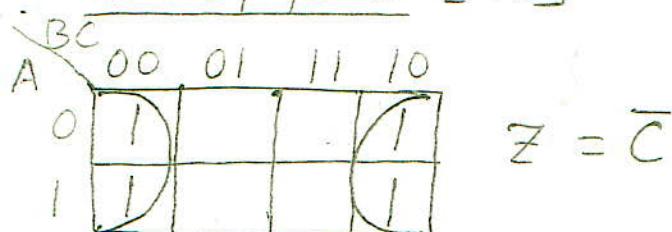
$$X = AB + BC + CA$$

K-map for Y [1½]



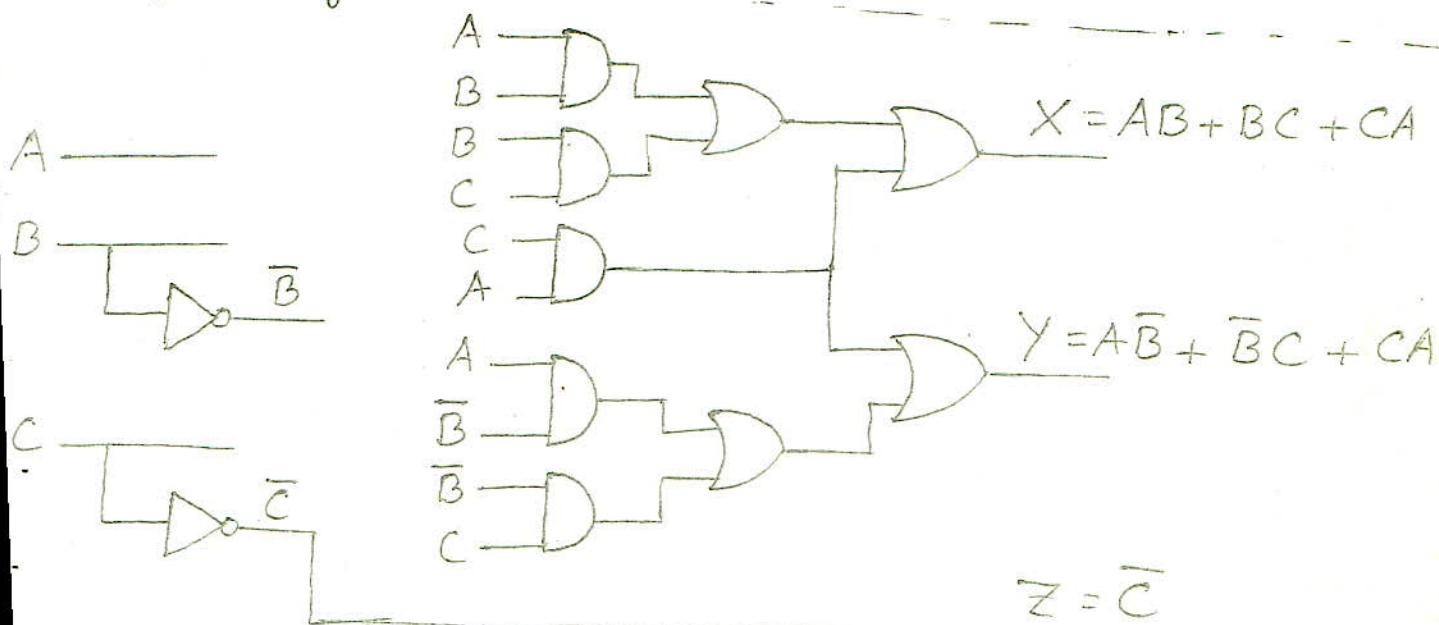
$$Y = A\bar{B} + \bar{B}C + CA$$

K-map for Z [1½]



$$Z = \bar{C}$$

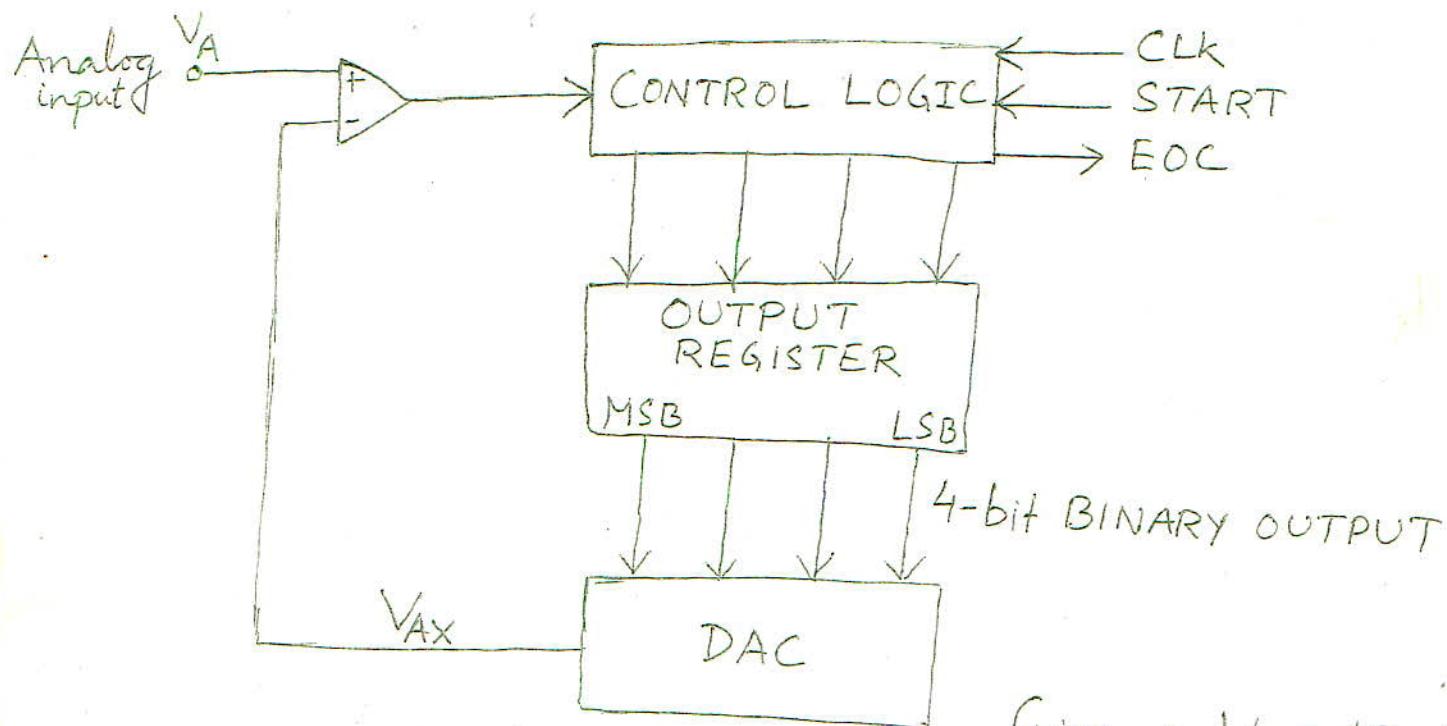
Logic diagram [1]



(20)

(20)

b) Block Diagram of a 4-bit SA-type ADC [1]



Given: $V_A = 12.6 \text{ V}$

WORKING [1½]

- 1) The bits of the DAC are enabled one at a time, starting with the MSB. As each bit is enabled, the comparator produces an output that indicates whether the analog input is greater or less than the output of the DAC i.e. V_{AX} .
- 2) If $V_{AX} > V_A$, the comparator output is LOW, causing the bit in the control register to reset.
- 3) If $V_{AX} < V_A$, the comparator output is HIGH, and the bit is retained in the control register.
- 4) After all the bits of the DAC have been tried, the conversion cycle is complete and the control logic activates its EOC output to signal that the digital equivalent of V_A is now in the output register.

| | CLK | OP register | V_{AX} | V_A | Comparator o/p | Bit status |
|---|-----|-------------|----------|-------|----------------|-----------------------------|
| | MSB | LSB | | | | |
| 1 | 1 | 0 0 0 | 8V | 12.6V | 1 | Bit set retained |
| 2 | 1 | 1 0 0 | 12V | 12.6V | 1 | Bit retained |
| 3 | 1 | 1 1 0 | 14V | 12.6V | 0 | Bit reset |
| 4 | 1 | 1 0 1 | 13V | 12.6V | 0 | Bit reset |
| | 1 | 1 0 0 | | | | |

(21)

(19)

(21)

Digital output = $(1100)_2$ or ~~$(12)_{10}$~~ (12)₁₀ volts [1/2]

Clock frequency = 1 MHz ; Time period = 1 μ s

Conversion time = $4 \times 1 \mu\text{s} = 4 \mu\text{s}$ [1/2]

New $V_A = 14.8 \text{ V}$

$$t_c = N \times \frac{1}{f_{\text{clock}}}$$

Successive-Approximation type ADC has a fixed conversion time which is independent of the value of the analog i/p voltage V_A . This is because the control logic has to process each bit to see whether a 1 is needed or not.

Hence, new conversion time = 4 μs (same as previous one, since the no. of bits required for 14.8 V is also 4) [1/2]

c) Memory capacity = $64 \text{ K} \times 16$

$$2^k \times n = 64 \text{ K} \times 16$$

$$\Rightarrow 2^k = 64 \text{ K} = 2^6 \times 2^{10} = 2^{16} \quad \text{and } n = 16$$

$$\therefore k = 16, n = 16 \quad [1/2]$$

i) No. of data i/p lines = ~~n~~ $n = 16$ [1/2]

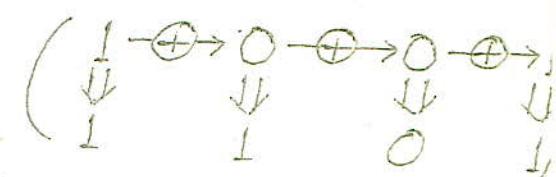
No. of data o/p lines = $n = 16$ [1/2]

ii) No. of address lines = $k = 16$ [1/2]

8. a) For Binary-to-Gray Converter [1/2]

4-bit Binary input = 1001

4-bit Gray output = 1101



For Hamming Code Encoder [2]

Data i/p = 1101

Parity \rightarrow Odd

| | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|
| P_1 | P_2 | D_3 | P_4 | D_5 | D_6 | D_7 |
| ? | ? | 1 | ? | 1 | 0 | 1 |

$$P_1 \oplus D_3 \oplus D_5 \oplus D_7 = 1 \Rightarrow P_1 = 0 \quad [1/2]$$

$$P_2 \oplus D_3 \oplus D_6 \oplus D_7 = 1 \Rightarrow P_2 = 1 \quad [1/2]$$

$$P_4 \oplus D_5 \oplus D_6 \oplus D_7 = 1 \Rightarrow P_4 = 1 \quad [1/2]$$

\therefore Hamming Code (7-bit) = 0111101 [1/2]

(22)

21

For Priority Encoder [1/2]

| Decimal i/p's | | | | | | | 3-bit Binary o/p | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|------------------|----------------|----------------|
| D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | B ₂ | B ₁ | B ₀ |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |

(Priority order: D₇ > D₆ > D₅ > D₄ > D₃ > D₂ > D₁)

For Magnitude Comparator [1]

$$A = A_1, A_0 = (B_2, B_1)_{PE} = 11$$

$$B = B_1, B_0 = (B_0)_{PE}^0 = 00$$

$$\therefore A > B,$$

$$\therefore E(A=B) = 0$$

$$G(A > B) = 1$$

$$L(A < B) = 0$$

All 3 outputs of the 2-bit
Magnitude Comparator

b) $F(A, B, C, D) = A\bar{B} + C\bar{D} + A\bar{C}$ (SOP form)
 $= A\bar{B}(C + \bar{C})(D + \bar{D}) + (A + \bar{A})(B + \bar{B})C\bar{D}$
 $+ A(B + \bar{B})\bar{C}(D + \bar{D})$

SSOP form $\left[\frac{1}{2}\right] \leftarrow$ $= A\bar{B}CD + A\bar{B}\bar{C}D + A\bar{B}C\bar{D} + A\bar{B}\bar{C}\bar{D} + ABC\bar{D}$
 $+ \bar{A}BC\bar{D} + \bar{A}\bar{B}C\bar{D} + AB\bar{C}D + AB\bar{C}\bar{D}$
 $= \sum m(2, 6, 8, 9, 10, 11, 12, 13, 14)$

Minterm form $\left[\frac{1}{2}\right]$

TT → Next page

(23)

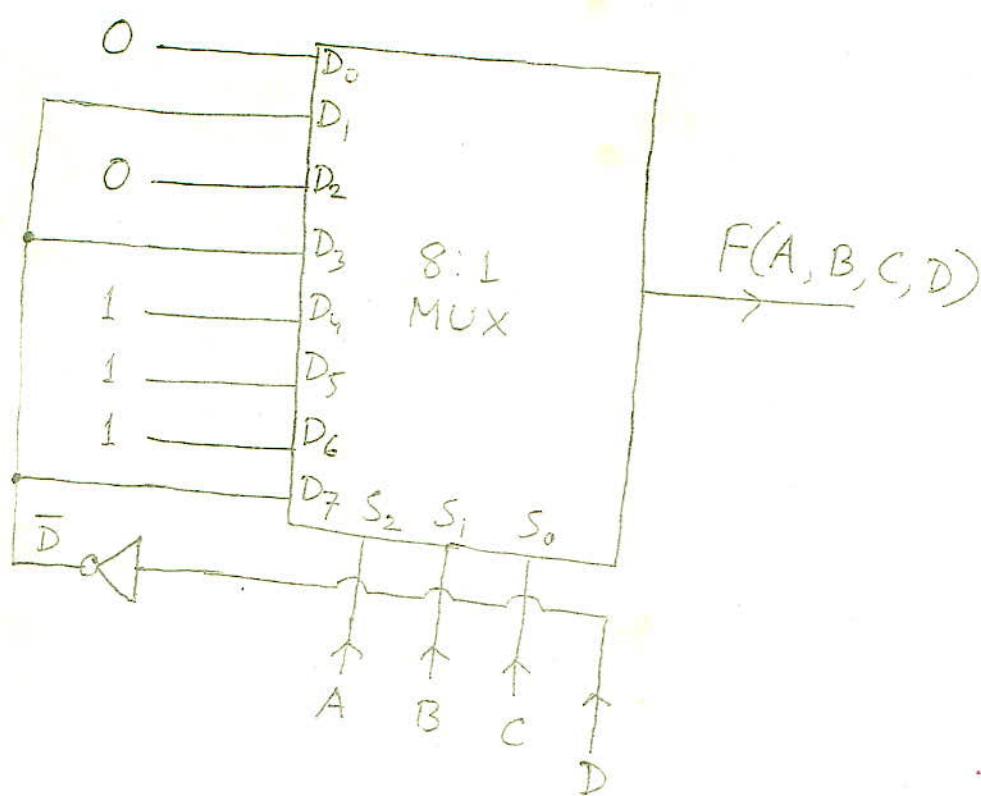
TT [2]

| Dec | A | B | C | D | $F(A, B, C, D)$ |
|-----|---|---|---|---|-----------------|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 2 | 0 | 0 | 1 | 0 | 1 |
| 3 | 0 | 0 | 1 | 1 | 0 |
| 4 | 0 | 1 | 0 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 | 1 |
| 7 | 0 | 1 | 1 | 1 | 0 |
| 8 | 1 | 0 | 0 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 | 1 |
| 10 | 1 | 0 | 1 | 0 | 1 |
| 11 | 1 | 0 | 1 | 1 | 1 |
| 12 | 1 | 1 | 0 | 0 | 1 |
| 13 | 1 | 1 | 0 | 1 | 1 |
| 14 | 1 | 1 | 1 | 0 | 1 |
| 15 | 1 | 1 | 1 | 1 | 0 |

(21)

(23)

Logic diagram [1]



| | N-bit Ring Counter | N-bit Johnson Counter | N-bit Ripple Counter |
|---------------------|--|---|--|
| 1. Modulus | N | $2N$ | 2^N |
| 2. Decoding circuit | Decoder/external gates are not required, since we can read the count by simply noting which FF is set. | It requires 2-input gates for decoding regardless of the size of the counter. | It requires more decoding circuitry than that required by Johnson counter. |

— X —

Debjit Ghosh

13/5/13