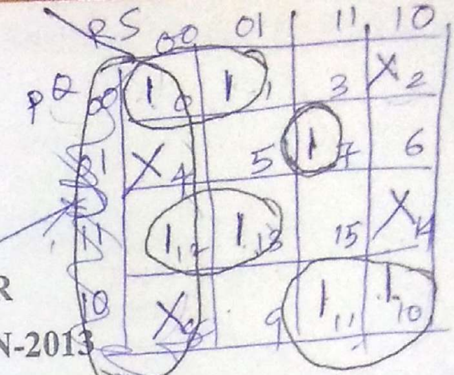


KIIT UNIVERSITY, BHUBANESWAR

SPRING MID SEMESTER EXAMINATION-2013

DIGITAL ELECTRONICS CIRCUITS [EC- 402]

Full Marks: 25 **Duration: 2Hrs**

$\overline{R}\,\overline{S}+\overline{P}\,\overline{Q}\,\overline{R}+PQ\overline{R}+P\overline{Q}R+\overline{P}QRS$.

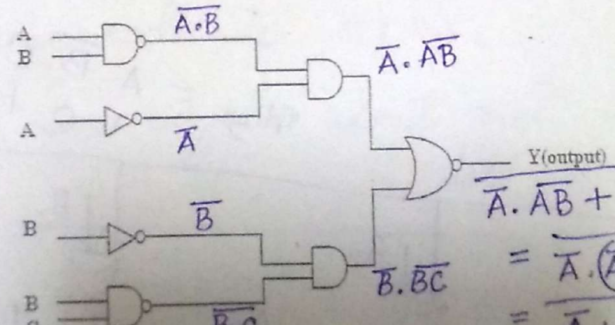
Answer any FIVE questions including question No.1 which is compulsory.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and *all parts of a question should be answered at one place only.*

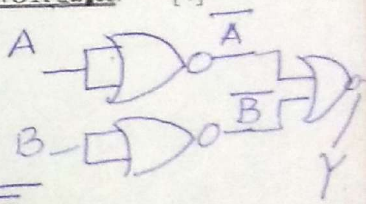
(1) a) "Gray codes are cyclic but not sequential & self-complementing." Justify. [1x5]
b) Perform following arithmetic: (i) BCD addition (749+858),
(ii)(-9) - (-6) using 2's complement method.
c) Show that, $U\overline{V}+UW+V\overline{W}=U+V\overline{W}$ where U, V and W are Boolean variables.
d) Define 'Positive logic system' and 'Negative logic system'.
e) Why the row and column values of the K- map are ordered in Gray code rather than binary numerical order, explain in brief.

(2) Obtain the minimized expression for the following 4-variable Boolean expression using K-map method and implement the minimized expression using **minimum numbers of universal gates.** [5]
$$F(P,Q,R,S)=\sum m\,(0,1,7,10,11,12,13)+d(2,4,8,14)$$

(3) a) Design 4-bit combined adder/subtractor circuit using **full adders & XNOR gates only** and explain the working in brief. [4]
b) Define Reflective codes and explain with proper example in brief. Gray codes. [1]

(4) a) Simplify the given logic circuit and implement the simplified expression using **only NOR gates**. [4]





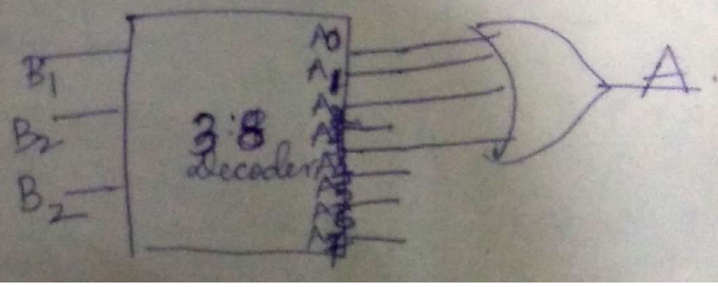
$\overline{A}.\overline{AB}+\overline{B}.\overline{BC}$
$=\overline{\overline{A}.(\overline{A}+\overline{B})+\overline{B}\,(\overline{B}+\overline{C})}$
$=\overline{\overline{A}+\overline{A}\,\overline{B}+\overline{B}+\overline{B}\,\overline{C}}$
$=\overline{\overline{A}+\overline{B}\,(\overline{A}+1+\overline{C})}$
$=\overline{\overline{A}+\overline{B}}$

b) What is the disadvantage of Ripple carry adder and how can it be minimized? [1]

(5) a) What is Decoder? Draw the circuit diagram and truth table of 2-4 decoder having active-LOW output terminals. [2]
b) In a room there are three electric lamps. For sufficient light intensity, at least two lamps must be ON at the same time. Design a circuit, using 3-8 decoder (having active HIGH output lines) and basic logic gates, which enables an alarm when light intensity in the room is not sufficient. [3]

B_1	B_2	B_3	A
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0

$A=\sum m(0,1,2,4)$.



(6) a) In the figure given below X, Y and Z are 7-bit Hamming codes. A, B and C are 4-bit data. [4]

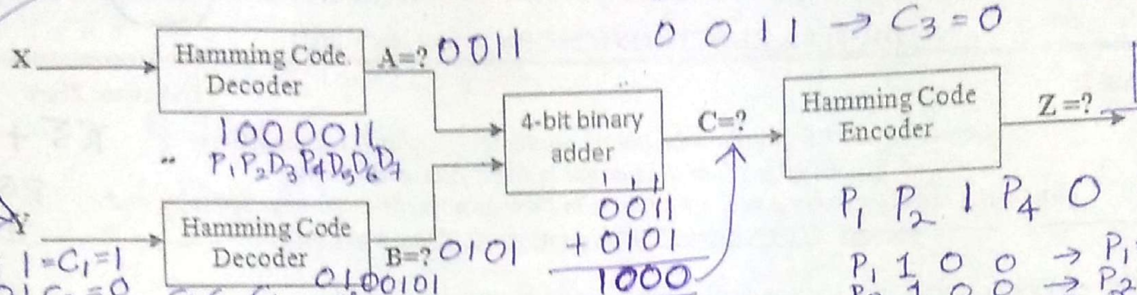
where **X: 1010011**

Y: 1100101

1 0 1 0 0 1 1
$P_1 P_2 D_3 P_4 D_5 D_6 D_7$

1 1 0 1 → $C_1 = 1$
0 1 1 1 → $C_2 = 1$
0 0 1 1 → $C_3 = 0$

$(C_3 C_2 C_1) = (0\ 1\ 1)_2 = 3^{rd}$ pa.



A = 0011, 1000011 ($P_1 P_2 D_3 P_4 D_5 D_6 D_7$)

1110000

0011
+ 0101
1000

$P_1\ P_2\ 1\ P_4\ 0\ 0\ 0$
P_1 1 0 0 → $P_1 = 1$
P_2 1 0 0 → $P_2 = 1$
P_4 0 0 0 → $P_4 = 0$

1 0 1 1 = $C_1 = 1$
1 0 0 1 $C_2 = 0$
0 1 0 1 $C_3 = 0$
$(C_3 C_2 C_1) = (0\ 0\ 1)_2 = 1^{st}$ pa.
B = 0101, 0100101

Find **A, B, C** and **Z.** [Assume (i) even parity system (ii) at most single bit error may take place.]

b) Define 'minterm' and 'maxterm' and show that $m_i = \overline{M_i}$, [1]
(where m_i : i^{th} minterm & M_i: i^{th} maxterm)

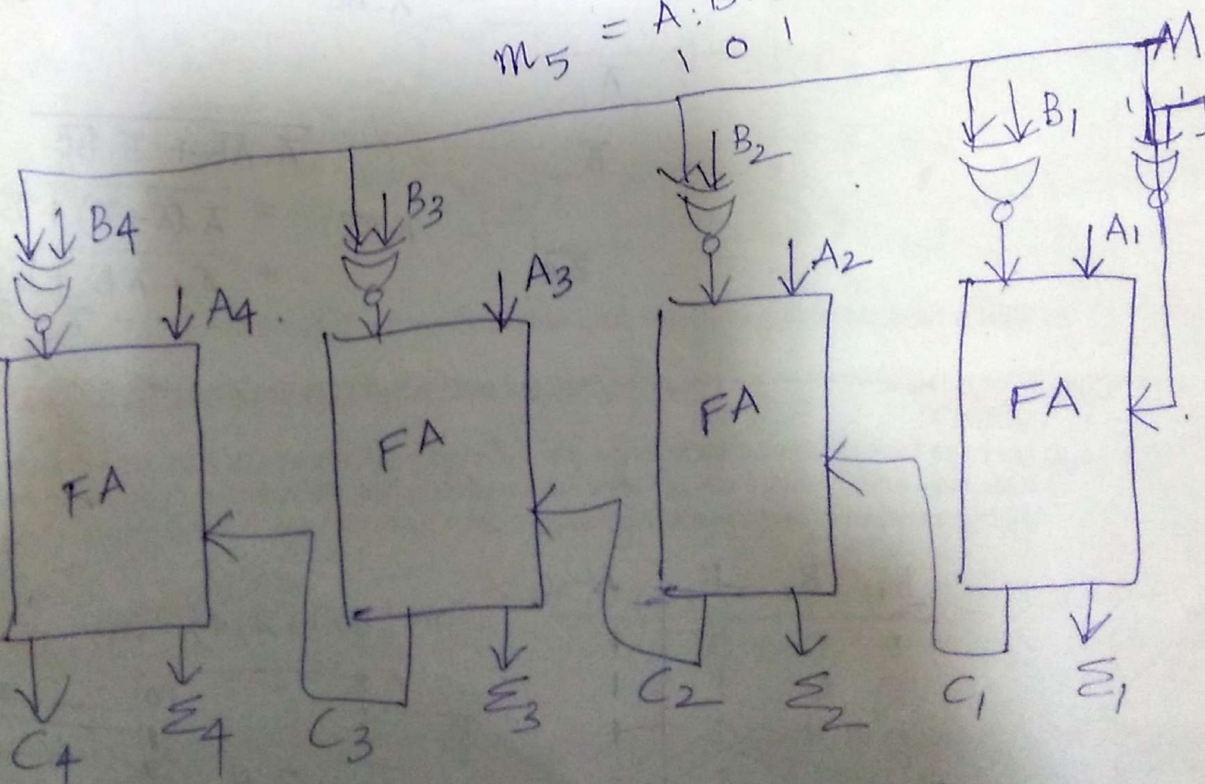
$M_5 = \overline{A} + B + \overline{C}$

$\overline{M_i} = \overline{\overline{A} + B + \overline{C}}$

$= \overline{\overline{A}} \cdot \overline{B} \cdot \overline{\overline{C}}$

$= A \cdot \overline{B} \cdot C$

m_5 1 0 1



M = 0
$0 \odot B$
$= 0 \cdot B + \overline{0} \cdot \overline{B}$
$= 1 \cdot \overline{B} = \overline{B}$
(Subtractor)

M = 1
$1 \odot B$
$1 \cdot B + \overline{1} \cdot \overline{B}$
$= B + 0 \cdot \overline{B}$
$= B$ (Adder).

$0 \cdot M + \overline{0} \cdot \overline{M}$
$= 1 \cdot \overline{M}$

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V.S. an 01 11. 10.

(01)

Q1) (a) Gray codes are cyclic because two adjacent code words have unit distance b/w them.

ex. 2 → 0011
3 → 0010 (only 1 bit change b/w adjacent codewords)

bit width

They are not sequential because we can't always get the succeeding code word by adding binary 1 to preceding code word. eg. 11 → 1110 (gray)
12 → 1010 (gray)

They are not self-complementing because we can't get the code word for 9−N by just complementing (1's complement) the code word for N.

eg. 4 = 0110 (gray)
↓ 1's complement
(9−4)=5 ≠ 1001 (gray)

For 5, gray code is 0111.

∴ "Gray codes are cyclic but not sequential & self-complementing."

(b) (i) 749 + 858

749 → $(0111, 0100, 1001)_{8421}$

858 → $+(1000, 0101, 1000)_{8421}$

1111, 1010, 0001 (Invalid BCD & carry)
+ 0110 0110 0110 Add 0110 to each nibble.

$\underbrace{1}_{1}\underbrace{0110}_{6},\underbrace{0000}_{0},\underbrace{0111}_{7}$

∴ 749+858=1607

Teacher's Signature :

(b) (ii) $(-9) - (-6)$

$= -9 + 6 = 6 + (-9) = 6 + (2\text{'s complement of } 9)$

$(+9) = 00001001$

$(-9) = 2\text{'s complement of } (+9) = 11110111$

$(+6) = 00000110$

$$\therefore \begin{array}{r} 00000110 \\ +\ 11110111 \\ \hline \underbrace{11111101}_{\therefore (-3)} \end{array}$$

(no carry). The result is –ve (MSB bit = 1) and is in 2's complement form.

$\therefore$ True ~~result~~ value =
2's complement of (2's complement form of result)

$= 00000011 = (+3)$

(c) $U\bar{V} + UW + V\bar{W} = U + V\bar{W}$

Applying Consensus theorem in 1st & 3rd term, we get additional $U\bar{W}$,

LHS =

$\Rightarrow U\bar{V} + UW + V\bar{W} + U\bar{W}$

$= U\bar{V} + UW + U\bar{W} + V\bar{W}$

$= U\bar{V} + U(W + \bar{W}) + V\bar{W}$ $[\because AB + AC = A(B+C)]$

$= U\bar{V} + U.1 + V\bar{W}$ $[\because A + \bar{A} = 1]$

$= U(\bar{V} + 1) + V\bar{W}$ $[\because A + 1 = 1]$.

$= U + V\bar{W} = RHS$

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(03)

(d) Positive Logic System → If ~~vcc~~ HIGH voltage level is used to represent 1 and LOW voltage level to represent 0, the system is called positive logic system.

Negative Logic System → If HIGH voltage level is used to represent 0 and LOW voltage level is used to represent 1, the system is called negative logic system.

(e) Row and column values of K-map are ordered in Gray codes rather than binary because gray codes are unit distance codes (there is change in one bit position only b/w adjacent code words).

(Q2)

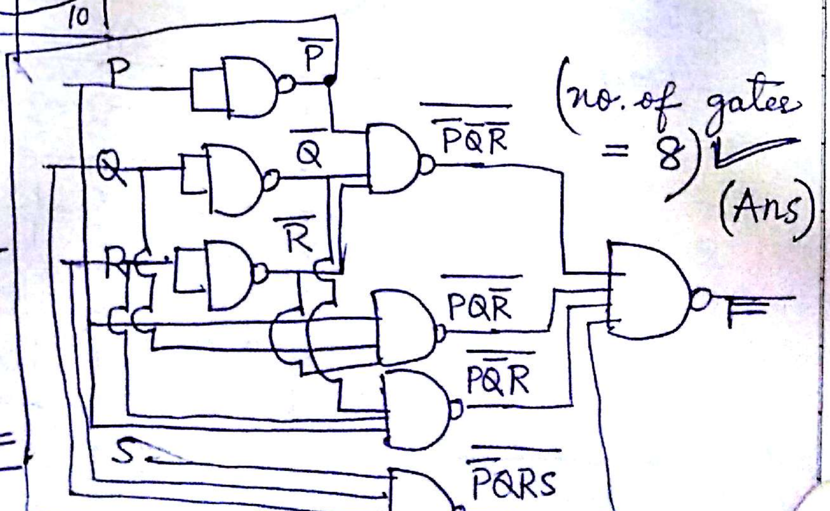
PQ \ RS	00	01	11	10
00	1 (0)	1 (1)	(3)	X (2)
01	X (4)	(5)	1 (7)	(6)
11	1 (12)	1 (13)	(15)	X (14)
10	X (8)	(9)	1 (11)	1 (10)

$F(P,Q,R,S) = \overline{P}\,\overline{Q}\,\overline{R} + PQ\overline{R} + P\overline{Q}R + \overline{P}QRS.$

Using NAND

$$F = \overline{\overline{\overline{P}\,\overline{Q}\,\overline{R} + PQ\overline{R} + P\overline{Q}R + \overline{P}QRS}}$$

$$= \overline{\overline{\overline{P}\,\overline{Q}\,\overline{R}} \cdot \overline{PQ\overline{R}} \cdot \overline{P\overline{Q}R} \cdot \overline{\overline{P}QRS}}$$

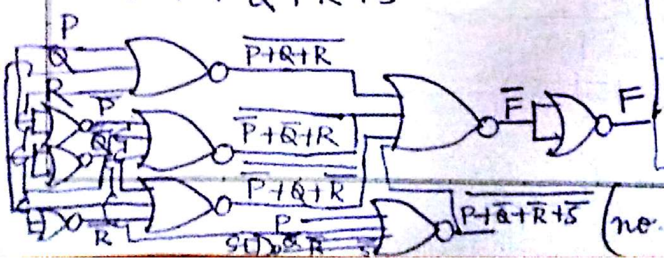


(no. of gates = 8) (Ans).

Using NOR

$$F = \overline{\overline{\overline{P}\,\overline{Q}\,\overline{R}} + \overline{PQ\overline{R}} + \overline{P\overline{Q}R} + \overline{\overline{P}QRS}}$$

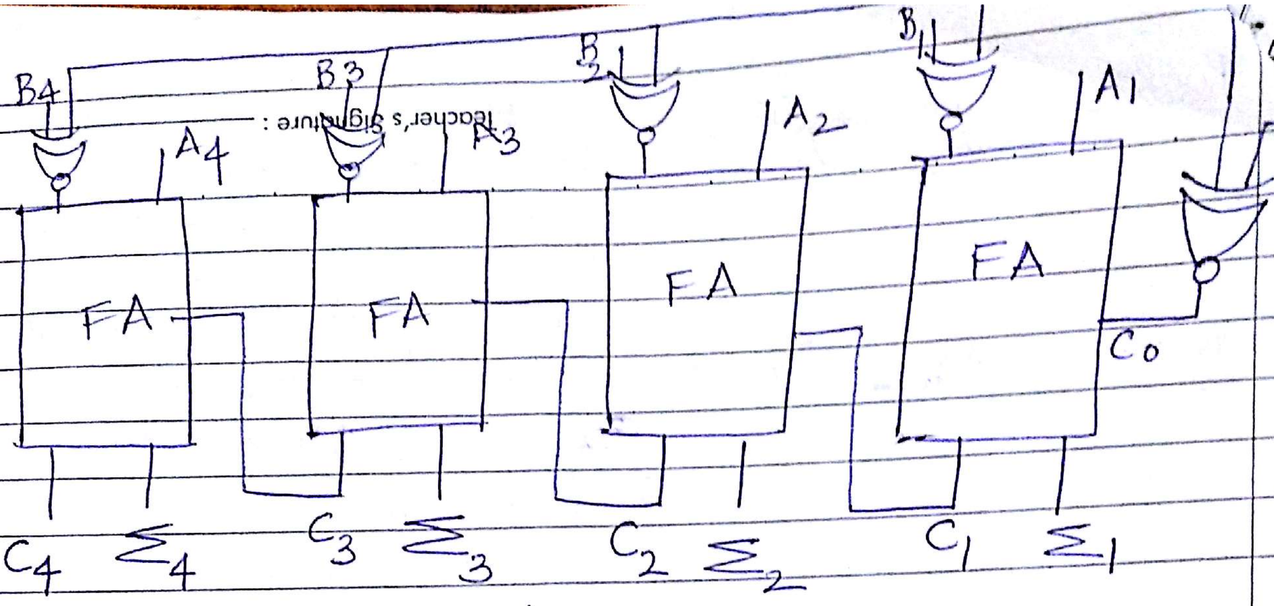
$$= \overline{P+Q+R} + \overline{\overline{P}+\overline{Q}+R} + \overline{\overline{P}+Q+\overline{R}} + \overline{P+\overline{Q}+\overline{R}+\overline{S}}$$



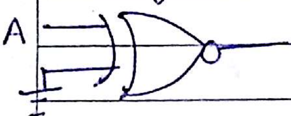
(no. of gates = 10)

04

(Q3)(a)



XNOR gate



A	B	$A \odot B$
0	0	1
0	1	0
1	0	0
1	1	1

If $M = 0$, subtractor. (2's complement method of subtraction)

$M \odot B$
$= MB + \overline{M}\,\overline{B}$
$= 0.B + \overline{0}.\overline{B}$
$= \overline{B}$

If $M = 1$, adder.

$M \odot B$
$= MB + \overline{M}\,\overline{B}$
$= 1.B + \overline{1}.\overline{B}$
$= B$.

(b) Reflective codes are those in which the 'n' LSB bits of the code words 2^n through $2^{n+1}-1$ are the mirror images of the code words 0 through 2^n.

eg. Gray codes.

Decimal	Gray code
0	0000
1	0001
2	0011
3	0010
4	0110
5	0111
6	0101
7	0100
8	1100
9	1101
10	1111
11	1110
12	1010
13	1011
14	1001
15	1000

mirror

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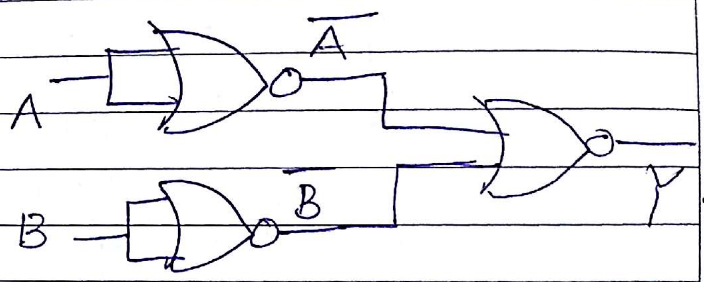
Q4) (a) $\boxed{Y = A \cdot B}$ after simplification using De-Morgan's laws

Using NOR.

$Y = \overline{\overline{A \cdot B}} = \overline{\overline{A} + \overline{B}}$



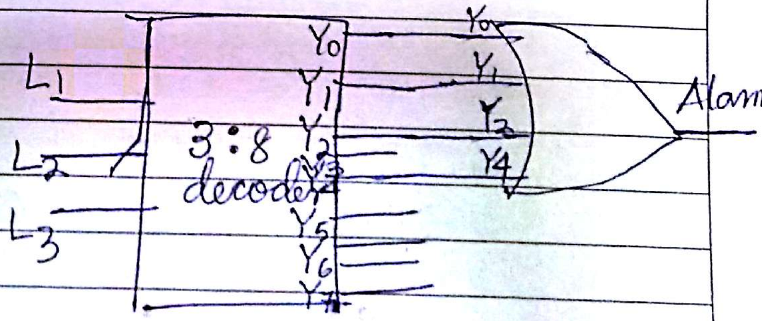
(b) → Carry Propagation Delay.
→ Using Look-Ahead Carry adder.

Q5) (a) Book. (given)

(b)

L_1	L_2	L_3	Alarm
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

$\therefore$ Alarm $= \Sigma m(0,1,2,4)$.



06

Q6) (a)

X (1010011) → Hamming code decoder → A = 0011

$P_1 P_2 D_3 P_4 D_5 D_6 D_7$

check error

$P_1 \oplus D_3 \oplus D_5 \oplus D_7 = 1 (C_1)$

$P_2 \oplus D_3 \oplus D_6 \oplus D_7 = 1 (C_2)$

$P_4 \oplus D_5 \oplus D_6 \oplus D_7 = 0 (C_3)$

Error at position $C_3C_2C_1 = (011)_2 = 3rd$.

Corrected code.

$= 1000011$

$P_1 P_2 D_3 P_4 D_5 D_6 D_7$

Y 1100101 → Hamming code decoder. B = 0101

$$\begin{array}{r} 0011 \\ +0101 \\ \hline 1000 \end{array}$$

C = 1000

$D_3 D_5 D_6 D_7$

→ Encoder.

Similarly,

$C_1 = 1 \oplus 0 \oplus 1 \oplus 1 = 1$

$C_2 = 1 \oplus 0 \oplus 0 \oplus 1 = 0$

$C_3 = 0 \oplus 1 \oplus 0 \oplus 1 = 0$

$C_3 C_2 C_1$

$= (001)_2 = 1st$

Corrected code = 0100101

Z =

$P_1, 1, 0, 0$ (even parity)

$\therefore P_1 = 1$.

$P_2, 1, 0, 0$ (even pari)

$\therefore P_2 = 1$.

$P_4, 0, 0, 0$ (")

$\therefore P_4 = 0$.

$\therefore \boxed{Z = 1110000}$

(b) $m_i = \overline{M_i}$.

Let $\cancel{M_2} = A + \overline{B} + C$

$ 0 \; 1 \; 0$

$\overline{M_2} = \overline{A + \overline{B} + C}$ (Apply De Morgan's law)

$= \overline{A} \cdot B \cdot \overline{C}$

$ 0 \; 1 \; 0$

$= m_2$