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EXPERIMENT-7

AIM - Design and simulation of a pseudo random sequence generator in Verilog. Implementation of pseudo random sequence generator using shift register.

COMPONENT/ SOFTWARE USED -

Component / Software	Specification
• ICs	7495, 7486
• Breadboard, Power Supply, LEDs, Resistors, Switches, Connecting wires	As per requirement
• Software (s) used	Vivado 2016.1

THEORY -

A register is a storage device that holds a number of bits. By connecting flip flops, we can create a shift register capable of moving binary information in a selected direction. Shift registers are synchronous circuits that transfers data from one flip flop to another when triggered by a clock pulse. They can shift data left or right, forming either left or right shift registers. An n bit register comprises n flip flops storing binary data, along with combinational gates for data processing. Flip flops store the information, while gates control how its transferred into the register.

Serial In - Serial Out :

The circuit shown in figure 7.1 represents a 4 bit serial in serial out (SISO) shift right register using four D flip flops. Each flip flop's Q output is connected to the D input of the

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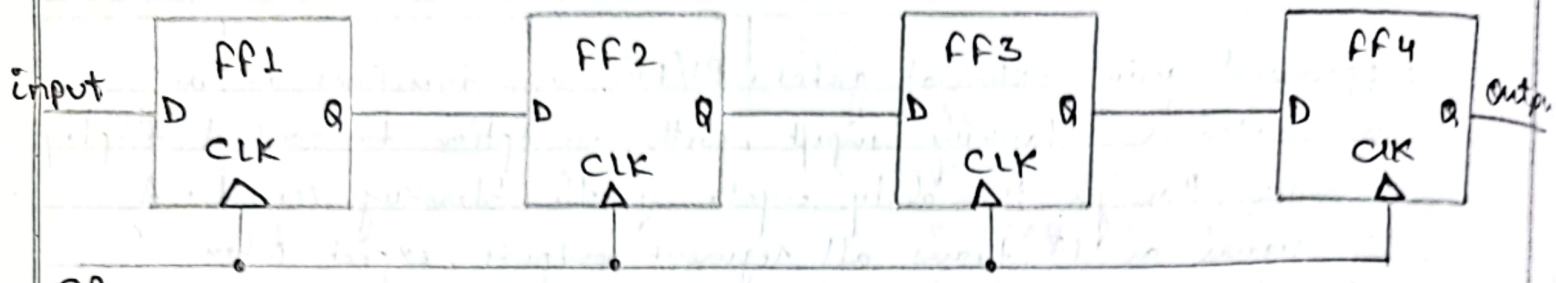
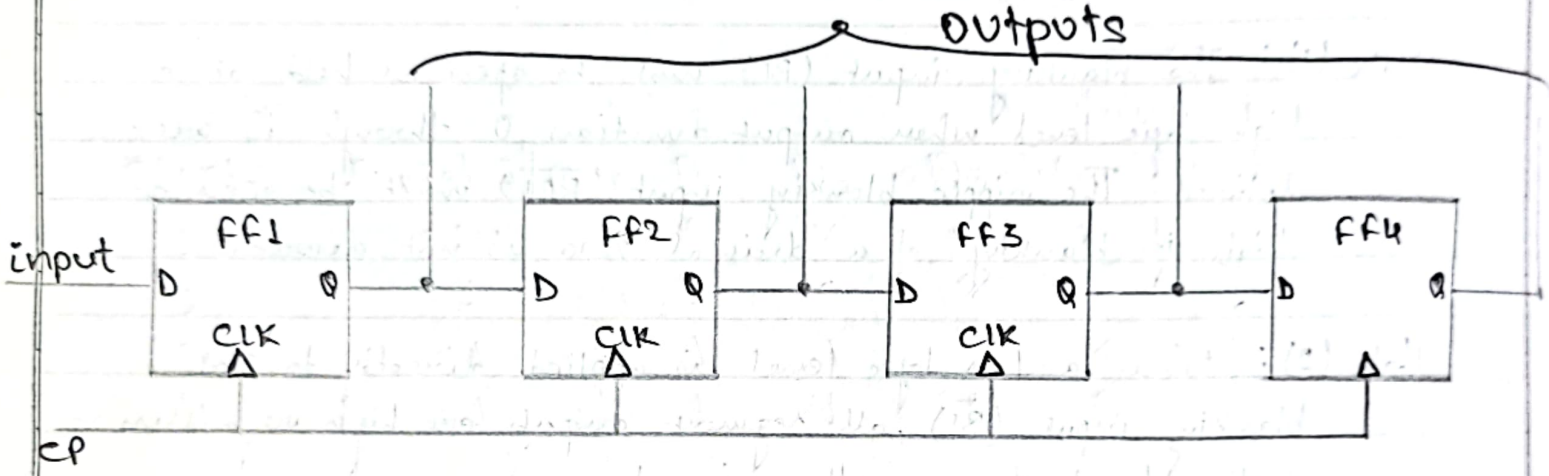


Logic Diagram of 4-bit SISO shift register



Logic Diagram of PIPO shift register

Clock	Serial I/P	Q_1	Q_2	Q_3	Q_4
1	= 0	0	X	X	X
2	= 1	1	0	X	X
3	= 1	1	1	0	X
4	= 1	1	1	1	0
5	X	X	1	1	1
6	X	X	X	1	1
7	X	X	X	X	1

Truth Table of 4-bit SISO Shift register

next flip flop allowing data to be shifted through the register with each positive edge of the clock pulse. The shifting process for a 4 bit data 'B3B2B1B0' occurs over four clock pulses and the specific shifts for each clock pulses are summarized in table 7.1. For example, if the initial 4 bit data is "1110", during the first clock pulse, B0 is shifted to Q1 (FF1). During subsequent clock pulses, the other bits are successively shifted to their corresponding flip flops. The data applied serially at the input eventually emerges serially at Q4 (FF4).

→ Parallel In Parallel Out

The data is loaded in parallel and read from the register in parallel i.e all bits are loaded simultaneously and read simultaneously. Figure 7.2 shows the circuit of a 4 bit parallel in parallel out (PIPO) shift right register using four D flip flops. The data in each flip flop is shifted to the output the arrival of a positive edge of a clock pulse. ~~Outputs~~ Output pulses. Output terminals and data are available at all of them together. The parallel data bits are $B_0B_1B_2B_3$ and $Q_1Q_2Q_3Q_4$ are the parallel data outputs. After one clock pulse, all the input data is available in the outputs.

→ Serial In Parallel Out

The data is loaded into the register serially but in parallel mode, i.e, data is available from all flip flops simultaneously. Figure 7.3 shows the circuit of a 4 bit serial in parallel out (SIPO) shift right register using four D flip flops. The Q outputs of one state are connected to the D input of the next input.

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Clock	Serial I/P	Q_1	Q_2	Q_3	Q_4
1	= 0	0	X	X	X
2	= 1	1	0	X	X
3	= 1	1	1	0	X
4	= 1	1	1	1	0

Truth Table of 4-bit SIPO Shift register

Clock	Parallel I/P	Q_1	Q_2	Q_3	Q_4
1	= 1110	1	1	1	0
2		X	1	1	1
3		X	X	1	1
4		X	X	X	1

Truth Table of 4-bit PISO Shift register

Thus, the inputs to second, to the third and fourth flip flops are conditioned by their preceding flip flops. The data in each flip flops is shifted to the next flip flop on the arrival of a positive edge of the clock pulse. Output terminals and data are available at all of them together. Since, it is a 4 bit register, after 4 clock pulses we see all the domains and data is available in the data of the outputs of this register.

The data shifting in 4 bit SIPO is summarized below in the table 7.2 with an example of a 4 bit data "1110". Load the shift register with a 4 bit data '$B_3 B_2 B_1 B_0$' one by one serially. In the 1st clock pulse, B_0 is shifted to Q_1 (FF1). In the 2nd clock pulse, B_0 is shifted to Q_2 (FF2) and B_1 is shifted to Q_1 (FF1). In the 3rd clock pulse, B_0 is shifted to Q_3 (FF3), B_1 is shifted to Q_2 (FF2) and B_2 is shifted to Q_1 (FF1). At the end of 4th clock pulse, B_0 is shifted to Q_4 (FF4), B_1 is shifted to Q_3 (FF3), B_2 is shifted to Q_2 (FF2) and B_3 is shifted to Q_1 (FF1). Thus after 4th clock pulse all the outputs are available.

→ Parallel In Serial Out

The data is loaded in parallel forms and read serially. Figure 7.4 shows the circuit of a 4 bit parallel in serial out (PISO) shift register with four bits. It uses D flip flops and four data input lines: B_0 (LSB), B_1, B_2 and B_3 (MSB).

The data shifting in the 4 bit PISO is summarized below in the table 7.3 with an example of 4 bit data "1110". Load the shift register with a 4 bit data '$B_3 B_2 B_1 B_0$' simultaneously in the

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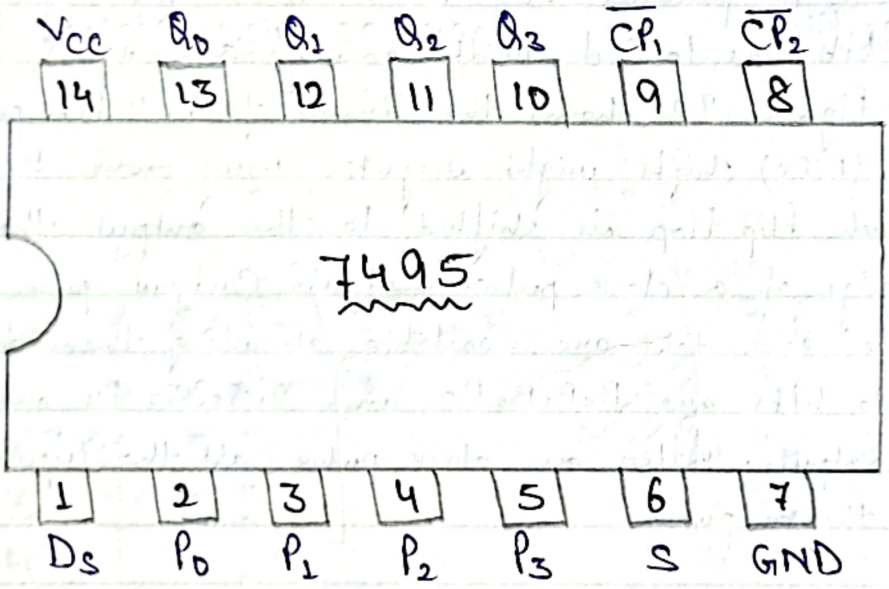
Pin No.	Pin Name	Pin Description
1	D_S	Serial Data i/p
2 to 5	P_0 to P_3	Parallel Data i/p 0 to 3
6	S	Mode control i/p
7	GND	Ground Pin
8		-ve edge parallel clk i/p
9		-ve edge serial clk i/p
10 to 13	Q_3 to Q_0	Parallel outputs 3 to 0
14	V_{CC}	Supply voltage

Pin Description of IC 7495



Pin Diagram of IC 7495

1st clock pulse. In the 2nd clock pulse, B_3 is shifted to Q_2 (FF2), B_2 is shifted to Q_3 (FF3) and B_1 is shifted to Q_4 (FF4). In the 3rd clock pulse, B_3 is the shifted to Q_3 (FF3) and B_2 is shifted to Q_4 (FF4). At the end of the 4th clock pulse B_3 is shifted to Q_4 (FF4).

- IC7495

The IC7495 is a 4 bit shift register offering both serial and parallel synchronous operating modes. It has a mode control input (S) and two clock inputs (CP1 and CP2) that enable either serial (right shift) or parallel data transfers during the transition from a HIGH to LOW state of the selected clock input. When S=1, overline CP2 is enabled, allowing parallel data transfer from P_0 to P_3 to Q_0 to Q_3 during the HIGH to LOW transition. Conversely, when S=0, overline CP1 is enabled, and a HIGH to LOW transition enables data transfer from the serial input DS to Q_0 with subsequent shifting from Q_0 to Q_1, Q_1 to Q_2 and Q_2 to Q_3. For left shift operation, connecting Q_3 to P_2, Q_2 to P_1 and Q_1 to P_0 and setting S=1 achieves the desired mode. Its important to note that changes in the state of S should occur only when both clock inputs are LOW to ensure normal operation.

Pseudo Random Sequence Generator

The sequence generator digital circuit which generates a set of outputs. This is a shift register whose the input is a combinational logic function of the outputs of the flip flops of the shift register. The sequence generator generates a sequence of binary bits. Thus, the length of the sequence is related to the numbers of flip flops that are required to design a sequence generator.

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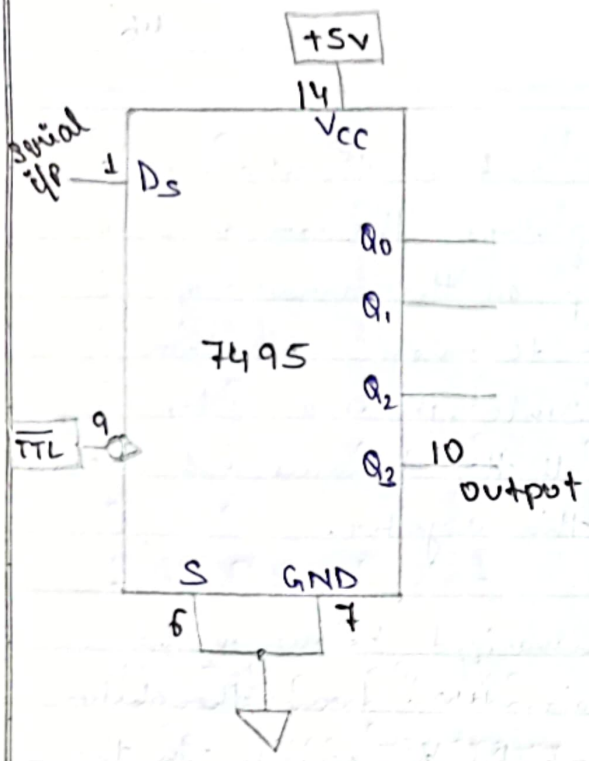
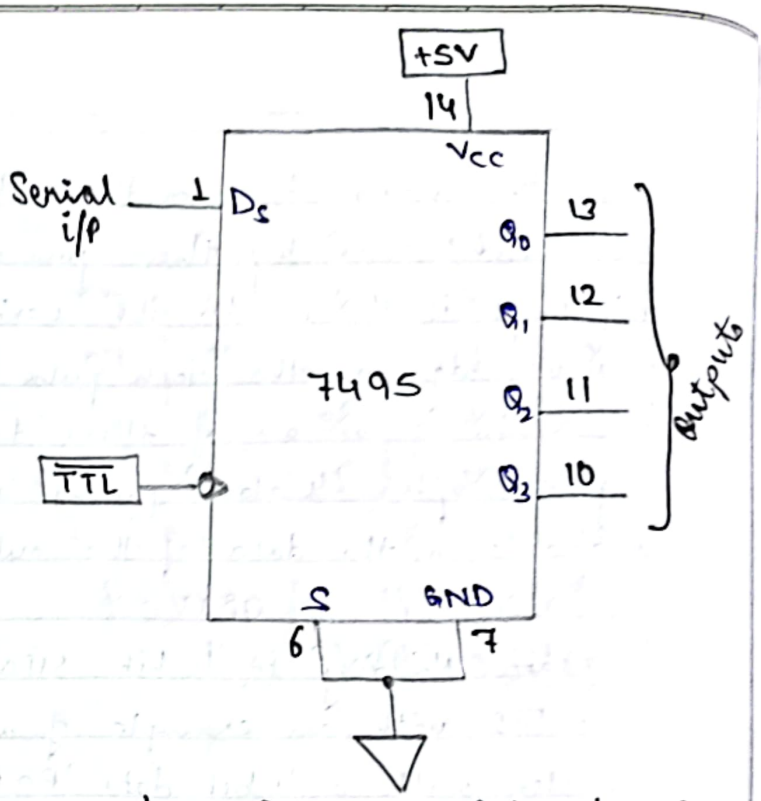
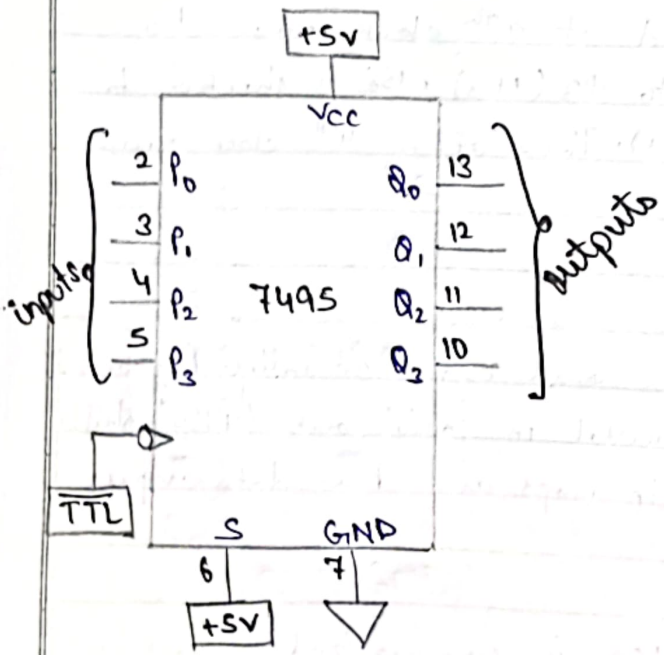


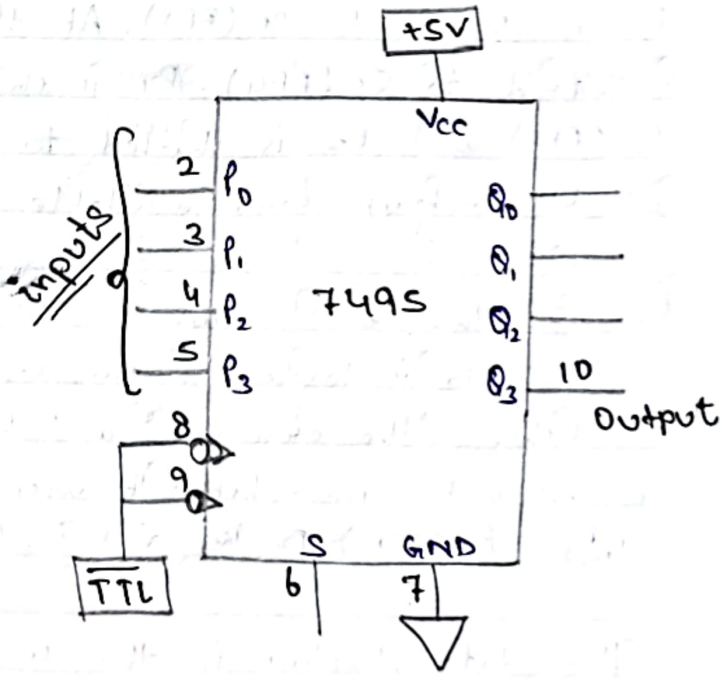
Logic Diagram of 4-bit SISO Shift register using IC 7495



Logic Diagram of 4-bit SIPO Shift register using IC 7495



Logic Diagram of 4-bit PIPO Shift register using IC-7495



Logic Diagram of 4-bit PISO Shift register using IC-7495

These generators are utilized in a wide variety of applications like coding and control. The length of the sequence is related to the number of flip-flops that are required to produce a sequence generator.

$$L \leq 2^n - 1$$

where L is the length of the sequence and n is the min number of of flip flops required.

Procedure

- For software simulation.

(a) Create a module with required number of variables and mention its input/output.

(b) Write the description of given Boolean function using operators or by using the built in primitive gates.

(c) Synthesize to create RTL schematic.

(d) Create another module referred as test bench to verify the Functionality and to obtain the waveform of input and output

(e) Follow the steps required to simulate the design and compare the obtained output with the corresponding truth table.

(f) Take the screenshots of the RTL schematic and simulated waveforms.

- For hardware implementation.

(a) Turn off the power of the trainer kit before constructing any circuit.

(b) Connect power supply (+5V DC) pin and ground pin to the respective pins of the trainer kit.

(c) Place the ICs properly on the bread board in trainer kit.

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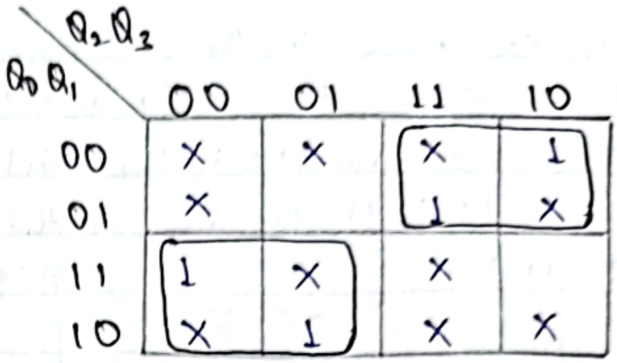
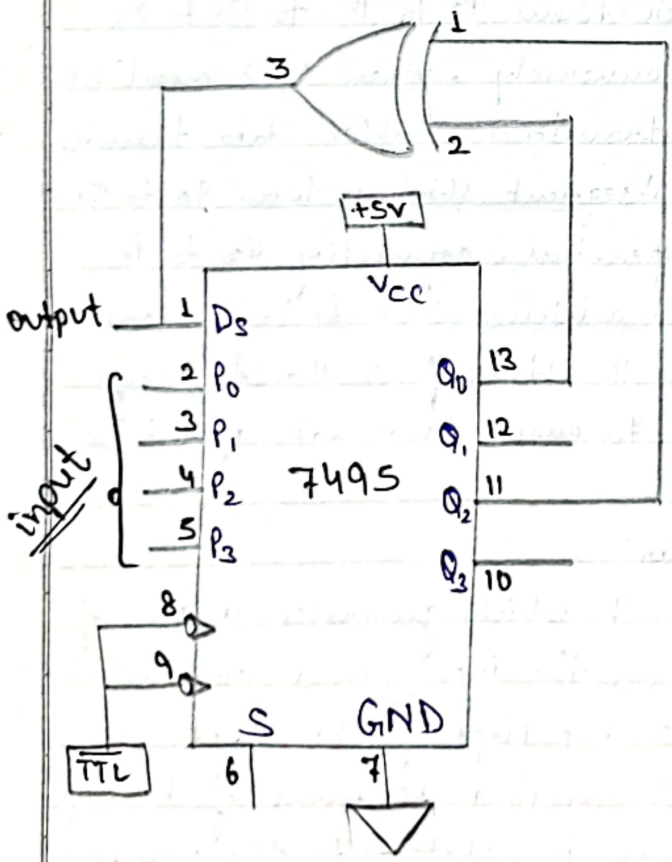
Q_0	Q_1	Q_2	Q_3	Q_4
1	1	0	0	1
1	1	1	0	0
0	1	1	1	1
1	0	1	1	0
0	1	0	1	0
0	0	1	0	1
1	0	0	1	1

Truth Table of the Sequence Generator



K-map for the input (D_3) of the Shift register



Logic Diagram of "1101001" sequence Generator using IC-7495

Clock Pulse	Q_1	Q_2	Q_3	Q_4
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0

Truth Table of 4-bit Ring Counter

(d) Connect Vcc and GND pins of each chip to the power supply and ground bus strips on the bread board.

(e) Connect the input and output pins of chips to the input switches and output LEDs respectively in the trainer kit.

(f) Check the connections before you turn on the power.

(g) Apply various combinations of inputs according to truth tables and observe outputs of LEDs.

- Design Source Code

```
module PNSeqGen(input clk, reset, output q3);
    reg q0, q1, q2, q3;
    wire ds;
    assign ds = q2^q0;
    always @(posedge clk)
    begin
        // initial state should not be 0000 => 1100
    if (reset) begin
        q0 <= 1;
        q1 <= 1;
        q2 <= 0;
        q3 <= 0;
    end else begin
        q0 <= ds;
        q1 <= q0;
        q2 <= q1;
        q3 <= q2;
    end
end
endmodule
```

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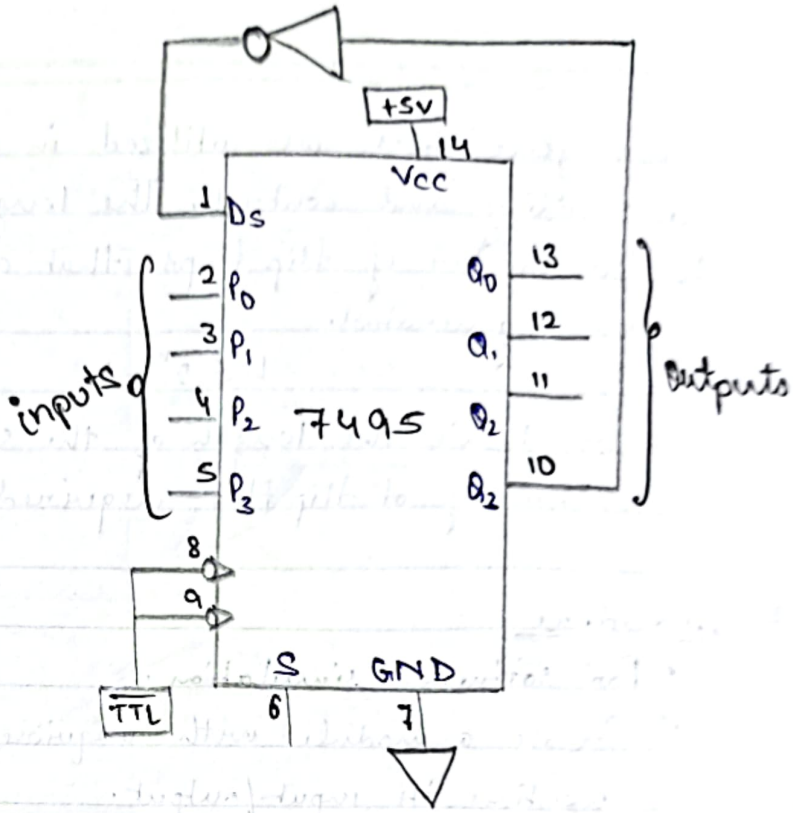
Clock Pulse	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Truth Table of 4-bit Johnson Counter



Logic Diagram of 4-bit Johnson Counter using IC 7495

Test bench Code

```
module Test_PNSeqGen;
    // inputs
    reg clk;
    reg reset;
    // outputs
    wire q3;
    // Instantiate the Unit Under Test (UUT)
    PNSeqGen uut (clk, reset, q3);
    initial begin
        // initial inputs
        clk = 0;
        reset = 0;
        // Wait 100 ns for global reset to finish
        #100;
        // Add stimulus here
        #10 reset = 1;
        #10 reset = 0;
        #200 $finish;
    end
    always begin
        #5 clk = ~clk
    end
endmodule
```

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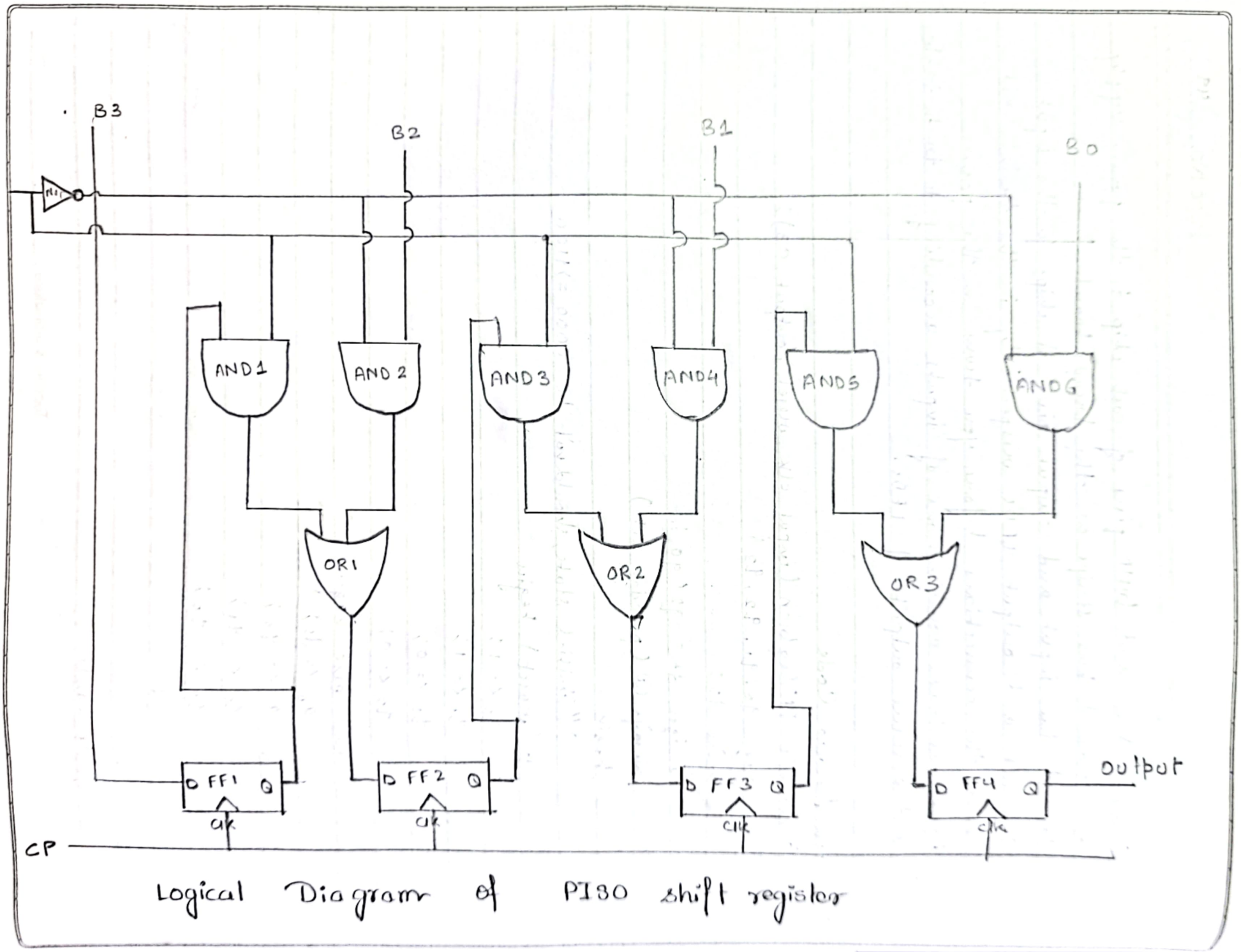

Logical Diagram of PISO shift register

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Design Problem

Design and simulation of 4 bit Ring Counter and 4 bit Johnson counter using Verilog HDL.

Hardware implementation of 4 bit Ring Counter and 4 bit Johnson counter.

Solution

- Ring counter:

Ring counter is a sequential logic circuit diagram that is constructed using shift register. Same data recirculates in the counter depending on the clock pulse. It consists of a group of flip flops connected in a circular chain or ring formation where the output of one flipflop is connected to the input of the next, and the last flip flop is connected back to the first.

When a clock pulse is applied to the ring counter, the data is shifted from one flip flop to the next, with each flip flop in the ring taking turns being in the high or low state. The output of each flip flop represents a different bit of the counters binary value, with the least significant bit (LSB) being the first flip flop in the ring and the most significant bit (MSB) being the last flip flop.

Assume initial states of the D flip flop from leftmost to rightmost is $Q_1\ Q_2\ Q_3\ Q_4$ = "1000". This states repeats for every four (4) clock pulse which is shown below in table 7.6. A 'mod n' ring counter will require 'n' number of flip flops connected together to circulate a single data bit providing n different output states. Each state repeats after every 'n' clock pulses.

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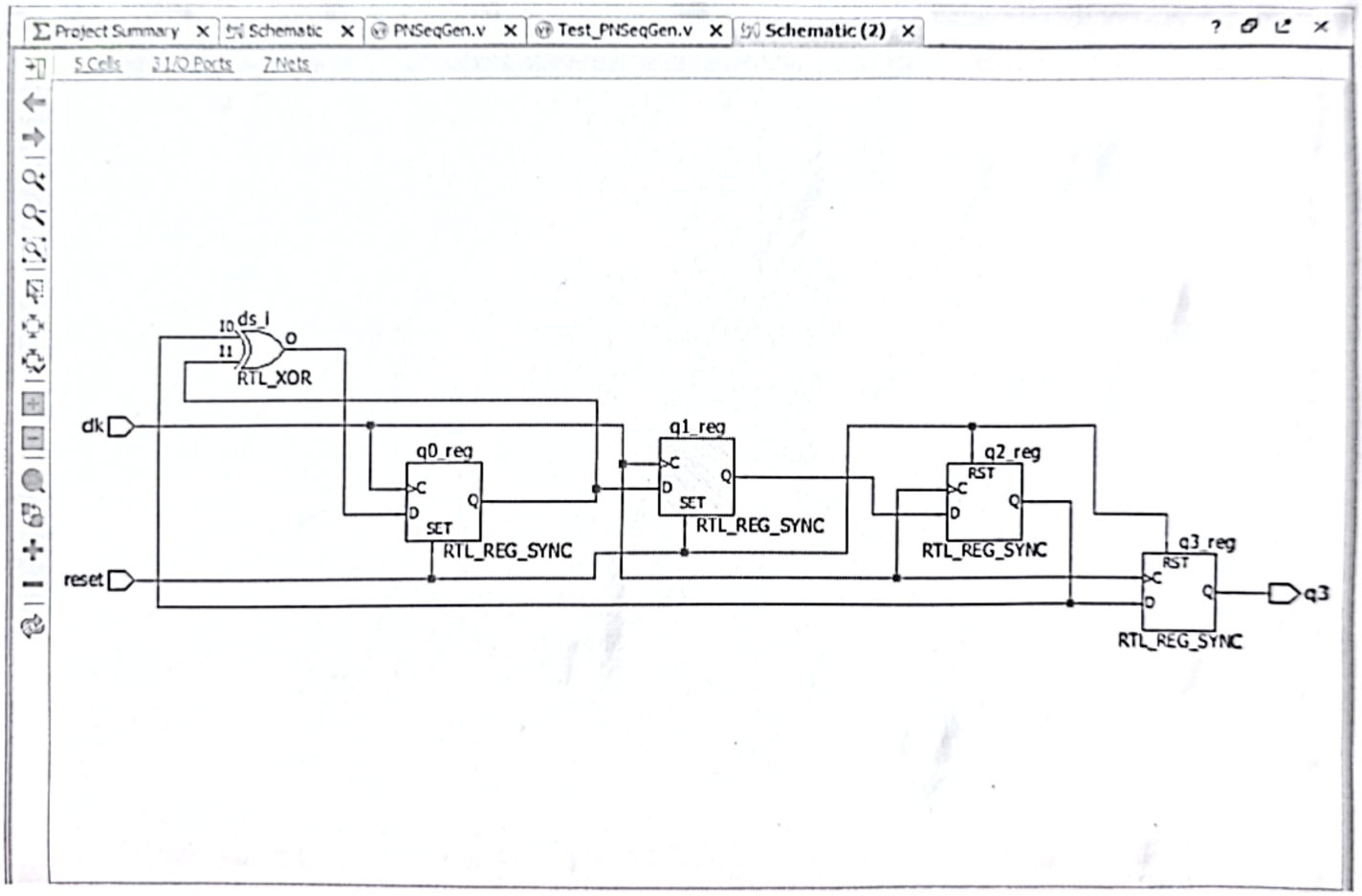

Schematic Diagram of Pseudo Random Sequence Generator

• Johnson Counter:

A Johnson Counter is a type of shift register that is similar to a ring counter, but with an additional inhert stage. It is sometimes also called a 'twisted ring counter' counter'. The operation of a Johnson counter is similar to that of a ring counter, with each flip flip output changing state on each clock pulse. However in Johnson counter, the output of the last flip flop is inverted and fed back into the first flip flop. This causes the counter to cycle through a sequence of states that includes both ascending and descending binary values.

Assume, initial status of the D flip flop from leftmost to rightmost is $Q_1 Q_2 Q_3 Q_4$ = "000". This status repeats for every Eight (8) clock pulse which is shown in below table 7.7.

A 'mod 2n' ring counter will require n number of flip flops connected together to circulate a single data bit providing '2n' different output states. Each state repeats after every '2n' clock pulse.

Conclusion

Design and simulation of a pseudo random sequence generator has been done and implemented successfully

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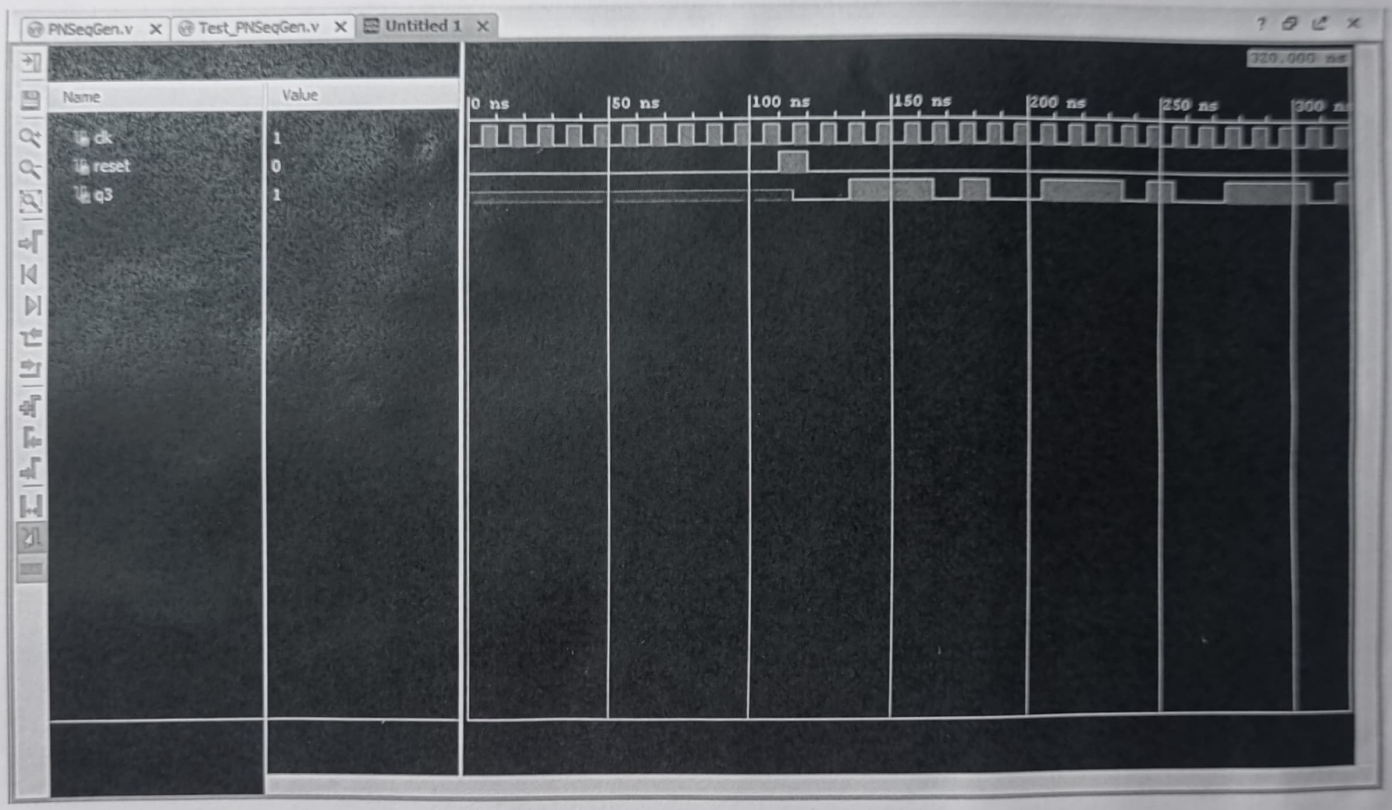

Waveform of Pseudo Random Sequence Generator