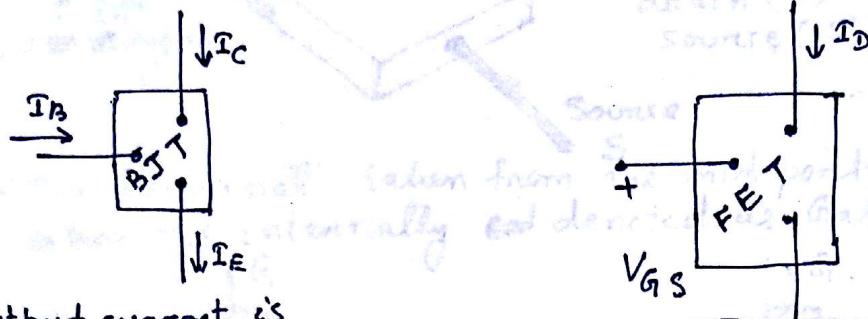


Field Effect Transistors

17

- BJT (Bipolar Junction Transistor) - The electrons & holes both are responsible for current flow.
- In FET either electron or hole is responsible for flow of current so called **Unipolar** device.

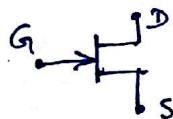


- Output current is controlled by i/p current I_B .
- So current controlled device
- Output current is controlled by input voltage V_{GS}
- So it is **Field Effect** means electric field or voltage controlled device.

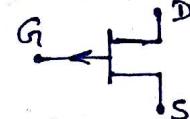
FET

Junction Field Effect Transistor (JFET)

N-channel JFET



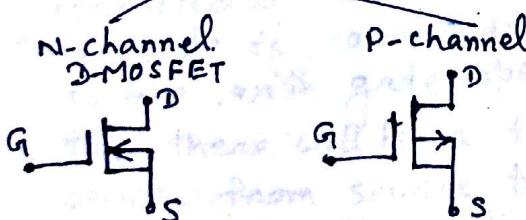
p-channel JFET



Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

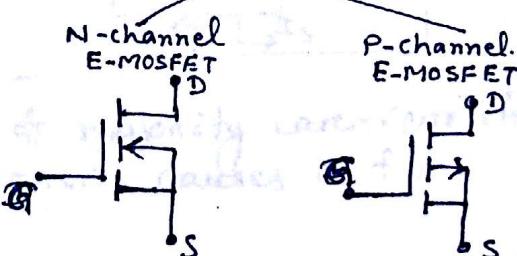
Depletion MOSFET (D-MOSFET)

N-channel D-MOSFET



Enhancement MOSFET (E-MOSFET)

N-channel E-MOSFET

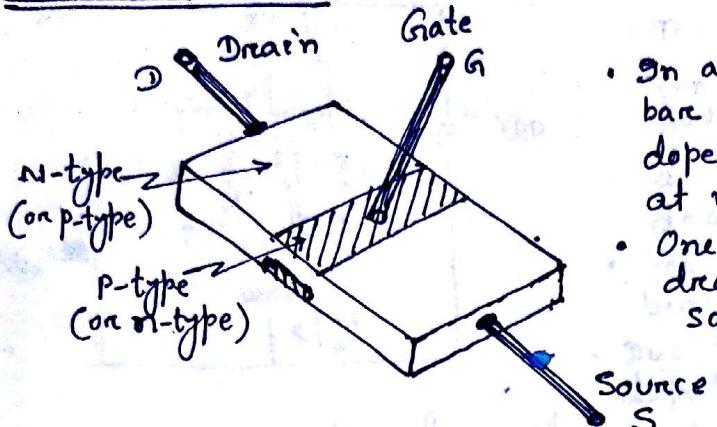


P-channel E-MOSFET

- Note MOSFET are the most important device used in design & used in construction of integrated ckt.
- MOSFET are primary device of VLSI design.

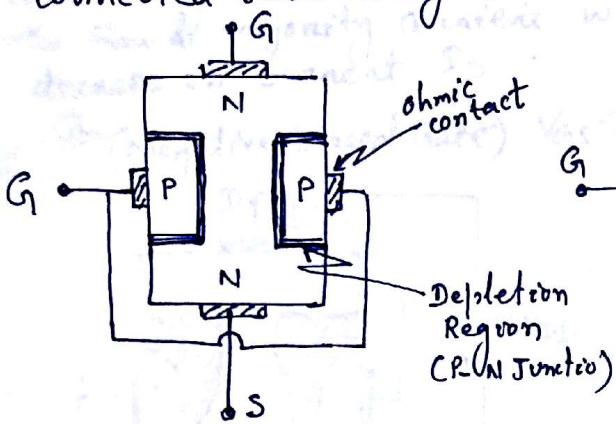
Structure of FET

(2)

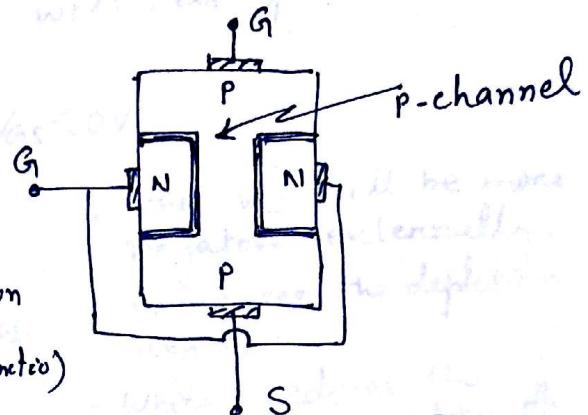


- On a N-type (or P-type) Silicon bar diffused with heavily doped p-type (or n-type) Silicon at mid portion.
- One end is denoted as drain (D) other end is source (S).

- The terminal taken from the mid portion which is connected internally and denoted as Gate (G).



[N-channel JFET]



[P-channel JFET]

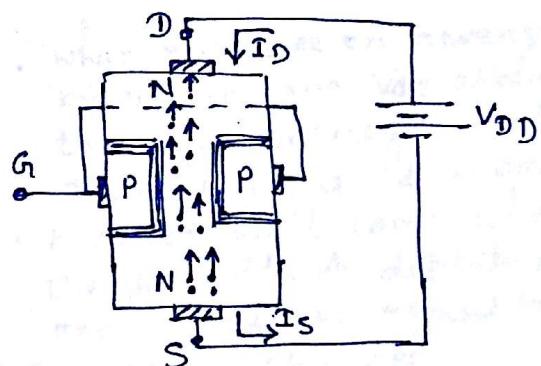
- The majority carriers from one side (called Source "S") to other side (called Drain "D").

Operation of JFET

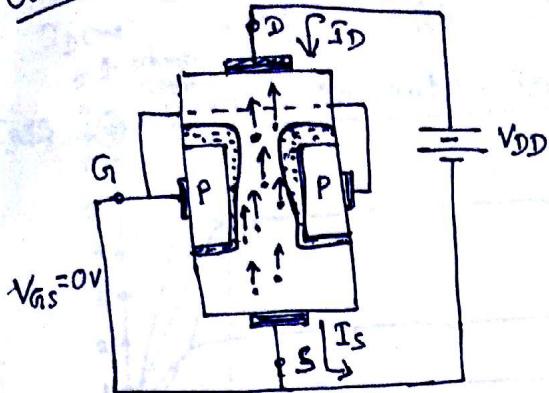
Case-I (Gate open)

when N-channel JFET

- is applied with external applied voltage ("V_{DD}"), +ve side is connected to Drain & -ve side is connected to Source, with gate open --
- Then there will be a flow of majority carriers (electrons) occurs from Source to drain, causes a flow of current $I_D = I_S$.
- where $I_D = \text{Drain Current} = I_S = \text{Source Current}$.
- The flow of majority carriers occurs through the passage between gate known as channel.
- The width of the channel can be varied by controlled by varying the gate voltage.



Case-II (No Bias Voltage to Gate) $V_{GS} = 0V$

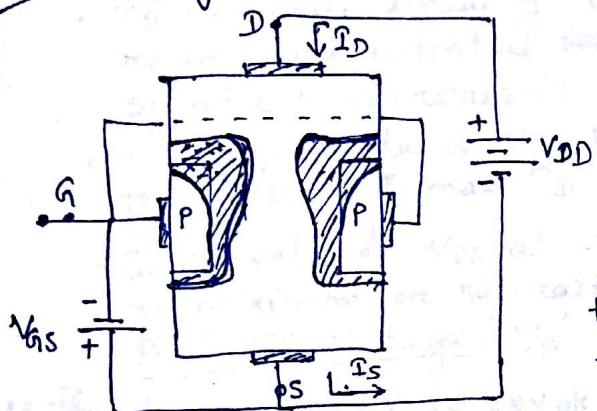


- The gate is directly connected to source, so gate & source both are at -ve potential w.r.t. drain.

- The P-N junction is reverse biased towards drain side.
- Due to gate is heavily doped the depletion region

spreads towards channel; which reduces the conducting path of the channel.
So flow of majority carriers will decrease gives rise to decrease in current I_D .

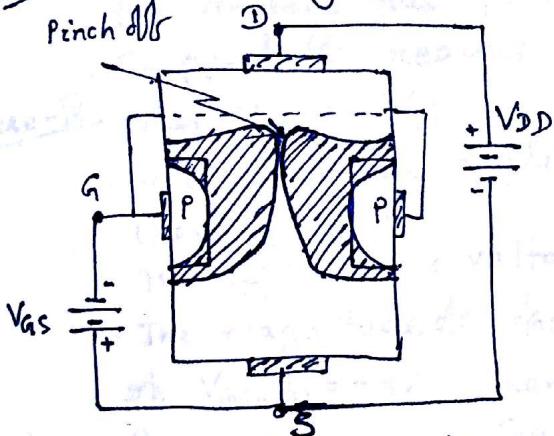
Case-III (Negative Biased Gate) $V_{GS} < 0V$



- When V_{GS} will be more negative externally, increases the depletion region.

- Which reduces the conducting portion of the channel, gives rise to reduction in I_D .

Case-IV (More Negative Biased Gate) $V_{GS} \ll 0V \approx V_{GS(\text{off})} \approx V_p$



- When increase in reverse biased voltage V_{GS} applied, the depletion region will increase more & more.

- A stage will come when the width of depletion region will be equal to width of channel.

- So the flow of current from drain to source will be zero. The V_{GS} is known as

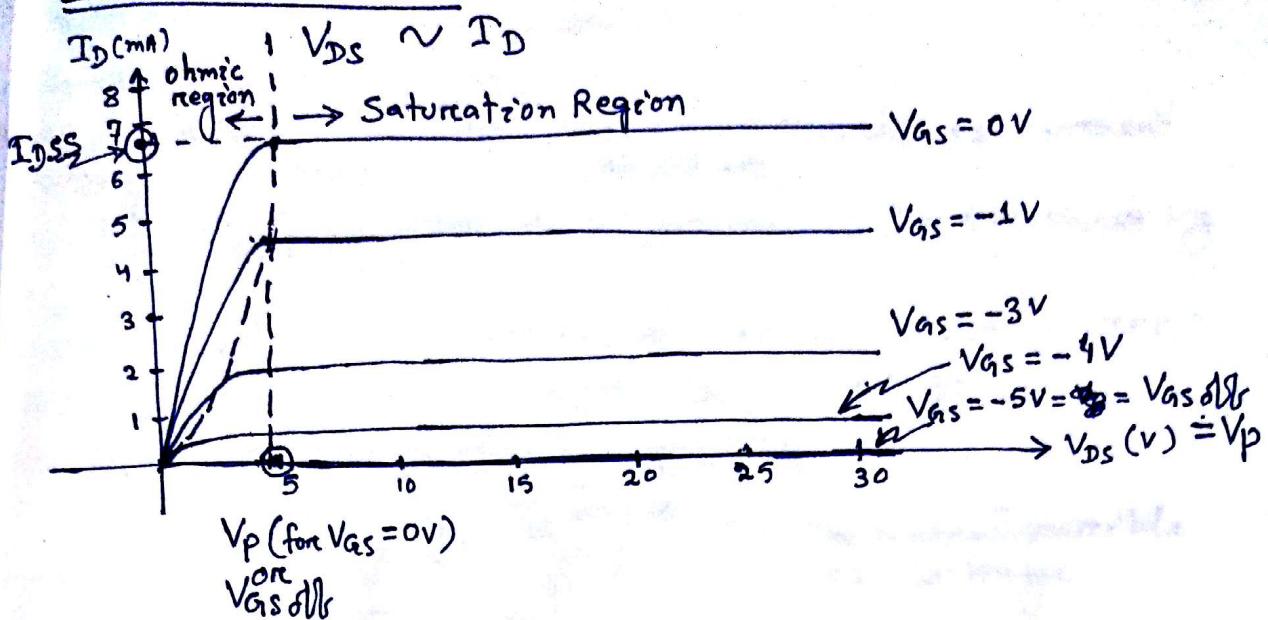
$V_{GS(\text{off})}$ or V_p (Pinch off voltage) at $V_{GS} = 0$.

Note But in reality there exist a small channel with a current of high density. So I_D does not drop off to zero level rather maintains a constant saturation level (maximum I_D current) known as

I_{DSS} . So I_{DSS} is maximum I_D at $V_{GS} = 0$ & $V_{DS} > V_p$ or at $V_{GS} \geq V_{GS(\text{off})}$.

V-I characteristic (Drain characteristic)

(4)



Case-I when $V_{GS} = V_{DS} = 0$, then $I_D = 0$

Case-II when $V_{GS} = 0$ with increase in V_{DS}

- I_D increases linearly but simultaneously the reverse bias potential difference increases, so rate of increase in I_D w.r.t. V_{DS} reduced.
- At certain value of V_{DS} pinch off occurs gives rise to a constant & max. I_D known as I_{DSS} .
- So the value of V_{DS} at which the current I_D flows in maximum or saturation level (I_{DSS}) called as Pinch OFF Voltage "V_p" at $V_{GS} = 0V$.

Case-III when $V_{GS} < 0V$ (-1V, -2V etc)

- The external applied -ve voltage increases the reverse bias potential difference more earlier.
- So pinch off reaches at a lower drain current.

Case-IV when $V_{GS} = -|V_p|$

- when external applied -ve voltage $V_{GS} = -|V_p|$ then $I_D = 0$.
 - The applied -ve voltage is called $V_{GS(\text{off})}$
 - The magnitude of $V_{GS(\text{off})}$ is $|V_p|$.
- if $V_{GS(\text{off})} = -4V$ then $V_p = -4V$

Ohmic Region

- Here the I_D varies with V_{DS} .
- The JFET behave as voltage variable resistance.

Saturation Region

- Hence the I_D remains constant with varying V_{DS} .
- FET operated in this saturation region.

Transfer characteristic

in BJT

$$I_C = \beta I_B$$

constant

The control variable is current.

It is a linear

relationship means if I_B doubles the I_C increases by a factor of two.

- But there is no linear relationship occurs in JFET
- The relation between I_D & V_{GS} defined by

Shockley's Equation

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Constant

The control variable is voltage.

- Transfer characteristic is a curve between $V_{GS} \sim I_D$

How to draw Transfer characteristic?

When $V_{GS} = 0$

$$I_D = I_{DSS} \left(1 - \frac{0}{V_P}\right)^2 = I_{DSS} (1 - 0)^2 = I_{DSS} (1 - 0)^2$$

$$\Rightarrow I_D = I_{DSS}$$

when $V_{GS} = V_P$

$$I_D = I_{DSS} (1 - 1)^2$$

$$\Rightarrow I_D = 0 A$$

when $V_{GS} = V_P/2$

$$I_D = I_{DSS} \left(1 - \frac{V_P/2}{V_P}\right)^2 = I_{DSS} \left(1 - \frac{1}{2}\right)^2$$

$$\Rightarrow I_D = \frac{I_{DSS}}{4}$$

when $I_D = I_{DSS}/2$

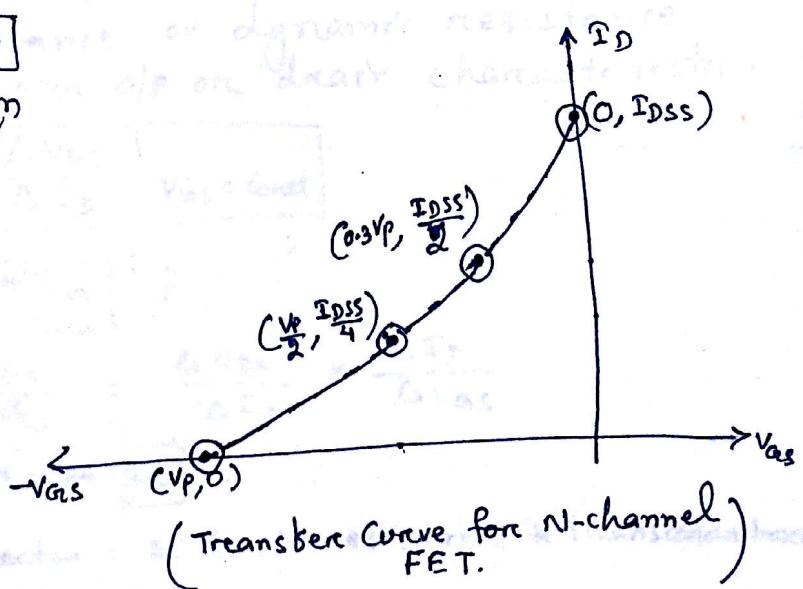
$$V_{GS} = V_P \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) = V_P \left(1 - \sqrt{\frac{I_{DSS}/2}{I_{DSS}}}\right) = V_P (1 - \sqrt{0.5})$$

$$\Rightarrow V_{GS} = 0.3 V_P$$

Finally

$V_{GS} \sim I_D$ from Shockley's Eqn

V_{GS}	I_D
0	I_{DSS}
$0.3 V_P$	$I_{DSS}/2$
$V_P/2$	$I_{DSS}/4$
V_P	0



(6)

Transconductance (g_m)

- g_t is the ratio of change in drain current to change in Gate to Source Voltage with constant drain to source voltage.
- Denoted by g_m .

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \quad | \quad V_{DS} = \text{const.}$$

- g_m is also called as mutual conductance.
- g_t 's unit is mS or mA/V
- The value of g_m at $V_{GS} = 0\text{V}$ is called as g_{m0} .

$$g_{m0} = \frac{2 I_{DSS}}{V_p}$$

So $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$

$$\Rightarrow \Delta I_D = 2 I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right) \left(-\frac{1}{V_p}\right) \Delta V_{GS}$$

$$\Rightarrow \frac{\Delta I_D}{\Delta V_{GS}} = \left(-\frac{2 I_{DSS}}{V_p}\right) \left(1 - \frac{V_{GS}}{V_p}\right)$$

$$\Rightarrow g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_p}\right)$$

Amplification Factor (μ)

- g_t is the ratio of change in V_{DS} with change in V_{GS} with constant I_D .

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \quad | \quad I_D = \text{const.}$$

Drain Resistance (r_d)

• r_d is ac resistance or dynamic resistance can be calculated from op or drain characteristic.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \quad | \quad V_{GS} = \text{const.}$$

(Q) Prove $\mu = r_d * g_m$?

Ans. $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} * \frac{\Delta I_D}{\Delta V_{GS}}$

$$\Rightarrow \mu = r_d * g_m$$

So Amplification factor = AC drain resistance \times transconductance

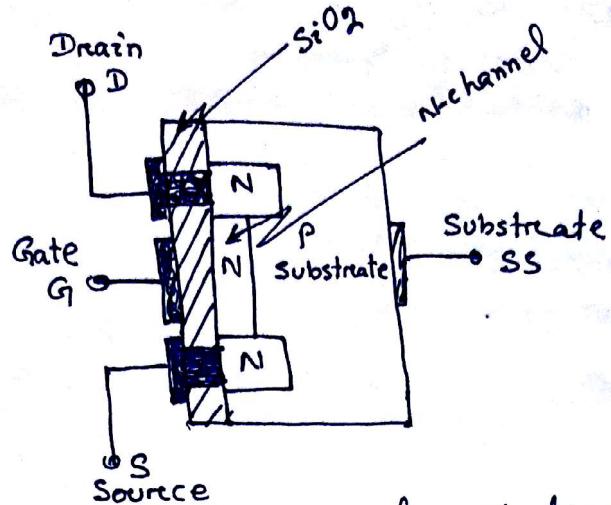
Depletion MOSFET

(D-MOSFET)

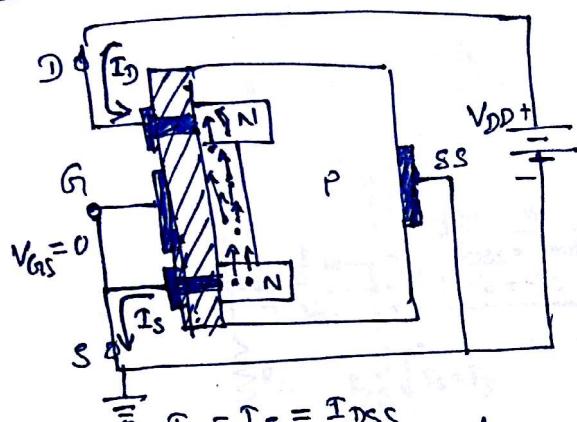
8

Construction

- Two highly doped N-region diffused into a lightly doped p-type substrate.
- One is represented as source another as drain.
- The source & drain is linked by N-channel.
- The drain & source terminal is directly in contact through metallic contacts.
- Gate terminal is insulated from the N-channel by a thin SiO_2 layer (which is a dielectric).
- Due to this insulating layer SiO_2 MOSFET gives high Input Impedance.
- The other name is Insulated Gate FET (IGFET).



Operation



- At a sufficient amount of V_{DS} the I_D will be constant or saturated called I_{DSS} . The Voltage V_{DS} is called Pinch-off Voltage "Vp".

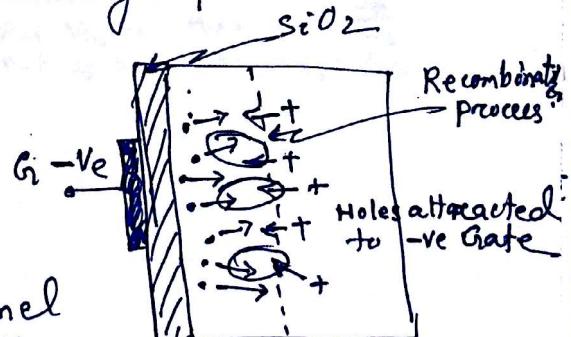
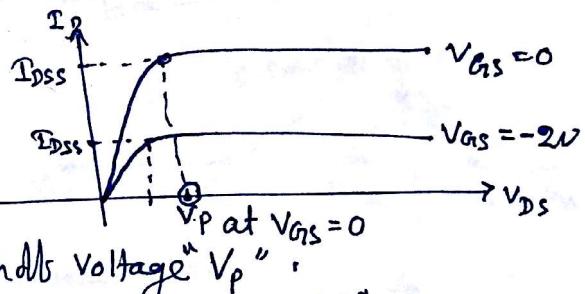
• When V_{GS} will be -ve the N-channel will be induced with -ve potential to repel the electrons & attract the holes.

• which starts the recombination process.

• By which the N-channel is depleted of electrons, thus decreasing the channel conductivity.

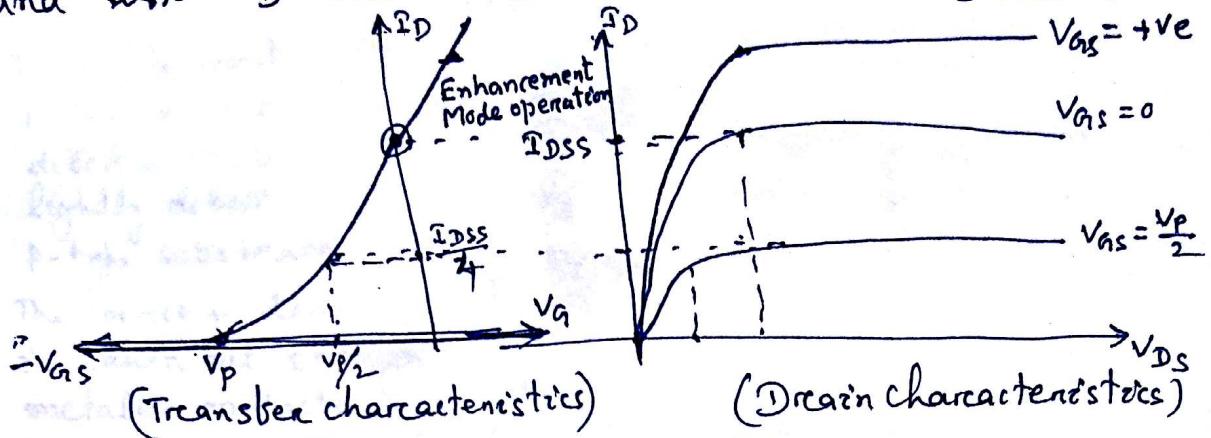
• which decreases the I_D current.

- When external voltage V_{DD} applied keeping $V_{GS} = 0$ the free electrons drifted towards +ve terminal, which is drain.
- This establishes a current $I_D = I_S = I_{DSS}$ at $V_{GS} = 0$



• When V_{GS} is applied with +ve potential additional electrons drawn from P-type substrate due to reverse leakage which establishes new carriers through collisions between accelerating particles.

• Due to this the V_{GS} increases to +ve direction and also I_D increases. Enhancement Mode operation of D-MOSFET.

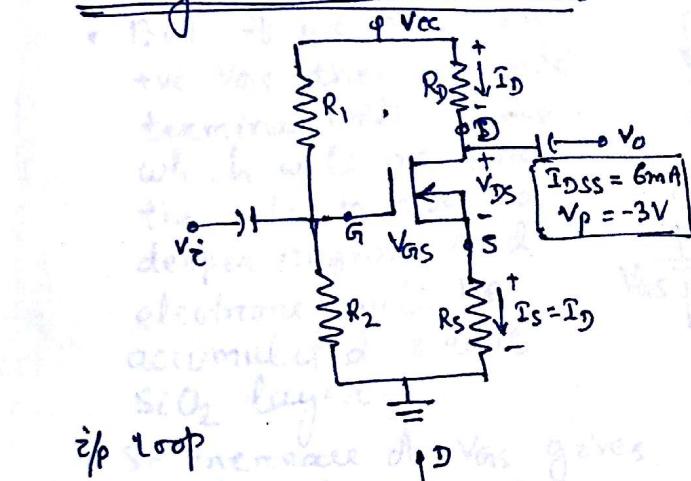


It follows the Shockley's Eqⁿ

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^n$$

Saturation

Voltage Divider Biased



$\frac{R_2 V_{DD}}{R_1 + R_2} = V_G$

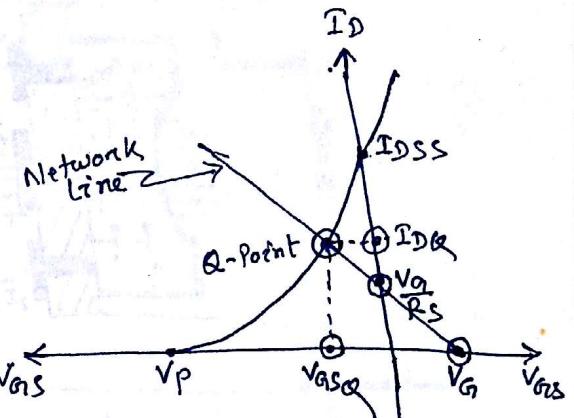
$$\frac{R_2 V_{DD}}{R_1 + R_2} = V_G$$

$$V_G - V_{GS} - I_D R_S = 0$$

$$\Rightarrow V_{GS} = V_G - I_D R_S$$

O/P Loop

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$



for network line

$$\text{Put } V_{GS} = 0 \text{ then } I_D = \frac{V_G}{R_S}$$

$$\text{Put } I_D = 0 \text{ then } V_{GS} = V_G$$

Enhancement - MOSFET

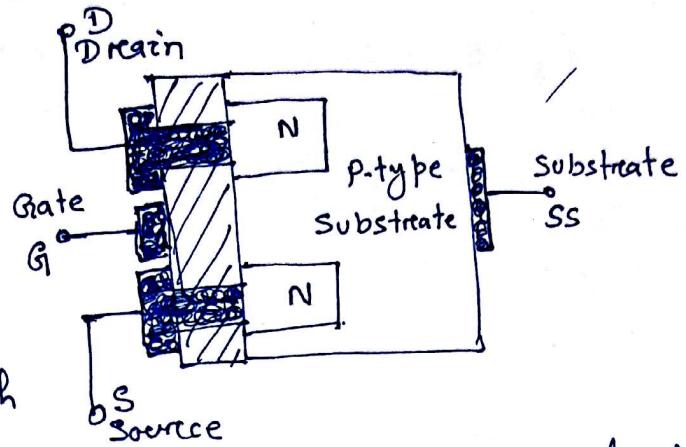
(E-MOSFET)

(10)

- The construction is similar to that of D-MOSFET except the channel between drain to source.
- The transfer characteristic is not defined by Shockley's equation.

Construction

- Two highly doped n-regions are diffused into lightly doped p-type substrate.



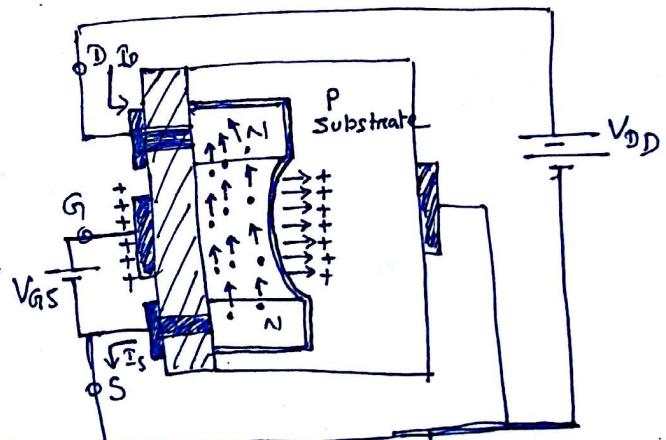
- The source & drain is taken out through metallic contacts.

- There is no physical channel present between drain & source.

Operation

- If we apply V_{DS} through an external voltage there will be practically zero current flow occurs due to absence of channel.

- But if we apply a +ve V_{GS} then the gate terminal will be +ve which will pressure the holes to move to deeper region and electrons will be accumulated near SiO_2 layer.

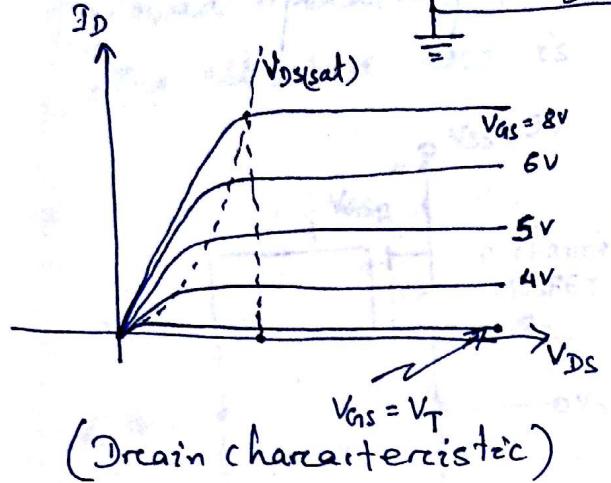
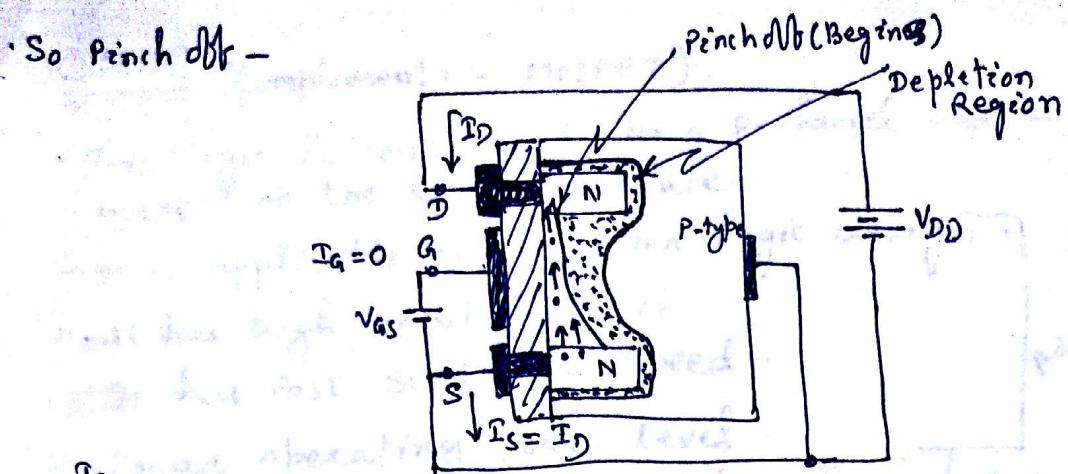


- So increase of V_{GS} gives a channel is created near SiO_2 layer, which gives rise to a current flow from drain to source.
- The level of V_{GS} at which there is a significant increase in drain current is called "Threshold Voltage" V_T .
- Since there is no channel exists at $V_{GS} = 0$ & at +ve V_{GS} the channel is "enhanced" So it is called E-MOSFET.

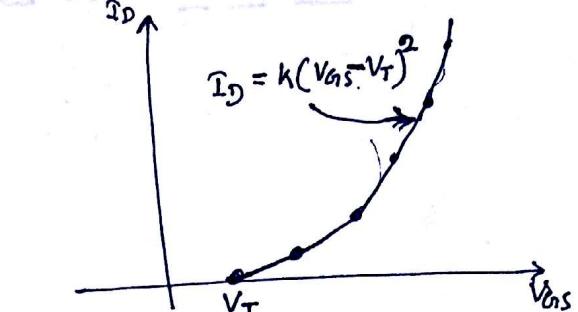
Pinch off at E-MOSFET ($V_{GS} = \text{constant with increase in } V_{DS}$)

- After a constant level of V_{GS} if it held constant and increasing the voltage V_{DS} the depletion region increases at drain side gives rise to a saturation level of I_D .

• So Pinch off -



(Drain characteristic)



(Transfer characteristic)

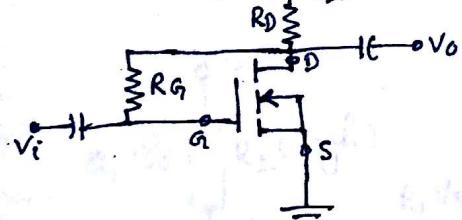
For $V_{GS} > V_T$ the relation bet'n drain current & V_{GS} is non-linear, given by

$$I_D = K (V_{GS} - V_T)^2$$

where K = Constant is a function of construction device.

$$K = \frac{I_D(\text{ON})}{(V_{GS(\text{ON})} - V_T)^2}$$

Popular type - Feedback Biasing



Due to $I_{DG} = 0$, $V_{RG} = 0$, a direct connection exist between drain & gate.

$$\text{So } V_D = V_G$$

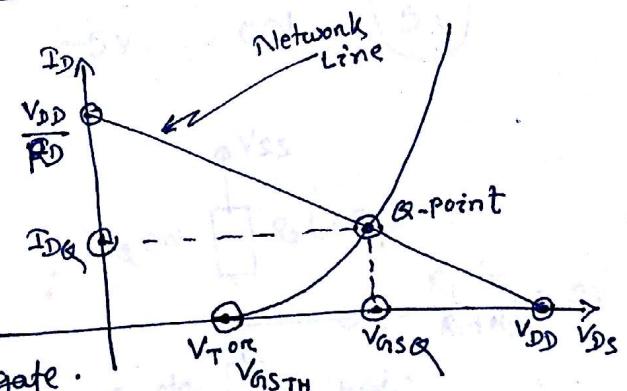
$$\Rightarrow V_{DS} = V_{GS}$$

of loop

$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$\Rightarrow V_{DS} = V_{DD} - I_D R_D$$

$$\Rightarrow V_{GS} = V_{DD} - I_D R_D$$



For network line

$$\text{Put } V_{GS} = 0, \text{ then } I_D = \frac{V_{DD}}{R_D}$$

$$\text{Put } I_D = 0, \text{ then } V_{GS} = V_{DD}$$