

EXPERIMENT - 6

■ AIM- Design and simulation of modulo counter using Verilog behavioural modelling. Design modulo counter using JK Flip Flops

■ Component / Software Used

Component / Software	Specification
• ICs	7476, 7408, 7490, 7447
• Bread board, power supply, LEDs, Resistors, Switches,	As per requirement
Connecting wires	
• Software's used	Vivado 2016.1

■ Theory

Flip Flop

A counter is one of the most beneficial and adaptable components of a digital system. The number of clock cycles can be counted using a counter that is powered by a clock. The function of a counter is to count the number of clock pulses. Since the clock pulses occur at known intervals, the counter can be used as an instrument for measuring time and therefore period or frequency. It can be used to keep a track of the number of events that have occurred, such as number of times a button has been pressed or the number of pulses received from a sensor. Flip flops are the basic building blocks of a counter. There are basically two different types of counters synchronous and asynchronous.

Synchronous counters use parallel operation for faster speed, triggered by a clock signal, with a consistent settling time. Asynchronous counters, also known as ripple counters are simpler but slower, with each flip flop triggered by the previous one, accumulating settling times. Synchronous counters may require additional hardware for speed improvement.

Counters use flip flops to count up or down, with number of bits determining their counting range. For instance, a 4 bit counter goes from 0 to 15. They find use in frequency, division, timing, delays, binary sequences, pulse generation and frequency counting.

The number of states or counting sequences through which a particular counter advances before returning once again back to its original first state is called the modulus (MOD). Modulus Counters, or simply MOD counters are defined based on the number of states that counter will sequence through before returning back to its original value. For example, a counter counts from 0_2 to 11_2 in binary. That is 0 to 3 in decimal, has a modulus value of 4 ($0_2 \rightarrow 1_2 \rightarrow 10_2 \rightarrow 11_2$, and return back to 0_2) so would therefore be called a modulo-4 or mod-4 counter.

Design procedure of a synchronous counter

- Find the number of flip flops required.

The number of flip flops required can be determined by using $M \leq 2^N$ where M is the MOD number and N is the number of required flip flops.

SL. No.	clock Pulse	Φ_C	Φ_B	Φ_A
1	0	0	0	0
2	1	0	0	1
3	2	0	1	0
4	3	0	1	1
5	4	1	0	0
6	5	1	0	1

Count table of MOD 6 Counter

Present State			Next State			Inputs of the FFs					
Φ_C	Φ_B	Φ_A	Φ_C	Φ_B	Φ_A	J _C	K _C	J _B	K _B	J _A	K _A
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1

Excitation table of MOD 6 Counter

2. Draw a state diagram for the given sequence
3. Draw the FF transition table (excitation table)
4. Use KMap to derive the logic expression of inputs of FF
5. Implementation using FFs and required combinational logic

Design of Mod-6 Counter using JK Flip Flop

To design the Mod 6 synchronous counter, contain six counter states (i.e. from 0 to 5). No. of FFs required = 3 given by Q_A , Q_B , and Q_C where Q_C is the MSB and Q_A is LSB to design this counter.

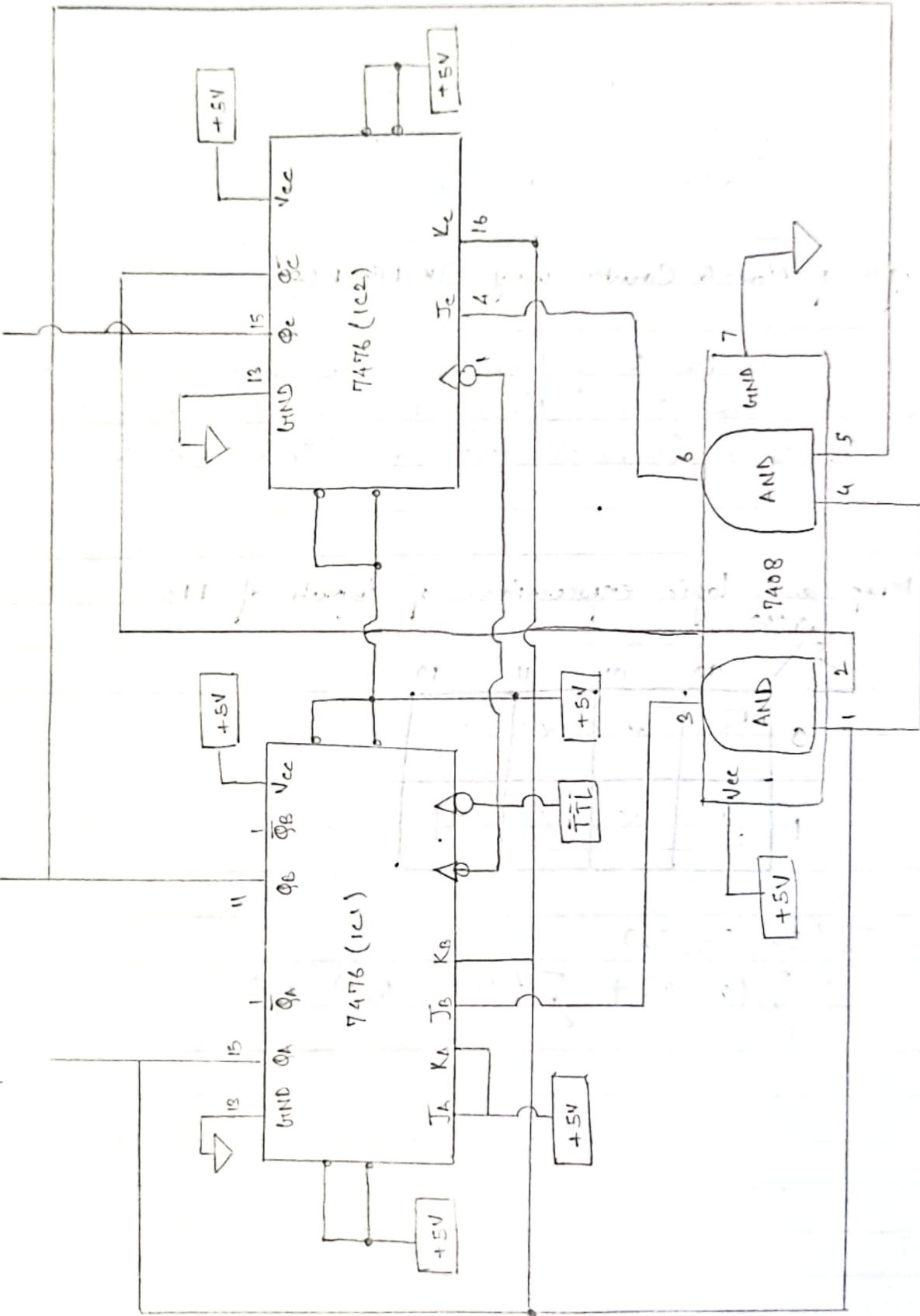
K Map and logic expressions of inputs of FFs

	00	01	11	10	
0	1	X	X	1	
1	1	X	X	X	

$$\bar{J}_A(Q_C, Q_B, Q_A)$$

$$= \sum (0, 2, 4) + \sum d(1, 3, 5, 6, 7) = 1$$

OUTPUTS



Logic Diagram of synchronous binary Mod-6 counter using IC 7476 and IC 7408

~~$\Phi_C \Phi_B \Phi_A$~~

	00	01	11	10
0	X	I	I	X
1	X	I	X	X

$$K_A(\Phi_C, \Phi_B, \Phi_A)$$

$$= \sum(0, 2, 4) + d(1, 3, 5, 6, 7) = 1$$

 ~~$\Phi_C \Phi_B \Phi_A$~~

	00	01	11	10
0		I	X	X
1			X	X

$$J_B(\Phi_C, \Phi_B, \Phi_A) = \sum(1) + d(2, 3, 6, 7)$$

$$= \Phi_C \Phi_A$$

 ~~$\Phi_C \Phi_B \Phi_A$~~

	00	01	11	10
0	X	X	I	
1	X	X	X	X

$$K_B(\Phi_C, \Phi_B, \Phi_A) = \sum(3) + d(0, 1, 4, 5, 6, 7)$$

$$= \Phi_A$$

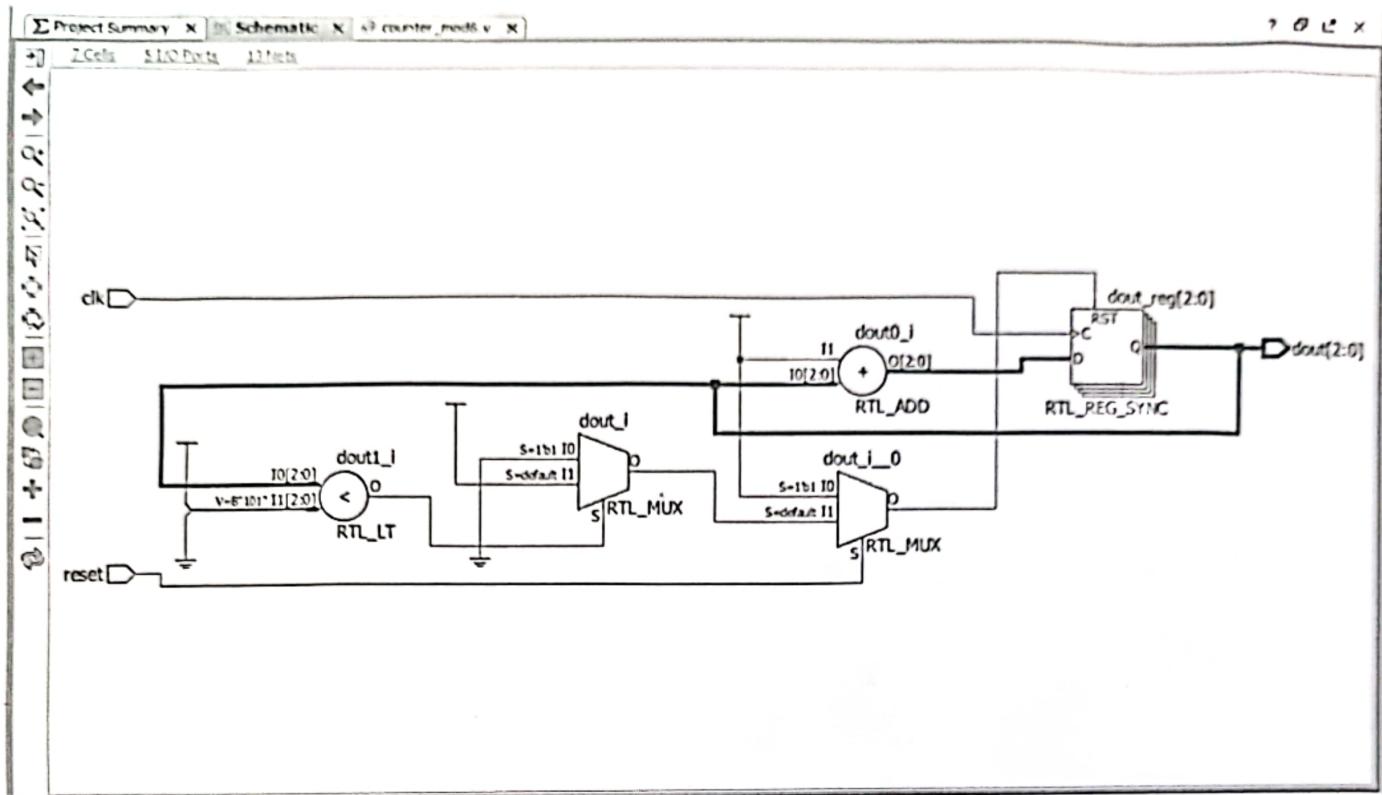
 ~~$\Phi_C \Phi_B \Phi_A$~~

	00	01	11	10
0	X	X	X	X
1		I	X	X

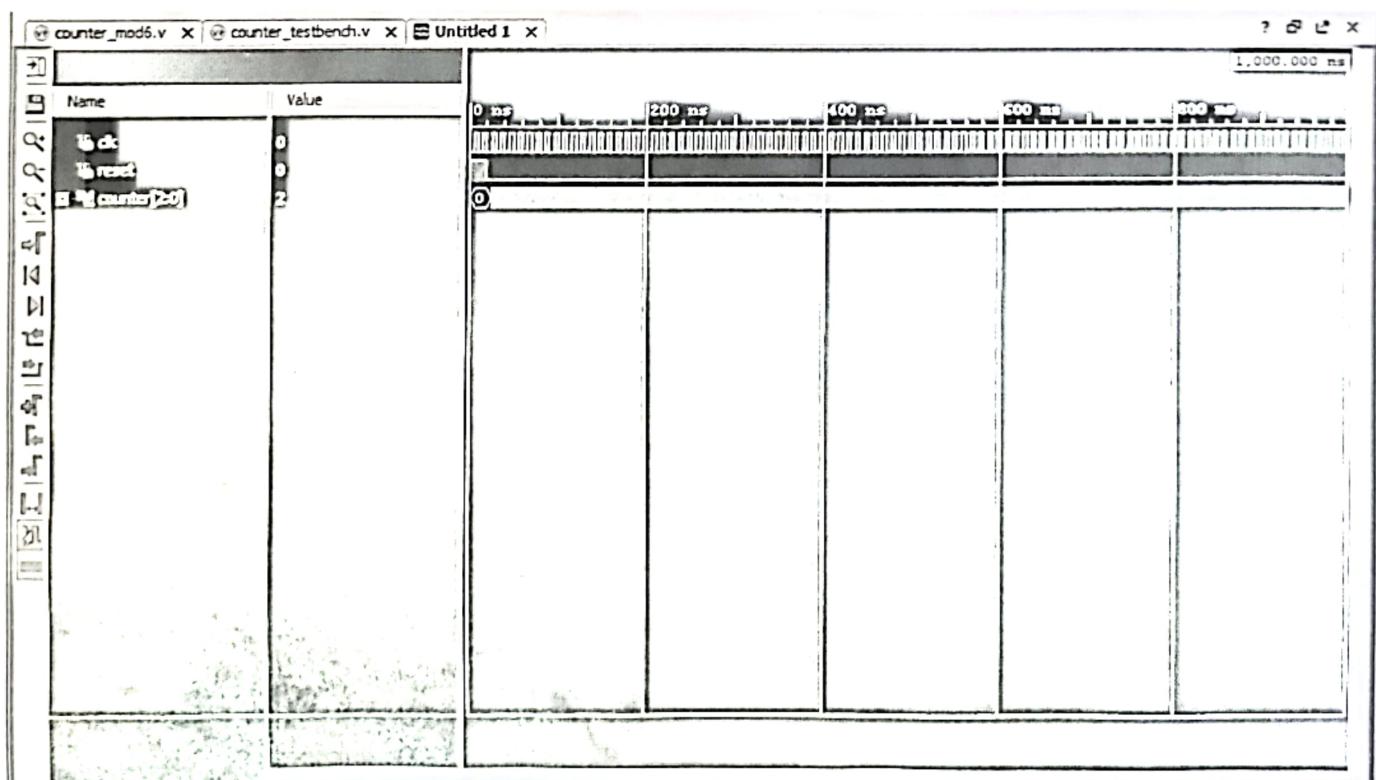
$$K_C(\Phi_C, \Phi_B, \Phi_A) =$$

$$= \sum(5) + d(0, 1, 2, 3, 6, 7)$$

$$= \Phi_A$$



SCHEMATIC REPRESENTATION OF MOD-6 COUNTER



WAVEFORM REPRESENTATION OF MOD 6 COUNTER

Qc	00	01	11	10
0			1	
1	X	X	X	X

$$J_c(\Phi_c, \Phi_B, \Phi_A) = \Sigma(3) + d(4, 5, 6, 7) = \Phi_B \Phi_A$$

Procedure

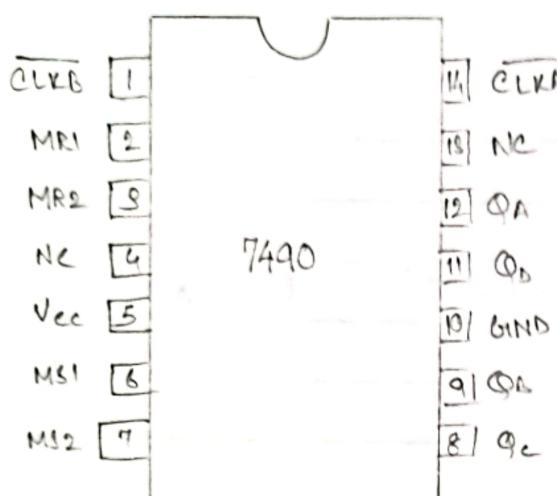
- For software simulation

- i) Create a module with required number of variables and mention its input/output
- ii) Write the description of the boolean function using operators or by using the built in primitive gates.
- iii) Synthesize to create RTL Schematic
- iv) Create another module referred as test bench to verify the functionality and to obtain the waveform of input / output
- v) Follow the steps required to simulate the design and compare the obtained output with the corresponding truth table.
- vi) Take the screenshots of the RTL schematic and simulated waveform

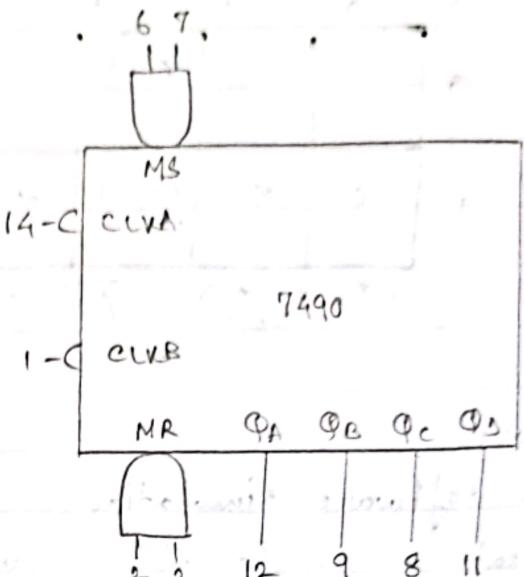
- For hardware implementation

- i) Turn off the power of trainer kit before constructing any circuit.
- ii) Connect power supply (+5V DC) pin and ground pin to the respective pins of the trainer kit.
- iii) Place the ICs properly on the bread board in the trainer kit
- iv) Connect Vcc and GND pins on each chip to the power supply and ground bus strips on the bread board

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PIN Diagram of IC 7490



V_{cc} = PINS 5, 13
GND = PIN 10

NC = PINS 4, 12

Logic Symbol of IC 7490

Reset / Set inputs				Outputs			
MRI	MRL	MSI	MS2	QD	QC	QB	QA
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	1	Count			
0	X	0	X	Count			
0	X	X	0	Count			
X	0	0	X	Count			

Count	OUTPUTS			
	QD	QC	QB	QA
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Mode Selection and Count Table of 7490 (Decade Counter)

- (V) Connect the input and output pins of chips to the input switches and output LEDs respectively in the trainer kit.
- (VI) Check the connections before you turn on the power.
- (VII) Apply various combinations of inputs according to truth tables and observe outputs of LEDs.

Design problem

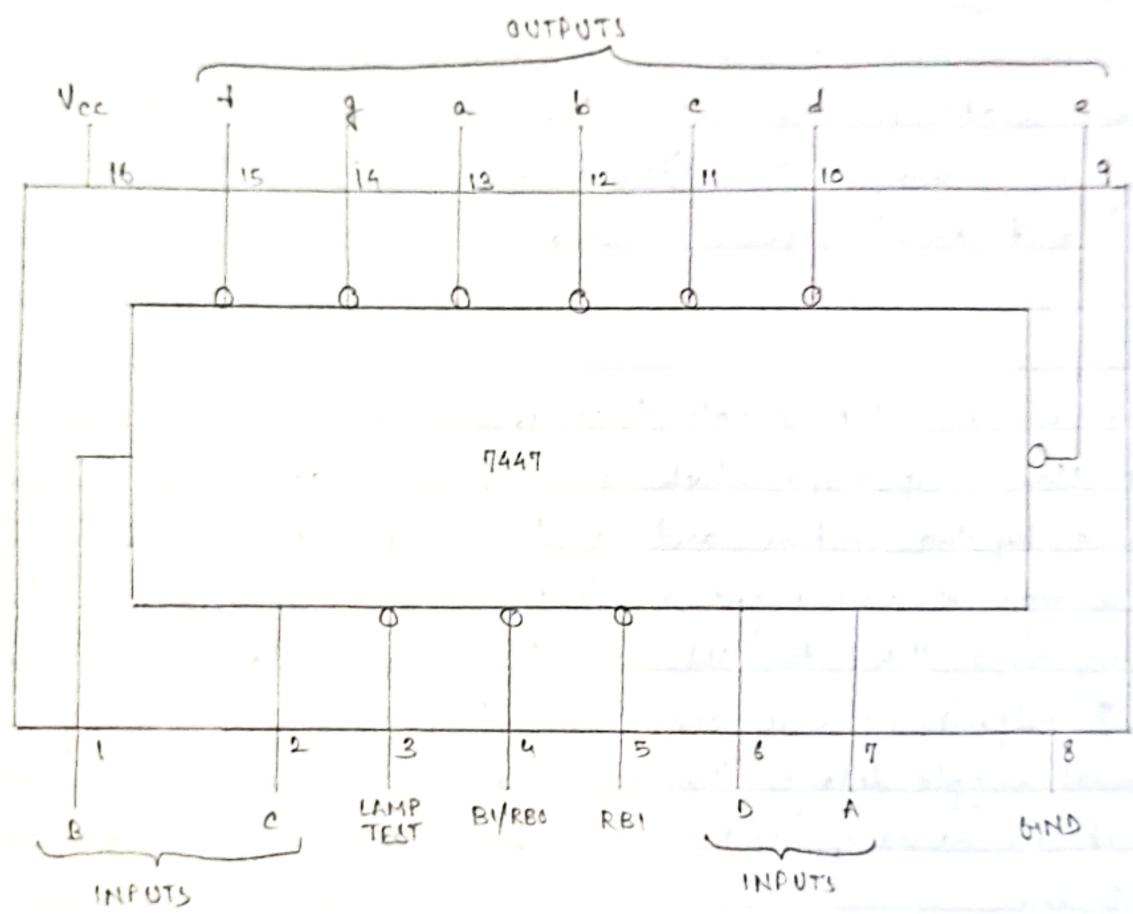
Hardware and simulation of decade counter using Verilog HDL. Hardware implementation of a decade counter to display the digits 0 to 9 using IC7490 (decade counter), IC7447 (BCD to decimal decoder) and seven segment display.

Solution:

IC7490 is a 4 bit ripple type decade counter. It consists of four master/slave flip flops which are internally connected to provide a divide by two section and a divide by 5 section. Each section has a separate clock input which initiates state changes of the counter on a HIGH to LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore decoded output signals are subject to decoding spines and should not be used for clocks or strobes.

A gated NAND asynchronous Master Reset (MR_1, MR_2) is provided which overrides clocks and resets (clears) all the flip flops. A gated NAND asynchronous Master Set (MS_1, MS_2). Since the output from the divide by two section is not internally connected to the succeeding stages, the device may be operated in various counting modes.

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PIN diagram of IC 7447

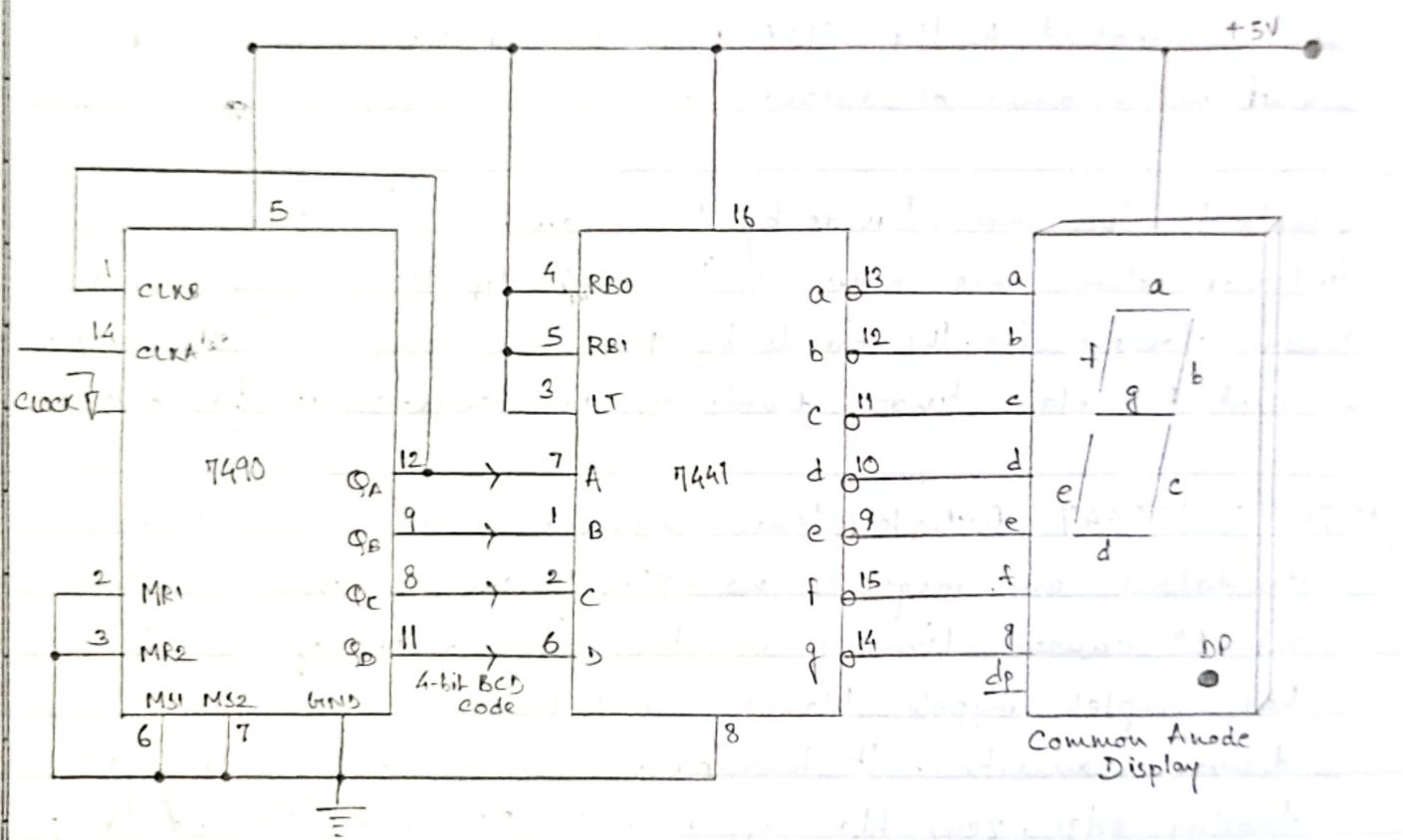
BCD Decade (8421) Counter: The $\overline{CLK_B}$ input must be externally connected to the \overline{QA} output. The $\overline{CLK_A}$ input receives the incoming count producing a BCD count sequence.

Symmetrical Biquinary Divide-By-Ten Counter: The Q_0 output must be externally connected to the $\overline{CLK_A}$ input. The input count is then applied to the $\overline{CLK_A}$ input and a divide by ten square wave is obtained at output Q_0 .

Divide by Two and Divide by Five Counters: No external interconnections are required. The first flip flop is used as a binary element for the divide by two function. The $\overline{CLK_B}$ input is used to obtain binary divide by five operation at the Q_0 output.

IC 7447: IC 7447 BCD-to-Seven Segment Decoder. The IC is standalone and requires no external components other than the LED current limiting resistors. The output of the IC has complete ripple blanking and requires no external driver transistors. It incorporates automatic leading/or trailing edge, zero blanking control (\overline{RBI} and \overline{RBO}). A lamp test of these devices may be performed at any time when the $\overline{B1}/\overline{RBO}$ mode is at a high logic level.

The 7447 decoder follows table 6.4 and the segment identification illustration. When the input data is 0, a low signal on RBI blanks the display, enabling multi digit display. By connecting RBI and $B1/RBO$, leading and trailing zeroes can be suppressed. Simultaneously, leading and trailing zeroes can be



Logic diagram of Decade counter using IC 7490 and IC 7441

suppressed using external gates. BI/RBO also functions as an unconditional blanking input, with an option to control display intensity through the duty cycle of the blanking signal. A LOA signal on LT turns all segment outputs, except when BI/RBO is forced low.

Note (1): The blanking input ($\bar{B}I$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple blanking input ($\bar{R}BI$) must be open or high if blanking of a decimal zero is not desired.

Note (2): When a low logic level is applied directly to the blanking input ($\bar{B}I$), all segment outputs are high regardless of the level of any other input.

Note (3): When the ripple blanking input ($\bar{R}BI$) and inputs A,B,C,D are at a low level with the lamp test input high, all segment outputs go high and the ripple blanking output (RBO) goes to a low level (response condition).

Note (4): When the blanking output ($\bar{B}I / RBO$) is open or held high and a low is applied to the lamp test input all segment outputs are low. Input ($\bar{B}I / RBO$) is a wire-AND logic serving as $\bar{B}I$ or RBO .

B CONCLUSION

Design and simulation of modulo counter using verilog behavioural modelling has been done and implemented successfully.

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