

EXPERIMENT - 3

AIM : Design and simulation of 3 line to 8 line active high decoder using Verilog HDL. Realization of 3 variable boolean function using active low decoder

COMPONENT / SOFTWARE USED :

Component / Software	Specification
• ICs	7413, 7408
• Bread board, power supply, LEDs, Resistors, Switches,	As per requirement
Connecting wires	
• Software(s) used	Vivado 2016.1

THEORY :

Decoder:

Decoder is a combinational circuit that has N input lines and maximum of $(2)^N$ unique output lines. The name "Decoder" mean to translate or decode coded information from one format into another, so a digital decoder transforms a set of digital input signals into an equivalent decimal code at its output. Active high Decoder - the output line that is active will be HIGH (1) and rest all the outputs will be LOW (0). Active low decoder - the output line that is active will be LOW (0) and rest all the outputs will be HIGH (1).

This 3-to-8 line binary decoder consists of an array of eight AND gates. The three (3) binary inputs labelled I_0 , I_1 and I_2 are decoded into one of 8 outputs, hence the description of 3-to-8

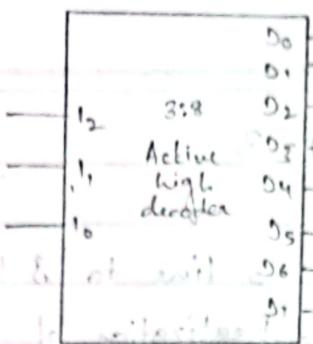
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binary decoder: Each output represents one of the minterms of the three input variables (each output is equal to a minterm)

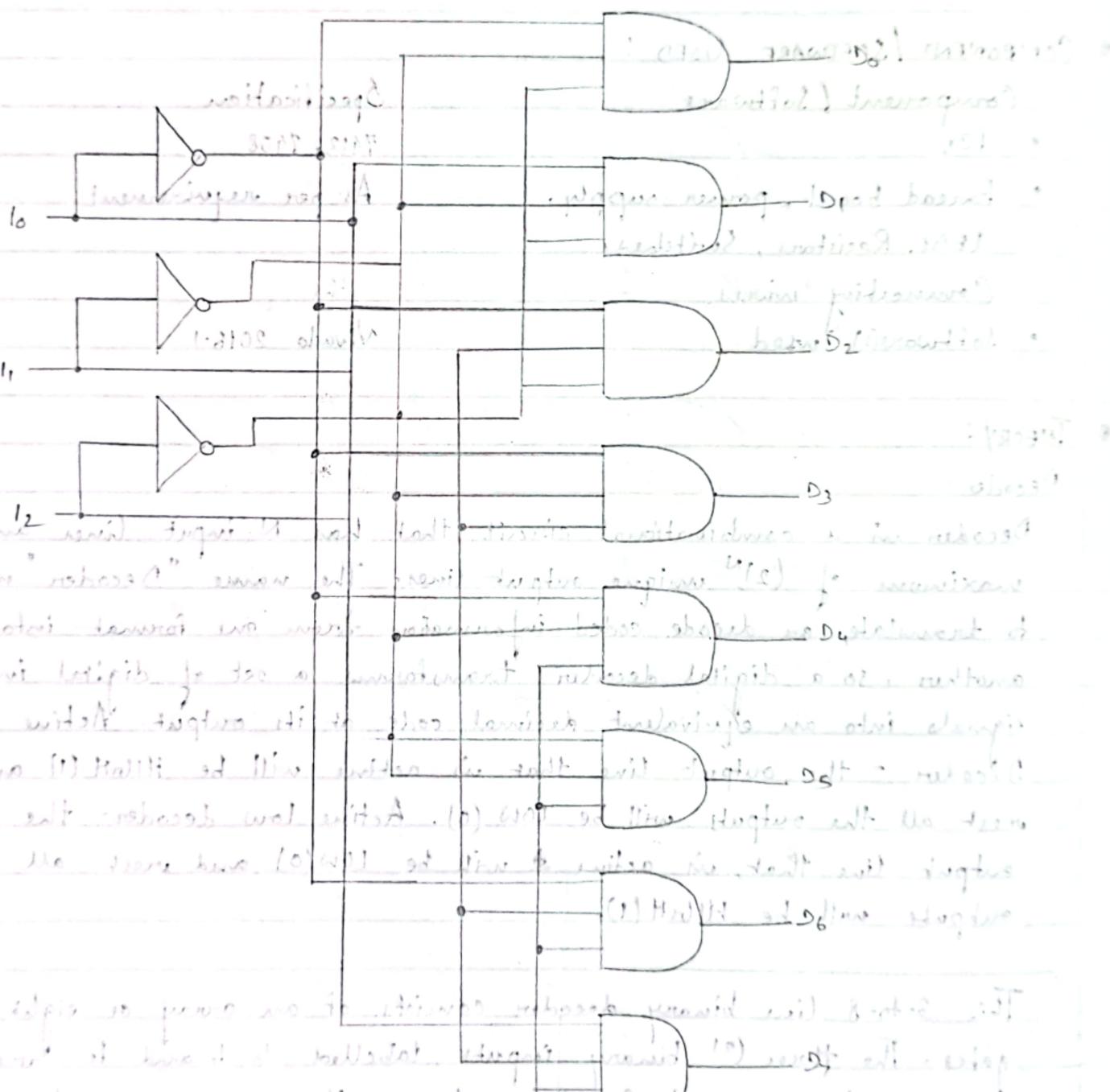
The binary inputs I_2 , I_1 , and I_0 determine which output line from D_0 to D_7 is "high" at logic level '1' while the remaining outputs are held low at logic "0" so only one output can be active (High) at any one time. Therefore, whichever output line is "High", identifies the binary code present at the input, in other words it "decodes" the binary input. Truth table of 3:8 active high Decoder is shown in table 3.1. In case of active low decoder output line from D_0 to D_7 is "low" while the remaining outputs are held "HIGH" so only one output can be active (Low) at any one time as shown in table 3.2.

INPUTS			OUTPUT							
I_2	I_1	I_0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Truth table of 3:8 active high Decoder



Block Diagram of 3:8 DECODER



LOGIC DIAGRAM OF 3:8 DECODER

$$D_0 (I_2, I_1, I_0) = m_0 = \bar{I}_2 \bar{I}_1 \bar{I}_0$$

$$D_1 (I_2, I_1, I_0) = m_1 = \bar{I}_2 \bar{I}_1 I_0$$

$$D_2 (I_2, I_1, I_0) = m_2 = \bar{I}_2 I_1 \bar{I}_0$$

$$D_3 (I_2, I_1, I_0) = m_3 = \bar{I}_2 I_1 I_0$$

$$D_4 (I_2, I_1, I_0) = m_4 = I_2 \bar{I}_1 \bar{I}_0$$

$$D_5 (I_2, I_1, I_0) = m_5 = I_2 \bar{I}_1 I_0$$

$$D_6 (I_2, I_1, I_0) = m_6 = I_2 I_1 \bar{I}_0$$

$$D_7 (I_2, I_1, I_0) = m_7 = I_2 I_1 I_0$$

Boolean Expression of Outputs of 3:8 decoder

Inputs			Outputs							
I_2	I_1	I_0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

Truth table of 3:8 active low decoder

$$D_0 (I_2, I_1, I_0) = \bar{m}_0 = \bar{\bar{I}}_2 \bar{I}_1 \bar{I}_0$$

$$D_1 (I_2, I_1, I_0) = \bar{m}_1 = \bar{\bar{I}}_2 \bar{I}_1 I_0$$

$$D_2 (I_2, I_1, I_0) = \bar{m}_2 = \bar{\bar{I}}_2 I_1 \bar{I}_0$$

$$D_3 (I_2, I_1, I_0) = \bar{m}_3 = \bar{\bar{I}}_2 I_1 I_0$$

$$D_4 (I_2, I_1, I_0) = \bar{m}_4 = \bar{\bar{I}}_2 \bar{I}_1 \bar{I}_0$$

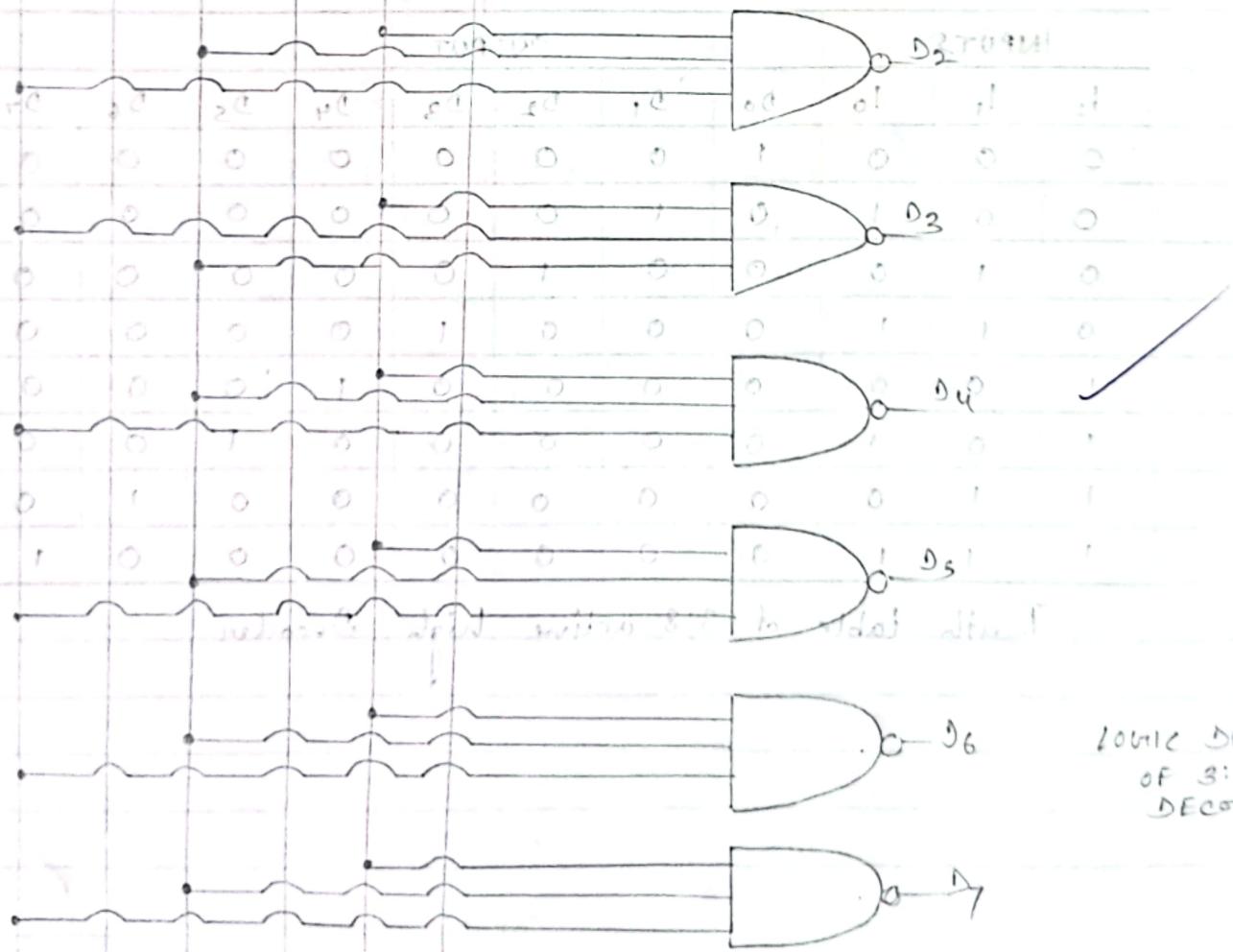
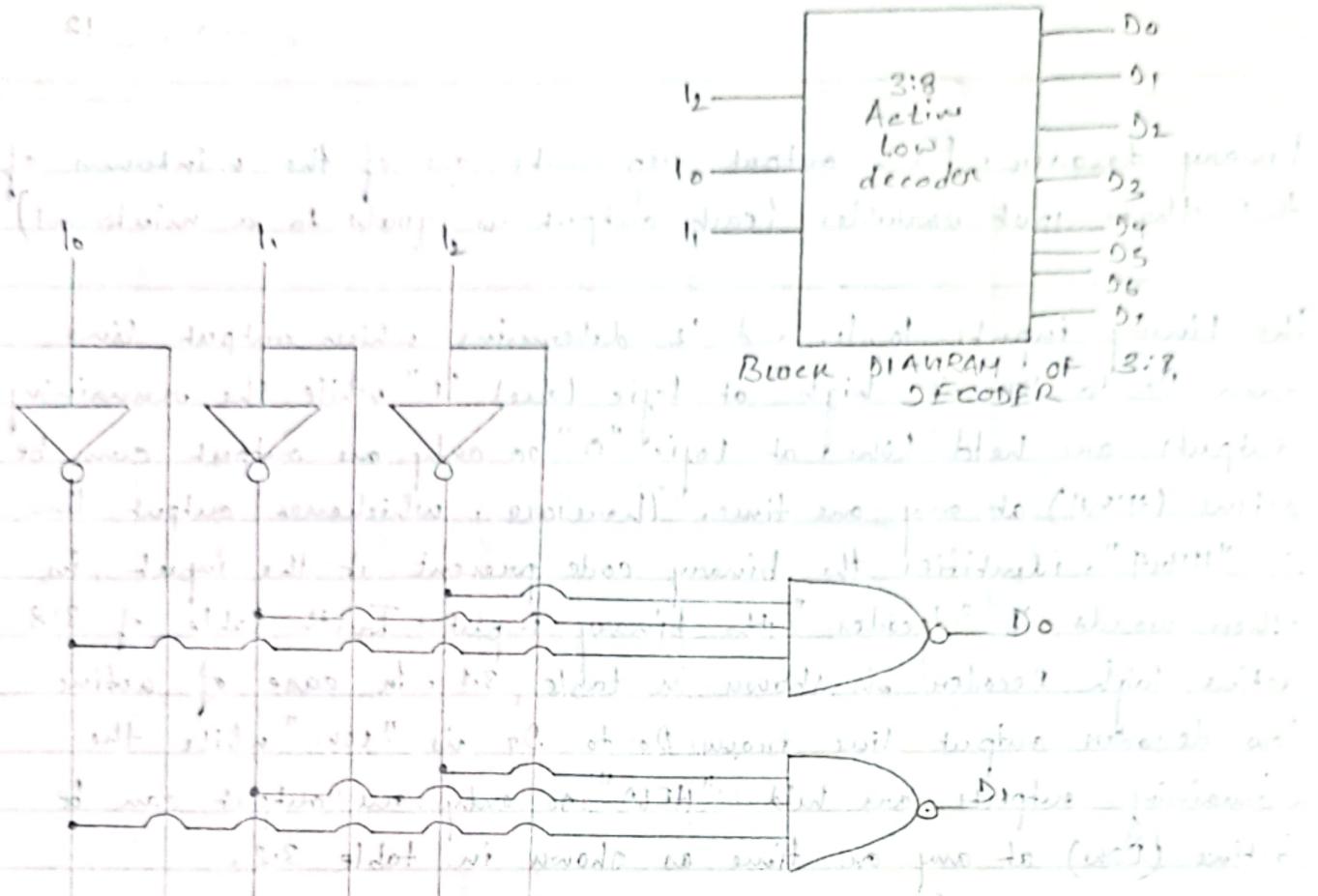
$$D_5 (I_2, I_1, I_0) = \bar{m}_5 = \bar{\bar{I}}_2 \bar{I}_1 I_0$$

$$D_6 (I_2, I_1, I_0) = \bar{m}_6 = \bar{\bar{I}}_2 I_1 \bar{I}_0$$

$$D_7 (I_2, I_1, I_0) = \bar{m}_7 = \bar{\bar{I}}_2 I_1 I_0$$

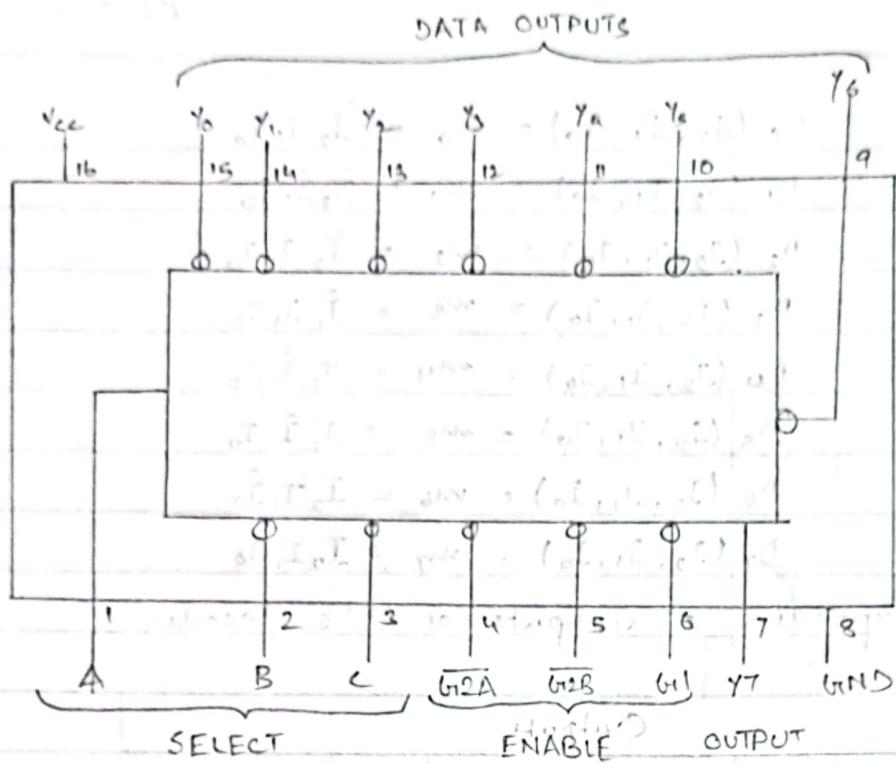
Boolean expression of Outputs of 3:8 active low decoder

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The IC-74138 is 3:8 active low decoder its pin diagram is shown in figure 3.5. The IC-74138 has 3 binary inputs A, B and C which are equivalent to l_0 , l_1 and l_2 respectively. It has 8 outputs Y_0 to Y_7 those are equivalent to D_0 to D_7 respectively. If this device is enabled, these inputs determine which one of the eight normally HIGH outputs will go low. The IC has two active LOW and one active HIGH enable (G_{1A} , G_{1B} , and G_{2B}) which will be helpful in cascading of decoders. The enable pins must be active for normal operation of decoder. The functioning of the IC74138 is illustrated in table 3.3 where 'X' denotes the Don't care in the table

INPUTS			OUTPUTS							
ENABLE INPUTS		SELECT	0	1	2	3	4	5	6	7
G_{1B}	G_{2A}	G_1	C	B	A	0	1	2	3	4
0	0	1	0	0	0	0	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1
0	0	1	0	1	0	1	1	0	1	1
0	0	1	1	0	0	1	1	1	0	1
0	0	1	1	0	1	1	1	1	1	0
0	0	1	1	1	0	1	1	1	1	0
0	0	1	1	1	1	1	1	1	1	X
X	X	0	X	X	X	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1
1	X	X	X	X	X	1	1	1	1	1



PIN DIAGRAM OF IC 74138

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	1	1	1	1	1	0	1	1	0	1	1	0	1	0	1
1	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1
1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0
1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	0
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0
1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

whereas each output 818 is selected by

$\bar{G}_1 \bar{G}_2 \bar{G}_3 \bar{G}_4 = (\bar{A}, \bar{B}, \bar{C})$

$\bar{G}_1 \bar{G}_2 \bar{G}_3 G_4 = (A, \bar{B}, \bar{C})$

$G_1 \bar{G}_2 \bar{G}_3 \bar{G}_4 = (\bar{A}, B, \bar{C})$

$G_1 \bar{G}_2 \bar{G}_3 G_4 = (A, B, \bar{C})$

$\bar{G}_1 G_2 \bar{G}_3 \bar{G}_4 = (A, \bar{B}, C)$

$\bar{G}_1 G_2 \bar{G}_3 G_4 = (A, B, C)$

$G_1 G_2 \bar{G}_3 \bar{G}_4 = (A, \bar{B}, \bar{C})$

$G_1 G_2 \bar{G}_3 G_4 = (A, B, \bar{C})$

whereas each output 818 is selected by voltages control

Boolean function implementation :

Any boolean function may be represented in sum of minterms or product of maxterms form, a hardware implementation of the function is provided by a decoder that creates the functions minterms and external gates that construct their logical sum. The process for creating a Boolean function with a decoder and external gates requires that a boolean function with a decoder and external gates requires that the boolean function be defined as the sum of minterms and product of maxterms. Then a decoder is chosen to create all the minterms or maxterms of the input variables. The inputs to each gate are chosen from the decoder outputs based on the list of minterms or maxterms for function. This approach is illustrated by implementing a Boolean function given below

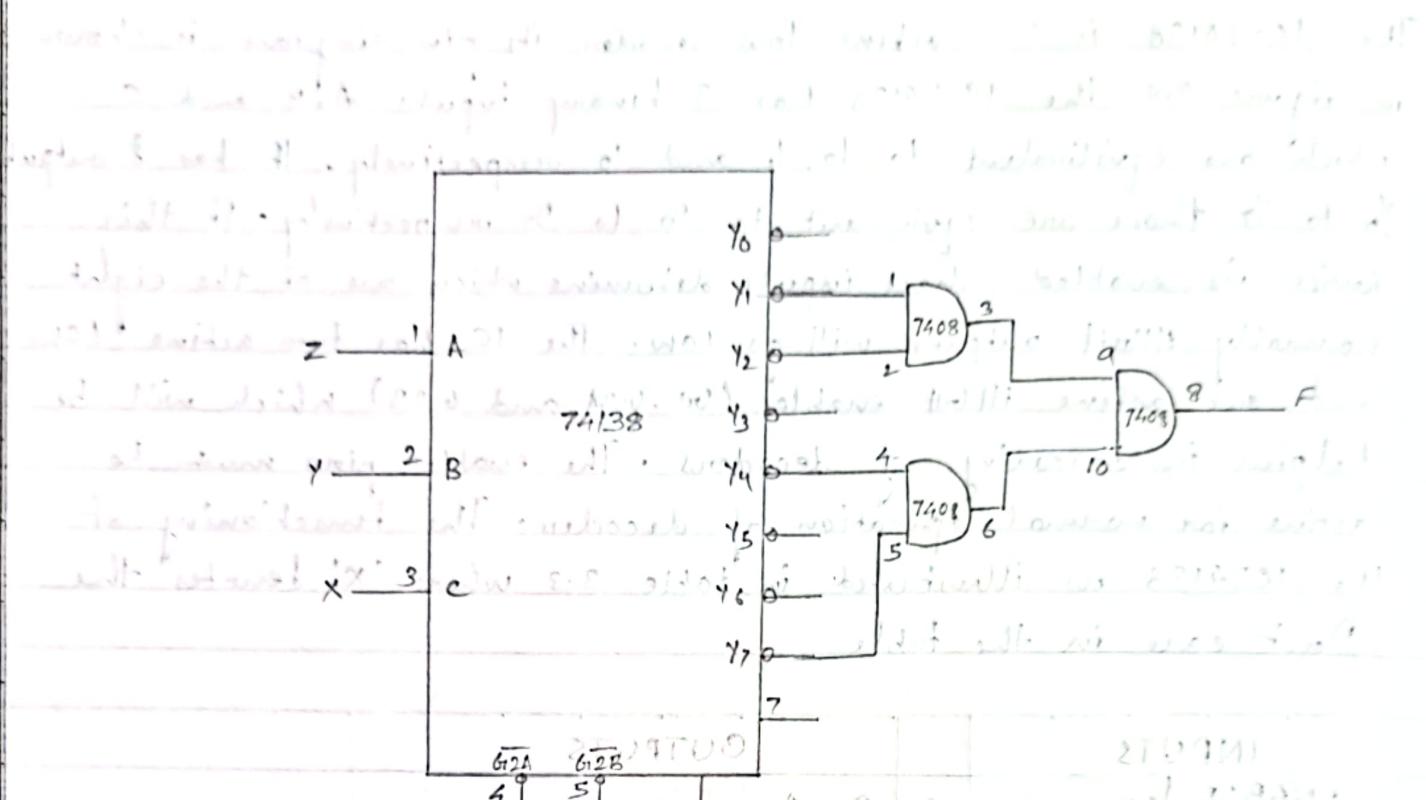
$$F(X,Y,Z) = \sum(0,3,5,6) = m_0 + m_3 + m_5 + m_6 \\ = \prod(1,2,4,7) = \overline{m}_1 \overline{m}_2 \overline{m}_4 \overline{m}_7$$

To implement the above boolean function a 3:8 active low decoder is chosen and AND gated are required. The implementation of the Boolean function using the block diagram of the decoder IC74138 is shown below in figure 3.6.

Procedure

④ For software simulation

- Create a module with required number of variables and mention its input / output.



BLOCK DIAGRAM OF BOOLEAN FUNCTION
 USING 3:8 DECODER

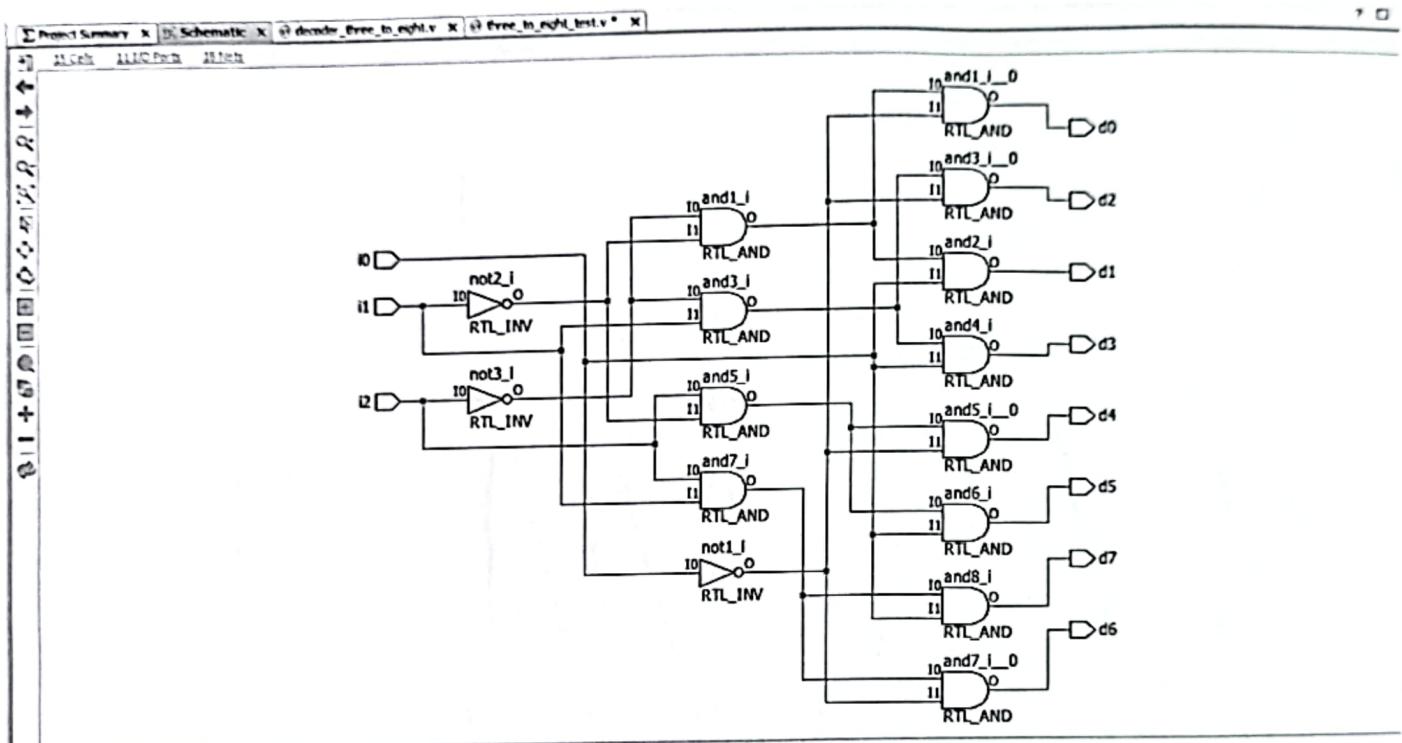
1	1	1	0	1	1	1	0	0	1	1	0
1	1	0	1	1	1	1	1	0	1	0	1
0	1	1	1	1	1	1	1	1	1	0	1
1	0	1	1	1	1	1	0	0	0	0	0
1	0	1	0	1	1	1	0	0	0	0	0
1	0	0	1	1	1	1	0	0	0	0	0
0	1	0	1	1	1	1	0	0	0	0	0
1	0	0	0	1	1	1	0	0	0	0	0
0	0	1	0	1	1	1	0	0	0	0	0
0	0	0	1	1	1	1	0	0	0	0	0
0	0	0	0	1	1	1	0	0	0	0	0

- (b) Write the description of given boolean function using operators or by using the built in primitive gates.
- (c) Synthesise to create RTL schematic.
- (d) Create another module referred to test bench to verify the functionality and to obtain the waveforms of inputs and outputs.
- (e) Follow the steps required to simulate the design and compare the obtained output with the corresponding truth table.
- (f) Take the screenshots of the RTL schematic and simulated waveform.

* For hardware implementation

- (a) Turn off the power of the trainer kit before constructing any circuit.
- (b) Connect power supply (+5V DC) pin and ground pin to the respective pins of the trainer kit.
- (c) Place the ICs properly on the bread board in the trainer kit.
- (d) Connect VCC and GND pins of each chip to the power supply and ground bus strips on the bread board.
- (e) Connect the input and output pins of chips to the input switches and output LEDs respectively in the trainer kit.
- (f) Check the connections before you turn on the power.
- (g) Apply various combinations of inputs according to truth tables and observe outputs of LEDs.

What would be the maximum value of
width of bus at bit level? At point of time we have
a 3-bit binary input & we want to find out the
maximum value of bus width. So for having one-bit width all
signals should be single bit. So for having one-bit width all
the bits of bus should be of same width.



SCHEMATIC REPRESENTATION OF 3 LINE TO 8 LINE
ACTIVE HIGH DECODER

bus width of bus is determined by the number of bits (3)

number of output lines = 2^n (n = no. of bits)

number of output lines = 2^3 = 8

number of output lines = 2^4 = 16

number of output lines = 2^5 = 32

HDL Code

```

module Decoder_three_to_eight ( output D0, output D1, output D2,
                                output D3, output D4, output D5, output D6, output D7,
                                input I2, input I1, input I0);

    wire W0, W1, W2;

    not NOT1 (W0, I0);
    not NOT2 (W1, I1);
    not NOT3 (W2, I2);

    and AND1 (D0, W2, W1, W0);
    and AND2 (D1, W2, W1, 10);
    and AND2 (D2, W2, I1, W0);
    and AND3 (D3, W2, I1, W0);
    and AND4 (D4, I2, W1, W0);
    and AND5 (D5, I2, W1, I0);
    and AND6 (D6, I2, I1, W0);
    and AND7 (D7, I2, I1, I0);

endmodule

```

TESTBENCH CODE

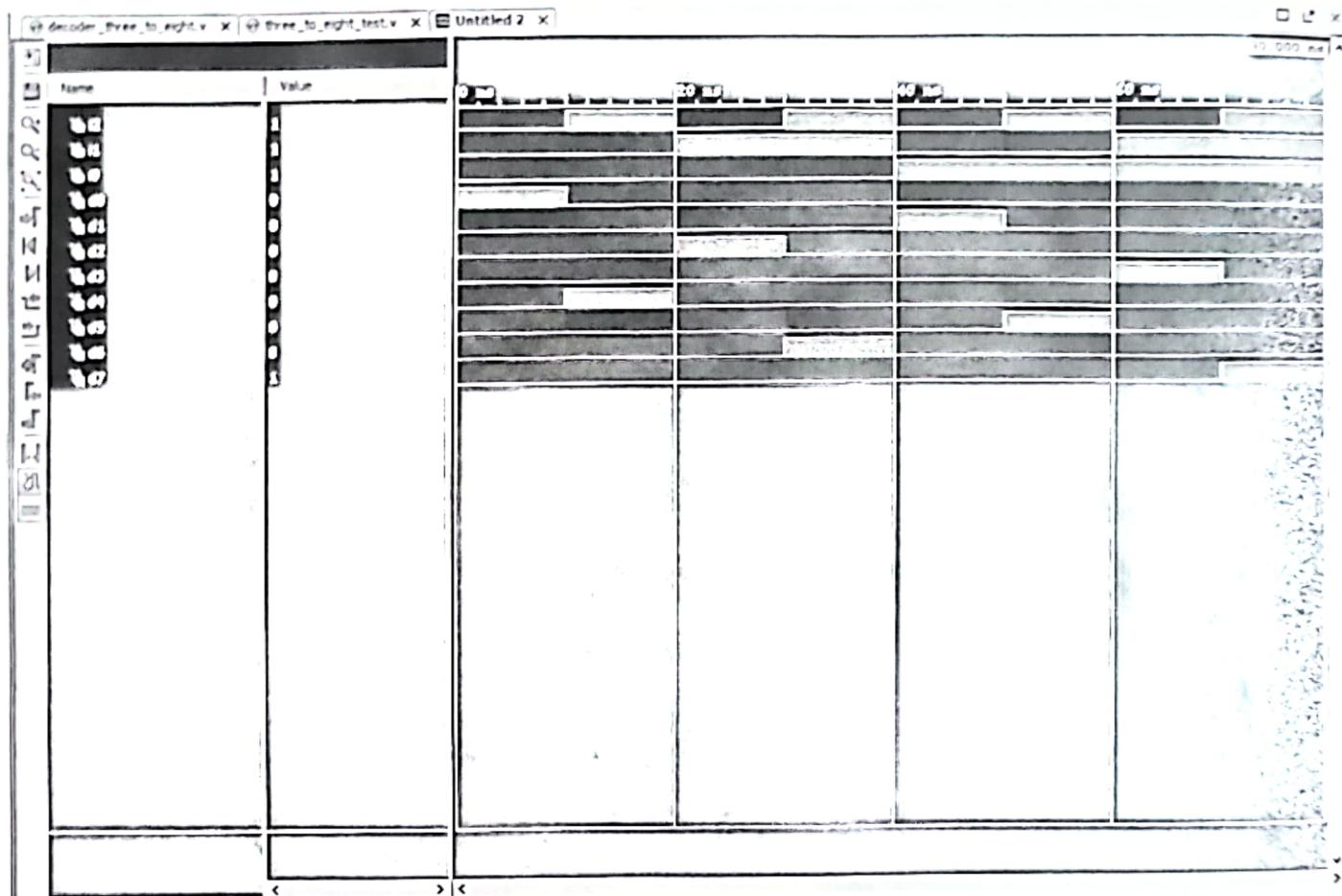
```

module three-to-eight test ();
    reg i2, i1, i0;
    wire d0, d1, d2, d3, d4, d5, d6, d7;
    decoder_three_to_eight dut (d0, d1, d2, d3, d4, d5, d6, d7, i2, i1, i0);

initial
begin

```

values for each input and see how it will work
by running a logic simulation of it.



3 LINE TO EIGHT LINE ACTIVE HIGH DECODER

WAVEFORM

Let's simulate this decoder with two inputs and see what output we get with each input. We'll start by giving a digital pin with the value 0 for the first input and 1 for the second input. We can see that the third input is 0, so the output Y0 is high. This means that when the first two inputs are 0 and the third input is 0, the output Y0 is high. This is because the decoder takes the first two inputs and the third input as address lines, and the output Y0 is the active high output for the address 000.

Now let's change the value of the second input to 1. We can see that the output Y1 is high. This means that when the first two inputs are 0 and the third input is 1, the output Y1 is high. This is because the decoder takes the first two inputs and the third input as address lines, and the output Y1 is the active high output for the address 001.

Now let's change the value of the first input to 1. We can see that the output Y2 is high. This means that when the first two inputs are 1 and the third input is 0, the output Y2 is high. This is because the decoder takes the first two inputs and the third input as address lines, and the output Y2 is the active high output for the address 010.

Now let's change the value of the third input to 1. We can see that the output Y3 is high. This means that when the first two inputs are 0 and the third input is 1, the output Y3 is high. This is because the decoder takes the first two inputs and the third input as address lines, and the output Y3 is the active high output for the address 011.

```

i2=0; i1=0; i0=0
#10 i2=1; i1=0; i0=0
#10 i2=0; i1=1; i0=0
#10 i2=1; i1=1; i0=0
#10 i2=0; i1=0; i0=1
#10 i2=1; i1=0; i0=1
#10 i2=0; i1=1; i0=1
#10 i2=1; i1=1; i0=1
#10
$finish
end
endmodule

```

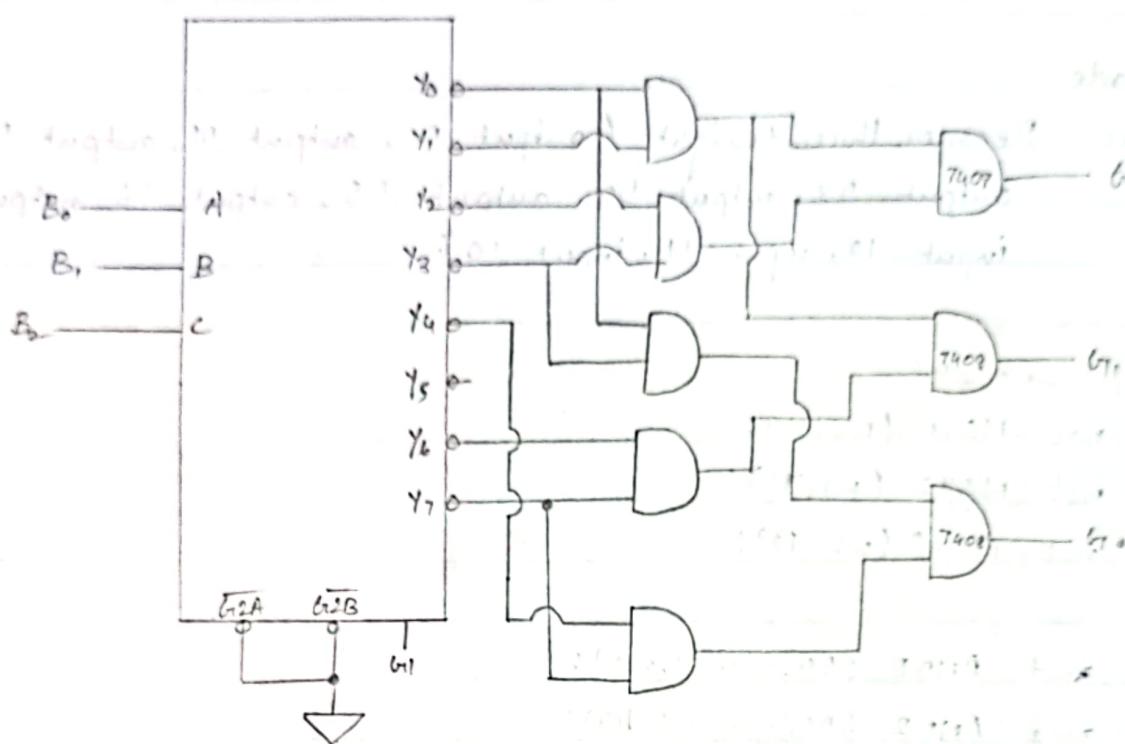
DESIGN PROBLEM: Design and simulation of 3 bit binary to Gray code converter using decoder

Solution:

Binary to Gray code converter is a logical circuit that is used to convert the binary code into its equivalent Gray code. By putting the MSB of 1 below the axis and the MSB of 1 above the axis and reflecting the $(n-1)$ bit code about an axis after 2^{n-1} rotations, we can obtain the n bit gray code.

In table 3.4, the truth table of 3 bit binary to Gray code converter is shown. The implementation of the gray code converter using block diagram of the decoder IC 74138 is shown below in figure 3.7.

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Block Diagram of 3 BIT BINARY TO GRAY CODE
CONVERTER USING DECODER

	INPUTS			OUTPUTS			
	B ₂	B ₁	B ₀	G ₁₀	G ₉	G ₈	
	0	0	0	0	0	0	
	0	0	1	0	0	1	
	0	1	0	0	1	1	
	0	1	1	0	1	0	
	1	0	0	1	1	0	
	1	0	1	1	1	1	
	1	1	0	1	0	1	
	1	1	1	1	0	0	

Truth table of 3 bit binary to Gray code converter & its minterms

$$G_{10}(B_2, B_1, B_0) = \Sigma(4, 5, 6, 7)$$

$$G_9(B_2, B_1, B_0) = \Sigma(2, 3, 4, 5)$$

$$G_8(B_2, B_1, B_0) = \Sigma(1, 2, 5, 6)$$

• HDL Code

```
module Binary_to_Gray (output G10, output G9, output G8, input B2,
                      input B1, input B0);
  wire w0, w1, w2, w3, w4, w5, w6, w7;
```

Decoder three-to-eight Decoder1 (w0, w1, w2, w3, w4, w5, w6, w7, B2, B1, B0)

or OR1 (G10, w4, w5, w6, w7);

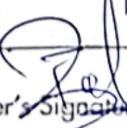
or OR2 (G9, w2, w3, w4, w5);

or OR3 (G8, w1, w2, w5, w6);

endmodule

■ CONCLUSION

Design and simulation of 3 line to 8 line active high decoder using Verilog HDL has been done and implemented successfully.


Teacher's Signature