**CMOS Digital-to-Analog and Analog-to-Digital Converter Design**

**4-bit SAR ADC building blocks and design**

1. **Introduction**

1.5 V 4-bit SAR ADC is designed, and its characteristics measured. The design blocks are detailed below.

1. **Analog Blocks**

**[Comparator]**

**Description:**

To achieve the common-mode range of 0.1-1.4 V and rail-to-rail swing, the two amplifier blocks are cascaded .The amplifier block is shown in Figure below.

The voltage gain is controlled by the input devices M3-M4. The output resistance is controlled by the devices M7-M10. Increasing the length of these devices, affects the voltage gain, by increasing the output impedance. Keeping large input devices, increases the offset of the Comparator. Hence the size of M3-M4 was reduced.

Transistors have been sized according to the table below.

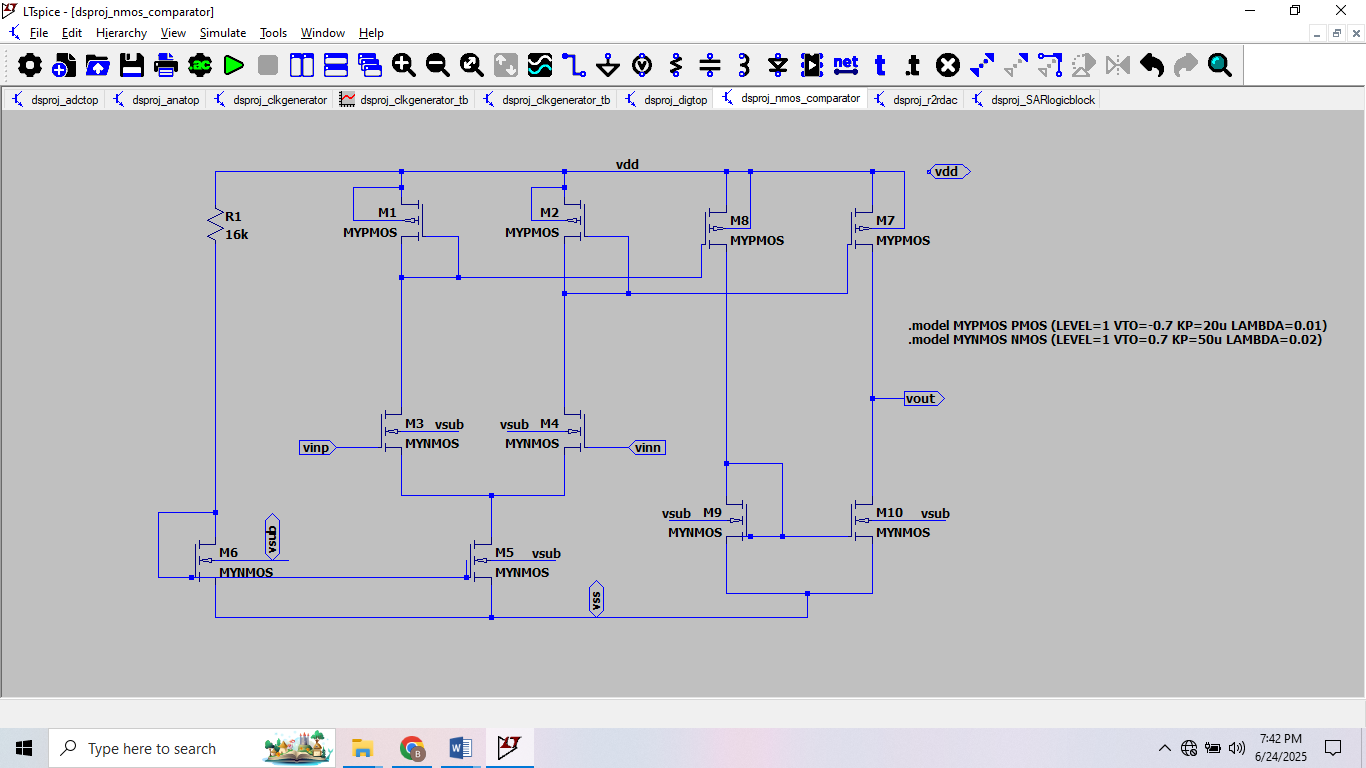
|  |  |  |  |
| --- | --- | --- | --- |
| **Transistor** | **W/L [µm/µm]** | **M[multiplier]** | **IB [µA]** |
| M1 | 1.2/0.18 | 2 | 0-51 |
| M2 | 1.2/0.18 | 2 | 0-51 |
| M3 | 1.2/0.18 | 3 | 0-51 |
| M4 | 1.2/0.18 | 3 | 0-51 |
| M5 | 10/3 | 2 | 51 |
| M6 | 10/3 | 2 | 51 |
| M7 | 1.2/0.25 | 2 | 20 |
| M8 | 1.2/0.25 | 2 | 20 |
| M9 | 1.2/0.25 | 1 | 20 |
| M10 | 1.2/0.25 | 1 | 20 |

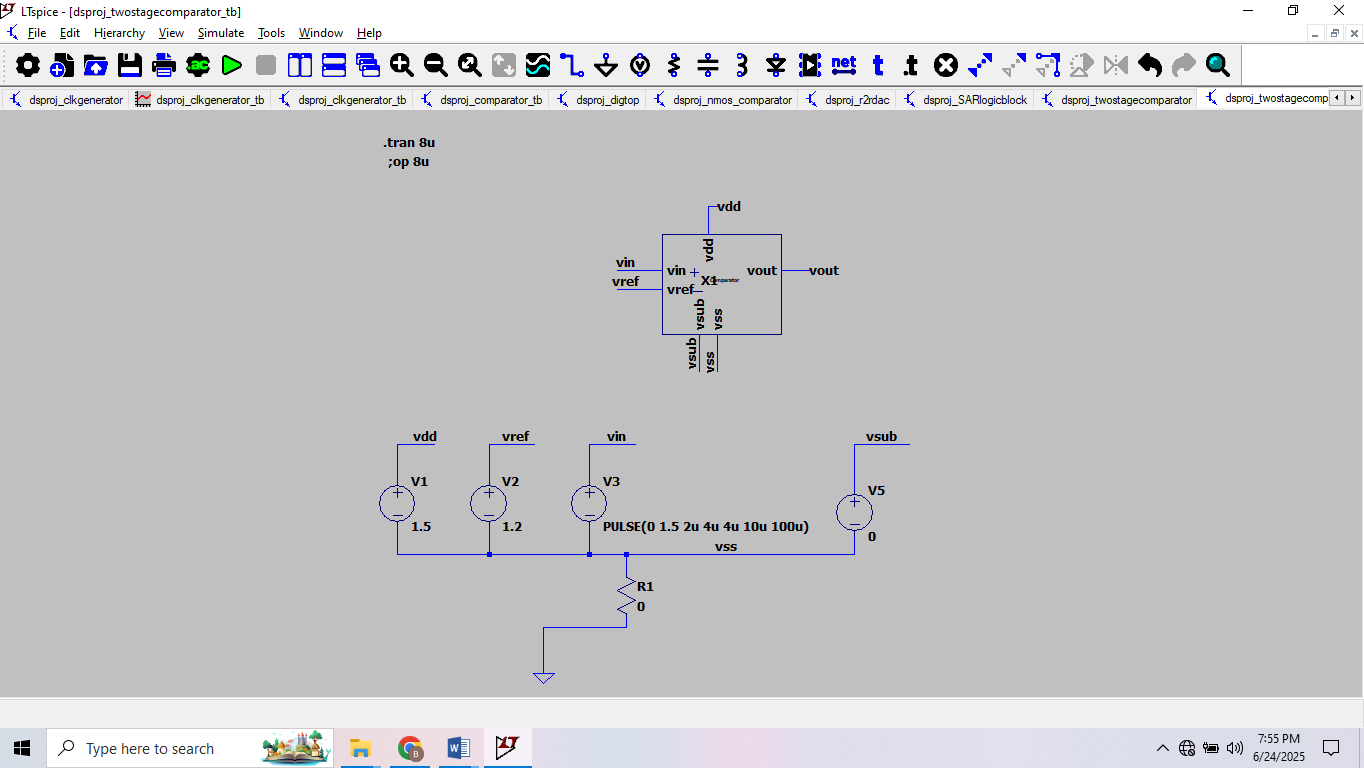
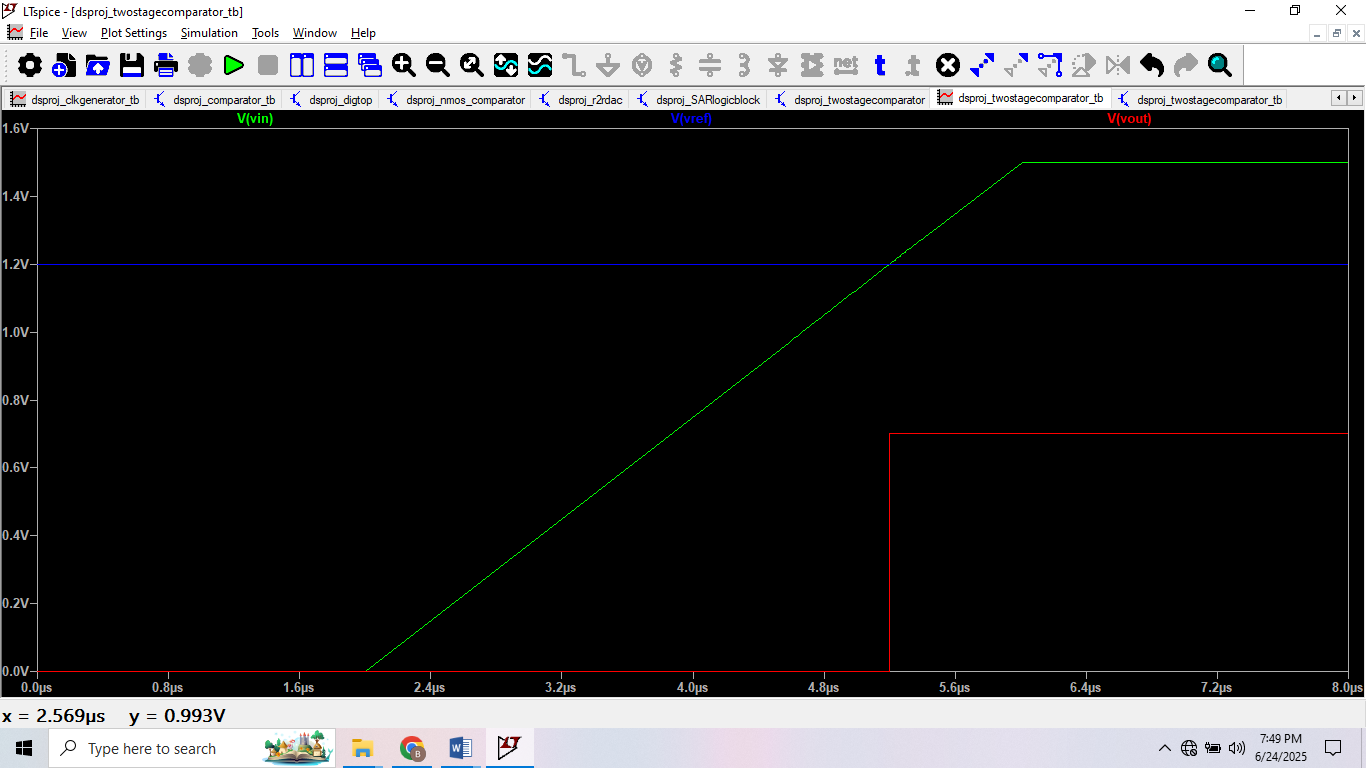
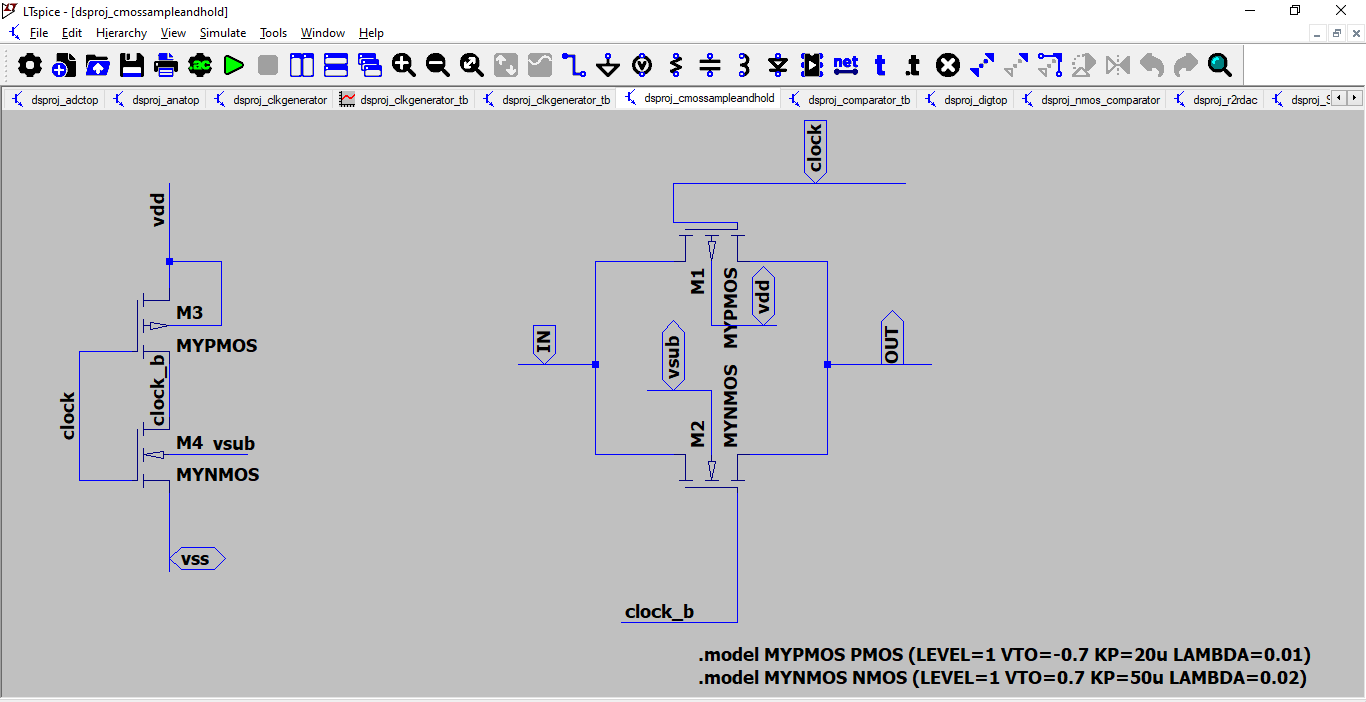
The resistors R1 = 2.1k and R2 = 0.9k were sized to generate the required over-drive for the entire common mode range to achieve rail-to-rail swing. The comparator response to the various inputs is depicted in figures 4-5-6. For the 1.4V case, the comparator output does not swing all the way to a high, due to insufficient gain. Having a relatively low gain helps in combating mis triggers, for the ADC as a system. In hindsight, the size of the tail transistors can be reduced, to save area.

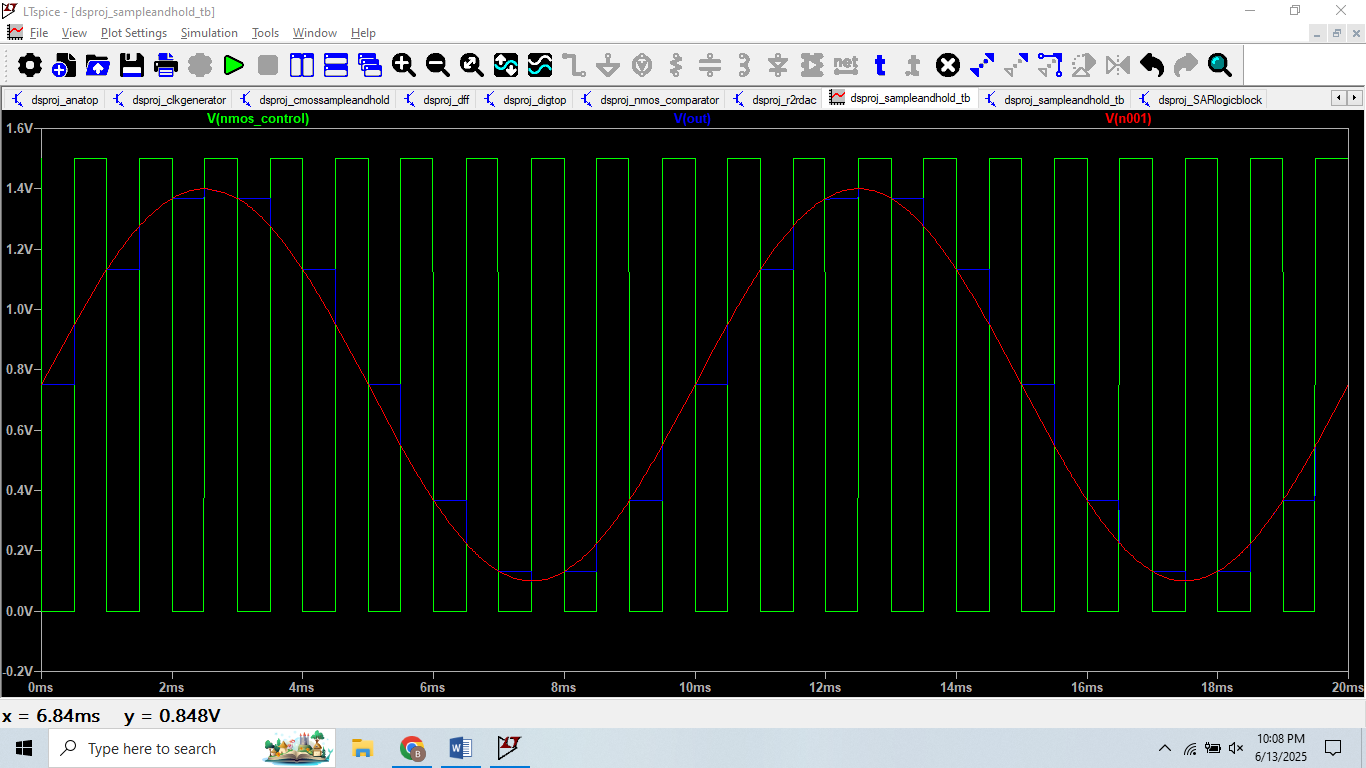
**[Sample and Hold Circuit]**

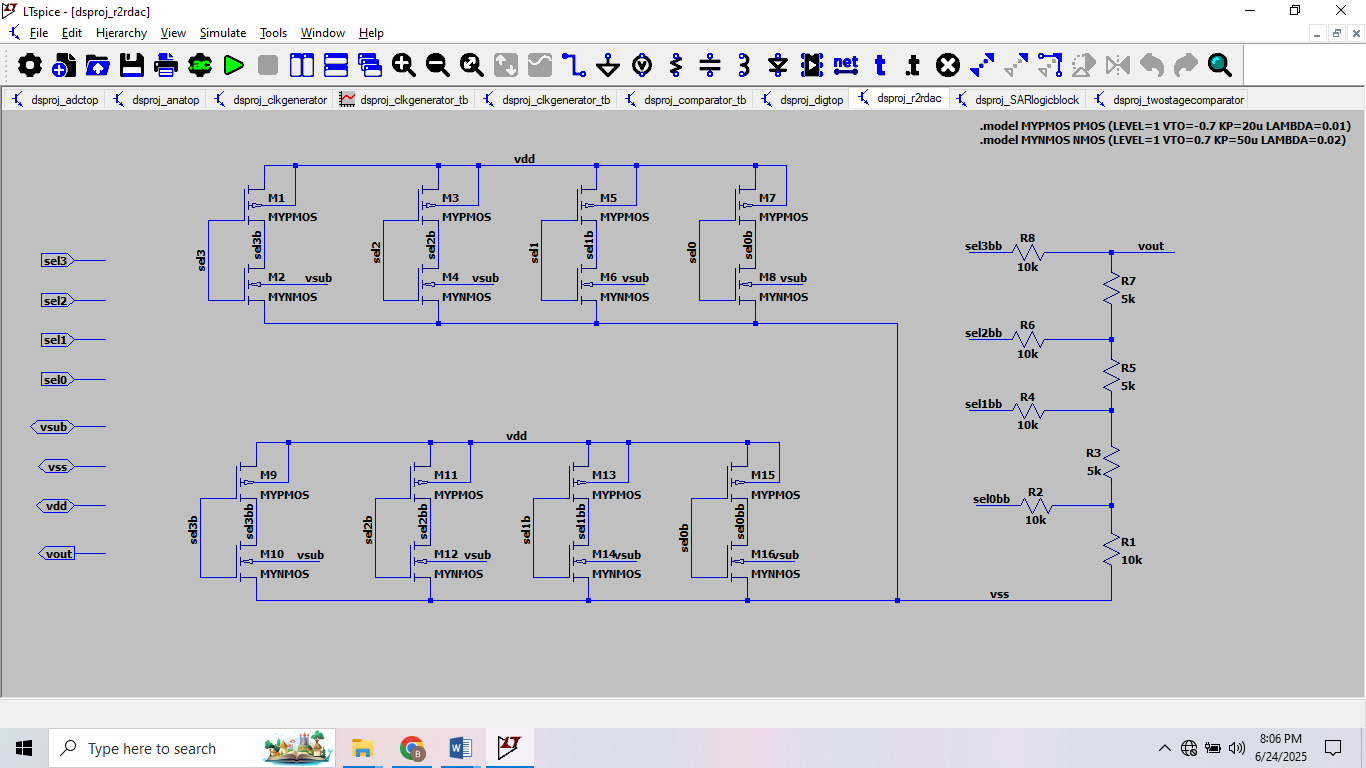
**Description:**

The sample and hold switch consist of a CMOS transmission gate, with independent PMOS and NMOS gate control. An external capacitor (in this case of 20pF) needs to be added at the output the TX gate, for reducing the voltage droop.



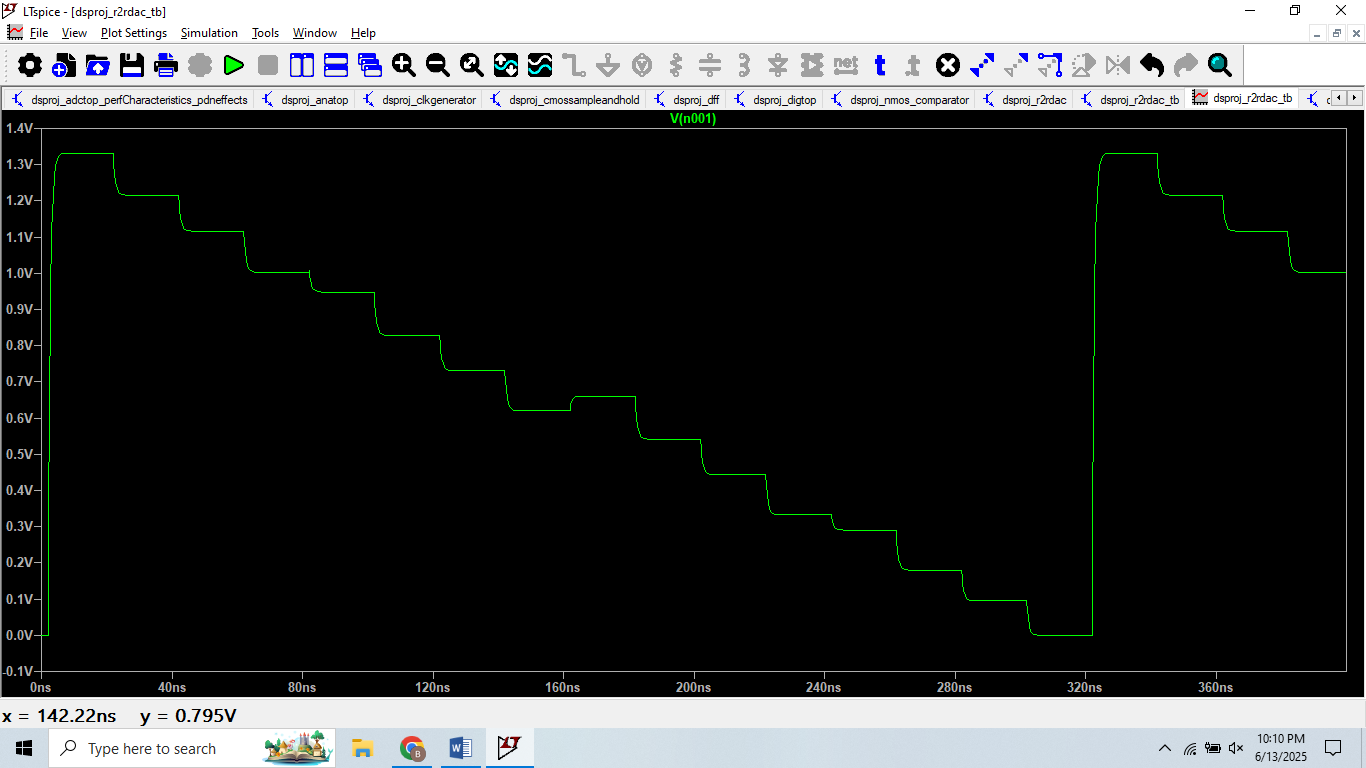


**[R-2R DAC]**



**Description:**

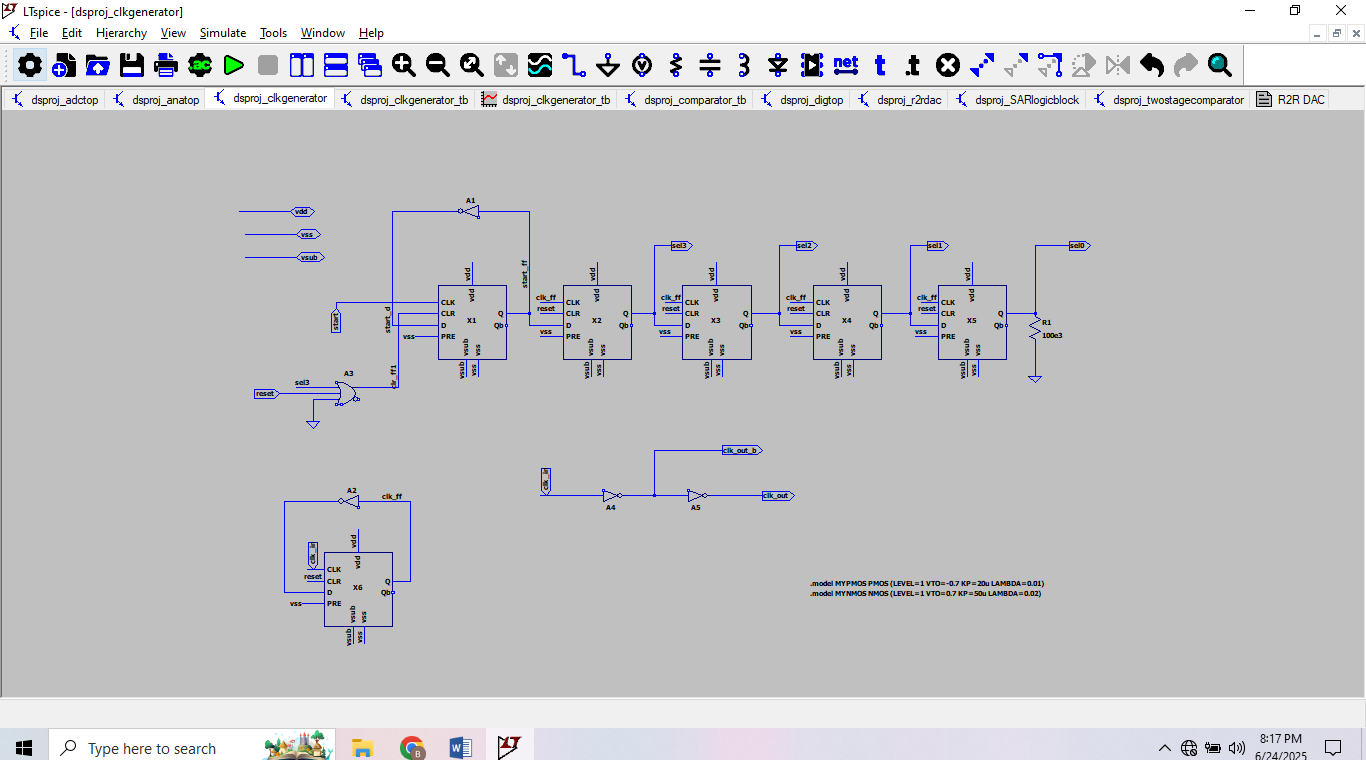
To generate the reference voltages for comparison, an R-2R DAC is utilized. The schematic is shown in Figure. By connecting R2-R4-R6-R8 to either vdd or vss the required voltages can be generated. This can easily be verified with the help of superposition. The CMOS switches are made wide to offer negligible resistance when closed.



**[Clock-generator]**

**Description:**

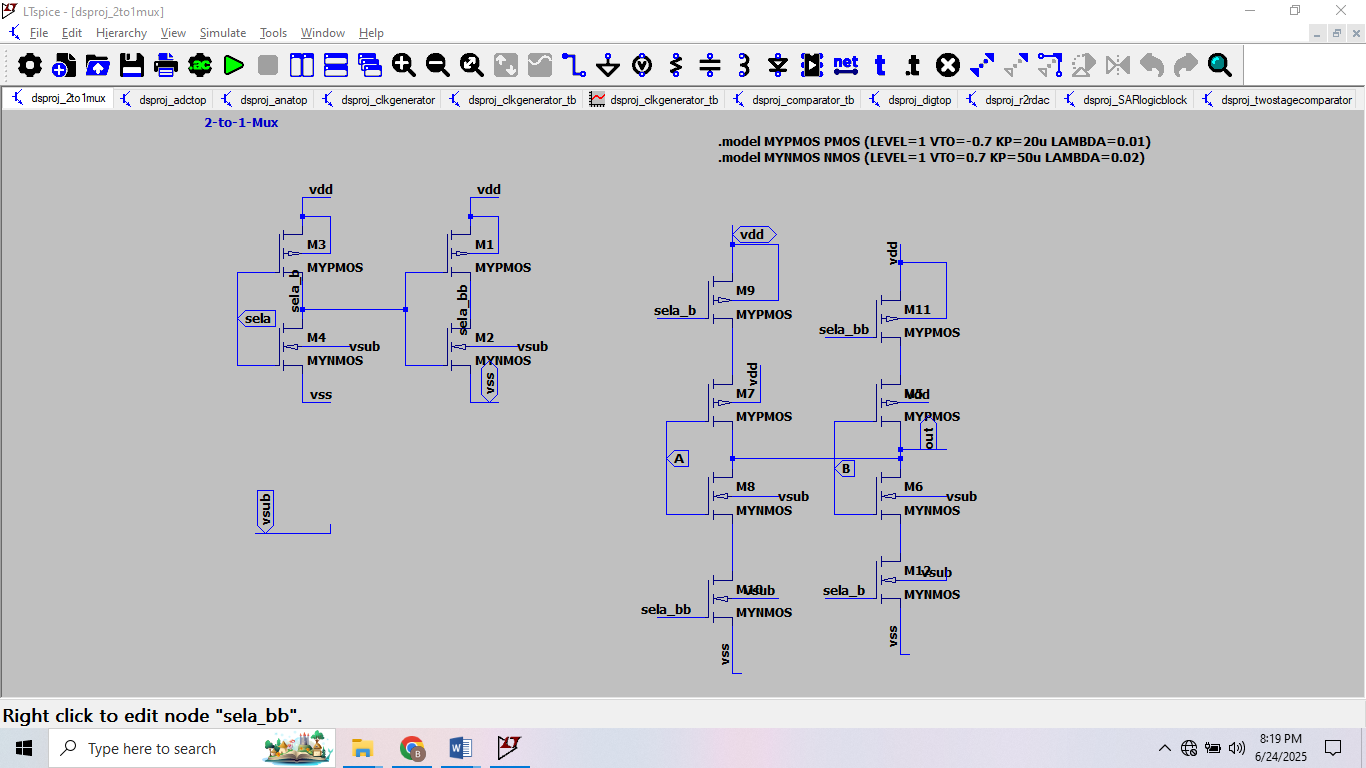
The clock-generator outputs a phase-shifted select signals. The schematic is shown in Figure 13. The test bench outputs are shown in Figure below.



**[2-to-1 Multiplexer]**

**Description:**

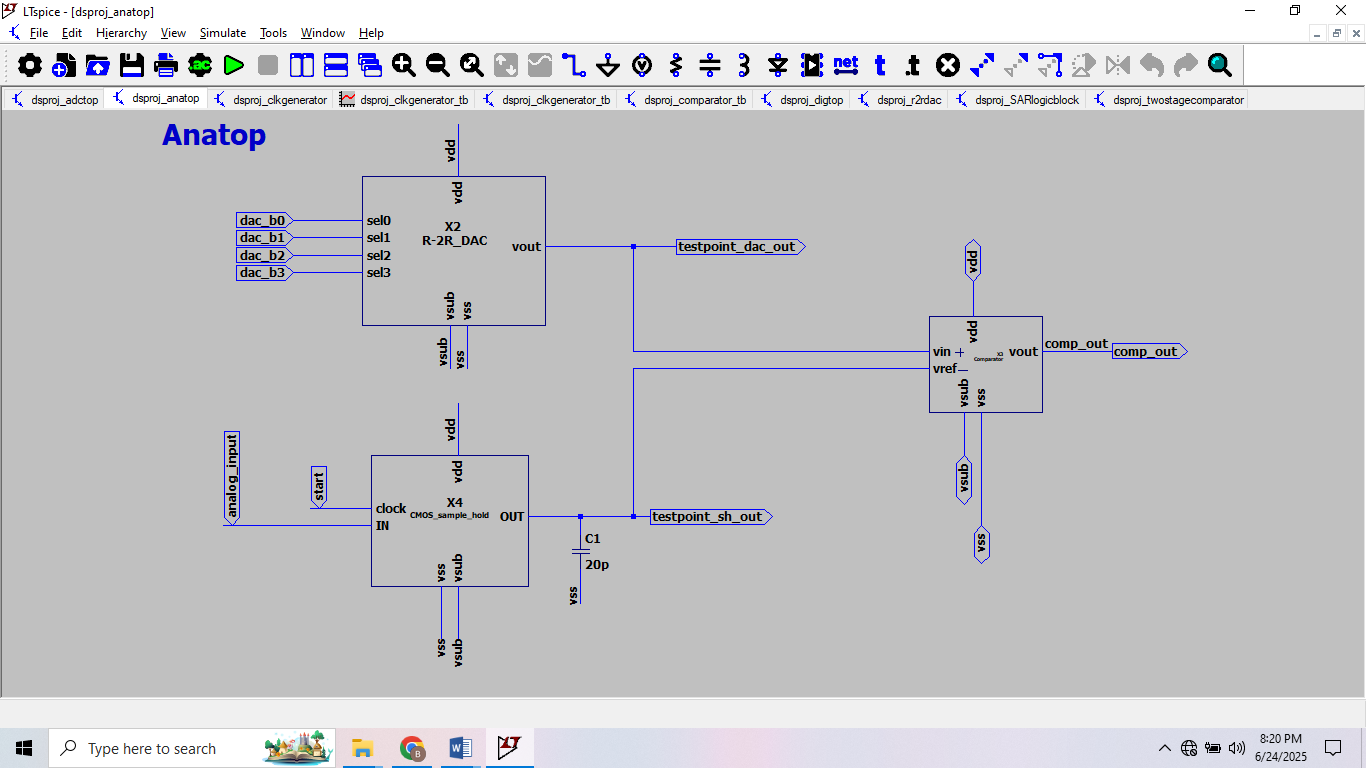
The schematic is shown in figure below. Out = sel\*(Abar) + selbar \*(Bbar).



**4.Top-level**

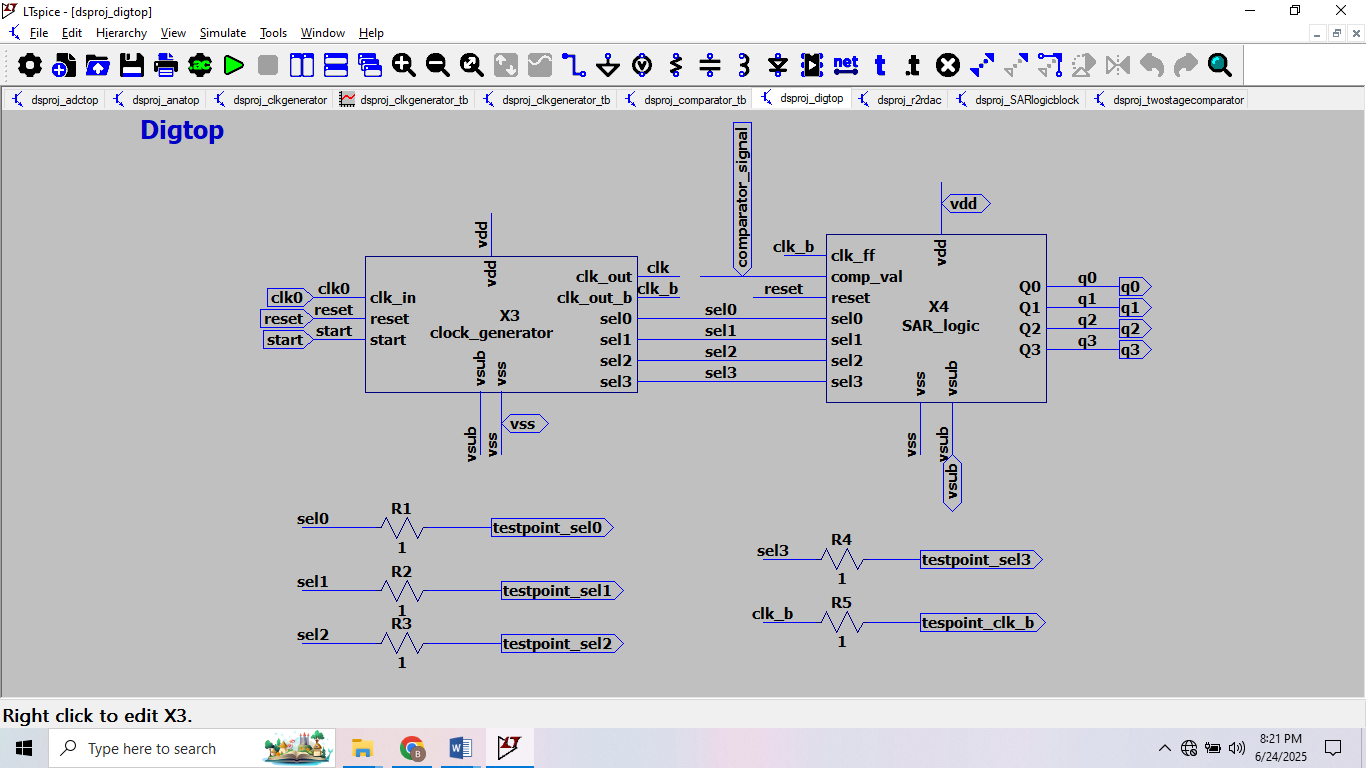
**a. [Anatop]**

**Description:**

This block primarily compares the digital output and the sampled input. Here the comparison is as follows: comp\_out = (dac\_out > sh\_out)? 1:0. A 10pF capacitor is externally added to the CMOS sample and hold to increase the hold time and reduce voltage droop. The “start” pin going high, indicates the beginning of the hold mode.

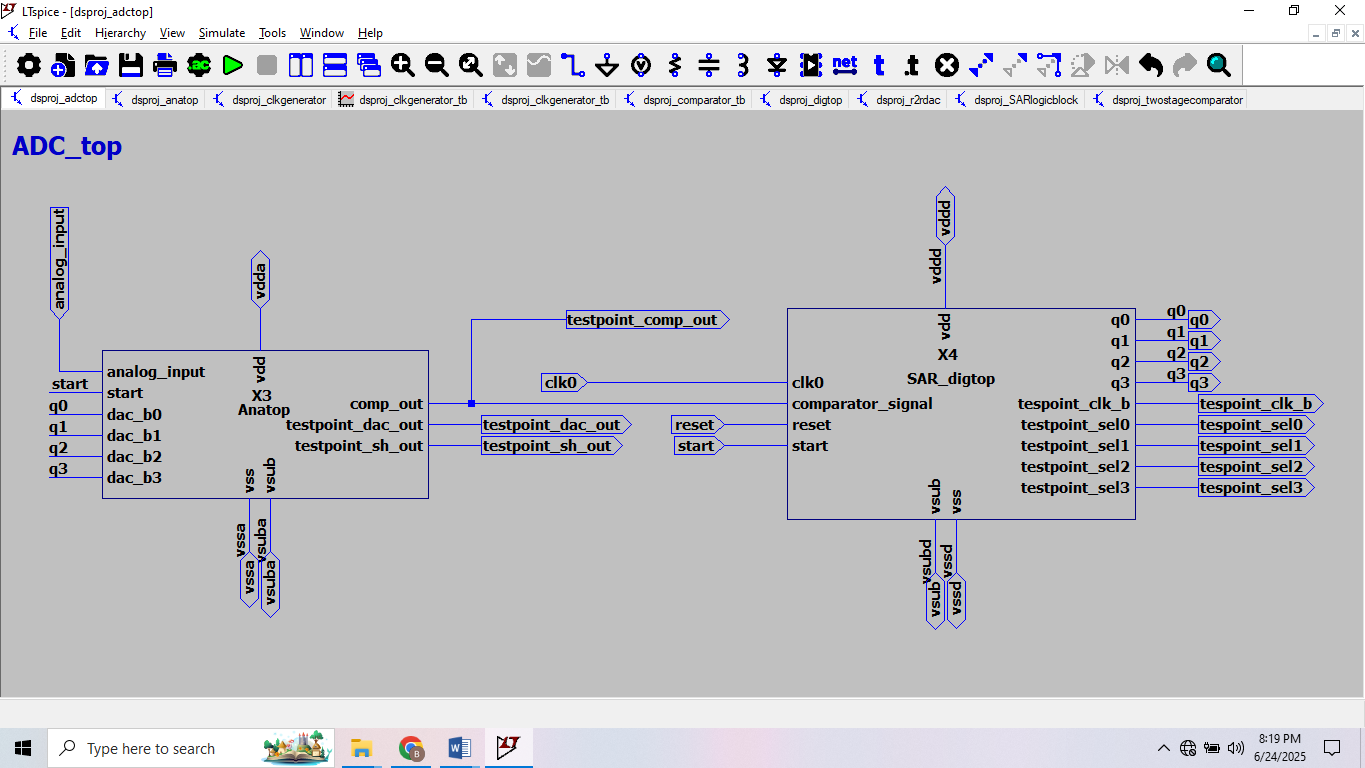
**b. [Digtop]**

**Description:**

Shown in Figure is the primary block associated with the digital logic. The externally generated clk0 drives the sequential logic. This block is responsible for generating the output code of the sampled analog signal, with q3 being the MSB of the code. The select bits control the bit position of the analog to digital conversion. For example, when Sel3 goes high the MSB(q3) of the digital code is being decided. Both the clock generator and the SAR logic are being controlled by the common reset signal.

**[SAR ADC top]**

**Description:**

The ADC top level is shown in Figure below. The digital code generated in dig-top drives the R-2R DAC. The comparator output is fed back to the digital. The power domains of the analog and the digital are separated to provide noise isolation. An externally generated clock drives the SAR state machine. To ease the droop requirements on the sample and hold circuit, the conversion speed can be increased by increasing the clock frequency.