ASSIGNMENT-6

STA Assignment

Flop-1 and Flop-2 Data:
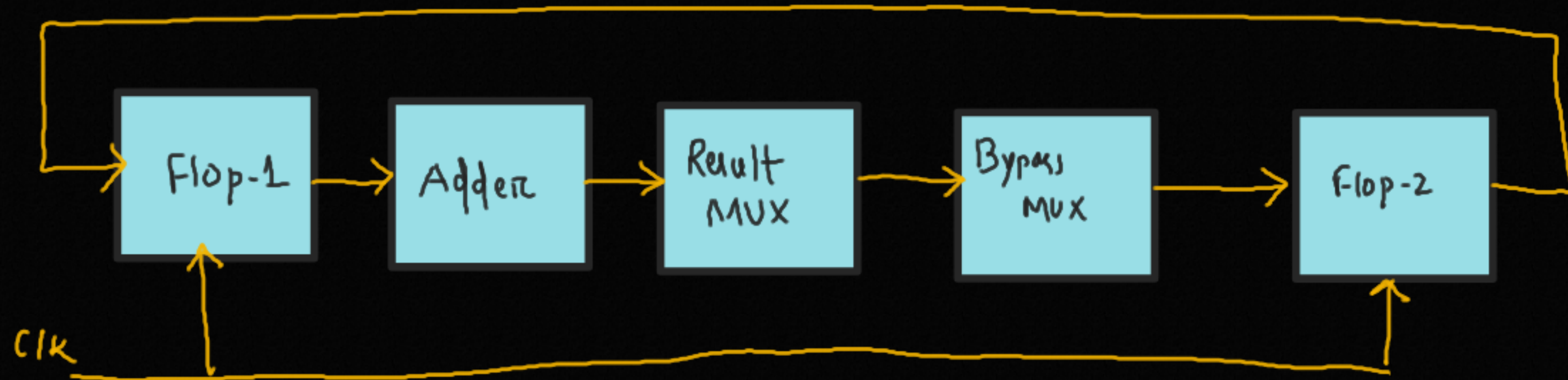
T_{setup}	62 ps
T_{hold}	10 ps
T_{pcq}	90 ps
T_{ccq}	75 ps

Combinational Circuit Data:

Component	T_{pd}	T_{cd}
Adder	590 ps	100 ps
Result MUX	60 ps	35 ps
Bypass MUX	80 ps	55 ps

If T_{clk} = 815 ps, then
a) Is setup time violated?
b) Is hold time violated?

Flop-1 → Adder → Reult MUX → Bypass MUX → F-lop-2

clk

$T_{setup} = 62\,ps$

$T_{hold} = 10\,ps$

$T_{pcq} = 90\,ps$

$T_{ccq} = 75\,ps$

$T_{pd} = 590\,ps$

$T_{cd} = 100\,ps$

$T_{pd} = 60\,ps$

$T_{cd} = 35\,ps$

$T_{pd} = 80\,ps$

$T_{cd} = 55\,ps$

$T_{setup} = 62\,ps$

$T_{hold} = 10\,ps$

$T_{pcq} = 90\,ps$

$T_{ccq} = 75\,ps$

given, $T_{clk} = 815\,ps$

In order to avoid set-up time violation,

$\therefore$ Hence, set-up time is violated.

$$T_{CLK} \geq T_{pd} + T_{pcq} + T_{set-up}$$
$$= (590 + 60 + 80) + (90 + 90) + (62 + 62)$$

$T_{pd} + T_{pcq} + T_{set-up}$

$$= 1034\,ps \qquad \text{So, } T_{clk} \leq 1034\,ps.$$

(b) <u>Hold Time :–</u>

$$T_{hold} \leq T_{ccq} + T_{cd} \qquad T_{hold} = 20\,ps$$

$$T_{ccq} + T_{cd} = (2 \times 75\,ps) + (100 + 35 + 55)\,ps$$

$$= 340\,ps$$

$T_{hold} \leq 340\,ps$ $\therefore$ Hence, the hold time is not violated.