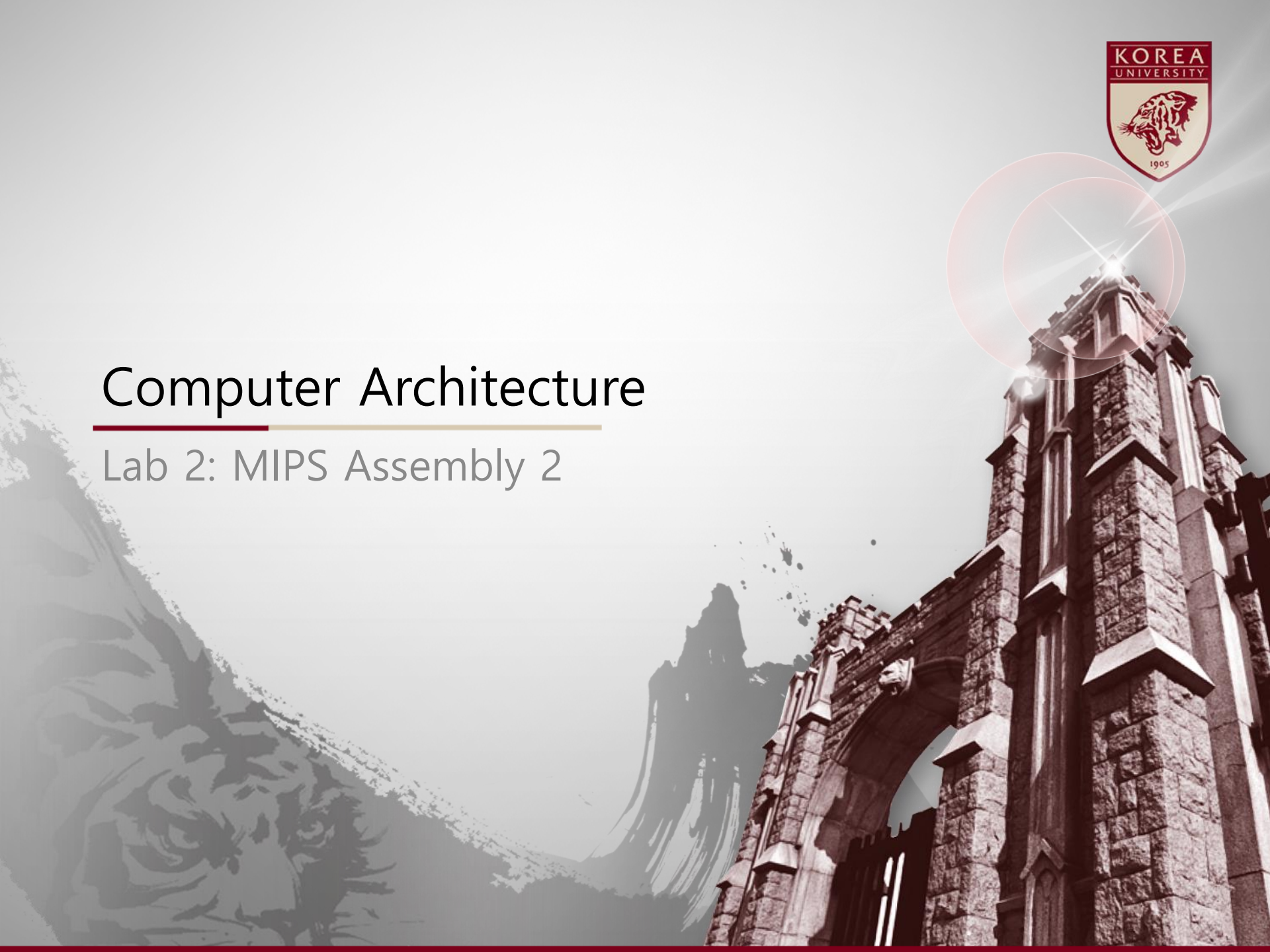

Computer Architecture

Lab 2: MIPS Assembly 2

Getting Started

- Open a web browser and go to https://dannyqiu.me/mips-interpreter/

Lab 2-1

- Translate the following C code to MIPS assembly code. The base address of the array is 0x0001f000.

```
int array[10];
int i;

for (i=0; i < 10; i = i + 1)
   array[i] = array[i] + 8;
```

Lab 2-1 (cont'd)

```
# $s0 = array base address, $s1 = i
# initialization code
  lui  $s0, 0x0001              # $s0 = 0x00010000
  ori  $s0, $s0, 0xF000         # $s0 = 0x0001F000
  addiu $s1, $0, 0              # i = 0
  addiu $t2, $0, 10             # $t2 = 10

loop:
  slt  $t0, $s1, $t2            # i < 10?
  beq  $t0, $0, done            # if not then done
  nop                           # delay slot
  sll  $t0, $s1, 2              # $t0 = i * 4 (byte offset)
  addu  $t0, $t0, $s0           # address of array[i]
  lw   $t1, 0($t0)              # $t1 = array[i]
  addiu $t1, $t1, 8             # $t1 = array[i] + 8
  sw   $t1, 0($t0)              # array[i] = array[i] + 8
  addiu $s1, $s1, 1             # i = i + 1
  j    loop                     # repeat
  nop                           # delay slot
done:
```

Lab Assignment

- Translate the following C code to MIPS assembly code. The base address of the array is 0x0001f000.
- Submit your source code to Blackboard.

```
int array[10];
int i, sum;

i = 0;
sum = 0;
for (i=0; i < 10; i = i + 1) {
   if(sum < 30)
     sum = sum + i;
   array[i] = sum;
}
```

Expected Results

0x0001f004	1	0x00000001	0b00000000000000000000000000000001
0x0001f008	3	0x00000003	0b00000000000000000000000000000011
0x0001f00c	6	0x00000006	0b00000000000000000000000000000110
0x0001f010	10	0x0000000a	0b00000000000000000000000000001010
0x0001f014	15	0x0000000f	0b00000000000000000000000000001111
0x0001f018	21	0x00000015	0b00000000000000000000000000010101
0x0001f01c	28	0x0000001c	0b00000000000000000000000000011100
0x0001f020	36	0x00000024	0b00000000000000000000000000100100
0x0001f024	36	0x00000024	0b00000000000000000000000000100100