Computer Architecture

Lab 6: Datapath

Getting Started

- Download alu.sv, regfile.sv, imem.sv and dmem.sv from Blackboard
- Open a web browser and go to https://www.edaplayground.com/

Structural Modeling - Hierarchy

```
module and3(input  logic a, b, c,
            output logic y);
  assign y = a & b & c;
endmodule


module inv(input  logic a,
           output logic y);
  assign y = ~a;
endmodule


module nand3(input  logic a, b, c
             output logic y);
  logic n1;                                  // internal signal

  and3 andgate(a, b, c, n1);                 // instance of and3
  inv  inverter(n1, y);                      // instance of inverter
endmodule
```

Structural Modeling – Better Way

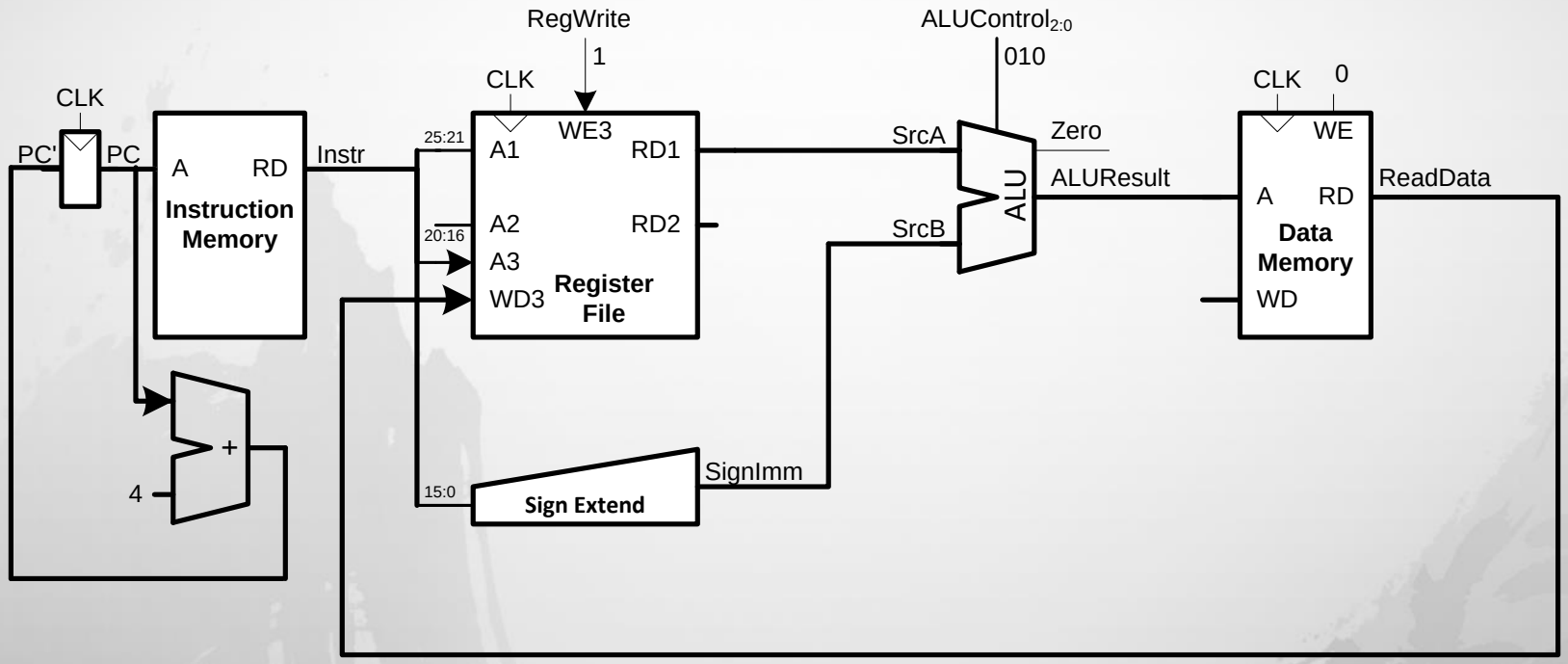
```
module and3(input  logic a, b, c,
            output logic y);
  assign y = a & b & c;
endmodule
```

```
module inv(input  logic a,
           output logic y);
  assign y = ~a;
endmodule
```

```
module nand3(input  logic a, b, c
             output logic y);
  logic n1;

  and3 andgate(
      .a    (a),
      .b    (b),
      .c    (c),
      .y    (n1)
  );
  inv  inverter(
      .a    (n1),
      .y    (y)
  );
endmodule
```

Datapath for lw Instruction



Testbench

- Copy the following testbench code to “testbench.sv” on the left

```
module testbench_lw();
  logic clk;
  logic reset;
  logic regwrite;
  logic memwrite;
  logic [2:0] alucontrol;

  datapath dut(
    .iClk                       (clk),
    .iReset                     (reset),
    .iRegWrite   (regwrite),
    .iMemWrite   (memwrite),
    .iALUControl(alucontrol)
  );

  always     // no sensitivity list, so it always executes
    begin
      clk = 1; #5; clk = 0; #5;
    end

  initial begin
    $dumpfile("dump.vcd"); $dumpvars;
    reset = 0; #21;
    reset = 1; #10;
    regwrite = 1; memwrite = 0; alucontrol = 3'b010;
    reset = 0; #10;

    #10; $stop;
  end
endmodule
```

Datapath

- Copy the following code to “design.sv” on the right

```
`include "alu.sv"
`include "regfile.sv"
`include "imem.sv"
`include "dmem.sv"

module datapath(
  input logic iClk,
  input logic iReset,
  input logic iRegWrite,
  input logic iMemWrite,
  input logic [2:0] iALUControl
);


endmodule
```

Building Blocks

- Click “+” right after “design.sv”
- Upload “alu.sv”

- Upload regfile.sv, imem.sv, and dmem.sv in the same way

Lab Assignment

- Finish the implementation of the datapath module
  - Implement the program counter and sign extension
  - Connect modules
- Save and submit the link of your design to the Blackboard.
  - Click  in the bottom window to copy the URL of your design.

Expected Result