# Fundamentals of III-V Semiconductor MOSFETs

Serge Oktyabrsky • Peide D. Ye Editors

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### **Preface**

Is it true that III-V semiconductor materials are back in play for mainstream digital ICs? Or it is just another round of interest to other-than-silicon materials when Si CMOS technology is approaching just another "fundamental limit". There is no simple answer. Moreover, the answer depends not only on physics, materials and technologies, but on economics, demand from other industries, etc. Anyway, we would like the reader to answer these questions on his/her own. The book will help by presenting the fundamentals and current status of research on III-V compound semiconductor metal-oxide-semiconductor field-effect transistors (MOSFETs). We believe it is just the right time to summarize results and provide guidelines for the future efforts because of the following recent developments in digital electronics:

- After almost 50 years of research, it is finally clear that there are technologies
  to make better-than-silicon MOSFETs. Although the efforts were not sustained
  during this long time period with ups and downs, this area is now very active
  with yet growing interest of researches and engineers in electronic industry and
  academia. The number of papers published recently on III-V MOSFETs are way
  higher than at any given time in the past.
- Silicon oxide is out of play in mainstream Si CMOS. That means that the key
  materials advantage of silicon for CMOS circuits is gone. Introduction of high-k
  oxides into Si ICs makes the perspectives of III-V integration significantly more
  feasible.
- Further scaling of transistors relaxes some of the requirements to the gate stack, such as interface trap density, D<sub>it</sub>. In fact, due to increased oxide capacitance, the circuits can handle much higher levels of D<sub>it</sub> which previously considered as detrimental.
- Si IC companies, mainly INTEL and IBM and their consortia, have shown interest beyond just research.

Apparently, there are still a lot of challenges to be overcome before manufacturing becomes viable. According to Robert Chau, Director of transistor research and nanotechnology at INTEL Corporation, there are following four major challenges (CSIC 2005 Tech. Digest): (1) compatible high-quality gate dielectric; (2) scaling with acceptable  $I_{ON}/I_{OFF}$  ratio; (3) p-channel with a reasonable transport; and

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(4) integration onto Si substrate. This book addresses research covering the first three of these challenges. We believe the integration with Si involves significantly different materials problems, than those covered in this book. In addition, there are a few good books and reviews on this topic (E. Towe (Ed.) Heterogeneous optoelectronics integration, SPIE Press, 2000; E. Fitzgerald, ECS Trans. 19, 345, 2009; F. Letertre, AIP Conf. Proc. 1068, 185, 2008).

The book begins with a concise historic review (Chap. 1) of challenges and breakthroughs that led to the evolution of today's III-V MOSFETs. Two chapters on device simulations (Chaps. 2, 3) present performance analysis of MOSFETs with different III-V channels with the focus on benefits, potential showstoppers, and novel promising device structures (Chap. 2); and device physics and technology issues for InGaAs HEMTs based on close comparison with recent experimental results (Chap. 3). The chapters on ab initio density function theory simulations include concise introduction into DFT (Chaps. 4, 5) and simulation results on oxide/III-V interfaces with a particular focus on amorphous oxides (Chap. 5), and on bulk and surface properties of HfO, and ZrO, high-k oxides and metal-oxide interfaces (Chap. 4). Chapter 6 reviews the interfacial chemistry of III-V's, with particular attention to native and deposited oxide gate dielectrics, and correlation with electrical properties of these interfaces. Chapter 7 proposes an empirical model to correlate the experimental work on III-V MOSFETs with the existing oxide/III-V interface models. It follows by six chapters (Chaps. 8-13) on high-k/III-V integration and device work on III-V MOSFETs. Chapter 8 begins with comparison of HEMT for logic applications to MOSFET technology with emphasis on current transport and interface passivation. Chapter 9 presents the new progress on InGaAs, Ge and GaN MOSFETs with MBE Ga<sub>2</sub>O<sub>2</sub>(Gd<sub>2</sub>O<sub>2</sub>) or ALD Al<sub>2</sub>O<sub>2</sub> as gate dielectrics. Chapter 9 discusses the critical process issues for self-aligned III-V MOSFET and presents the device work on self-aligned GaAs enhancement-mode MOSFETs using regrown source and drain regions. Detailed work on HfO<sub>2</sub> with silicon interface passivation on various III-V substrates are summarized in Chap. 11. The new progress on III-V p-channel MOSFETs, one of the grand challenges in III-V CMOS technology, is reviewed in Chap. 12. Chapter 13 describes materials growth, deposition and fabrication technology, device characteristics, reliability, and applications of insulated gate group III-nitride field effect transistors. The book is ended by the Chap. 14 as a III-V circuit chapter, where the complete technology-circuit assessment of III-V FETs and the co-design approach from the device/SPICE models, logic/memory circuit analysis and technology requirements are presented.

After over 40 years of success of  $\mathrm{Si/SiO}_2$  material system in digital circuits, high-k oxides became attractive for further CMOS scaling at the end of 1990s and instigated explosive research growth that resulted in its successful commercialization. We hope that the III-V research is currently at a similar stage as high-k's were in 1990s, and that the combined efforts in academia and industry will make the long-standing GaAs MOSFET dream a commercial technology.

We have benefited greatly from suggestions and discussions with Dmitri A. Antoniadis, Robert Chau, Jesus del Alamo, Eugene Fitzgerald, Max Fischetti. This book has become possible due to support of Focus Center Research Program and

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Albany and West Lafayette September, 2009 Serge Oktyabrsky and Peide D. Ye

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### Chapter 1 Non-Silicon MOSFET Technology: A Long Time Coming

Jerry M. Woodall

**Abstract** A summary of the important materials science issues associated with the realization of viable III-V MOSFET technologies is presented. The key science breakthrough was the unambiguous identification of which components of the non-stoichiometric native oxides were responsible for surface Fermi level pinning (FLP). The components that cause FLP are the anion oxides and the elemental anion associated with a particular III-V compound semiconductor. For GaAs, these are As<sub>2</sub>O<sub>3</sub> and elemental As respectively. The physics of FLP is also applicable to Schottky barriers. Although many attempts were made to explain FLP, the most comprehensive theory is that the elemental anion acts to cause FLP via its Schottky barrier workfunction. During the past decade several technologies have succeeded in mitigating these chemical barriers and III-V MOSFET technology is now a component of the MOSFET menu.

#### 1.1 Introduction

The purpose of this chapter is to provide the reader with a brief, non-comprehensive overview of the history, scientific and technological barriers, pre-device solutions, and seminal research results that led to the evolution of today's non-silicon MOS-FET (NSMOSFET) technology.

If you are living on planet Earth, you must know that silicon MOSFET (SMOSFET) technology, with a 2008 worldwide chip sales of more that \$250 billion, is essentially the only semiconductor technology used by all electronics based industries. By contrast, the total 2008 sales of *all* compound semiconductor devices and chips are about \$20 billion, and most of this revenue was generated by heterojunction based photonic devices and chips. In contrast, none of the revenue was produced by NSMOSFETs sales (save some devices sold for testing and military applications).

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Why is Si technology the dominant semiconductor technology? To answer this at the highest level, let me tell the reader the answer I give my undergraduate students during the first lecture of Purdue's core semiconductor course. Even though Si is an inferior electronic and photonic material compared to, for example, GaAs, Si is still king because Si is cheap and the rust on Si is electronically exquisite, whereas the rust on nearly all compound semiconductors of interest is either inferior or non-functional electronically. In other words, both price-performance advantages of SMOSFET technology and the lack of a viable NSMOSFET technology during the early R&D efforts have hampered its development. This chapter will discuss why the electronic and chemical properties of compound semiconductor rust were not suitable for the "O" material for NSMOSFETs.

Another question, possibly rhetorical, comes to mind at this point. Even if the application specific performance of NSMOSFET technology could be far superior to planned performance for SMOSFET technology, will it supplant Si technology? Is it too little or too late? This situation can be likened to the current global energy crisis. Let us equate Si technology with fossil fuel technology (ignoring carbon footprint issues). Both are the overwhelming dominant incumbents. Now let us equate alternative solar energy technology with NSMOSFET technology. The central question for both fossil fuel and Si technology is whether there is a business model for solar energy technology and NSMOSFET technology that will result in supplanting the current fossil fuel and Si incumbents. Or, will Si, for example, stay on a revised "Moore's Law" path? This question will be addressed in a later chapter in this book.

### 1.2 Brief and Non-Comprehensive History of the NSMOSFET

Any discussion of the history of any MOSFET technology, or of any other transistor technology, must begin with the Heil and Lilienfeld Patents [1, 2]. Examination of Heil's patent clearly indicates that a MOSFET was being described. Amusingly, Heil's 1934 patent date is 13 years before the commonly accepted birth date of the transistor. It is less amusing to note that neither Heil nor Lilienfeld were included in the Nobel Prize for the invention of the transistor.

The next seminal event, also not recognized by the Nobel Committee, was the first public report of the SMOSFET by Kang and Atalla [3]. This report was seminal in that the SMOSFET became the dominant material for commercial MOSFETs. Very rarely does the early work ever evolve into the dominant technology.

The 1960s and 1970s were a period of intense development and rapid progress of SMOSFET technology. Hundreds of worldwide workers in corporate and university laboratories contributed to this progress. However, except for isolated successes limited to laboratory scale III-V and II-VI compound thin film transistor (TFT) devices, attempts during this period to develop a NSMOSFET technology were essentially unsuccessful. An exception to this notable lack of progress in NSMOSFET development was the work of Brody and Kunig, who, in 1966, realized both